

On-the-Fly Reconfigurable Logic

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ABSTRACT

Reconfigurable Circuit (RC) platforms can be configured to implement complex combinatorial and sequential logic. In this paper we investigate various RC technologies and discuss possible methods to optimise their power, speed and area. To address the drawbacks of existing RC technologies we propose a generic architecture we call “OFRL” (On-the-Fly Reconfigurable Logic). Our objective is to provide a low power, high speed platform for reconfigurable circuit and dynamically reconfigurable logic applications that use fewer transistors than existing technologies.

Keywords: Reconfigurable circuits, Threshold logic gates, Dynamically reconfigurable logic

1. INTRODUCTION

System on chip (SoC) circuits to support innovative electronic products are rapidly becoming more complex. The cost of developing such complex semiconductor systems, as well as rapid changes in product requirements, lead to significant uncertainty in design and “time to market” decisions. Reconfigurable Circuit (RC) platforms that allow circuit logic to change, subsequent to chip fabrication, have evolved to meet such design challenges. RC chips can be configured to implement complex combinatorial or sequential logic. They have been widely used over the past few decades to implement DSP functions for wireless communication, multimedia and biomedical applications.

In this paper we present a survey of existing RC technologies and propose a new RC architecture: “OFRL” or On-the-Fly Reconfigurable Logic that is inspired by Shibata’s “flexware” paradigm.¹ Our aim in this work is to provide a low power, high speed RC platform that uses fewer transistors, for a given application, than current RC technologies.

Existing RC circuits can be statically, dynamically or partially dynamically configured. Dynamic configuration, as indicated in Fig. 1, allows the circuit function to change while the chip is in operation. Dynamically Reconfigurable Logic (DRL) of this kind facilitates the implementation of evolvable algorithms,^{2,3} which are difficult to build with either fixed hardware or conventional software. As its name implies, our new RC architecture, OFRL can be dynamically reconfigured. One of the goals in its development is to provide support for DRL applications.

Although DRL circuits provide high flexibility, they have poor performance in terms of speed, area and power when compared to conventional circuits.⁴ At the transistor level, Padure *et al*,⁵ have presented interesting results concerning the capacity of Threshold Logic Gate (TLG) circuits to be reconfigured at run time. Past research⁷⁻¹¹ in TLG has shown a significant reduction in the number of transistors required to implement combinatorial and sequential logic. Their experiments^{9,10} also point to a potential benefit in terms of delay and power. It would

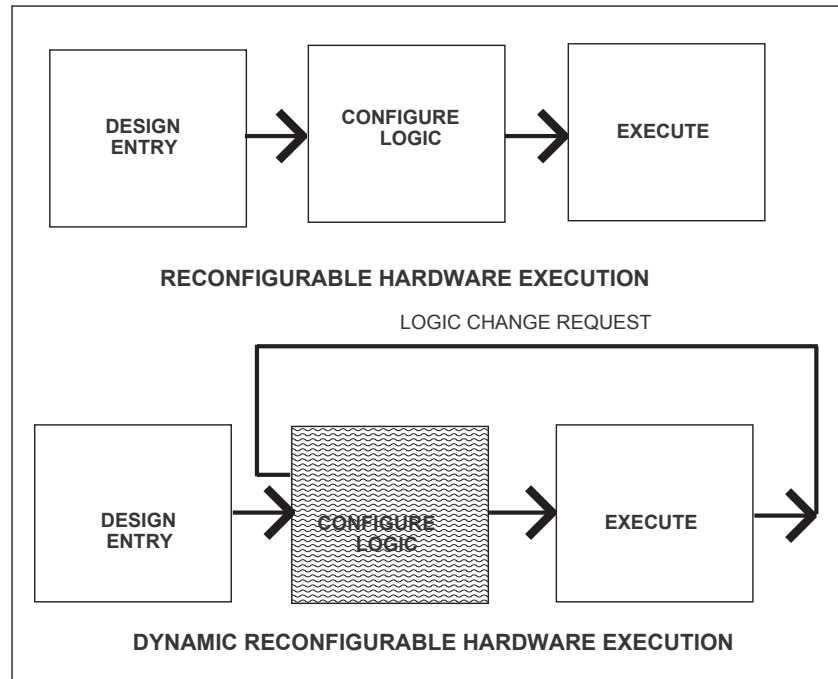


Figure 1. Reconfigurable and dynamically reconfigurable logic.

appear therefore, that TLG circuits have the characteristics we require for a new RC technology: they are dynamically reconfigurable, have low power consumption and low delay and can implement complex functions with few transistors. However there are challenges in TLG circuit design, including a lack of a CAD framework to implement large scale circuits and a lack of optimisation techniques to meet timing, power and area constraints.

In Section 2 we survey existing RC technologies and compare their performance in terms of power and area. Section 3 provides a brief survey of reconfigurable circuits implemented using TLG gates. Finally in Section 4 we propose our new RC architecture, OFRL, which makes use of TLGs.

2. RECONFIGURABLE CIRCUIT ARCHITECTURES

In this section we survey current commercial RC architectures.

2.1. LUT Based Reconfigurable Logic

As shown in Fig. 2.1, Look-Up-Table (LUT) based reconfigurable cells consist of a small RAM, usually of 8 or 16 bit capacity, that implements a combinatorial logic function of 3 or 4 inputs respectively. The main drawbacks of LUT based cells are power consumption and configuration time, which are very high as LUT size grows.¹³ Steve Wilton et al,^{14,15} have performed extensive research aimed at minimising the power consumption of LUT based cells.

There is a trade-off between the power and delay of LUT based designs with power becoming a problem as the size the LUTs increase and speed becoming a problem when there are many small LUTs. It has been shown¹³ that a mixture of 3-input and 4-input LUTs provides a reasonable balance between speed and power. However, LUT based designs still lag behind custom microprocessor and DSP designs in terms of area utilisation, delay and power.

There are also problems with current CAD tools for LUT based designs. These tools require a specific RTL programming style be followed to achieve best results. They also tend to waste entire LUTs when implementing small logic functions. LUTs are also wasted for latches rather than implementing complex combinatorial functions.

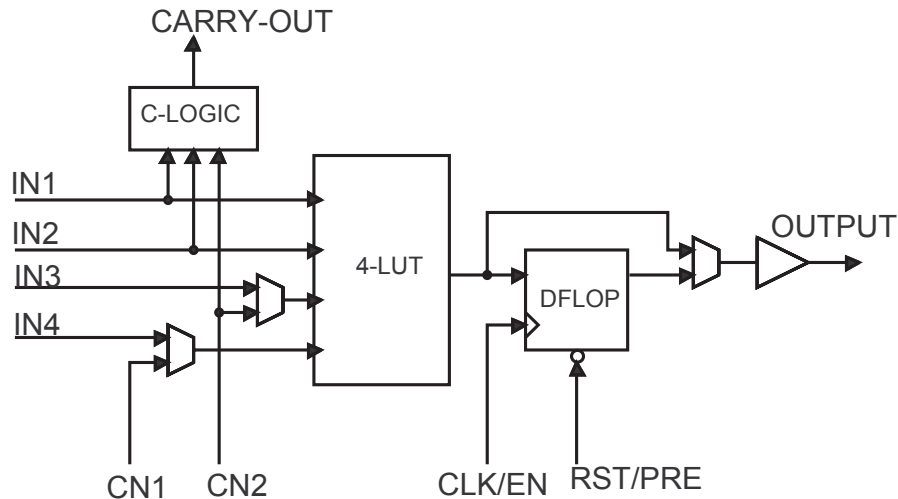


Figure 2. A LUT based reconfigurable cell.

Finally, although some LUT based platforms do support DRL, they are very expensive in terms of power during dynamic reconfiguration.

2.2. MUX Based Reconfigurable Logic

MUX based reconfigurable logic uses cells consisting of 2-to-1 multiplexers and OR gates. The Actel¹⁶ Field Programmable Gate Array (FPGA) family is a good example of a MUX based logic cell architecture. As shown in Fig. 2.2, an Actel FPGA logic cell consists of three 2-to-1 multiplexers and an OR gate. Each of these MUX-RC cells can implement any combinational function of two inputs, any function of three inputs with at least one positive input, and also many functions of four inputs. Mapped designs in MUX based architectures is easy to decode information of the designs but this is not possible in LUT based and PLD based RC due to nature of their architecture. Due to this drawback MUX based is not popular as LUT based RC though they can achieve better performance than PLD based designs in larger designs.

2.3. PLD Based Reconfigurable Logic

A PLD (Programmable Logic Device)¹⁷ is a device which consists of an array of AND and OR gates, which are programmed through small memories. They are available in different families as Antifuse, EPROM and EEPROM based PLD devices. Altera PLDs are mostly considered to be EPROM Based PLDs, which is the one we used in our evaluation. In general, PLD architectures are suitable for smaller designs but in larger designs they have performance issues.

2.4. Evaluation of Reconfigurable Circuit Architectures

To compare the timing and power of RC architectures, synthesis and simulation of the various logic cell structures was carried out. Table 2.4 shows the results for LUT, MUX and PLD logic cells, synthesised in a 0.25 μm CMOS technology.

FPGA synthesis was then used to map simple arithmetic circuits to the different RC architectures. Simulation was used to measure circuit delays. The results are shown in Table 2.4. Note that the circuits were synthesised with the same timing constraints.

From the results for the 4-bit adder circuit (add4) one can see that the LUT based approach has lowest delay. The whole circuit is mapped in a single logic cell and hence suffers little from routing delays. The other

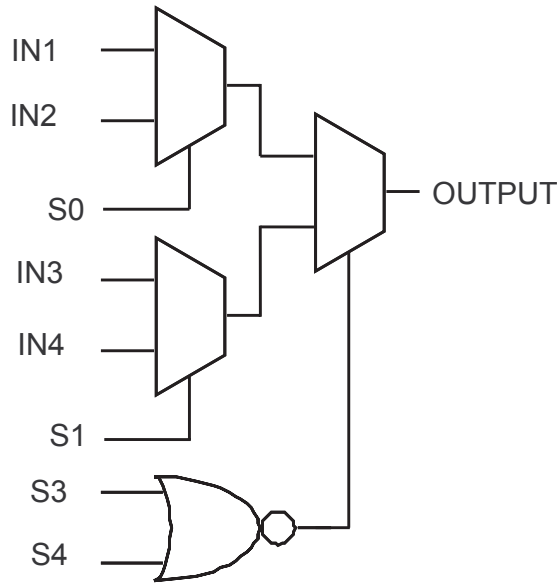


Figure 3. A MUX based reconfigurable cell.

RC element	Switching Power μW	Cell Power μW	Dynamic Power μW	Leakage Power nW	Delay ns
4-LUT-RC	7.3104	4.6925	12.0029	4	4.36
4-MUX-RC	17.3222	24.9653	42.2875	14	9.16
4-PLD-RC	3.2018	2.6698	8.8716	3	3.13

Table 1. Power consumption and critical path delay results of programmable logic cells (synthesised in $0.25 \mu\text{m}$ TSMC technology @ 50 MHz).

architectures suffer significant routing delays. This is because they have fine grained logic architectures with smaller logic cells than the LUT based approach.

In recent times, SRAM-based LUT FPGAs have been more popular than other architectures due to their fast reprogram time and better performance. The main drawback of the LUT based architecture is that there is no pre-determined correlation factor between LUT-based FPGA CAD tools and hardware devices allowing the prediction of real-time performance. Also as mentioned in Section 2.1, LUTs are wasted for implementing small logic functions.

Circuits	LUT-RC (ns)	MUX-RC (ns)	PLD-RC (ns)
add4	9.0	38.7	19.8
add1	11.7	26.7	5.0
count	6.9	13.6	4.0
mult8	35.9	127.3	19.0
latch3	9.8	13.6	2.0
crcgen	9.0	6.9	2.0

Table 2. Delay analysis of circuits mapped in LUT, MUX and PLD. (Results are based on FPGA compiler synthesis)

3. THRESHOLD LOGIC GATE BASED RECONFIGURABLE CIRCUITS

Threshold logic gates are a generalised form of conventional logic gates. They work like a neuron in a neural network, computing a weighted sum of inputs and triggering on a threshold value.^{5,6} We propose to use TLGs to develop efficient low power reconfigurable circuits. To minimise power consumption during dynamic reconfiguration, and to manage leakage power, a mixture of MTCMOS (Multi-Threshold CMOS)^{18,19} and VTCMOS (Variable Threshold CMOS)²⁰ cells could be used.

3.1. Previous Work

Aunet *et al.*²¹ explored universal linear threshold elements to implement a real-time circuit reconfiguration. Their work demonstrated reconfiguration through UV programming techniques. For this technology, reduction in the interconnections between the threshold elements is an important step for power reduction as the rate of switching between interconnect switches is less during dynamic operation. Lack of interconnect architecture shows that the power increases if there is no suitable interconnect matrix between the reconfigurable elements.

Aoyama *et al.*²² introduced a new reconfigurable element composed of threshold gates, which are implemented in a 2-level feed-forward neuron MOS circuit. This has been demonstrated by using a 3 input variable ν MOS circuit with four control signals. This can realise any symmetric logic (AND, XNOR, NOR, XOR) or multiplexer functions. They use functional simulation to demonstrate reconfigurable behaviour of their implementation; however other circuit effects need to be explored in-order to fabricate this logic.

Sugahara *et al.*²³ proposed a SPIN-MOSFET based reconfigurable logic gate in which logic functions can be realised using a SPIN-MOSFET as a driver or an active load of CMOS using a neuron MOS input stage. The logic functionality of the gate can be changed by adjusting the magnetisation configuration for the source and drain of the MOSFET. The features of this logic would be less beneficial for the scope of DRL architecture designs.

Ferrera *et al.*²⁴ designed a HHE (Hybrid Hall Effect) based threshold element to address its special features compared to SRAM based programming and EEPROM based programming elements. They also address the low power characteristics of HHE device. Their work shows that the HHE based architecture draws more power than SRAM LUT and EEPROM PLD architectures but it has better configuration time.

Thoma *et al.*²⁵ developed a reconfigurable chip called POETic, which includes a circuit to implement a dynamic routing algorithm to speed the execution time of evolvable algorithms. The POETic chip has been developed to ease the development of bio-inspired applications. One of the features of the POETic chip is that it can achieve dynamic routing and the custom microprocessors, which can access the configuration bits to speed up the evolvable algorithms, which is not yet possible by Virtex II Pro¹³ and any other commercially available chips. Result of their work shows that their chip has been developed for specific reconfigurable application and not for general reconfigurable applications. The highlights of their work in this chip is the novel routing architecture design, which is considered to be a suitable candidate for dynamic reconfigurable circuits.

From the review of previous work in threshold logic gates shows that the TLG has a great potential in the implementation of reconfigurable architectures to achieve high performance designs.

4. OFRL ARCHITECTURE: A CONCEPTUAL VIEW

Based on the results of previous and existing RC architecture, we propose a generic programmable gate array architecture to suit current digital designs. This contains an array of Programmable Black Box Cells (PBCs) connected through a low power interconnect switch with an intelligent shift register/cache system at the corners of the architecture. This acts like a boundary scan and sets the PBC control registers for maximum utilisation of PBC resources.

A hexagon interconnect structure is used as on-chip interconnect to provide fast communication between the PBCs. This provides a large degree of flexibility to dynamically route control signals in order to minimise the interconnect delay between the PBCs.

We also proposed a suitable routing architecture to suit our OFRL logic architecture.

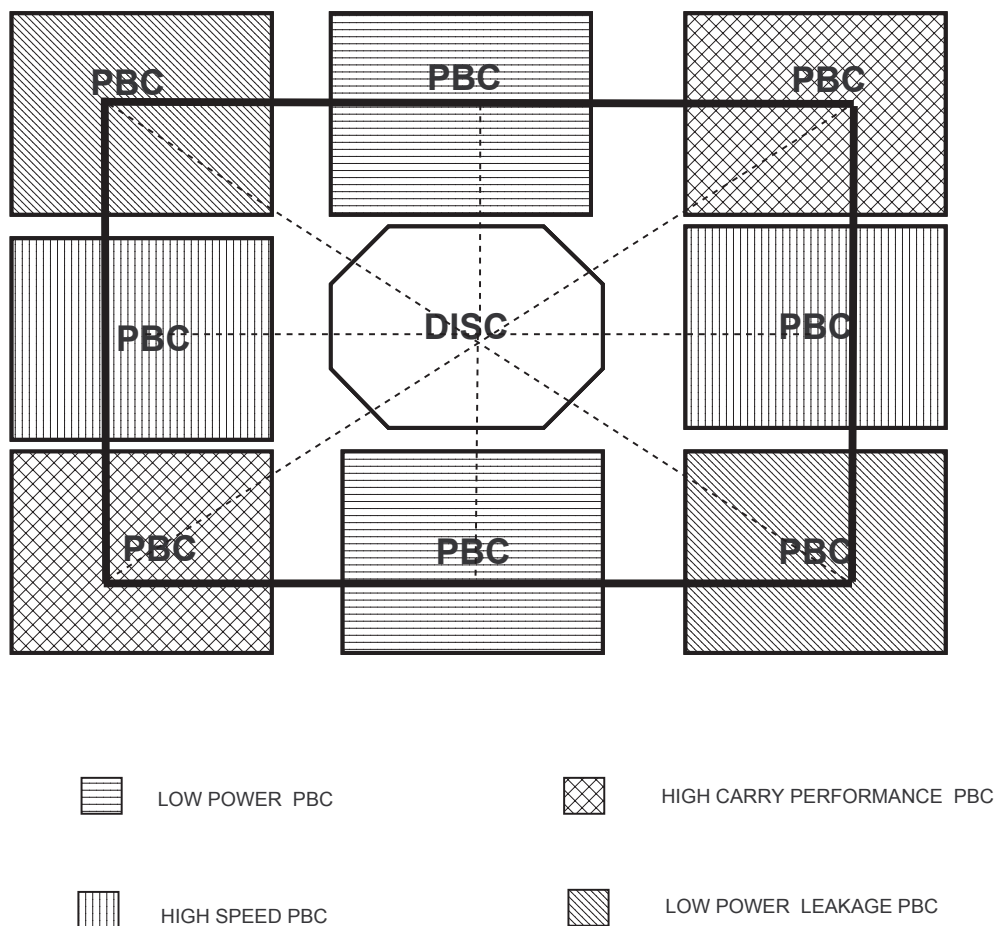


Figure 4. Conceptual diagram of the proposed OFRL architecture.

4.1. Programmable Black Box Cell (PBC)

Our proposed OFRL architecture contains four types of PBC. The PBC array consists of low power PBCs, high speed PBCs, low power leakage PBCs and high carry performance PBCs. Each PBC has a specially characterised array of Generic Function Gates (GFG). Each GFG has the ability to be dynamically configured as a NAND, NOR, OR, AND or XOR logic gate. Neuron-MOS^{1,28} may provide the functional behaviour of the GFGs and specially designed threshold gates^{1,26} may provide the reconfigurability.

4.2. Dynamic Interconnect Switch Core (DISC)

For the OFRL interconnect we propose a special switch called the “DISC” (Dynamic Interconnect Switch Core). This contains an array of programmable and dedicated interconnects to suit various high speed designs mapped to the device.

Fig. 4.2 shows that the DISC contains 3 types of interconnect. Dedicated interconnects are used between PBCs of the same type and are used for timing or retiming large designs. Programmable switch interconnects used to connect between diagonally located PBCs of different types. Routing mesh interconnects are fast interconnects designed to minimise the delay between PBCs during dynamic reconfiguration operation.

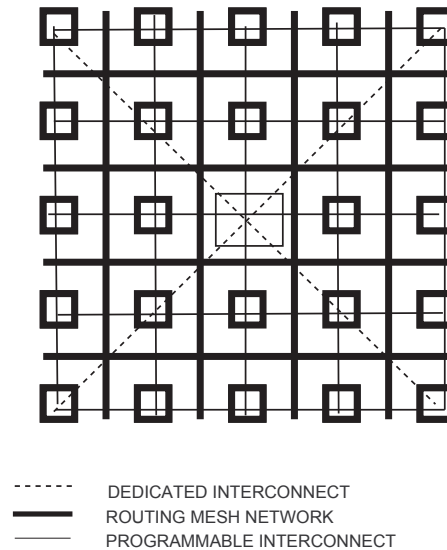


Figure 5. DISC: the proposed OFRL interconnect mesh architecture.

5. CONCLUSION

In the last few decades, increases in design complexity have increased the design implementation uncertainty of various applications, including some in genetics and space applications. This is expected to become a critical issue in the next decade. To meet the demand in evolvable hardware applications, reconfigurable devices have been developed to prototype designs. By reducing the design effort these make it possible to evaluate systems at a reasonable cost.

In this paper, we have proposed a new model to address drawbacks in current programmable devices. Our evaluation of existing reconfigurable cells shows that LUT and PLD based RC structures are superior to MUX based architectures in terms of speed and power consumption. Circuit analysis shows that the PLD approach is suitable for small designs and LUT based architectures are suitable for larger designs.

To overcome the software and hardware unfriendly environment of the FPGA world, we have proposed a model to achieve a maximum level of dynamic reconfiguration capability and maintain a closer correlation between software design mapper tools and hardware realisation for initial design entry. Once our device is integrated in the application environment, we aim to increase the self reprogrammable capability through hardware interrupts.

The features of our DRL devices will be highly utilised for applications such as bio-inspired devices, self repairing/testing space applications and evolvable hardware developments. They will provide low cost in terms of power, timing and area. Future work in this area will include a detailed simulation and virtual chip prototype of the proposed OFRL architecture. We also plan to develop a virtual run-time application environment to prove the DRL capability of our hardware model.

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