Investigation of Critical Slowing Down in a Bistable S-SEED

B. A. Clare, K. A. Corbett, K. J. Grant, P. B. Atanackovic, W. Marwood, and J. Munch

***Abstract*—A simulation of S-SEED switching based upon experimental data is developed that includes the effect of critical slowing down. The simulation's accuracy is demonstrated by close agreement with the results from experimental S-SEED switching. The simulation is subsequently used to understand how the phenomenon of critical slowing down applies to switching of an S-SEED and how the effect on photonic analog-to-digital (A/D) converter performance may be minimized.**

***Index Terms*—Critical slowing down, optical bistability, self-electrooptic-effect device (SEED).**

I. Introduction

THE ability to digitize directly the radio-frequency (RF) carrier of communication signals at high resolution is very desirable, as it avoids the use of an intermediate frequency that degrades the signal-to-noise ratio. Switching speed and clock jitter are two of the factors that limit the achievement of higher resolution and speed in state-of-the-art electronic analog-to-digital (A/D) converters [1]. Photonics offers devices that have properties superior to their electronic counterparts. These include high-speed switches [2], fast low-noise and low-jitter clocks [3], and interconnects with reduced sensitivity to crosstalk.

A photonic A/D was proposed in [4] that utilized self-electrooptic-effect devices [5] (SEEDs) constructed from multiple quantum well p-i-n diodes in an oversampled sigma–delta architecture. The sigma–delta architecture was chosen due to its suitability for a photonic implementation, as the required elements of a 1-bit comparator, subtractor, and logic gates had previously been demonstrated using SEEDs [6]–[8]. In [4], the subtractor utilized SEEDs in self-linearized mode, while the remainder of the design comprised electronics.

The proposed all-photonic design uses a 1-bit comparator consisting of two SEEDs in series (S-SEED) operating in bistable mode. As a consequence of bistability, the comparator will exhibit critical slowing down [7]. The phenomenon of critical slowing down causes the switching time to tend toward infinity when the bistable system is close to a transition, or critical point. This will have a deleterious effect upon the A/D operation, because an A/D accepts a continuous range of inputs. For inputs close to the transition points, critical slowing down will limit the response time of the comparator and cause output errors. Therefore, it is important to understand the variation of the switching time for values of parameters close to the critical ones.

In this paper, a model is developed to assist in the investigation of critical slowing down of a comparator based upon an S-SEED. Previous approaches to modeling S-SEED switching include those of [7] and [9]. In [7], a linear approximation to the differential equation of the S-SEED's equivalent circuit was used to derive an equation for the switching time. In [9], a piecewise linear approximation to the experimental responsivity curve of an MQW p-i-n diode was used to investigate switching behavior. However, neither of these approaches was accurate enough to quantitatively describe the effect of critical slowing down.

In our effort to include critical slowing down in a description of S-SEED switching, we include the measured device parameters of responsivity, dark current, and capacitance in a numerical solution of the full nonlinear circuit equation. To validate the simulation, we compare the results from a clocked switching experiment with the output of the simulation. The relevance of this comparison to a comparator is discussed in Section IV. We subsequently use the simulation to determine the parameters necessary to switch the S-SEED close to the critical points. The testing of the prediction with an S-SEED switching experiment reveals critical slowing down. We demonstrate a power-law dependence for the switching time near a critical point. Finally, the simulation is used to minimize critical slowing down and determine potential functions that aid in the understanding of the effect.

In this paper, we first describe the optical switching process in Section II, where attention is paid to the parameters affecting switching and the necessary switching conditions. Section III provides a description of the computer simulation and details of the experimental data that were used. The experiment used to verify the simulation is discussed in Section IV. Section V presents experimental and simulated results for the phenomenon of critical slowing down. Conclusions are given in Section VI.

II. Description of Optical Switching

To understand the switching process and the origin of critical slowing down, it is first necessary to consider the IV characteristics of the two MQW p-i-n diodes that form an optical switch, or comparator.

To create a bistable optical switch, we connect two SEEDs electrically in series with a voltage source to form what is known as a symmetric SEED (S-SEED) [8], as shown in Fig. 1.

This figure also shows that the S-SEED has two optical inputs P_{fixed} and P_{in}, two optical outputs P_{out1} and P_{out2}, and

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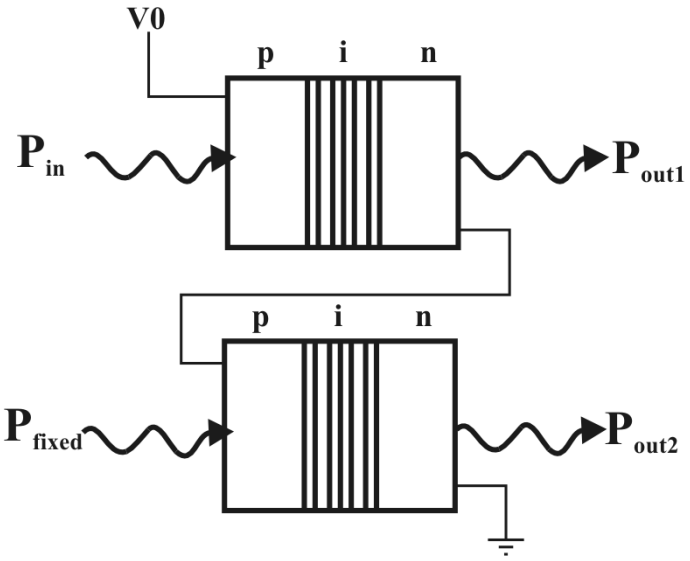

Fig. 1. Schematic of an S-SEED showing the voltage source V_0, the optical inputs $P_{\rm in}$ and $P_{\rm fixed}$, and the optical outputs P_{out1} and $P_{\rm out2}$.

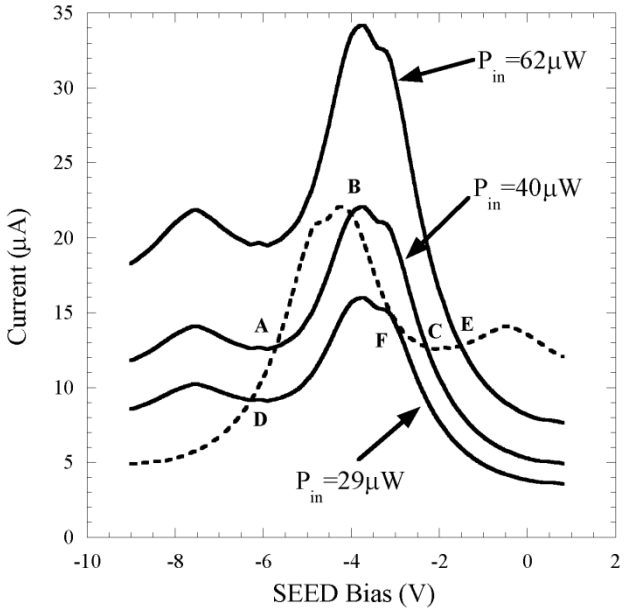

Fig. 2. Loadline plot that consists of IV curves for each of the devices in an S-SEED with $V_0 = -8$ V. The loadline is shown for three different values of $P_{\rm in}$ (solid) and one value of $P_{\rm fixed}$ (dashed).

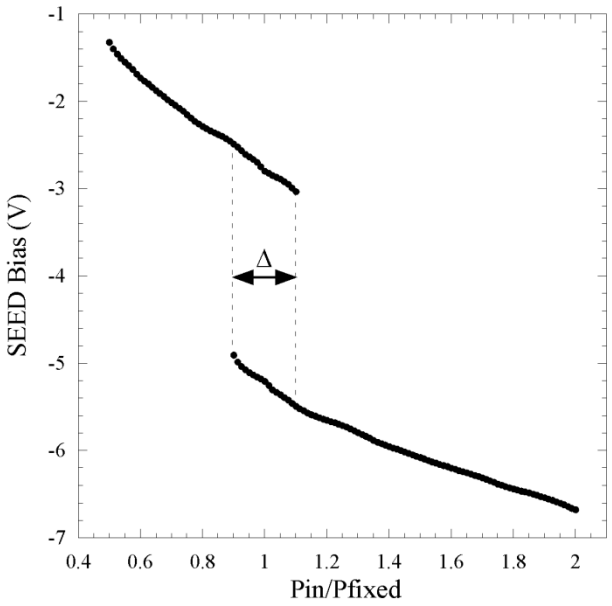

Fig. 3. Simulated plot of the solution of the circuit V against the input power $P_{\rm in}/P_{\rm fixed}$ for $V_0 = -8$ V, depicting hysteresis of width Δ.

a supply voltage V_0. The two optical inputs (pulsed or continuous wave beams) set the voltage and transmission state of the S-SEED. This can be understood by examining a loadline plot of the S-SEED, as shown in Fig. 2. The loadline plot shows experimentally measured IV curves for each device in the S-SEED. The IV curves acquire their shape from the quantum confined Stark effect (QCSE) [10], which is utilized to red shift the absorption peak as a function of electric field.

Fig. 2 illustrates the bottom device in Fig. 1, which experiences an applied voltage of V and an optical input of $P_{\rm fixed} = 40\ \mu$W, using a dashed line. The top device experiences $V_0 - V$ and is plotted for three different values of $P_{\rm in}$, as depicted with a solid line. Consider first the case of $P_{\rm in} = 62\ \mu$W, where the curves for the top and bottom devices intersect at the point labeled E in Fig. 2. Since the two diodes are in series, the same current must pass through each. Therefore, the intersection gives the solution of V for the S-SEED circuit. For the case of $P_{\rm in} = 40\,\mu{\rm W} = P_{\rm fixed}$, three intersections occur at the points labeled A, B, and C. Following the stability analysis presented in [7], the solution labeled B is found to be unstable, while the other two are stable. It is bistability, the existence of two distinct stable solutions to the circuit, that is exploited in the creation of an optical switch. Finally, consider the case of $P_{\rm in} = 29\ \mu$W where intersections occur at points D and F. The solution at point D is stable and in a region where only a single solution occurs, as was the case with point E. However, at point F the two curves touch tangentially as the stable and unstable solutions C and B converge. This implies that point F is on the edge of stability, and it is termed a critical point. By plotting the solution V as a function of the input power $P_{\rm in}/P_{\rm fixed}$, as done in Fig. 3, the ranges of each of the two stable solutions can be seen. The overlap of the two ranges results in hysteresis of width Δ, and at the limits of the overlap the critical points exist. Therefore, we find that due to the geometric nature of the switching points, to switch the S-SEED from $|V_{\rm low}|$ to $|V_{\rm high}|$, the input must be such that $P_{\rm in}/P_{\rm fixed} > (1/2)(\Delta+\sqrt{\Delta^2+4})$; and to switch in the opposite direction requires $P_{\rm in}/P_{\rm fixed} < (1/2)(-\Delta+\sqrt{\Delta^2+4})$.

III. Simulation Method

To provide a better understanding of the S-SEED switching behavior and to be able to predict the parameters necessary for an experiment, a computer simulation was developed. The simulation was based on the equivalent circuit model shown in Fig. 4, similar to those used in [9] and [11].

The model represents the p-i-n diode as a current source dependent upon voltage, optical power, and optical wavelength $I_{\rm photo}(V, P, \lambda)$. A voltage-dependent capacitor $C(V)$ and diode dark current $I_d(V)$ are added in parallel. We have found that the

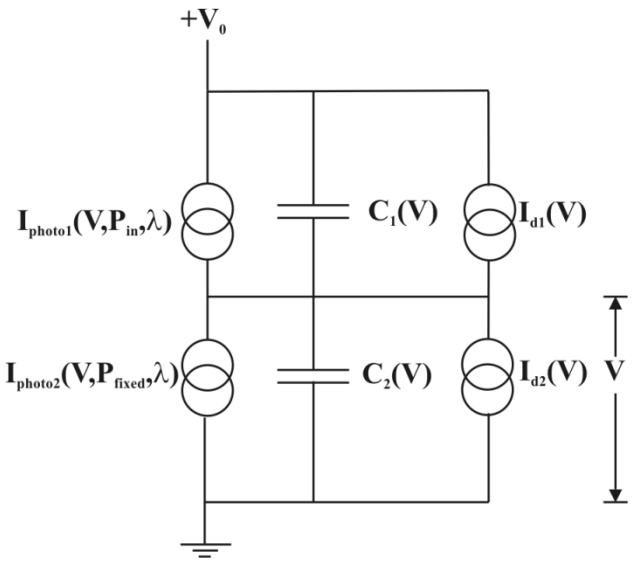

Fig. 4. Equivalent circuit model of an S-SEED. $I_{\text{photo}\,i}(V,P,\lambda)$ represents the voltage and wavelength dependent photocurrent, $C(V)$ the voltage dependent capacitance, and $I_d(V)$ the dark current of the diode.

diodes can become forward biased in an S-SEED, making the dark current an important component of the model.

Given the applied bias V_0 and optical inputs P_{in} and P_{fixed}, as depicted in Fig. 1, the application of Kirchoff's current law to the circuit shown in Fig. 4 yields the differential equation (2). The total current is defined in (1), and it is assumed that the photocurrent increases linearly with applied power (i.e., $I_{\text{photo}}(V,P,\lambda) = P\,S(V,\lambda)$, where S is responsivity)

$$I_{\text{total}}(V,\lambda) = P_{\text{in}}S(V_0 - V,\lambda) - I_{d2}(V) - P_{\text{fixed}}S(V,\lambda) + I_{d1}(V_0 - V) \quad (1)$$

$$\frac{dV}{dt} = \frac{I_{\text{total}}(V,\lambda)}{C_1(V_0 - V) + C_2(V).} \quad (2)$$

Where our simulation departs from those previously published is in the use of experimental data for $S(V,\lambda), C(V)$, and $I_d(V)$. The dark current was measured with a Keithley K236 source meter, and the capacitance with a HP 4279A CV meter. To measure $S(V,\lambda)$, the wavelength of light incident on an MQW p-i-n diode was stepped in increments of 0.3 nm, and at each value of λ the supply voltage was ramped from -9.0 to 0.9 V. The current was recorded at each step and divided by the incident power on the device. Dark current was subsequently subtracted to give responsivity. To perform this experiment, the following instruments were computer controlled via GPIB: Newport 2832C power meter, Burleigh WA1000 wavemeter, K236 source meter, and Coherent 899 Ti:sapphire laser.

The measured responsivity as a function of wavelength and applied bias is shown in Fig. 5, revealing the heavy hole (larger peak) and light hole exciton peaks. Fig. 5 shows how the QCSE reduces the magnitude and red shifts the wavelength of the excitons as the applied bias is increased.

To simulate the switching behavior of the S-SEED, it was necessary to solve (2) for $V(t)$. In order to represent our experimental data as accurately as possible, the data were linearly interpolated within the *Mathematica* environment to form what is

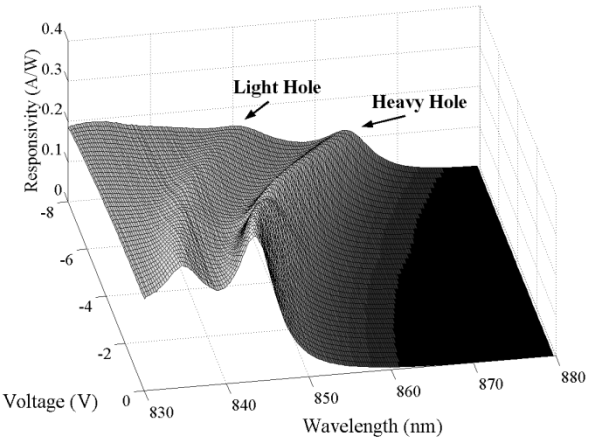

Fig. 5. Measured responsivity in A/W as a function of wavelength and applied bias.

termed an *interpolating function*. A numerical differential equation solving routine was applied, which implements Adam's or Gear methods, giving $V(t)$.

Results from the simulations are presented in the next section.

IV. Results

A clocked switching experiment was chosen to test the accuracy of the simulation. Such an experiment is most relevant to the optical A/D, as it simulates the comparison function [12]. In the clocked switching process, two different low power beams are compared by the S-SEED, which is set into one of two voltage states. Two equal high-power beams are then applied to read the state of the S-SEED, without switching the device. All the parameters affecting the switching process are included in the simulation, as demonstrated by excellent agreement between the simulation and experiment presented in the following section.

A. Experimental Setup

The molecular beam epitaxy (MBE)-grown MQW p-i-n diodes that constitute our S-SEED were designed with 50 $Al_{0.31}Ga_{0.69}As/GaAs$ quantum wells. To produce devices, 500 $\times$ 500 μm square mesas and ohmic contacts were fabricated. The entire growth structure is shown in Fig. 6.

The experimental setup for the clocked switching experiment is shown in Fig. 7. The tunable Ti:sapphire laser was coupled with a Cambridge Research & Instrumentation laser power controller to remove amplitude fluctuations. The beam was split into two: one arm providing the clock beam and the other supplying lower power signal levels. Polarizing beam splitters and halfwave plates were subsequently used to split each beam into P_{in} and P_{fixed} signals and to enable simple adjustment of the relative powers. Synchronized acoustooptic modulators were used to impart the signals on the beams. The typical input impedance of a SEED is approximately 10 MΩ. Therefore, to measure accurately the voltage across the SEED connected to ground on a Tektronix TDS520 oscilloscope, it was necessary to use an AD620 instrumentation amplifier with an input impedance of

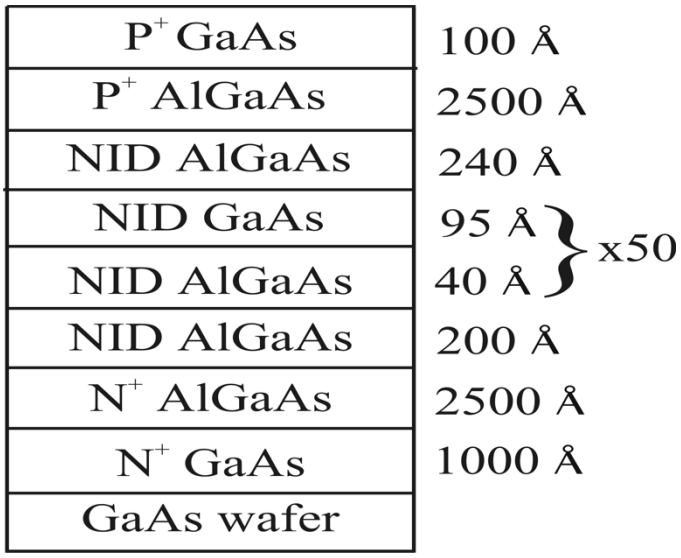

Fig. 6. Schematic of MBE grown p-i-n structure. The aluminum mole fraction of the AlGaAs layers is 31%. The active region contains 50 quantum wells of 95-A GaAs wells and 40-A AlGaAs barriers that are not intentionally doped.

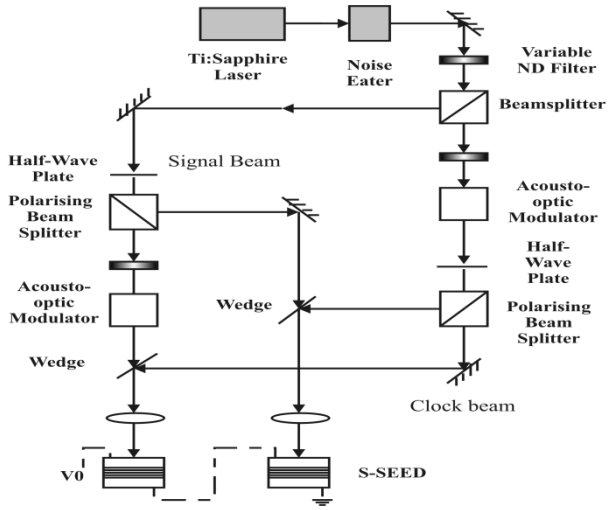

Fig. 7. Experimental setup for the clocked switching experiment.

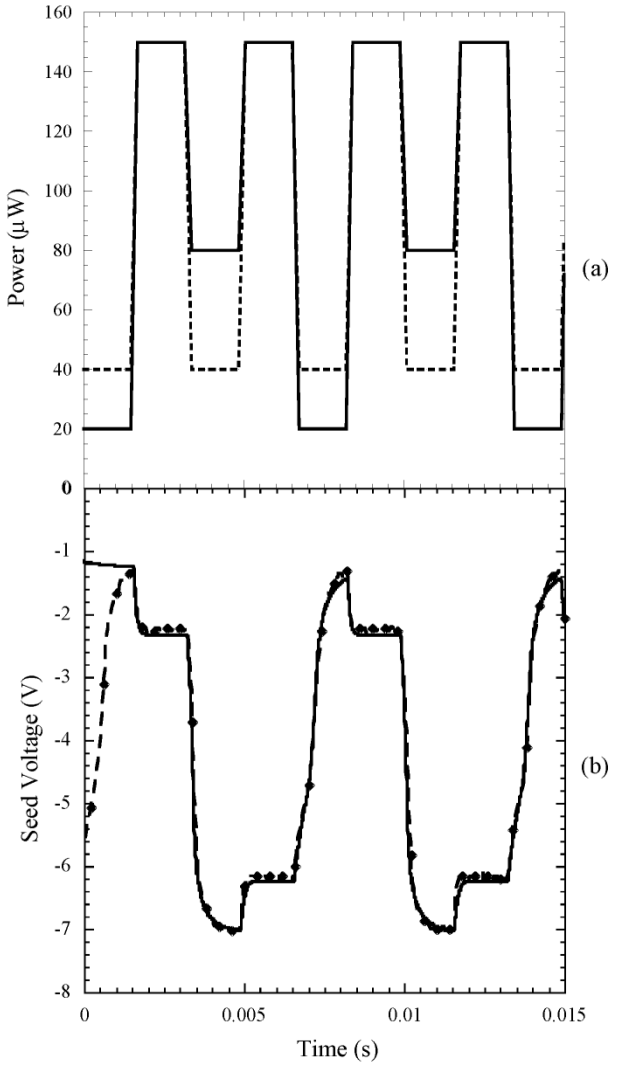

Fig. 8. (a) Timing diagram for the optical inputs $P_{\rm in}$ (solid line) and $P_{\rm fixed}$ (dashed line). (b) Comparison of the simulated (solid line) and experimental (dashed line with circles) results for V from the clocked switching experiment performed at a wavelength of 850 nm.

10 GΩ. As measured by the CV meter, the measurement equipment contributed 59 pF in parallel with the S-SEED. This additional contribution was included in the simulation.

B. Comparison of Simulation and Experiment

Experimental and simulated results for the clocked switching experiment are presented in Fig. 8. Fig. 8(a) plots the optical power applied to the top device $P_{\rm in}$ as a function of time with a solid line. $P_{\rm in}$ varies between two values used to set the state of the S-SEED that are interleaved with a much higher clock pulse. The dashed line in Fig. 8(a) represents the optical power applied to the bottom SEED $P_{\rm fixed}$, which is again interleaved with a clock pulse. The two clock pulses are of equal power and are used to read the state of the S-SEED. Fig. 8(b) shows the comparison of experimental (dashed with circles) and simulated (solid) measurements for the voltage across the bottom SEED (V) as a function of time.

To compensate for power meter drift, the values of $P_{\rm in}$ and $P_{\rm fixed}$ used in the simulation were allowed a 3% window of adjustment. Within this error, very good agreement is seen between experiment and simulation. Not only are the switching levels accurate, but so is the transient behavior. Therefore, the simple equivalent circuit of Fig. 4 has proven sufficient to achieve an accurate simulation of S-SEED switching. It should be noted that the very slow switching speed is due to the SEED's large capacitance, nominally 100 pF, and the relatively small difference in power between $P_{\rm in}$ and $P_{\rm fixed}$ of 20 μW [8].

Due to the slow switching speed, it was not necessary to model the effects on the transit time caused by tunnelling of the carriers through the quantum-well barriers, since the RC time constant dominates. However, even for much faster devices, others [13] have demonstrated that the RC time constant is the limiting factor in determining the switching speed for devices with thin barrier quantum wells. Therefore, we believe that this simulation technique is useful for accurately mod-

eling higher order structures, such as A/D architectures at significantly greater speeds.

V. Critical Slowing Down

As a stable system approaches an instability, a phenomenon known as critical slowing down often occurs, in which the system exhibits an extremely slow return to steady state upon perturbation. In the case of bistable systems, the effect of critical slowing down is to increase the system's switching time near the transition or critical points [19]. To understand this, consider the system

$$\frac{dV}{dt} = Q(V) \tag{3}$$

with the fixed point solution at V^*. That is

$$Q(V^*) = 0. \tag{4}$$

To determine the stability of V^*, we linearize (3) about V^* via a Taylor expansion to first order

$$\frac{dV}{dt} = Q(V) \simeq Q(V^*) + \frac{dQ}{dV}_{V=V^*}(V - V^*). \tag{5}$$

Now define $\xi = V - V^*$ and set

$$\lambda = \left.\frac{dQ}{dV}\right|_{V=V^*} \tag{6}$$

then

$$\frac{d\xi}{dt} = \lambda\xi \tag{7}$$

which has the solution

$$\xi(t) = \xi(0)e^{\lambda t}. \tag{8}$$

The parameter λ now determines stability. If $\lambda < 0$, then $\xi(t) \to 0$ as $t \to \infty$, which implies that V^* is a stable solution. However, if $\lambda > 0$, then $\xi(t) \to \infty$ as $t \to \infty$, which implies that V^* is unstable. Now consider the case $\lambda = 0$. Then $\xi(t) = \xi(0)$ and the system does not progress past its initial condition. From (7), we see that the velocity of the system $(d\xi/dt)$ tends to zero for the situation where $\lambda \to 0$, referred to as critical slowing down [19].

A. Results

To demonstrate the effect of critical slowing down, we performed an experiment similar to that of Section IV, with the omission of the clock pulses. By applying different optical powers to the two devices, the S-SEED was switched between two voltage states. The lower state was adjusted to reveal the effect of λ approaching zero. The experimental and simulated results are presented in Fig. 9 by points and lines, respectively.

The value of P_{fixed} was maintained at 100 μW, and the square wave applied to P_{in} varied between $P_{\text{in}}^H = 270$ μW and three different values of P_{in}^L, equal to 74, 81, and 83 μW, as depicted in Fig. 9. The figure demonstrates that the switching is much slower when P_{in}^L is equal to 83 μW compared to 74 μW. We can establish that critical slowing down is the cause of the decreasing switching speed by considering the λ parameter as a function of P_{in}^L. However, since the derivative of the interpolated

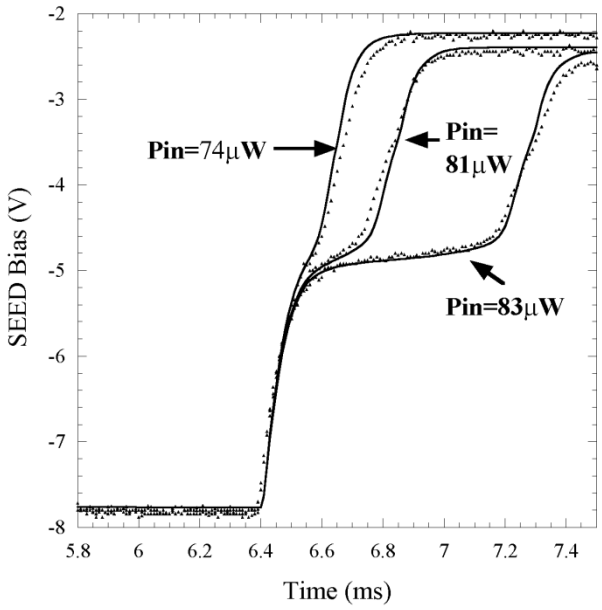

Fig. 9. Switching of S-SEED with $P_{\text{fixed}} = 100$ μW and P_{in} switched from 270 μW to the three different powers of 74, 81, and 83 μW to demonstrate critical slowing down. The solid lines represent the simulation, while experimental results are depicted with points.

data is only piecewise continuous, we were unable to calculate the behavior of the λ parameter from the experimental data. To demonstrate qualitatively the behavior of the λ parameter, we fit the responsivity data for a wavelength of 850 nm with an analytic function, given in (9)

$$S(V) = \beta_{\text{hh}} e^{(-0.5((V-\sigma_{\text{hh}})/\Gamma_{\text{hh}})^2)} + \beta_{\text{lh}} e^{(-0.5((V-\sigma_{\text{lh}})/\Gamma_{\text{lh}})^2)} + \alpha. \tag{9}$$

Equation (9) models the heavy hole (hh) and light hole (lh) excitonic responses as Gaussian curves, where Γ_i, β_i, and σ_i are the width, strength, and position of the excitons and α is a fitting parameter to represent the continuum absorption.

To find λ, (9) was first used to calculate the steady-state solution of (2). The solution was substituted into (6), yielding the results presented in Fig. 10(a).

Fig. 10(a) demonstrates how $\lambda \to 0$ at the critical points, which are identified by the dashed line at the limits of the hysteresis region from the accompanying curve in (b). Therefore, according to the definition of critical slowing down as discussed in the introduction to this section, the system exhibits a decay time approaching infinity in the vicinity of these critical points. Fig. 10(b) also includes steady-state solutions derived from experimental data, depicted using a thinner line, demonstrating the validity of (9). For illustrative purposes, Fig. 10(a) includes the unstable static solutions, which have positive values of λ.

An alternative quantitative method of describing critical slowing down, that also includes transient effects, is to consider a potential function. If we take (2) as an equation of motion for V [14], then the potential function $U(V)$ is defined as follows:

$$\frac{dV}{dt} = -\frac{\partial U}{\partial V}$$
$$U(V) = -\int_0^V \frac{I_{\text{total}}(V', \lambda)}{C_1(V_0 - V') + C_2(V')}\, dV'. \tag{10}$$

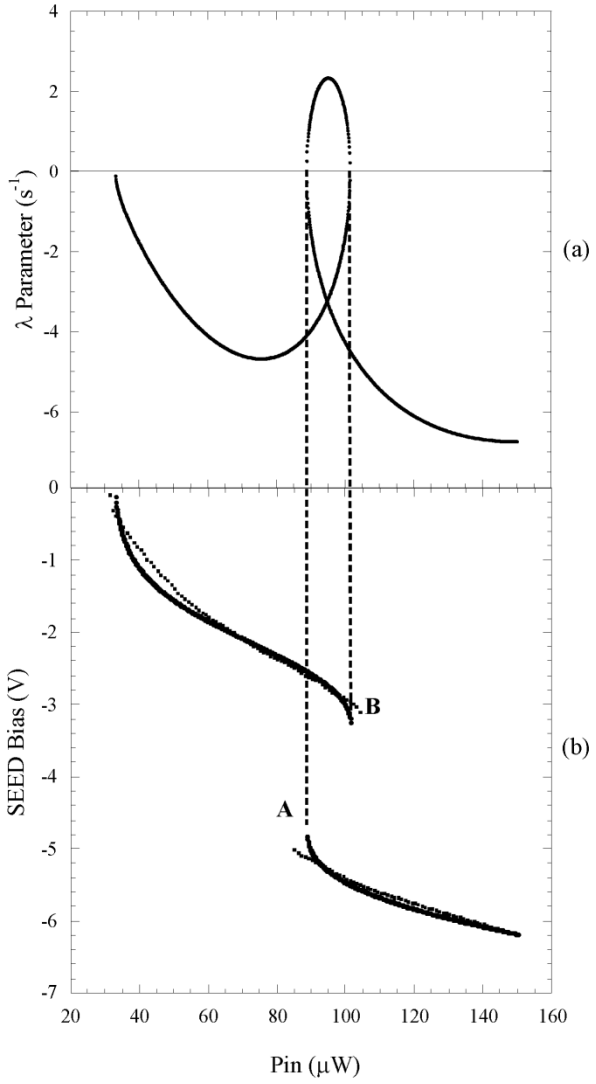

Fig. 10. (a) Graph of the values of λ as a function of $P_{\rm in}^L$, showing stable and unstable solutions with $\lambda > 0$. (b) Plot of the hysteresis curve, generated from stable voltage solutions for the fitted data, as per (9). Two devices of different peak responsivities were used, which caused the hysteresis region to shift from that depicted in Fig. 3. Overlaid in a thinner line is the corresponding result using experimental data. The critical points are marked with a dashed line and the labels A and B.

The potential function has a local minimum at a stable solution, and the slope of $U(V)$ determines the velocity and direction of movement of V. For this technique, critical slowing down is identified when $(dU/dV)(V) \rightarrow 0$ and V is not equal to a stable solution of the system. As this is a global definition, it has the advantage that it can be used to describe the transient behavior on both sides of the transition point.

For the switching experiment of Fig. 9, we can plot three potential function curves, as shown in Fig. 11. The three curves correspond to the values of $P_{\rm in}^L$ equal to 74 (dashed line), 81 (dot-dashed), and 83 μW (solid).

In the process of switching $P_{\rm in}$ from 270 μW to $P_{\rm in}^L$, the S-SEED voltage will traverse the path of the potential function from -7.8 V to the minimum at -2.25 V. Fig. 11 reveals that the slope of the potential function approaches zero as $P_{\rm in}^L$ is increased to 83 μW. Since the speed of the system traversing this

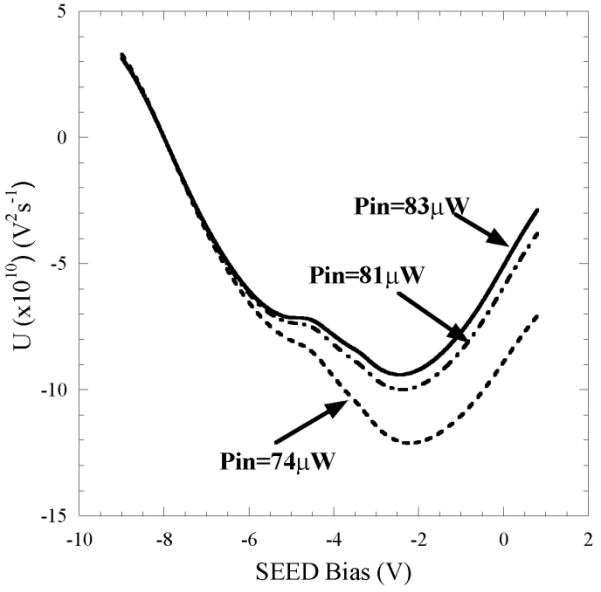

Fig. 11. Potential function $U(V)$ for three values of $P_{\rm in}$: 74, 81, and 83 μW. The stable solutions occurs around -2.3 V, and critical slowing down can be seen at -4.9 V.

curve is determined only by the slope, the system slows down around -4.9 V as $P_{\rm in}^L$ approaches the critical point labeled A in Fig. 10(b). Thus the potential function shows that the S-SEED experiences critical slowing down and demonstrates the cause of the effect. Increasing $P_{\rm in}^L$ further so that $P_{\rm in}^L$ lies in the hysteresis region, will produce two local minima in $U(V)$. Following the treatment of [19] for optical bistability, the presence of two local minima indicates that the system is analogous to a first-order phase transition in a nonequilibrium situation, for which critical slowing down has been demonstrated [18], [19].

An experimental technique to demonstrate that the S-SEED is experiencing critical slowing down is to measure the switching time as a function of $P_{\rm in}^L$. The switching time was defined as the time taken for the system to get from the initial voltage state V_i to 95% of the the final voltage state V_f, labeled as $V_{\rm switch\ criterion}$ in (11). The experiment represented in Fig. 9 was repeated with several values of $P_{\rm in}^L$ ranging from 55 to 83 μW, and the switching times were measured directly from the plotted experimental switching data. The results are presented in Fig. 12

$$V_{\rm switch\ criterion} = V_i + 0.95 \times (V_f - V_i). \tag{11}$$

The data of Fig. 12 are fitted with a function of the form

$$t_s = a + \frac{b}{\sqrt{|P_{\rm critical} - P_{\rm in}|}} \tag{12}$$

where a and b are fitting parameters. References [15]–[17] demonstrate that the critical slowing down in optical bistability follows the form given in (12).

Finally, the simulation was used to study how variation of V_0, which alters the hysteresis width, affects the critical slowing

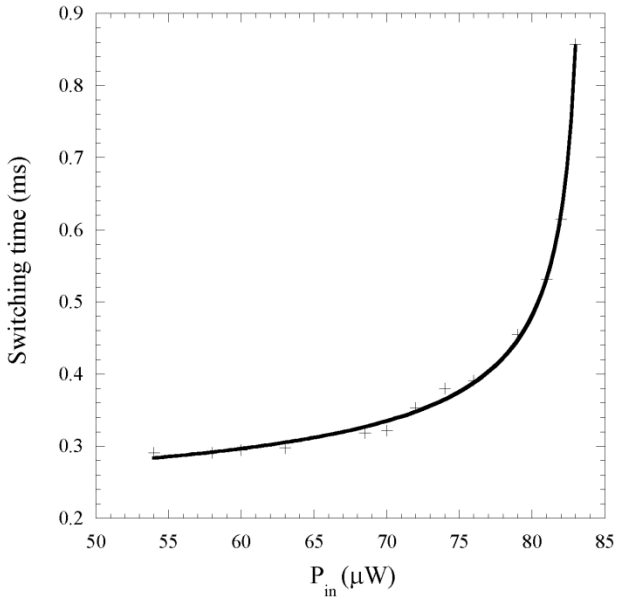

Fig. 12. S-SEED switching time, as defined in the text, as a function of $P_{\text{in}_{\text{low}}}$. A power law as described by (12) is fitted to the data with a high degree of correlation ($R^2 = 0.998$).

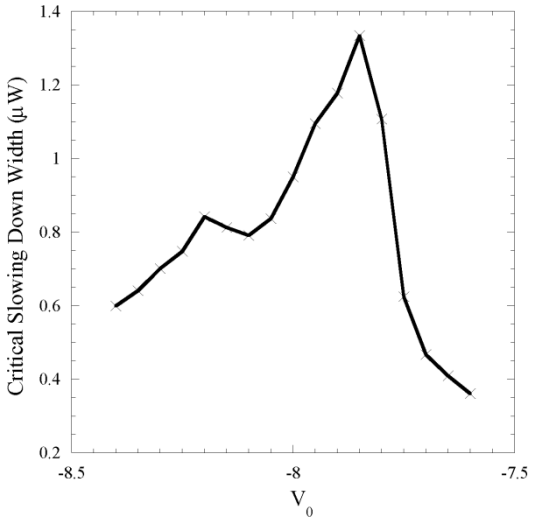

Fig. 13. Width of the input region over which critical slowing down will have a significant effect on the switching time, as a function of V_0.

down behavior. To determine the switching time, the following integration was performed numerically:

$$t_s = \int_{V_i}^{V_{\text{switch criterion}}} \frac{C_1(V_0 - V) + C_2(V)}{I_{\text{total}}(V, \lambda)}\, dV. \qquad (13)$$

An arbitrary threshold switching time was defined to be 0.7 ms. The difference between the value of P_{in}^L at the threshold P_{thres} and the value of P_{critical} was calculated and plotted as a function of V_0 in Fig. 13. The value P_{critical}-P_{thres} determines the range of comparator input powers where the switching time is slower than the defined threshold and therefore problematic.

Fig. 13 demonstrates that the range of values of P_{in} where critical slowing down has a significant effect on device performance can be reduced by optimizing the bias applied to the S-SEED.

VI. Conclusion

We have developed an accurate model of the switching of an S-SEED in which the differential equation for the circuit of an S-SEED was solved numerically. Included were the effects of dark current and voltage dependent device capacitance. The degree of accuracy of this approach is determined by the quality of the measured parameters. We have shown that with our measured data, the agreement between simulation and experiment is excellent.

The phenomenon of critical slowing down was experimentally demonstrated. The model was then used to replicate the results and describe the effect. Since this is not a desirable effect for an A/D, the simulation was used to find values of a parameter that minimizes this effect. Future work is planned to simulate a photonic sigma–delta A/D by extending our simulation of S-SEED switching.

References

[1] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Select. Areas Commun.*, vol. 17, pp. 539–550, 1999.

[2] D. K. Serkland, I. J. Fritz, C. T. Sullivan, J. H. Burkhart, and J. F. Klem, "Fast-switching symmetric self-electrooptic-effect device at 865 nm," in *Proc. CLEO 2000 Ann. Meeting*, pp. 381–382. paper CWU4.

[3] T. R. Clark, T. F. Carruthers, P. J. Mathews, and I. N. Duling III, "Phase-noise measurements of ultrastable 10 GHz harmonically mode-locked fiber laser," *Electron. Lett.*, vol. 35, pp. 720–721, 1999.

[4] B. L. Shoop, "Optical oversampled analog-to-digital conversion," Ph.D. dissertation, Stanford Univ., 1992.

[5] D. A. B. Miller, "Quantum well self-electro-optic effect device," *Opt. Quantum Electron.*, vol. 22, pp. S61–S98, 1990.

[6] E. A. De Souza, L. Carraresi, G. D. Boyd, and D. A. B. Miller, "Self-linearized analog differential self-electro-optic-effect device," *Appl. Opt.*, vol. 33, pp. 1492–1497, 1994.

[7] D. A. B. Miller, D. S. Chemela, T. C. Damen, T. H. Wood, C. A. Burrus Jr., A. C. Gossard, and W. Wiegmann, "The quantum well self-electrooptic effect device: Optoelectronic bistability and oscillation, and self-linearized modulation," *IEEE J. Quantum Electron.*, vol. QE-21, pp. 1462–1476, 1985.

[8] A. L. Lentine, H. S. Hinton, D. A. B. Miller, J. E. Henry, J. E. Cunningham, and L. M. F. Chirovsky, "Symmetric self-electrooptic effect device: Optical set-reset latch, differential logic gate, and differential Modulator/Detector," *IEEE J. Quantum Electron.*, vol. 25, pp. 1928–1936, 1989.

[9] L. M. Loh, J. L. LoCicero, and A. L. Lentine, "S-SEED switching characteristics," *J. Lightwave Technol.*, vol. 12, pp. 2122–2130, 1994.

[10] D. A. B. Miller, D. S. Chemla, T. C. Damen, A. C. Gossard, W. Weigmann, T. H. Woods, and C. A. Barrus, "Band-edge electroabsorption in quantum well structures: The quantum-confined stark effect," *Phys. Rev. Lett.*, vol. 53, pp. 2173–2176, 1984.

[11] A. L. Lentine, "Circuit model of a multiple-quantum-well diode," *Appl. Opt.*, vol. 33, pp. 1376–1379, 1994.

[12] S. F. Al Sarawi, P. B. Atanackovic, W. Marwood, B. A. Clare, K. A. Corbett, K. J. Grant, and J. Munch, "Differential oversampling data converters in SEED technology," *Microelectron. J.*, vol. 33, pp. 141–151, 2002.

[13] G. D. Boyd, A. M. Fox, D. A. B. Miller, L. M. F. Chirovsky, L. A. D'Asaro, J. M. Kuo, R. F. Kopf, and A. L. Lentine, "33 ps optical switching of symmetric self-electro-optic effect devices," *Appl. Phys. Lett.*, vol. 57, pp. 1843–1845, 1990.

[14] M. Hosoda, K. Kawashima, K. Tominaga, T. Watanabe, and K. Fujiwara, "A global stability analysis for symmetric self-electrooptic effect device systems using a potential function method," *IEEE J. Quantum Electron.*, vol. 31, pp. 954–961, 1995.

[15] G. Grynberg and S. Cribier, "Critical exponents in dispersive optical bistability," *J. Phys. Lett.*, vol. 44, pp. L-449–L-453, 1983.

[16] S. Cribier, E. Giacobino, and G. Grynberg, "Quantitative investigation of critical slowing down in all-optical bistability," *Opt. Commun.*, vol. 47, pp. 170–172, 1983.
[17] H. A. Al-Attar, H. A. MacKenzie, and W. J. Firth, "Critical slowing-down phenomena in an InSb optically bistable etalon," *J. Opt. Soc. Amer. B*, vol. 3, pp. 1157–1163, 1986.
[18] R. Bonifacio and P. Meystre, "Critical slowing down in optical bistability," *Opt. Commun.*, vol. 29, pp. 131–134, 1979.
[19] E. Abraham and S. D. Smith, "Optical bistability and related devices," *Rep. Prog. Phys.*, vol. 45, pp. 815–885, 1982.

B. A. Clare, photograph and biography not available at the time of publication.

K. A. Corbett, photograph and biography not available at the time of publication.

K. J. Grant, photograph and biography not available at the time of publication.

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