High Quality Micromachined Inductors for Integrated Communication Systems

A Dissertation Submitted to the Faculty of Sciences of the University of Neuchâtel, in Fulfillment of the Requirements for the Degree of "*Docteur ès Sciences*"

by

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High Quality Micromachined Inductors for Integrated Communication Systems

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FACULTE DES SCIENCES

La Faculté des sciences de l'Université de Neuchâtel,
sur le rapport des membres du jury

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autorise l'impression de la présente thèse.

Neuchâtel, le 4 juillet 2006

Le doyen :

J.-P. Derendinger

To my mother, Loredana
and my father, Roberto

ABSTRACT

Low power consumption is certainly one of the most stringent requirements to be met by new generation wireless communication systems. The quality factor (Q-factor) displayed by the numerous passive components of RF front-end transceivers plays a fundamental role on the overall power consumption of the portable electronic devices. Inductors, either in discrete or integrated form, are essential passive components of every RF front-end. They perform critical functions in radio-frequency integrated circuits (RFIC's), such as low noise amplifiers (LNA's), voltage controlled oscillators (VCO's), impedance matching networks, passive filters and baluns. A high Q-factor is of utmost importance since it contributes to reduce phase noise in oscillators, power consumption in amplifiers and insertion loss in filters. Generally, the Q-factor exhibited by on-chip inductors fabricated in standard IC technologies is drastically limited by RF power dissipation through the semiconducting silicon substrate and by the increase of the metal resistance as a consequence of the skin and proximity effects.

The work reported in this thesis addresses the fabrication and characterization of high-performance miniaturized planar inductors fabricated with innovative and low-thermal budget micromachining processes. Skin and proximity effects in the metal tracks have been addressed by providing highly conducting thick layers of sputter deposited Al or electroplated Ag, and by designing circular and hollow spirals, respectively. On the other hand, energy dissipation in the substrate has been mitigated by using low-loss substrates, such as high-resistivity Si (HRS) or Pyrex.

An empirical study of inductor performances has been carried out in order to shed light on the role played by the type of substrate, spiral conductivity and layout parameters. Inductors fabricated on Pyrex achieve better performances, in terms of Q-factor and self-resonance, than their counterparts implemented on HRS. Particularly, peak-Q values exhibit an improvement up to 40%, with a concomitant increase of f_{SR} by about 1-2 GHz. A Q-factor of 50 at 4.5 GHz and a self-resonance above 10 GHz have been exhibited by a 5 nH inductor implemented on Pyrex with a 12 µm-thick Ag spiral; while, a peak-Q of 38 has been obtained from an inductor with identical layout fabricated with a 8 µm-thick Al spiral.

Measured data of inductors have been accurately matched using an equivalent compact model based on frequency-independent elements. Accurate matching of measured performances have also been provided by full-wave EM simulations.

In general, the measured performances challenge those exhibited by state-of-the-art micromachined inductors with similar inductance values. Moreover, the proposed planar geometry is more robust compared to reported developments of suspended or out-of-plane assembled architectures and consequently can withstand violent mechanical shocks and vibrations and also simplifies the packaging procedure of the final device.

A library of 500 inductors ranging from 0.5 to 20 nH has been established. With the insight gained from the various trends issued from the analysis of experimental data, a set of design rules aiming at the improvement of the performances from a layout point of view has been delineated. In addition, the study of inductor performances as a function of the layout parameters has made possible to design inductors tailored for a given inductance value. The RF characterization of these optimized inductors has pointed out inductance values falling within 5% of their predicted value.

As a further step of the research, lumped-element baluns have been fabricated by co-integrating optimized inductors with MIM capacitors so as to form low-pass and high-pass filter sections. The proposed baluns are designed for operating in a 50 Ω-single-ended/100 Ω-balanced environment and target the ISM frequency band (2400-2480 MHz). Typical values of amplitude imbalance obtained within the frequency band of interest are 0.45-0.55 dB and the corresponding phase imbalance is less than 2°. The reflection loss at the single-ended port, S_{11} is generally better than -20 dB. The single-to-differential insertion loss, S_{ds21} ranges from -0.8 to -1.0 dB. In general, these performances are comparable to published results concerning micromachined baluns of similar type.

In conclusion, the promising performances obtained from the proposed inductors and baluns make these devices well-suited building-blocks for implementing low-power wireless communication systems.

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CHAPTER 1

INTRODUCTION

WIRELESS communications systems, such as cellular phones, pagers, and global positioning systems (GPS) are familiar and successful examples of the enormous growth experienced by the consumer market over the last ten years. The success of today's handsets is strongly related to the cost, battery lifetime, functionality and weight. The increasing demand for ever more sophisticated products has spurred the manufacturers to develop new solutions for increasing integration and miniaturization of the front-end transceivers, in order to reduce power consumption, increase functionality, reduce size and cost.

Today a situation has been reached where the presence of a multitude of rather cumbersome off-chip passive components, such as inductors, baluns, capacitors, varactor diodes, surface acoustic wave (SAW) and ceramic filters, represents a bottleneck against further miniaturization of radio-frequency (RF) transceivers [1]. In fact, these passive components are currently implemented on the PCB in discrete form. They are not directly integrated onto the IC's because the standard microelectronics technologies do not enable the fabrication of the well-controlled, high-Q elements required by RF applications. This problem is particularly acute in the case of inductors. Inductors are extensively used in RF front-end circuits. They play a key role many applications, such as voltage controlled oscillators (VCOs),

low-noise amplifiers (LNAs), LC filters and impedance matching networks. However, inductors integrated in today's typical silicon processes cannot meet the high performance specification required for RF IC's. For this reason, their off-chip counterpart are still widely used in applications where a high Q-factor is needed. An additional huge drawback of using discrete components is that their assembling in a complete system represents a significant part of the total cost of the final product.

A solution for increasing the level of integration and miniaturization would be the fabrication of circuit blocks and passive elements on the same substrate using a single technology. In recent years, silicon-based technologies have found a wide range of applications in the GHz-range and consequently have emerged as a cost-effective choice for RF front-end circuits [2, 3].

Since the late 70's, single crystal Si has become increasingly available for the rapidly growing IC's industry. This has favoured the advent of micromachining technologies developed for microelectromechanical systems (MEMS) [4] and has made possible the fabrication of miniaturized mechanical structures, devices and systems. A few of the advantages inherent to the MEMS technology include cost reduction through batch fabrication, high level of device reproducibility through advanced lithography and etching techniques, and access to the third dimension, including the ability to create free-standing structures. In addition, by using materials such as silicon and fabrication techniques compatible with IC's technology, MEMS components can be monolithically integrated with electronics. Compared with other more mature MEMS technology fields [4], RF MEMS (or MEMS for radio-frequency applications) is relatively new, but has already generated a great interest [5]. RF MEMS technology is currently under development in a large number of laboratories around the world. Important advantages that this technology can offer are the potential to build a multitude of miniaturized components such as switches, phase shifters, tunable capacitors, inductors, bulk acoustic wave (BAW) resonators and micromechanical resonators [6, 7]. To date, however, only BAW resonators have become a high-volume product. These devices are based on a thin film of piezoelectric aluminum nitride (AlN) vibrating in a thickness resonance mode and exhibit very large Q-factors [8, 9]. Miniature BAW resonators are mostly used for implementing duplexers, receive (RX) and transmit (TX) filters of cell phones [10, 11]. The integration of BAW devices with RF IC's can be realized either using a system-in-package (SiP) procedure [11], or with a monolithic approach enabled by the similar thermal budget involved in the fabrication process of RF IC's and BAW filters [12].

From a more general point of view, the advent of the BAW technology has made possible to get rid of the bulky ceramic front-end filters, SAW filters and the lossy LC tanks.

In conclusion, by combining standard IC's with MEMS technology, a complete communication system could be reduced to a multi-chip module made of an RF IC, a digital IC and a chip bearing all the high-Q components. Such system-on-a-chip (SoC) approach could be foreseen as a first step toward a cheap, miniaturized, and low-power consumption platform dedicated to the present and next-generation wireless communication systems.

1. 1 Aim of the research

The work presented in this thesis is foreseen as a first step toward the realization of a miniaturized multichip module obtained by co-integrating BAW filters with either micromachined inductors, or with more complex circuits such as lumped-element baluns.

In the first case, monolithic inductors could be used for tuning the resonance frequency of single resonators and extend the passband of the filter without recurring to off-chip inductors [13, 14].

Whereas, in the second case, micromachined baluns would be cascaded to differential BAW filters so as to fulfill different functions in a RF front-end transceiver depending on its configuration. Examples of applications that can be envisioned are the use of a balun between the single-ended output of the antenna and the first bandpass filter in the Rx path, or the use of a balun between the single-ended output of the LNA and the following filter. From this perspective, micromachined baluns could be used for replacing integrated or surface mount LTCC baluns.

The first goal of the research is the fabrication of high-Q inductors by means of micromachining processes. High-frequency dissipation mechanisms that traditionally limit the performance of integrated inductors are addressed by providing thick conductor layers and by using low-loss substrates, such as high-resistivity Si or Pyrex. As a further step, inductors tailored for a given inductance value are used for implementing balun circuits.

1. 2 Organization of the thesis

The first part of Chapter 2 gives an overview of the energy dissipation mechanisms that manifest whenever an inductor is operated at RF frequencies. These dissipation mechanisms, namely metal losses and substrate losses, ultimately degrade the achievable performances of RF inductors in terms of Q-factor and self-resonant frequency. It is shown how the high-frequency losses in metal tracks, that manifest themselves as skin and proximity effect, can be successfully addressed by a proper choice of the conductor thickness (for a given operating frequency) and by an appropriate design. The second part of the chapter outlines various well-established or currently investigated methods available for circuit designers in order to mitigate or even overcome the various forms of power dissipation. Furthermore, the state-of-the-art of RF inductors, based on the most promising published performances, is delineated in the last part of the chapter and will constitute a reference for comparing the performance obtained by the inductors fabricated in this work.

Chapter 3 presents the development of three simple and low-thermal budget micromachining processes enabling the fabrication of high-Q monolithic planar spiral inductors. The essential features of the first process are the use of thick sputter deposited aluminum films patterned by a highly anisotropic dry-etching process. Al films with different thickness have been characterized in terms of electrical conductivity and residual stress in order to assess their reliability.

The second process based on Ag electroplating into thick polymer molds has been investigated since electroplating traditionally enables the fabrication of very thick metal films. This characteristic is especially well-suited when a drastic reduction of the DC resistance is desired. Ag has been preferred over Cu due to its higher bulk conductivity.

A third processing route involving a post-processing step of surface micromachining by means of HF vapor phase etching has been developed for the fabrication of suspended aluminum structures. The attractiveness of HF vapor phase etching resides in the suppression of stiction phenomena of the released structures. Although the robustness inherent to a monolithic planar structure is partially sacrificed, the main advantage of a suspended architecture is a reduction of the parasitic capacitive coupling to the substrate. Therefore, this process potentially opens a new perspective toward the fabrication of post-CMOS

compatible inductors, even tough direct integration of micromachined inductors on CMOS substrates is not the primary concern of this thesis.

Chapter 4 focuses on the RF characterization of inductors fabricated using the processing routes described in Chapter 3. Particularly, numerous inductors have been designed for covering the inductance range going from 0.5 to 20 nH. An empirical study of inductor performances has been conducted as a function of the substrate type, spiral conductivity, layout parameters and spiral geometry. This study has been motivated by the need to establish accurate design rules enabling the fabrication of optimized inductors tailored for a given inductance value. Such optimized inductors will constitute the building-blocks for more complex circuits such as lumped-element baluns.

Chapter 5 deals with electromagnetic (EM) simulation of inductors. Since in general simulation is a rather time-consuming procedure, the aim of the presented work is primarily dedicated to the development of necessary knowledge enabling to get fast an accurate matching of measured data. The establishment of a set of optimum simulation conditions will thus help for an efficient simulation procedure of more complex and memory-demanding circuits, such as lumped-element baluns. Furthermore, EM simulation represents a very useful tool for providing physical insight on the role played by the material properties on the achievable performance and for taking into account parasitic coupling phenomena that cannot be easily modeled with circuit simulators.

Chapter 6 presents the essential issues of design, fabrication and characterization of lumped-element baluns obtained by co-integrating optimized inductors with metal-insulator-metal (MIM) capacitors so as to form low-pass and high-pass filter sections. The proposed baluns target the ISM frequency band (2400-2480 MHz) and are designed for operating in a 50 Ω-single-ended/100 Ω-balanced environment. The formalism of mixed-mode S-parameters is introduced and exploited since it enables a rigorous characterization of the behavior of a balanced device. The measured performances will be compared to those exhibited by reported similar types of micromachined baluns and also by commonly used baluns implemented with LTCC technology. The last part of the chapter deals with EM simulation of baluns.

Concluding remarks and perspectives are summarized in Chapter 7.

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CHAPTER 2

STATE-OF-THE-ART OF RF INDUCTORS

SINCE RF inductors implemented in standard silicon processes suffer from poor Q-factors, as a consequence of physical phenomena that convert electromagnetic energy into heat, RF IC's requiring better quality factors, still rely on off-chip discrete inductors. Over the past two decades, intensive research efforts have been made aiming at the improvement of the performance of on-chip spiral inductors in terms of Q-factor and self-resonant frequency. The large amount of published studies witnesses the fact that the implementation of high-Q inductors largely remains an empirical affair because the inductor performances are strongly related to the operating frequency and to the properties of the materials involved in the specific fabrication processes. Material properties include the conductivity of metals layers and substrate, and the permittivity and loss tangent of dielectrics. In addition, the layout parameters and the inductor footprint also play an important role on the achievable performance.

The first part of the chapter gives the definition of the inductor Q-factor. The second part addresses the two main classes of power dissipation mechanisms, namely metal losses and substrate losses, that degrade the performance of on-chip

RF inductors. A literature review discussing various techniques available for mitigating or even suppressing the loss mechanisms is presented in the last part of the chapter. Here, the most promising performances currently establishing the state-of-the-art of RF inductors are summarized.

2. 1 Inductor Q-factor

Inductors with high Q values are necessary for designing RF circuits with low insertion loss, low noise, high gain and good frequency selectivity [1]. The Q-factor of an inductor is an index of the stored electromagnetic energy versus dissipated energy [2] :

$$Q = 2\pi \cdot \frac{\textit{energy stored in the inductor}}{\textit{energy lost in one oscillation cycle}} \tag{2.1}$$

The above definition does not specify what stores or dissipates the energy. However, for an inductor, only the energy stored in the magnetic field is of interest. Any energy stored in electric fields due to parasitic capacitances is thus counterproductive and will degrade the achievable Q-factor. Therefore, the energy stored in the inductor is equal to the difference between the peak of magnetic and electric energies :

$$Q = 2\pi \cdot \frac{|W_m| - |W_e|}{P_{diss}} \tag{2.2}$$

where W_m and W_e are the peaks of magnetic and electric energy stored in the inductor, and P_{diss} is the power dissipated. From (2.2) the self-resonant frequency, or f_{SR}, of the inductor corresponds to the frequency where the peaks of magnetic and electric energy are equal. Consequently, Q drops to zero at f_{SR} and the impedance of the inductor turns capacitive if the operation frequency exceeds f_{SR}. The self-resonant frequency is the upper bound for an inductor to be functional, its value is determined by the parasitic capacitances resulting from the coupling to the substrate and between metal traces.

The traditional approach for obtaining Q from RF measurements involves the computation of :

$$Q = \frac{Im(Z)}{Re(Z)} \cong \frac{|X_L|}{R_s} = \frac{\omega L_s}{R_s} \qquad (2.3)$$

where Z is the input impedance of the inductor derived from the measured scattering parameters. At low frequency, the quality factor is well described by the ratio $\omega L_S/R_S$; however, as the frequency increases, Q starts to deviate from $\omega L_S/R_S$ due to substrate effects, which account for various forms of energy dissipation. Furthermore, as the frequency continues to increase, the self-resonance effect becomes increasingly important due to the increase in the peak of electric energy stored in the capacitor formed between the spiral and the substrate. The self-resonant frequency corresponds to the point where Im(Z) is zero. Despite (2.3) has the drawback to deliver a Q of zero at f_{SR}, this definition is meaningful when the inductor is operated well below its self-resonance.

2. 2 Dissipation mechanisms

2. 2. 1 Metal losses

The resistance of a spiral inductor is frequency-dependent due to magnetically induced eddy currents in the metal traces, that manifest themselves as *skin* and *proximity* effects [3, 4]. Skin effect losses arise from the magnetic field due to the self-inductance of a metal trace, which pushes moving charges away from the field lines and concentrate those charges to a confined portion at the outer skin of the conductor. Moreover, due to the close proximity between conductor segments in a spiral inductor, the current in each segment can induce eddy currents in other segments causing a non-uniform current flow across the trace width. The consequence of skin and proximity effects is addictive and cannot easily be distinguished. However, the net result produced by these effects is an effective reduction of the cross-sectional area of the conductor. This, in turn increases the high-frequency resistance of the metal traces and lowers the achievable Q-factor.

2. 2. 1. 1 Skin effect

The current density in a conductor is uniform in DC mode since its entire cross-sectional area is available for the transport of charge carriers. The DC resistance of a conductor with rectangular cross sectional area is given by :

$$R_{DC} = \frac{\rho \cdot l}{w \cdot t} \tag{2.4}$$

where ρ is the metal resistivity, l, w and t represent the dimensions of the conductor, i.e., the length, width and thickness, respectively. However, as the frequency increases, the concomitant increased magnetic field at the core of the conductor presents an impedance to the charge carriers, thus decreasing the current density at the core of the conductor and increasing the current density around its perimeter [5]. The current density reaches its maximum value (100%) at the conductor surface and decays in amplitude exponentially with the distance from the surface. The depth into the conductor at which the current density has decreased to $1/e$ (or 37%) of its surface value is known as the skin depth, δ, and is expressed by :

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu \cdot f}} \tag{2.5}$$

where ρ is the metal resistivity [Ω·m], $\mu=\mu_0 \cdot \mu_r$ is the permeability of the medium [H/m], and f is the frequency [Hz]. The skin effect is negligible only if the depth of penetration at a certain frequency is much greater than the conductor thickness.

Table 2.1 lists the values of bulk resistivity and skin depth at 2.4 GHz calculated for the most common electrodes available in microtechnology processes, i.e., silver, copper, gold and aluminum. Figure 2.1 illustrates the exponential decay of the skin depth as a function of frequency. For example, the skin depth of aluminum is 1.66 µm at 2.4 GHz and decreases to 0.81 µm at 10 GHz.

TABLE 2.1 : BULK RESISTIVITY AND SKIN-DEPTH, δ CALCULATED AT 2.4 GHZ FOR THE MOST COMMON CONDUCTORS AVAILABLE IN MICROTECHNOLOGY.

Metal	Resistivity [μΩ·cm]	δ @ 2.4 GHz [μm]
Silver (Ag)	1.62	1.31
Copper (Cu)	1.72	1.35
Gold (Au)	2.44	1.6
Aluminum (Al)	2.62	1.66

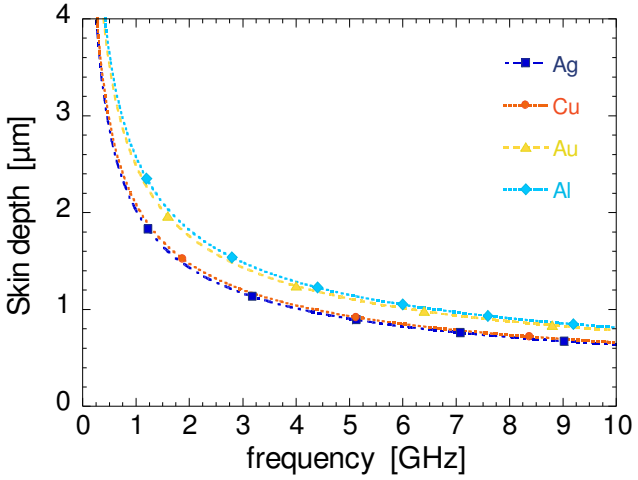

Figure 2.1 : Exponential behavior of the skin depth, δ as a function of frequency.

The exponential attenuation of the current density J [A/m²] as a function of distance x away from the surface of a conductor is given by :

$$J = J_0 \cdot e^{-x/\delta} \qquad (2.6)$$

The current I [A] is obtained by integrating J over the conductor cross-sectional area. Since J only varies in the x direction, I can be calculated as :

$$I = \int J \cdot dA = \int_0^t J_0 \cdot e^{-x/\delta} \cdot w \cdot dx = J_0 \cdot w \cdot \delta \cdot (1 - e^{-t/\delta}) \qquad (2.7)$$

where t is the physical thickness and w is the width of the conductor. From the above expression, an effective thickness, t_{eff} can be defined as follows :

$$t_{eff} = \delta \cdot (1 - e^{-t/\delta}) \qquad (2.8)$$

The effective thickness, as illustrated in Figure 2.2, represents an amount defining a fictive thickness for which the current intensity is equal to 100% of its surface value.

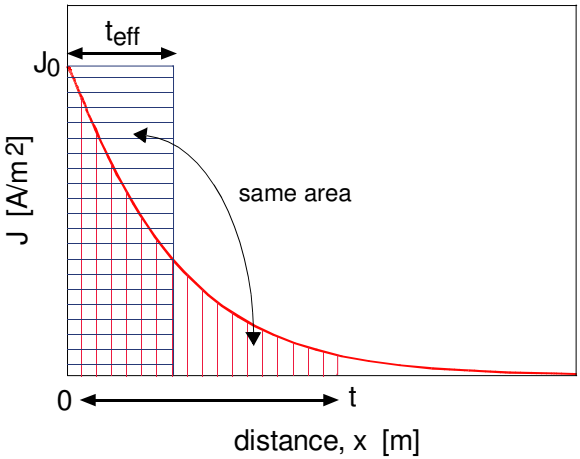

Figure 2.2 : Effective thickness, t_{eff} of a conductor with a physical thickness t under the skin effect.

Figure 2.3 displays the calculated t_{eff} as a function of frequency plotted for several values of physical thicknesses, t of aluminum films.

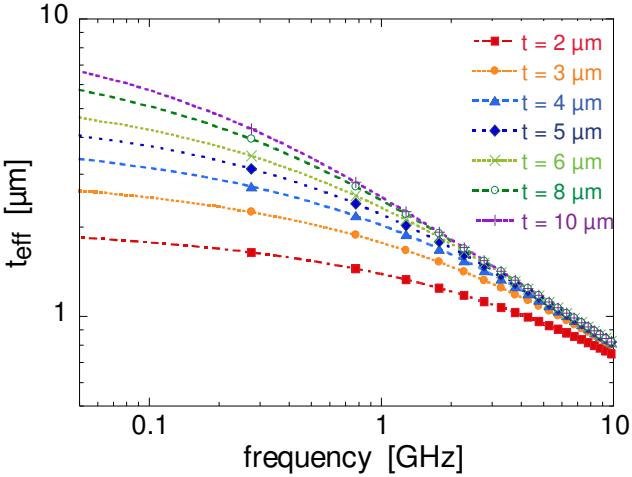

Figure 2.3 : Effective thickness, t_{eff} as a function of frequency for several values of physical thickness, t of Al layers.

From (2.5) and (2.8), an expression taking into account the skin depth effect on the high-frequency resistance is written as follows :

$$R = \frac{\rho \cdot l}{w \cdot t_{eff}} = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})} \qquad (2.9)$$

The above relationship has been used for evaluating the frequency-dependent resistance of an inductor as a function of the spiral thickness. The bulk resistivity of Al reported in Table 2.1 is taken for the calculation. The layout parameters defining the total length of the coil, l are the following : outer diameter, D_{out} = 500 µm, track width, w = 20 µm, turn-to-turn spacing, s = 6 µm, number of turns, n = 4. Thus, the coil length is approximated by summing the length of four concentric rings. The first ring has a radius, R_1 given by $0.5 \cdot (D_{out} - w)$, the radius of the second

ring is $R_2 = 0.5 \cdot (D_{out} - 2 \cdot w - 2 \cdot s)$, and so forth. Figure 2.4 shows the calculated resistance as a function of frequency for various inductors with spiral thickness ranging from 2 up to 10 µm.

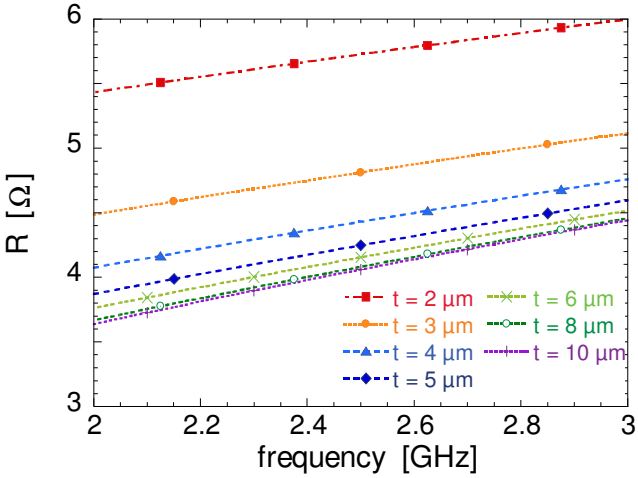

Figure 2.4 : Resistance as a function of frequency for various inductors with identical layout but with different spiral thickness.

A 16% decrease of resistance is obtained at 2.4 GHz when increasing the coil thickness from 2 to 3 µm. Further metal thickening still shows a significant benefit, though more and more reduced, up to 8 µm; whereas, a coil thickness exceeding 8 µm does not lead to any appreciable decrease in resistance. The lower limit reached by the metal resistance is a consequence of the saturation of the conductor cross section that effectively sustains the flow of charges.

Figure 2.5 emphasizes the saturation of the effective thickness of aluminum films as a function of frequency. Considering the frequency range between 2 and 3 GHz, an appreciable increase of the effective thickness can be achieved using films up to 8 µm. The increased effective thickness results in a reduced resistance and hence in a higher Q-factor.

However, the increase of Q-factor cannot be sustained indefinitely, especially at high frequency, due to the fact that the series resistance will reach a critical value as a result of the saturation of the effective metal thickness.

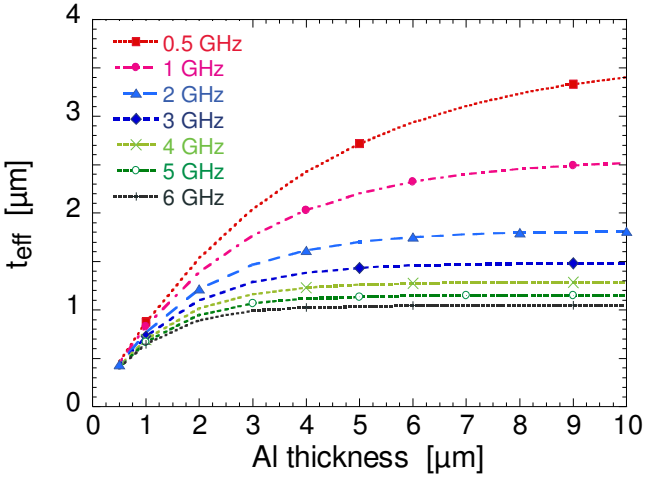

Figure 2.5 : Effective thickness, t_{eff} of aluminum films as a function of the physical film thickness, t plotted at different frequencies.

The above developments based on a fictive aluminum spiral inductor targeting the 2.4 GHz operating frequency, have pointed out that there is a strong interest to provide metal films with thickness up to 8 µm. In fact, despite the skin effect, a significant reduction of series resistance can be expected for such thick metal films. An aluminum film of 8 µm corresponds to approximately 5 skin depths at 2.4 GHz.

2. 2. 1. 2 Proximity effect

A portion of a multiturn spiral inductor is depicted in Figure 2.6 illustrating the mechanism responsible for the proximity effect [3, 6]. The multiturn inductor carries a current, $\boldsymbol{I}_{coil}$, and generates an associated magnetic field, $\boldsymbol{B}_{coil}$, that has maximum intensity at the center of the spiral. Here, the magnetic field is oriented in the direction coming out from the page. Due to the time-varying nature of the current circulating in the coil, the magnetic field also varies with time. As the magnetic field lines of adjacent turns penetrate a trace normal to its surface, according to Faraday's and Lenz's laws [7], an electric field is magnetically induced on these inner turns producing circular eddy currents, $\boldsymbol{I}_{eddy}$, which flow in the direction where their magnetic flux is opposite to the applied magnetic field. So the opposing magnetic field, $\boldsymbol{B}_{eddy}$, due to eddy currents is established and has a direction flowing into the page. This effect is highlighted in turn 5. The magnitude of the induced electric field, $\boldsymbol{I}_{eddy}$, is proportional to the derivative of $\boldsymbol{B}(t)$ with respect to time, suggesting that this effect becomes very significant at GHz-frequencies.

The eddy currents in the metal traces cause a non uniform current flow in the inner turns of the spiral. Particularly, on the inner side of the innermost turns, the coil current, $\boldsymbol{I}_{coil}$ and eddy currents, $\boldsymbol{I}_{eddy}$ flow in the same direction, so the current density is larger than average. At the outer side, the currents flow in opposite direction, hence the current density is smaller than average.

This phenomenon causes a current constriction, or current crowding, that increases the effective resistance above the value that would exist for a uniform flow throughout the entire trace width. This problem is particularly acute when the spiral inductor is filled with turns up to the center, since in this case a large part of the magnetic field goes through these inner turns.

Although the problem of current crowding is well-known, little information is available in the literature for quantifying its effect on the high-frequency resistance without recurring to numerical simulations [4].

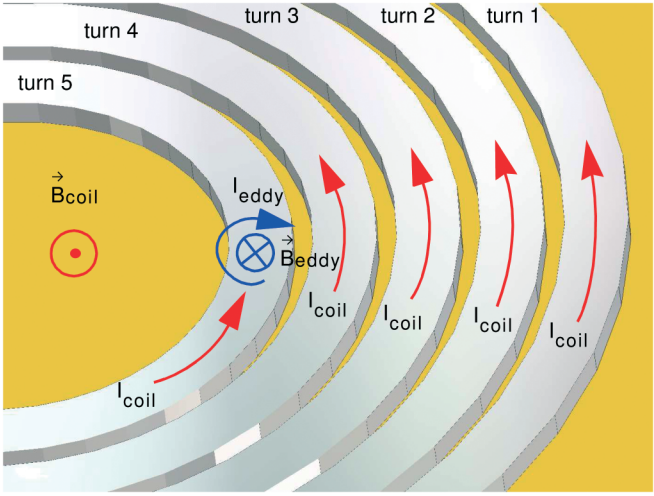

Figure 2.6 : Proximity effect in the metal traces of a spiral inductor due to eddy currents. The magnetic field, $\boldsymbol{B}_{coil}$ generated by the current, $\boldsymbol{I}_{coil}$ flowing in the multi-turn spiral, passes perpendicularly through the traces, setting up eddy currents loops, $\boldsymbol{I}_{eddy}$ that constrict the current flow toward the inner trace edges.

2. 2. 2 Substrate losses

Integrated passive components often reside on top of a conductive silicon substrate. The conductive nature of Si is a major source of power loss and operating frequency limitation. Loss into the volume of the substrate ultimately results in the conversion of electromagnetic energy into heat [8]. To provide more physical insight into this problem, three loss mechanisms can be distinguished. First of all, electric energy is coupled to the substrate through displacement currents due to turn-to-substrate capacitances (see Figure 2.7). These displacement currents flow through the substrate to nearby grounds, that can be located either at the surface or at the backside of the wafer, or both. These electrically induced currents flow vertically or laterally, but always perpendicular to the device segments. In the case of a highly doped Si substrate, electrically induced currents are a dissipation mechanism that dominates over dipole losses. On the other hand,

for insulating substrates, the loss tangent of the material may be the dominant substrate loss mechanism.

Second, if the substrate is sufficiently conductive, magnetically induced currents, or bulk eddy currents, flow into the substrate as a consequence of the time-varying magnetic field penetrating the substrate. Faraday's law implies that this magnetic field induces time-varying solenoidal electric fields, that flow parallel to the spiral segments. The direction of the bulk eddy currents is such that they oppose to the original change in magnetic field, that is in a direction opposite to the current in the inductor. For this reason these currents are also called "image currents".

The inductance value is affected by the substrate eddy currents. Since these currents flow in a direction that is opposed to the coil current, the magnitude of the magnetic field will be reduced and hence the inductance generated by the device will be decreased.

Last, all other loss mechanisms can be grouped into radiation. However, these electromagnetically induced losses occur at much higher frequencies, where the physical dimension of the device approaches the wavelength at the frequency of propagation in the medium of interest, e.g. air or silicon.

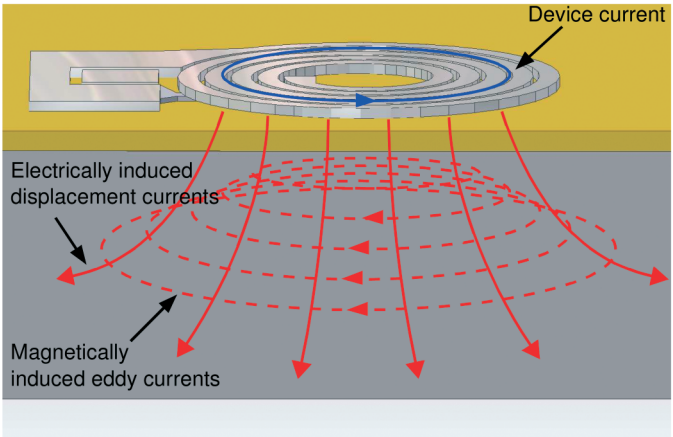

Figure 2.7 : Schematic representation of substrate currents : displacement currents due to turn-to-substrate capacitances (solid lines), and magnetically induced eddy currents (dashed lines) flowing in a direction opposite to the current in the inductor.

In standard CMOS technologies, the heaviest losses result from eddy currents induced in the low resistivity substrate (typically 0.01-10 Ω·cm), that often dominate and mask the effects of losses in the metal traces and displacement currents, and finally limit the Q-factor to values around 5. Moreover, for values of silicon resistivity lower than 0.1 Ω·cm, eddy currents cause their associated magnetic field to weaken the primary field of the spiral. This in turn decreases the inductance value of the device [6]. Inductors built in bipolar processes (or bipolar-derived BiCMOS) often exhibit larger Q values (5 to 10) due to relatively higher substrate resistivity (e.g., 10-30 Ω·cm), which reduce eddy currents to negligible values, but may still suffer from significant losses due to displacement currents [9].

2. 3 Literature review

In 1990, Nguyen and Mayer were the first to show that inductors could be used in silicon IC [10]. A 9.7 nH inductor was reported with a measured maximum Q-factor of 3 at 0.9 GHz. In 1996 Ashby *et al.* [11] demonstrated inductors with peak-Q of 12 at 3.3 GHz for an inductance of 2.9 nH. Since then, a great deal of work was focused at increasing the quality factor of on-chip spiral inductors, by mitigating dissipation mechanisms associated to the semiconducting substrate, or decreasing the metal trace resistance, respectively.

Figure 2.8 outlines the different technologies investigated and developed for these purposes. The most promising published performances, which currently establish the state-of-the-art of RF inductors, are summarized at the end of the chapter. For clarity, the reported performance are separated into two broad groups. The first one lists the performance of monolithic planar inductors fabricated without recurring to any step of surface or bulk micromachining (Table 2.2). Whereas, the second group lists the performances achieved by inductors whose fabrication processes involve post-processing steps of either surface or bulk micromachining (Table 2.3).

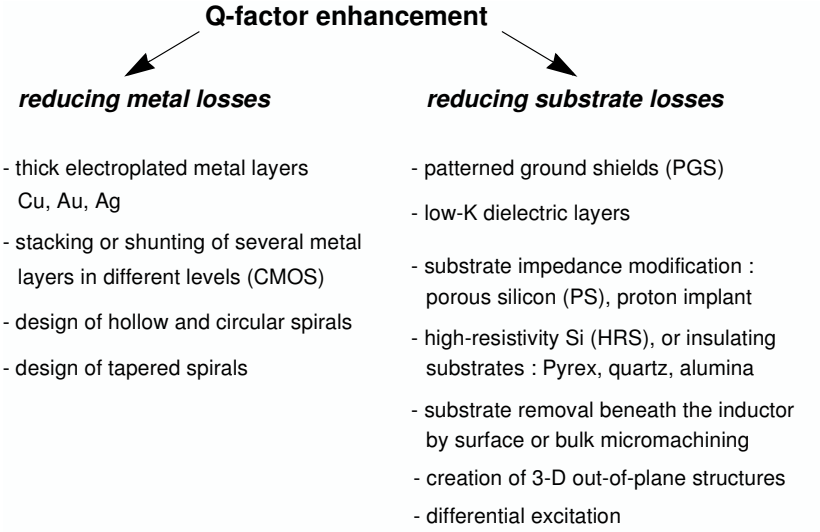

Figure 2.8 : Schematic classification of the different technologies proposed for decreasing the metal trace resistance, or mitigate substrate losses, respectively.

Increasing the metal conductivity is the most efficient way currently known to increase the Q-factor in the frequency region below the maximum Q-factor. From this perspective, several methods have been investigated in order to increase the metal thickness, such as shunting several metal layers in different levels through interconnect via-holes [12, 13]. Another solution is to replace aluminum traditionally used in IC processes, with thick electroplated copper [14, 15] or gold metallizations [16, 17] in a post-processing step.

Alternatively, stacking several spirals in series through multilevel interconnects, so as to assimilate a solenoidal structure, has been reported as an effective method to maximize the inductance per unit area and, hence, improve the Q-factor [18-22].

The magnitude of the time-varying magnetic field generated by a planar inductor is strongest in the center of the spiral and thus produces eddy currents of greatest strength in the volume of conductors near the center of the device. As a consequence, the inner turns contribute in a large extent to the total increase of high-frequency resistance. At the same time, these inner turns play a minor role on

the total inductance of the device due to their small diameter. For these reasons, Craninckx and Steyaert [6, 23] suggested to remove the inner turns so as to create a "hollow" spiral. Another approach to mitigate eddy currents in the metal tracks consists in decreasing the width of the inner turns to effectively move these turns closer to the outer edge. This approach results in what is generally referred as a tapered inductor [24-26].

However, the reduction of the substrate related losses remains the major hurdle for enabling high-performance silicon-based inductors. For overcoming substrate losses, several approaches have been proposed. The insertion of a patterned conductive ground shield (PGS), made either of metal or polysilicon, between the inductor and the silicon substrate attenuates the induced magnetic field, and consequently reduce the eddy currents flowing beneath the device [2, 27-29]. The slots patterned in the shield are made narrow enough to preclude the vertical electric field from penetrating down to the underlying silicon. Moreover, the patterned slots act as an open circuit impeding the circular path of the eddy currents. However, the improvement of Q-factor enabled by using a patterned conductive shield comes at the expense of a reduced f_{SR}. In fact, since the field lines terminate closer to the device, the parasitic capacitance is increased. Nevertheless, the PGS has been demonstrated to be especially useful when attempting to realize an inductor on very low-resistivity substrates, i.e., $\rho < 0.1$ Ω·cm [2].

Another approach to reduce the fields that couple to the substrate is to insert a low-loss low-K dielectric layer between the device and the lossy silicon substrate. Several low-K dielectrics have been investigated such as benzocyclobutene (BCB) [30-32], SU-8™ [31], Polyimide [17, 33, 34], Silk™ [35, 36]. Cu electroplated inductors with a metal thickness of 6 µm using 6 µm of BCB ($\varepsilon_r = 2.65$) to isolate the device from the silicon substrate ($\rho_{Si} = 20$ Ω·cm) have shown a peak Q-factor of 23 at 1.7 GHz for a corresponding inductance of 3.2 nH [30].

A more attractive and cost-effective solution for on-chip inductors is to realize them above the passivation using thin-film post-processing techniques, in a wafer-level-packaging approach [32]. Inductors employing BCB have been fabricated in a multi-chip module (MCM) on glass substrate exhibiting Q-factor > 100 [37].

Increasing the substrate resistance is another effective means for reducing substrate losses. The use of high-resistivity silicon (HRS) [38-43], sapphire [39, 44, 45], quartz [38, 39], glass [46], GaAs [17, 38], or alumina (Al_2O_3) [47], have been used by many researchers to demonstrate high-Q planar inductors (Q > 15). As an example, Benaissa *et al.* [41] have reported a 4.5 nH inductor fabricated on

HRS (ρ_{Si} > 1 kΩ·cm) achieving a peak Q-factor of 17.5 at 3.5 GHz. This corresponds to an almost three-fold improvement compared to the same inductor fabricated on low-resistivity Si (ρ_{Si} < 5 Ω·cm). Recently published work has also demonstrated the fabrication of high-performance inductors on plastic substrate achieving a peak-Q > 30 for 3 nH [48].

Furthermore, a localized increase of the silicon substrate resistivity can be achieved by means of the formation of porous silicon (PS) [49-52], or with proton bombardment [53-59]. PS formed by anodization of silicon is emerging as an attractive material for RF applications because of its resistivity in the order of 10^6 Ω·cm [60] and its compatibility with very large-scale integrated (VLSI) technology. Kim et al. have reported a 5.7 nH spiral inductor exhibiting a peak-Q of 29 at 7 GHz built on a socket of 200 µm of porous silicon formed in a Si substrate with initial resistivity of 0.007 Ω·cm. On the other hand, the high resistivity achieved after proton bombardment (typically 10^5-10^6 Ω·cm) on wafers of initial resistivity of about 10 Ω·cm is a consequence of free carriers removal by proton-created charge trappings [61].

With the advent of micromachining technologies developed for microelectromechanical systems (MEMS), innovative processes based on surface or bulk micromachining have been investigated in order to get rid of substrate parasitics. By using selective etching techniques, the silicon substrate can be removed in a post-processing step from underneath the inductor, either by etching from the top [62-68], or from the backside of the wafer [25, 69, 70]. This effectively suppresses induced currents and parasitic capacitance, and consequently shifts the self-resonance frequency toward higher values, thus extending the operating frequency range of the inductor. Alternatively, without altering the substrate itself, it is possible to separate the spiral inductor from the underlying substrate by creating an air gap using sacrificial molds of photoresist [71-73] or sacrificial metallic layers [74, 75]. This results in what is generally referred to as a levitated architecture. Air gaps of 50-60 µm separating the planar inductor from the substrate have been demonstrated. Very promising performance of levitated inductors have been reported by Yoon *et al.* [75], they demonstrated a peak Q-factor of 35 at 5 GHz for a 5 nH inductor fabricated on glass substrate.

Unlike the conventional planar spiral inductor, where the magnetic and electric fields penetrate the silicon substrate perpendicularly, the magnetic and electric fields of the solenoidal inductor are generated parallel to the substrate. As a consequence, substrate losses can be significantly reduced. Based on these considerations, three-dimensional (3-D) structures, such as solenoid inductors

have been fabricated using high aspect ratio molds [76-84]. Toroidal structures have also been proposed since they better confine the magnetic flux mostly parallel to the substrate with only fringing fields penetrating the substrate [85, 86].

In recent years, more advanced techniques have been developed aiming at the out-of-plane self-assembly of 3-D architectures. Basically, the portion of the structure to be assembled is first released from the substrate by the removal of a sacrificial layer, subsequently the assembly process takes place causing the structure to be lifted away from the surface. The assembly mechanism can be driven by stress-engineered metal films [87-89], surface tension [90], or by the torque generated by an applied magnetic field [91, 92].

A common feature of all these micromachining techniques is the substantial elimination of the resistive losses related to the substrate. However, this also requires extra non-standard processing steps and raises serious reliability issues such as packaging yield and long-term mechanical stability. Fragility to shocks and encapsulation issues are serious bottlenecks that currently hinder the application of micromachined inductors in RFIC's and MMIC's.

The Q enhancement of planar inductors can also be achieved by using differential excitation techniques [93-97]. In the differential excitation, the voltages or currents, of two input or output signals are 180° out of phase, but with the same magnitude. The differential excitation has become an important operation mode in high-performance mixed-signal circuits because it has the advantage of better immunity to environmental noise and offer common-mode rejection. Commonly used IC's that employ these inductors are differential VCOs, double balanced mixers and differential amplifiers. Spiral inductors excited differentially play an important role in these circuits. The Q-factor of such inductors is enhanced and is maintained over a broader bandwidth, compared to single-ended configuration, because of smaller substrate loss.

TABLE 2.2 : STATE-OF-THE-ART PERFORMANCES OF MONOLITHIC RF PLANAR INDUCTORS.

Authors/year/affiliation/ reference	Technology	Substrate	Q_{max} @ f_{max} [GHz]	L [nH]
Choi et al., 2004, KAIST, Korea [14]	Thick Cu electroplating (5 to 22 µm) on 7 µm of oxide	silicon (1-30 Ω·cm)	55 @ 3.3	4.5
Burghartz et al., 2004, DIMES, Delft [15]	Local thickening of top Al level (1 µm) with Cu electroplating (3.4 µm)	silicon (5 Ω·cm)	13.2 @ 1	10
Yim et al., 2002, Uni of Florida, Gainesville [28]	Spiral inductors (3 µm Al) on poly-Si patterned ground shield (PGS)	silicon (20 Ω·cm)	13.8 @ 2.5	4.8
Pieters et al., 2001, IMEC, Leuven [37]	Multichip module approach : Cu spiral (3 µm) embedded in BCB (10 µm)	glass	115 @ 8	2
Carchon et al., 2004, IMEC, Leuven [32]	Wafer-level-packaging (WLP) approach : Cu spiral (10 µm) embedded in BCB (16 µm)	silicon (20 Ω·cm)	38 @ 4.7	1
Huo et al., 2002, Uni of Science and Technol., Hong Kong [30]	Cu electroplated inductors (6 µm) on low-K BCB (6 µm)	silicon (20 Ω·cm)	23 @ 1.7 20 @ 1	3.2 5.2
Jeon et al., 2003, Purdue Uni, West Lafayette [31]	Spiral inductors (3.6 µm Au) on SU-8 (6 µm)	HRS	17 @ 8	3.2
Zu et al., 1996, Rutgers Uni, Piscataway [33]	Staggered double metal-layered inductor (Al 2.5 µm) on polyimide (5 µm)	HRS (2 kΩ·cm)	30 @ 1	4
Park et al., 1998, ETRI, Korea [40]	Spiral inductor (2 µm Al)	HRS (2 kΩ·cm)	11.5 @ 3	13
Burghartz et al., 1998, IBM, New York [39]	Spiral inductor (Cu)	quartz	20 @ 0.75	80
Dekker et al., 1997, Philips, Eindhoven [46]	Spiral inductor (3.5 µm Al) transferred on glass	glass	38.9 @ 4. 19 @ 1.5	2.6 23.9
Wu et al., 1999, National Central Uni, Taiwan [47]	Spiral inductor (6 µm Au)	Al_2O_3	36 @ 4	2.7
Nam et al., 1997, KAIST, Korea [50]	Spiral inductor (2.3 µm Au) on oxidized porous Si (25 µm)	silicon (5-7 Ω·cm)	13.3 @ 4.6	6.3
Kim et al., 2001, UCLA [51]	Spiral inductor (4 µm Al) on unoxidized porous Si (50-200 µm)	silicon (0.007 Ω·cm)	29 @ 7	5.7
Yang et al., 2003, TSMC, Taiwan [53]	Spiral inductor (3 µm Cu) on substrate post-processed with proton bombardment	silicon (10 Ω·cm)	20.7 @ 6.8 20.6 @ 6.6 18.5 @ 4.1	1.1 2 3.5

TABLE 2.3 : SATE-OF-THE-ART PERFORMANCES OF MICROMACHINED RF INDUCTORS.

Authors/year/ affiliation/reference	Technology	Substrate	Q_{max} @ f_{max} [GHz]	L [nH]
Yoon et al., 1999, KAIST, Korea [75]	Surface micromachined suspended inductors: Ni sacrificial molds (50 µm) and Cu electroplating (15 µm)	glass	57 @ 10 35 @ 5 38 @ 1.8	1.75 5 14
Yoon et al., 2002, KAIST, Korea [71]	Surface micromachined suspended inductors: photoresist sacrificial molds (50 µm) and Cu electroplating (10 µm)	silicon (1-30 Ω·cm)	70 @ 6 38 @ 2.3 32 @ 2.1	1.38 2.6 4.1
Lakdawala et al., 2002, Carnegie Mellon, Pittsburg [66]	Surface micromachined suspended inductors : air gap (30 µm) created by isotropic RIE etching of Si	silicon	12 @ 7.5 10.5 @ 5.7	3.2 4.15
Jiang et al., 2000, Cornell Uni, Ithaca [64]	Surface micromachined suspended inductors : air gap created by HF etching of SiO_2 (30 µm), encapsulation of poly-Si structures by Cu electroless	silicon	23 @ 7.5 36 @ 5	2 2.7
Wang et al., 2004, JiaoTong Uni, Shanghai [72]	Surface micromachined suspended inductors: photoresist sacrificial molds (60 µm) and Cu electroplating (5 µm)	glass	37 @ 1.5	4.2
Park et al., 1999, Georgia Tech, Atlanta [63]	Surface micromachined suspended inductors: polyimide sacrificial molds (60 µm) removed by plasma O_2 and Cu electroplating (15 µm)	silicon (3-7 Ω·cm)	16 @ 0.1	16
Lopéz-Villegas et al., 2003, Uni of Barcelona [25]	Bulk micromachined suspended inductors: KOH etching of Si from the wafer backside	silicon	17 @ 1.5	35
Yoon et al., 1998, KAIST, Korea [76]	Solenoid inductor using photoresist sacrificial molds and Cu electroplating	glass	19 @ 5.5 14.5 @ 2.8 12.5 @ 2.3	2.5 5.2 10
Chua et al., 1998, PARC, Palo Alto [88]	3-D coils self-assembled by stress engineered sputtered MoCr alloy	silicon	85 @ 1 70 @ 1	7.8 9.2
Yoon et al., 2005, Georgia Tech, Atlanta [83]	Solenoid inductor using a back-bone of SU-8 covered by Cu electroplating	glass	84 @ 2.6	1.17
Lu et al., 2004, Uni of Texas, Dallas [81]	Solenoid inductor using SU-8 sacrificial molds and Cu electroplating	Pyrex	72.8 @ 9.7 43 @ 2	2.15 28
Young et al., 1997, Uni of California, Berkeley [84]	Cu electroplated traces (5 µm) around an Al_2O_3 core	silicon (10 Ω·cm)	30 @ 1	4.8

2. 4 References

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CHAPTER 3

TECHNOLOGY

PLANAR spiral inductors have been fabricated using simple and innovative micromachining processes. The planar architecture, while being most easily implemented from a processing point of view compared to reported 3-D out-of-plane structures, also promotes the mechanical reliability of the fabricated device. The proposed inductor architecture consists of two metal levels separated by a dielectric layer. Patterns created in the first metal level form the underpass, i.e., the feed-through path necessary for connecting the probing pad to the centre of the spiral. The spiral is formed by patterning the second metal level. Via-holes locally opened through the dielectric layer permit the connection between the two metal levels.

Different types of substrates have been investigated in order to emphasize the role of the resistivity on the inductor performances in terms of Q-factor and self-resonant frequency. These substrates are : doped silicon wafers with a nominal volume resistivity of 1-30 Ω·cm (Siltronix), float zone high-resistivity silicon wafers (FZ HRS, Topsil Semiconductor Materials) with a measured volume resistivity of 3'500 Ω·cm, and Pyrex7740 wafers with a resistivity in the order of 10^{10} Ω·cm (Sensor Prep). As a preliminary step, a 3 µm-thick thermal oxide layer has been grown on high-resistivity and doped silicon wafers for providing an

electrical insulation between the device and the substrate. The thermal oxidation of silicon substrates has been carried out in a furnace at 1'100°C in a mixed O_2 and H_2 atmosphere. The growth rate of this thermal oxide is 0.19 µm/h, resulting in a rather expensive and time-consuming process. On the other hand, the front-side of Pyrex substrates has been coated with 100 nm of sputtered SiO_2. This protective film is necessary for avoiding potential contamination of the equipment used throughout the fabrication process due to ionic dopants present in the bulk of Pyrex. Furthermore, as a usual procedure, the backside of Pyrex wafers has been coated with a thin aluminum film of 20-30 nm. This step is required not only for preventing contamination, but also to allow for a correct handling of the insulating Pyrex wafers on the equipment using capacitive detection systems or electrostatic clamping.

Sputter deposited aluminum films patterned into spirals by an anisotropic dry-etching process are the essential features of the first process presented. Al has been chosen due to its low cost, good conductivity and compatibility with CMOS manufacturing. Moreover, the sputtering technique permit the deposition of highly pure films with thickness up to several micrometers and with excellent uniformity. The present work demonstrates for the first time the use of patterned Al films up to 8 µm-thick for implementing MEMS in general and RF passives in particular.

The second developed process is based on silver electroplating into polymer moulds. Among the deposition technologies available in the MEMS world, electroplating is certainly the most suitable for providing highly-pure and very thick metal films. The use of Ag has been investigated as this metal displays the highest bulk conductivity, i.e., + 6% compared to Cu (see Table 2.1). The well-known susceptibility of Ag towards electromigration and corrosion in the presence of moisture and applied bias [1] has been reported to be of minor concern in microwave passives, due to their large size and to the low current densities involved in most of the portable systems dedicated to RF applications. Recently published work has demonstrated the reliability of silver for implementing coplanar waveguides (CPWs) [2].

The third development deals with a post-processing step of surface micromachining carried out on Al planar inductors. Here, the selective removal of a sacrificial layer of SiO_2 by means of hydrofluoric acid (HF) vapor phase etching (VPE) has been investigated for the fabrication of suspended spiral inductors. The attractiveness of such a free-standing structure is that the air gap separating the spiral from the substrate reduces the parasitic capacitive coupling and consequently allows for better performances in terms of self-resonance and peak

Q-factor. Although, a suspended spiral inductor is more susceptible to failure due to mechanical shocks and vibrations, this technology has been developed since it potentially allows for the integration of passive components directly on top of standard CMOS wafers.

3. 1 Aluminum inductors

3. 1. 1 Sputter deposition

In the sputter deposition process [3, 4], a target made of the material to be deposited is brought to a negative voltage. This is the cathode. A second electrode (the anode), kept as ground, or biased to collect electrons, acts as substrate holder. A gas, usually argon, is introduced into the system and ionized by the electric field applied between cathode and anode. The positive ions are attracted to the negatively biased target and the faster electrons are attracted to the anode. The physical bombardment of the target by the flux of inert ions dislodges atoms that gradually coat the wafer.

In this work, magnetron DC sputtering is used for depositing metal films (i.e., Al, Ti, Pt); whereas, magnetron RF sputtering is used for depositing dielectric films of SiO_2. Prior to the film deposition itself, the substrate may be sputter etched in Ar atmosphere by connecting it to an RF source. This step of sputter cleaning (or RF-etching) enables the elimination of passivation layers and promotes the adhesion of subsequent metallizations.

3. 1. 2 Dry-etching

The objective of the etching process is to selectively remove materials using a masking template, e.g., photoresist, SiO_2 or Al. In order for the etching process to be successful, there must be sufficient selectivity between the mask and the material being etched. The gases used in a plasma based dry-etching process are selected such that their dissociative products react with the material to be removed by breaking chemical bonds and forming volatile products that desorb from the surface and that are successively evacuated from the process chamber through the pumping system.

The basic principle of plasma-phase etching involves the generation of chemically reactive radicals and ions that are accelerated under the effect of an

electric or magnetic field towards a target substrate. These reactive species are formed by the collision of molecules in a reactant gas with a cloud of energetic electrons excited by an RF field. When the etching process is purely chemical, powered by the spontaneous reaction of radicals with the material to be removed, it is referred as "plasma etching". But if ion bombardment of the target surface plays a synergistic role in the chemical etching reaction, the process is then referred to as reactive ion etching (RIE). It is the directionality of the accelerated ions that gives RIE its anisotropy.

High density plasma sources, such as inductively coupled plasma (ICP) provide many distinct advantages over conventional parallel plate plasma systems. In conventional RIE, the plasma density is limited by the method of coupling RF energy into the plasma. This limits the rate at which certain materials can be etched. The utilization of an ICP source provides further excitation to the electron cloud and to the reactive ions by means of a RF magnetic field (13.56 MHz) applied by means of an external coil surrounding the process chamber. The ICP source creates high-density, low-pressure and low-ion energy plasmas allowing for high etch-rates and great ion directionality [4]. The combination of these characteristics enables the fabrication of vertical patterns with high aspect ratio[1]. Furthermore, processing at lower pressure has a number of significant benefits. It allows for a tight control of anisotropy in high-aspect ratio structures and reduces microloading effects.

Dry-etching processes based on chlorine chemistry are commonly used in the semiconductor microelectronics for etching different kinds of materials. An advantage of chlorine-containing plasma is the ability to form highly volatile chlorides [5]. Plasma etching of aluminium and aluminium alloys has been traditionally performed in chlorine-containing gases, such as Cl_2/BCl_3 [6, 7], BCl_3 only [8], $Cl_2/BCl_3/CH_4$ [9], $Cl_2/BCl_3/CHCl_3/N_2$ [10], Cl_2/CCl_4 [11]. Pure aluminum is readily etched in Cl_2 plasma due to formation of aluminium chloride dimers, such as of $AlCl_3$ and Al_2Cl_6 [6]. Since these products are volatile they are evacuated from the reactor by the pumping system. However, it is well known that aluminium films are spontaneously covered by a native oxide layer. A plasma based on pure Cl_2 does not etch this oxide. For this reason, BCl_3 is added to increase the amount of sputtering and to scavenge the oxygen in the aluminium oxide layer.

1. *The aspect ratio (AR) is defined as the ratio of the thickness to the width of a structure.*

Bromine containing gas, such as BBr_3/Br_2 [6], or Br_3 only [8] have also been investigated. However, the presence of BCl_3 is preferred to BBr_3 since the former allows for a faster etching of the aluminum oxide [6].

The etching of high-aspect ratio vertical patterns in thick metal films requires the use of a plasma-based process. In fact, since wet-etching of metals is an isotropic process, the etching procedure carried out on thick metal films would lead to severe mask undercutting (or lateral etching) and thus to the inability of patterning structures with high aspect ratio. Figure 3.1 illustrates this problem by comparing the results obtained from Al films patterned by standard wet-etching to the patterns enabled by the ICP dry-etching process. In both cases the film thickness is 6 µm. The solution used for the wet-etching of Al (Selectipur®) is composed of phosphoric acid (H_3PO_4), acetic acid (CH_3COOH) and nitric acid (HNO_3). SEM inspection of the patterned film clearly reveals that the wet-etching process carried out on such thick metal films leads to an unacceptable mask undercut. In contrast, the dry-etching ICP process has been demonstrated to be highly anisotropic. Particularly, it has enabled the fabrication of structures with vertical walls, characterized by an aspect ratio greater than unity.

In the present work, dry-etching of aluminum has been performed using a Multiplex ICP etching tool from Surface Technology Systems (STS). The plasma process is based on a mixed gas chemistry containing chlorine (Cl_2) and boron trichloride (BCl_3). The flow-rate of both these gases is regulated to 10 sccm. The etching process is performed by applying a RF power of 1000 W to the source (i.e., the coil surrounding the reactor chamber) and 200 W to the substrate holder. The working pressure in the reactor is stabilized to 3.0 mTorr. This low working pressure allows for the creation of a high-density plasma.

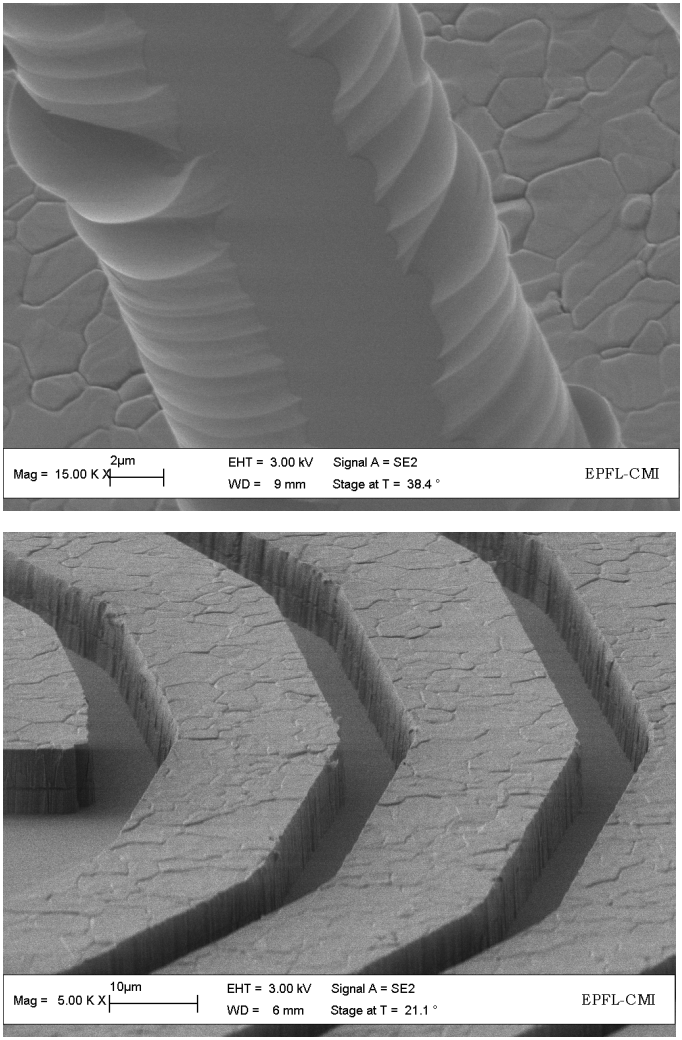

Figure 3.1 : SEM close-up views of aluminum films patterned by isotropic wet-etching (top), and anisotropic dry-etching ICP (bottom). In both cases the thickness of the Al films is 6 µm.

3. 1. 3 Fabrication process

Figure 3.2 shows the schematic cross-section of the 3-mask process developed for fabricating Al planar spiral inductors. All the sputter depositions have been carried out in a Spider-600 tool from Pfeiffer-Vacuum. This is a multichamber equipment that enables the deposition of metals (in DC mode), as well as dielectrics (in RF mode). Typically, the base pressure achieved in the process chambers is in the order of $8 \cdot 10^{-8}$ to $2 \cdot 10^{-7}$ mbar.

As a first step, 300 nm of Al are sputtered onto the substrate, either Pyrex or silicon, and patterned by standard wet-etching (Figure 3.2.a). Due to the limited thickness of this film, mask undercutting is not an issue. The patterns created will constitute the underpass for connecting the RF port to the centre of the spiral.

Next, 1 µm of SiO_2 is sputter deposited at room temperature with a RF power of 1000 W from a pure SiO_2 target. Via-holes through this dielectric film are then opened by a dry-etching ICP process based on CF_4 chemistry that is very selective towards Al (Figure 3.2.b).

When metallic aluminum is exposed to air, it immediately chemically reacts mainly with moisture forming a thin film of aluminum oxide (Al_2O_3) with a thickness of 2-3 Å and with excellent adhesion and protection properties [12]. However, the presence of this oxide would have nefast consequences on the future operation of the inductor. For this reason, before depositing the second metal layer, a low-power RF-etch in Ar atmosphere is carried out for removing the Al_2O_3 film formed in the opened via-holes. To do so, the wafer is plasma etched by applying an RF power of 200 W to the substrate holder during 3 minutes. Without breaking vacuum, the top Al layer is sputter deposited at room temperature from a pure Al target with 2000 W DC power. The deposition rate achieved under these conditions is 6.8 nm/s. Usually, the thickness of the top Al layer that will form the spiral ranges from 3 up to 8 µm, depending on the different device version. However, such range of thickness ensures an excellent step coverage onto the via-holes, which have a depth of 1 µm.

Subsequently, Clariant's AZ9260, a Novolak-based positive-tone photoresist, is spin-coated with a thickness of 8 or 10 µm, and used as masking material during the etching process of aluminum. The energy required for the exposure of the photoresist is 160 mJ/cm^2 for the 8 µm-thick film and 220 mJ/cm^2 for the 10 µm-thick film.

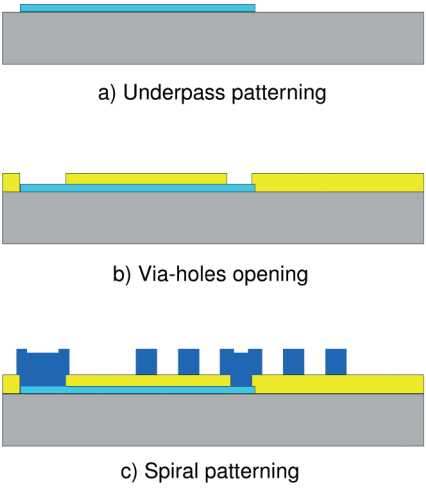

Figure 3.2 : Schematic view of the 3-mask process for the fabrication of aluminum planar inductors.

The development is carried out in AZ 400K 3:1 using an automated puddling method consisting of several alternating cycles of development and rinsing. It is noteworthy to mention that post-bake of the developed photoresist film has not been done in order to prevent creep of the structures.

Finally, the thick Al layer is patterned into spirals (Figure 3.2.c) using the STS ICP reactor and the process parameters previously mentioned. The etch-rate achieved under these conditions is approximately 280 nm/min and the selectivity of the process toward the photoresist mask has been observed to be close to unity. During the etching process, the wafer is electrostatically clamped onto a helium cooled metal chuck. Particularly, the cooling is provided by helium flowing in open circular channels embedded in the chuck and covered by the clamped wafer. As previously mentioned, Pyrex wafers have been protected at the backside with a thin metal film in order to promote a correct electrostatic clamping. A bad substrate clamping during the etching process would prevent an efficient wafer cooling, and hence would cause the immediate destruction of the photoresist mask.

In the STS Multiplex ICP reactor, the end of process is detected optically by the operator. Practically, this is done by inspecting the etching progress inside the process chamber through borosilicate glass windows provided on top of the reactor lid. In the case of spiral inductors, metal residues remaining in areas to be opened by the etching process can lead to short circuits between lines and can result in a major loss of device yield. These unwanted residues can have two main origins, first of all, the aspect ratio itself of the area to be opened. Second, the non-uniformity of the film thickness at the wafer scale. In order to obtain opened areas clear from any metal residues, it is crucial to allow a sufficient over-etching time, i.e., the process is continued even if the optical inspection has revealed that the etching has occurred over the whole wafer surface. Typically, the required over-etching time is in the order of 20 to 40 seconds depending on the initial film thickness. Since the photoresist mask has been spun thick enough to withstand long etching processes, no undercutting is normally observed due to over-etching.

Removal of the residual photoresist mask is a delicate and crucial step that has to be realized as soon as the processed wafer is taken out from the load-lock of the etching equipment. In fact, when in contact with air, chlorine-based products present on the wafer readily form HCl, potentially leading to the corrosion of Al patterns. Photoresist removal has been usually carried out in a stripping solution of PGMEA/NMP at 70°C for about 15 min, followed by an oxygen plasma of 10 min.

The presented ICP dry-etching process has enabled the fabrication of vertical structures achieving aspect ratio greater than unity for the whole thickness range considered, i.e., from 3 to 8 µm. In the best case, a maximum aspect ratio of 1.33 has been demonstrated on a 8 µm-thick film. This performance is essential for creating a minimum spacing between adjacent tracks of an inductor and thus maximize the total inductance per unit area through an enhanced magnetic coupling. The role of the interturn spacing on the achieved inductance is an important issue that will be addressed in Chapter 4.

A SEM tilted view of a planar inductor fabricated from a 8 µm-thick Al film is shown in Figure 3.3. The same figure also shows a close-up view of the typical smooth and vertical walls obtained. Accurate wafer inspection did not reveal any phenomenon of mask undercut. This confirms that the etching process is indeed very anisotropic. Moreover, the opened areas are clear from metal residues, thus avoiding the risk of short circuits.

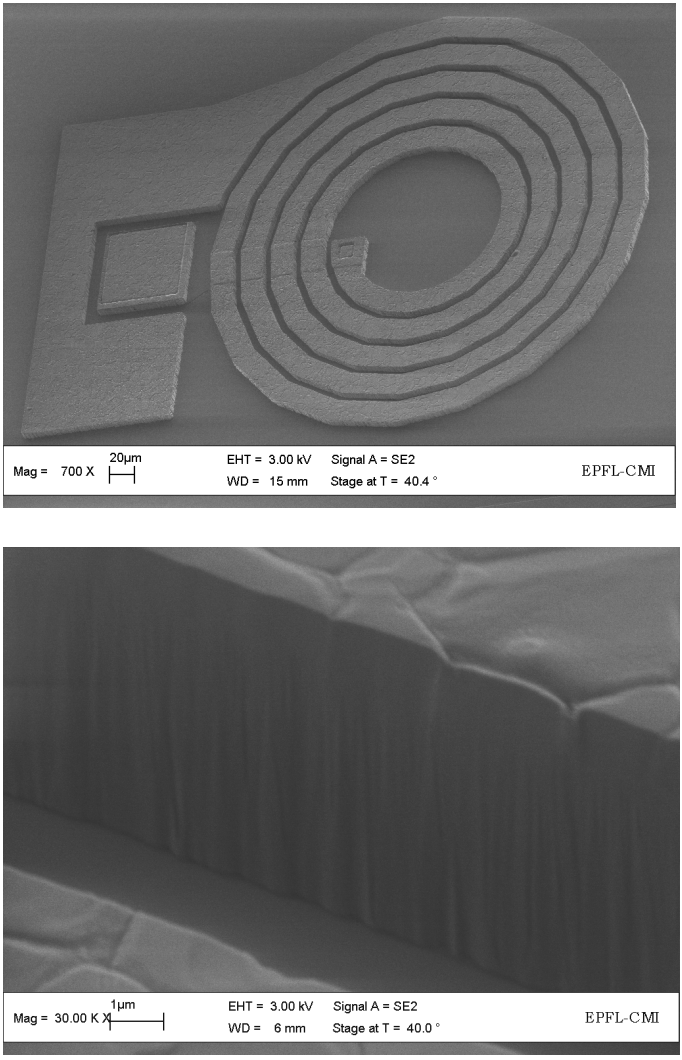

Figure 3.3 : SEM images of a 8 µm-thick Al spiral inductor with a turn-to-turn spacing of 6 µm (top), and a close-up view of the typical smooth vertical patterns enabled by the anisotropic ICP dry-etching process (bottom).

3. 1. 4 Characterization of sputtered Al films

The resistivity of aluminum films, ρ_{Al} has been calculated using the following relationship :

$$\rho_{Al} = \frac{R_{DC} \cdot w \cdot t}{l} \qquad (3.1)$$

where R_{DC} is the value of 4-points DC resistance measured on specific test structures, w and l are the width and the length of the test lines, and t is the film thickness measured by surface profilometry (AlphaSetp-500). The trend plotted in Figure 3.4 highlights that the resistivity exhibited by films with thickness exceeding 1 µm is only 10% higher compared to the reported bulk value ($\rho_{Al\text{-}bulk}$ = 2.62 µΩ·cm). These values are very promising. However, possible reasons explaining resistivity larger than the bulk value are likely due to the effect of grain boundaries, that hinders the current flow in thin films and, in a lesser extent, due to Ar impurities in the film. Experimental data is plotted within an error of ± 2%, that accounts for the standard deviation of the measured values of DC resistance.

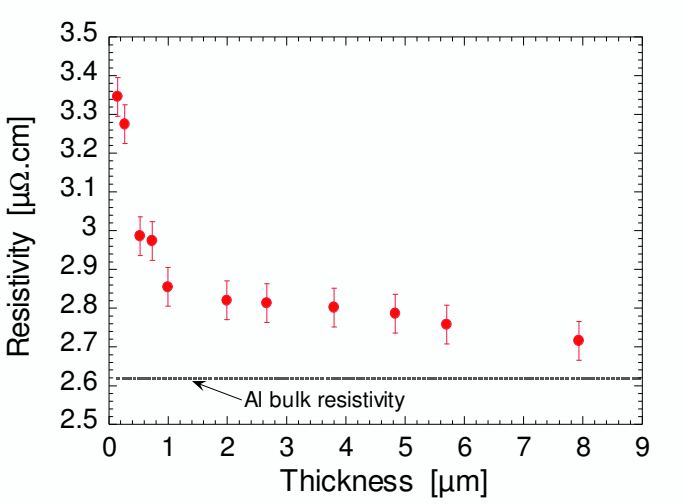

Figure 3.4 : Resistivity of aluminum films calculated from 4-points DC resistance measurements.

A cleaved cross section of a 5 µm-thick Al film is shown in Figure 3.5. The cleavage procedure of the wafer has been performed under cryogenic conditions allowing for a brittle failure mechanism. The original grain morphology formed during the sputter deposition is thus preserved. Grains with large dimensions are already visible since the early stage of the film growth. In general, the large grain size observed in the Al microstructure contributes in a large extent to the excellent conductivity of these films.

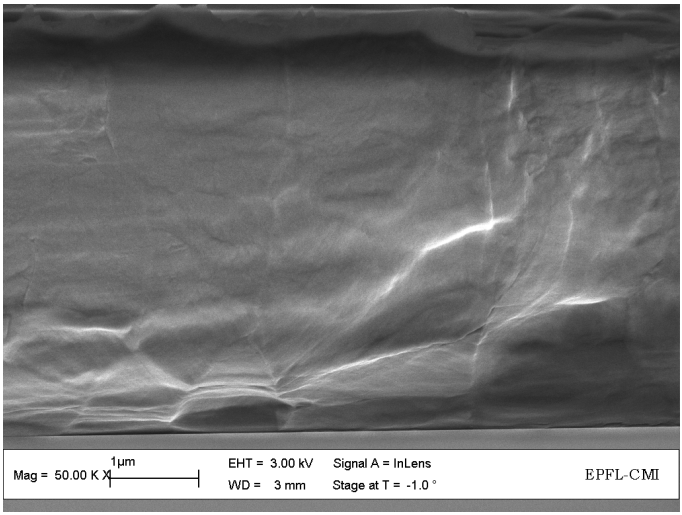

Figure 3.5 : SEM cross-section of a 5 µm-thick aluminum film. The original grain size characterizing the microstructure of the sputtered film is preserved by the cryogenic cleavage.

The residual stress after the deposition is an important issue for the integrity and the reliability of thin metal films. The in-plane stress as a function of the thickness is obtained by recording the change of the curvature radius of the wafer caused by the deposited film. This bowing is measured optically with a stress analyzer Tencor FLX-2320A.

The average in-plane stress, σ is calculated with the following expression known as Stoney's formula :

$$\sigma = \frac{E}{6(1-\upsilon)} \cdot \left[\frac{1}{R_1} - \frac{1}{R_0}\right] \cdot \frac{t_s^2}{t_f} \qquad (3.2)$$

where $E/(1-\upsilon)$ is the biaxial Young's modulus of the substrate (180.5 GPa for (100) oriented silicon wafers), t_s and t_f represent the thickness of the substrate and the film, respectively. R_0 and R_1 represent the curvature radii before and after deposition. The trend of residual stress versus film thickness is plotted in Figure 3.6. Films with thickness ranging from 200 nm to 8 µm exhibit moderate tensile stress with values ranging from 37 to 83 MPa.

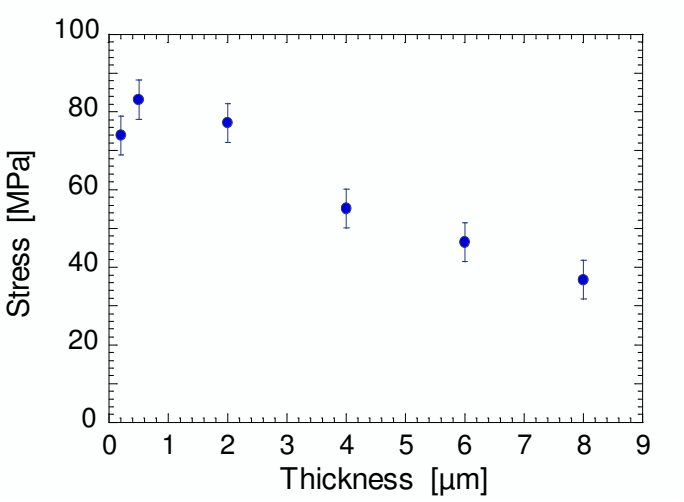

Figure 3.6 : Measured in-plane residual stress of aluminum films with thickness ranging from 200 nm to 8 µm.

3. 2 Silver inductors

3. 2. 1 Electroplating

In its most basic form, an electroplating cell consists of an anode, a cathode, metal ions in a solution and an external source of electricity (Figure 3.7). The wafer to be plated, with a metallic seed layer and with a photoresist mask defining the regions onto which the metal has to be deposited, is maintained at a negative potential (the cathode) relatively to the positively polarized counter electrode (the anode). The electroplating solution used in this work contains a reducible form of Ag ions. By imposing a negative bias to the surface to be plated, electrons are supplied to this surface and, consequently, Ag ions in the solution are reduced, causing a gradual coating of the surface.

$$Ag^{+} + e^{-} \rightarrow Ag \tag{3.3}$$

The different parts constituting the experimental set-up used to perform the electroplating process are a power supply (EG&G galvanostat/potentiostat 237A, Princeton Applied Research), a custom made Teflon® chuck (Figure 3.8), that encloses the wafer to be electroplated, a foil of pure Ag used as the anode, and a glass beaker containing the plating bath. The top part of the chuck contains a circular copper electrode glued onto a soft foam. Once the two parts of the chuck enclosing the wafer are screwed together, the system is sealed and the copper electrode adheres to the wafer edge providing a continuos electrical contact. The mask used for the step of mold patterning, has been designed in such a way that the first 1 cm from the wafer edge is not covered with photoresist. This way, the copper electrode contacts directly the metal seed layer all the way around the wafer edge.

The plating bath used in this work (SilverGlo3k®) is a commercial product from LeaRonal AG[2]. It consists of a solution of potassium silver cyanide ($AgK(CN)_2$) (66.5 g/l) and potassium cyanide (KCN) (90 g/l). The electroplating process has been performed at room temperature without stirring the bath.

2. *LeaRonal AG, Grossmatte 4, CH-6014 Littau, Switzerland.*

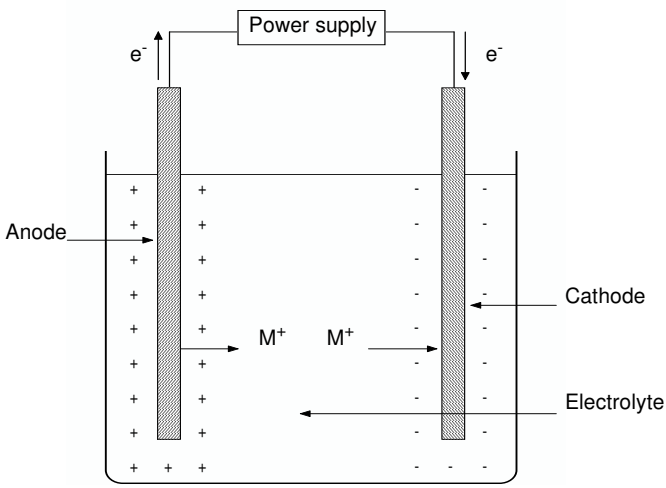

Figure 3.7 : Schematic view of the electroplating cell.

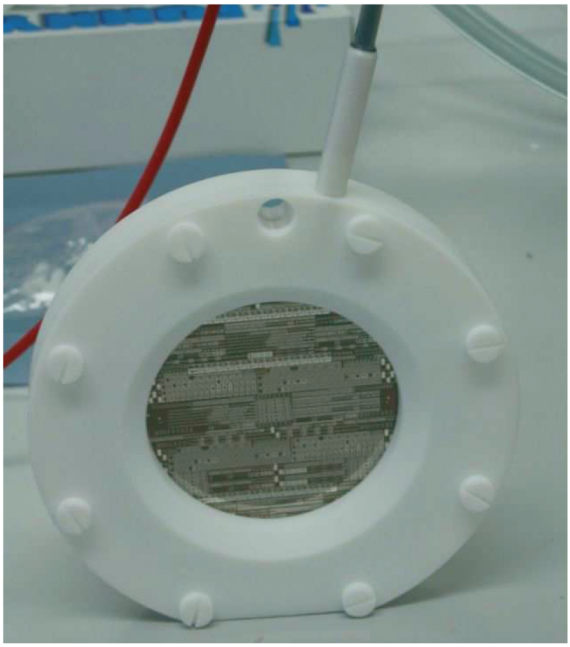

Figure 3.8 : Teflon chuck enclosing the wafer to be electroplated.

3. 2. 2 Fabrication process

Figure 3.9 illustrates the 5-mask process flow employed for the fabrication of Ag inductors. The processing steps regarding the underpass and the dielectric layer (Figure 3.9.a and b) are identical to those presented in the previous paragraph. Once via-holes through silicon dioxide are created and the native alumina film removed by RF-etching, without breaking the vacuum, a layer of Pt/Ti (50 nm/10 nm) is sputter deposited. This layer is successively patterned by dry-etching ICP in a mixed Cl_2/Ar chemistry. The Pt/Ti film is left only on the via-holes (Figure 3.9.c) in order to avoid passivation of the underlying Al. This additional step is crucial for preserving a good conductivity of the interconnects. Pt has been chosen since it is a noble metal and does not oxidize spontaneously in air.

As a next step, 300 nm of Ag are evaporated using 200 nm of Ti as adhesion layer. The equipment used is a Leybold e-beam evaporator. The wafers have been loaded into a planetary substrate holder. Evaporation in planetary mode is preferred over the conventional plateau mode, since the former allows for a greater angle between the evaporation source and the wafer. This, in turn enables a better step coverage. Subsequently, the evaporated Ag layer is patterned into spirals by wet-etching using a solution 8:1:1 of deionized water (DI H_2O), hydrogen peroxide (H_2O_2 40%) and ammonium hydroxide (NH_4OH 28%) (Figure 3.9.d). This solution being highly selective toward Ti, only Ag is removed. The etch-rate of Ag achieved using the mentioned dilution is 15 nm/s. The role played by the unpatterned Ti layer is to carry the charges all over the wafer surface during the electroplating process, while the structured Ag layer provides an adhesion site for the reduction of the Ag ions.

A 12 µm-thick photoresist layer (AZ9260) is then patterned into molds by means of UV-exposure (360 mJ/cm^2) and development using AZ 400K 3:1 (Figure 3.9.e). Figure 3.10 shows a SEM picture of fabricated photoresist molds. Structures with an aspect ratio of 2 have been achieved. The side-walls are smooth and well defined over the whole height. However, SEM inspections have revealed that in general the side-walls are not perfectly vertical, but instead are slightly curved inward, resulting in a reduced width that can be estimated to be about 1-1.5 µm at the half height of the structure. This is not surprising for such thick photoresist layers and is very likely due to UV scattering, and probably to an excessive development time. The quality of the molds has been observed to be very good over the entire wafer, meaning that the automated development process is homogeneous at the wafer-scale.

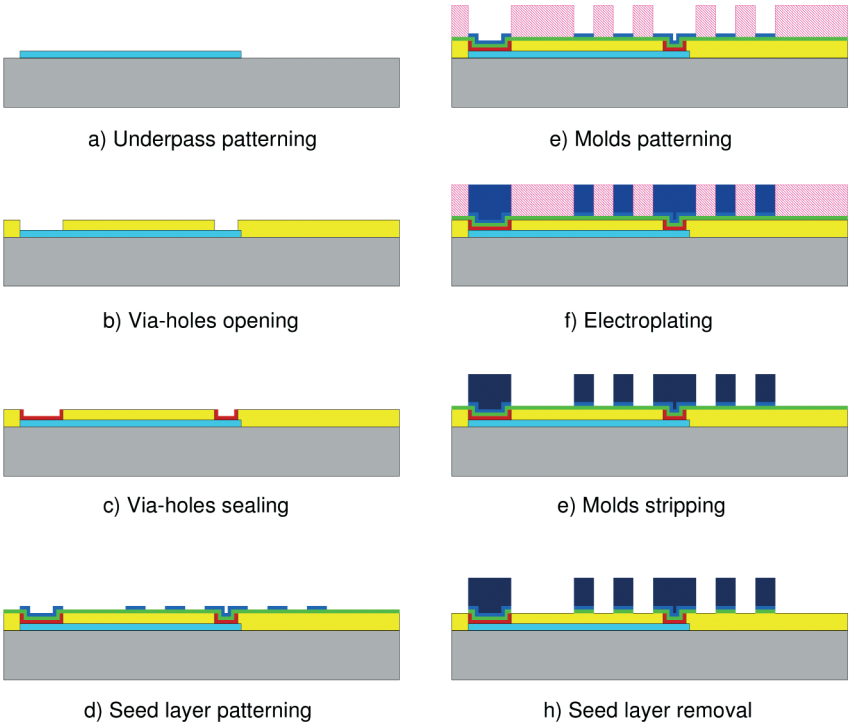

Figure 3.9 : Schematic cross-section of the 5-mask process developed for the fabrication of silver inductors.

The molds filling by means of electroplating is carried out by applying a constant current of 60 mA (Figure 3.9.f). This corresponds to a current density of about 1 mA/cm^2. The deposition rate of Ag achieved under these conditions is 350 nm/min. The photoresist molds are able to withstand very well the strongly alkaline environment of the plating bath (pH = 14) since no peeling or damages have been observed even after deposition processes of 30-40 minutes.

Once the plating process is completed and the wafer accurately rinsed, photoresist molds are stripped using a solution of PGMEA and NMP (Figure 3.9.g). Plasma O_2 after stripping has to be avoided as it severely reacts with Ag.

As a last step, the Ti seed layer is removed (Figure 3.9.h) by a dip of about 10 seconds in diluted hydrofluoric acid (HF 5%). During this procedure, Ag patterns act as masking material.

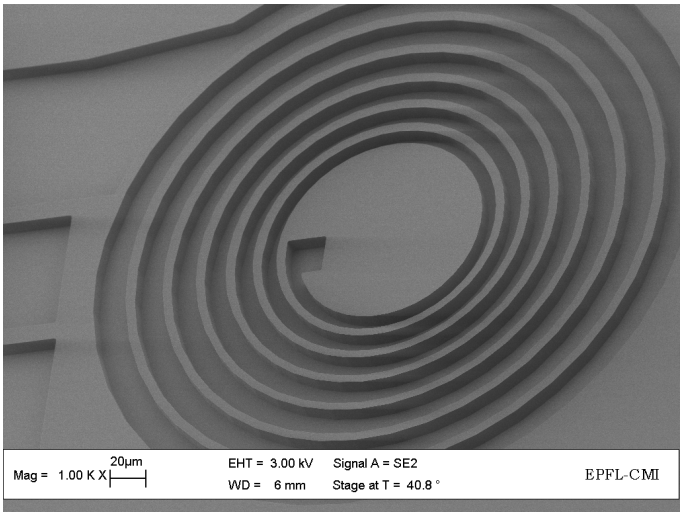

Figure 3.10 : SEM image of a mold patterned in a 12 µm-thick layer of photoresist AZ9260.

Figure 3.11 shows SEM pictures of a fabricated 12 µm-thick Ag inductor. The rounded profile of the electroplated patterns is due to the mold shape, which is not vertical. As a consequence, the gap between adjacent tracks is reduced compared to the original spacing on the mask. This fact has to be taken into account when discussing the results measured inductors. Figure 3.12 shows a test structure used to evaluate the size change of the fabricated patterns by optical measurement. It consists of two parallel scales constituted of open lines on one side and filled lines on the other side. The reference position is defined by the central pair of open and filled lines, which have the same width on the mask. The over or under sizing of the structure after electroplating is measured by counting the shift, from the reference lines, of the pair having the same width. Each shift corresponds to an enlargement or a reduction of 1 µm. In this case, an enlargement of 4-5 µm is measured between the fabricated pattern and the original design on the mask.

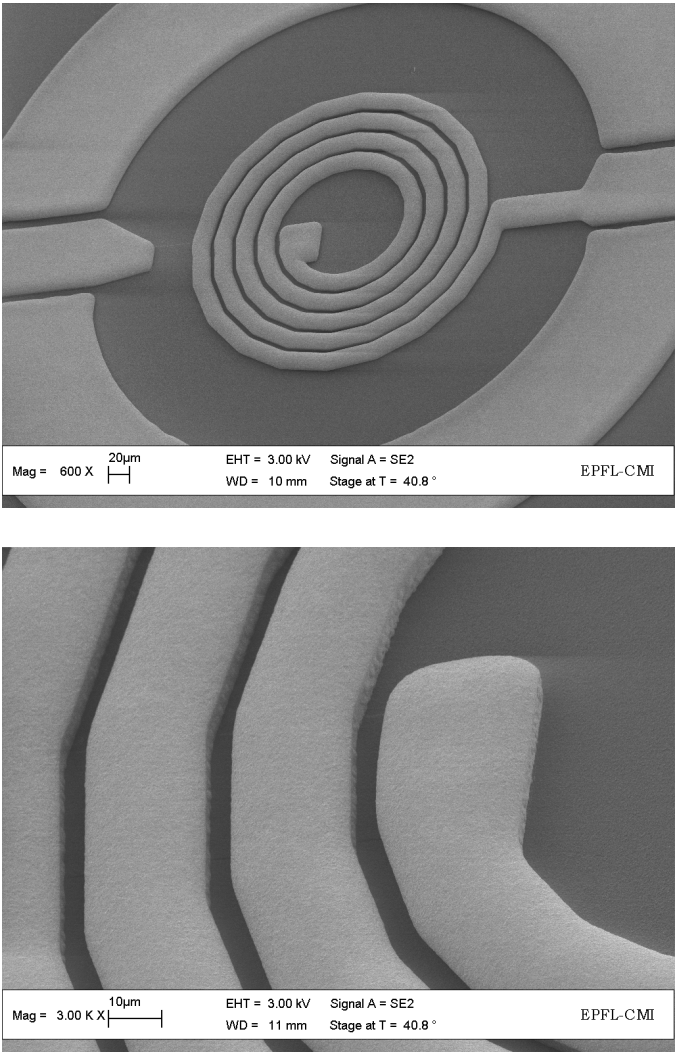

Figure 3.11 : SEM images of a fabricated 12 µm-thick Ag inductor (top), and close-up view of electroplated patterns revealing a rounded profile (bottom).

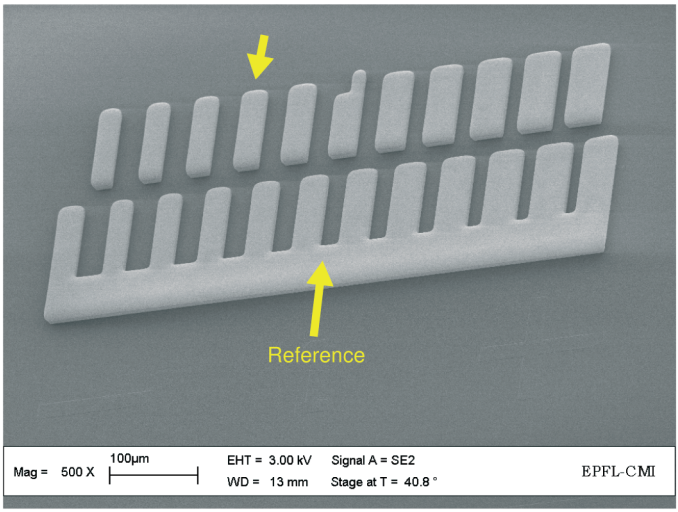

Figure 3.12 : SEM picture showing a test structure used to define the size change between the fabricated patterns and the original mask design. In this case, an enlargement of 4-5 µm is observed.

3. 2. 3 Characterization of electroplated Ag films

The 4-point resistivity measured on a 12 µm-thick Ag film is 1.8 ± 0.1 µΩ·cm. This value is 10% higher compared to the reported resistivity for the bulk metal (see Table 2.1). High purity electroplated films often have 5 to 10% higher resistivity and lower density compared to bulk values. Basically, the lower density and a small amount of trapped impurities contribute to the higher resistivity [1].

The uniformity of the metal thickness over the entire wafer is evaluated by surface profilometry. To do so, the thickness of several spirals has been measured at different locations on the wafer. The average thickness obtained at the centre is 11.7 ± 0.2 µm, while the average value on the edge is 14.0 ± 0.5 µm. This yields a thickness uniformity of 17% over the entire wafer surface. The non-zero thickness uniformity is a consequence of the ohmic drop occurring across the Ti seed layer, which results in a non-uniform deposition rate as a function of the distance from the wafer edge, i.e., the point where the current is injected into the seed layer. In comparison, the uniformity obtained with a single-point current feeding apparatus is 50%.

3. 3 Surface micromachined inductors

Deposition and etching of dielectric and metal thin-films to form 3-D structures is known as surface micromachining. Silicon dioxide is used in micromachining as an amorphous film. This film is subject to an isotropic etching because of the randomness of its microstructure. Wet-etching of a sacrificial layer of silicon dioxide in order to release the mechanical parts of sensors and actuators has become a popular surface micromachining technology [12]. Traditionally, the wafer to be etched is immersed in an aqueous solution containing HF [12-14] or buffered HF (BHF) [12]. The length of the undercut is controlled by the etching time. A huge inconvenience of this method is the well-known sticking effect. Sticking is often an irreversible and destructive phenomenon that occurs whenever liquids evaporate. Due to the cohesion forces of the liquid and in the presence of small gaps between the structures, the released parts tend to stick permanently to other structures or to the substrate.

3. 3. 1 Hydrofluoric acid (HF) vapor phase etching (VPE)

The key step of the developed fabrication process is the selective etching of the silicon dioxide layer separating the underpass from the spiral using hydrofluoric acid (HF) vapor phase etching (VPE). The use of the HF VPE enables the removal of the silicon dioxide in a vaporous environment rather than in an aqueous solution. This is of particular interest since sticking can be avoided. The set-up used for the vapor phase etching enables the etching of SiO_2 in a quasi-dry method, which means that the wafer never comes in contact with liquid. Moreover, cleaning or rinsing of the wafer is not needed afterwards. The chemical reaction between HF and silicon dioxide has been first published by Offenberg *et al.* [15]. A two-step reaction has been proposed, where first the SiO_2 surface is activated by adsorbed water, via the formation of silanol groups ($Si(OH)_4$). Subsequently, silanol groups are attacked by the HF to form volatile silicon tetrafluoride (SiF_4), that is successively desorbed from the surface.

$$SiO_2 + 2H_2O \rightarrow Si(OH)_4 \tag{3.4}$$

$$Si(OH)_4 + 4HF \rightarrow SiF_4 + 4H_2O \tag{3.5}$$

The above reactions show that water acts as initiator of the etching process as well as a by-product of the reaction. This fact suggests that the etching process can be temperature controlled to maintain in equilibrium the amount of H_2O needed to initiate the process and the amount of reactant H_2O [16]. The SiO_2 etch-rate can thus effectively be controlled by simply adjusting the wafer temperature. A higher temperature leads to less adsorbed water and hence to a reduced etch-rate.

Figure 3.13 shows the HF VPE equipment developed and commercialized by Idonus[3]. It consists of a wafer holder, a reaction chamber, a feedback system enabling to maintain a stable temperature during the process, and a sealeable container. The wafer holder consists of a PEEK® chuck onto which a Kapton® heating foil and a temperature sensor are glued. A heating element integrated in the wafer holder enables to set the wafer temperature. The wafer is fixed on the holder by a clamping ring. Screwing of the clamping ring is done from the backside of the apparatus, which never comes in direct contact with HF vapor. This way, only the wafer front-side is in contact with the HF vapor. Subsequently, the substrate holder is positioned upside-down onto the reservoir containing concentrated liquid hydrofluoric acid (HF 49%). The reaction chamber, is now sealed by the wafer holder. Since HF evaporates at room temperature the etching process starts spontaneously. The etch-rate is controlled by setting the wafer temperature, that can be adjusted from 35°C to 60°C.

3. 3. 2 Fabrication process

The schematic flow of the 4-mask surface micromachining process for the creation of free-standing planar spiral inductors is illustrated in Figure 3.14. The deposition and patterning of the Al underpass are performed with the conditions previously mentioned. After that, a 4 µm-thick SiO_2 layer is sputter deposited from a SiO_2 target in Ar plasma with an RF power of 1000 W. This thick silicon dioxide film plays the role of sacrificial layer. Via-holes are locally opened through this layer using dry-etching ICP based on C_4F_8 plasma. The equipment used is an Adixen AMS-200 DSE. The etch-rate of SiO_2 is 250 nm/min, with a selectivity of 1:5 towards the photoresist mask. Following the usual procedure, before depositing the next metal layer, a RF-etch in Ar atmosphere is performed for removing the native Al_2O_3 on the exposed areas of the underpass.

3. Idonus Sàrl, Jaquet-Droz 1, CH-2002 Neuchâtel, Switzerland. Website: http://www.idonus.com

Figure 3.13 : Experimental set-up used for the hydrofluoric acid (HF) vapor phase etching (VPE). The components are: the wafer holder with an integrated heating element, the reaction chamber containing liquid HF (49%), the feedback system used to control the temperature of the wafer holder, and a saleable container dedicated to the storage of used HF or to the refilling of the process chamber.

Without breaking vacuum, via-holes are filled by depositing 5 µm of Al. The metal film is subsequently removed by dry-etching ICP from the wafer surface, except for the via-holes regions that are protected by photoresist patterns. The Al etching process is followed by the strip of the residual photoresist mask using PGMEA/NMP and oxygen plasma. Again a step of RF-etch is performed for removing the native Al_2O_3 from the exposed metal patterns. In the same vacuum run a second 5 µm-thick Al film is deposited and patterned into spirals by dry-etching ICP.

After stripping the residual photoresist mask, the wafer is ready for the selective etching of the 4 µm-thick SiO_2 sacrificial layer. For this purpose, the wafer is fixed to the holder and positioned upside-down onto the reservoir containing the liquid HF. In this configuration, the HF vapor phase etching is in fact a maskless process.

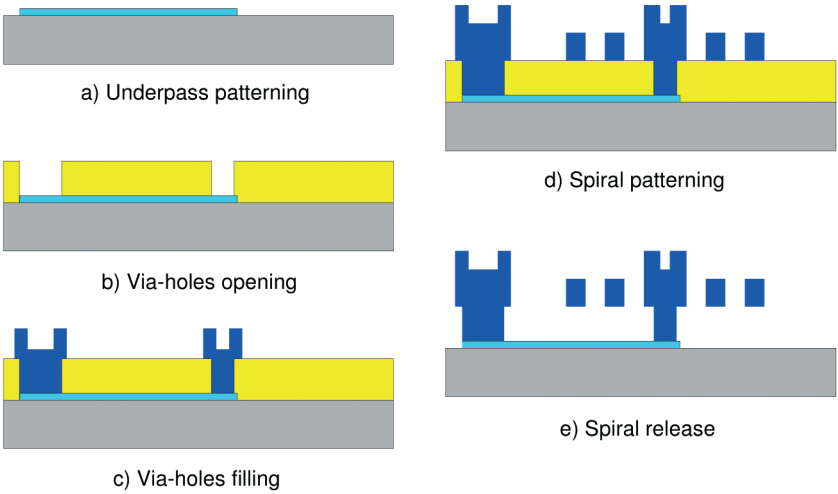

Figure 3.14 : Schematic view of the 4-mask process-flow for the fabrication of suspended planar inductors by means of HF vapor phase etching.

A constant temperature of 40°C has been imposed to the wafer during the etching process. Every 10 minutes the wafer has been taken out from the apparatus and inspected at the optical microscope in order to monitor the evolution of the etching progress. This has been indeed appreciable by the appearance of concentric rings of different colors in the SiO_2 film, revealing a non-uniform residual thickness. A careful characterization of the undercutting is of utmost importance in order to ascertain the effective release of the structure. For this purpose, the numerous test structures located at different zones of the wafer enable an accurate monitoring of the etching progress as a function of time. These structures consist of a series of isolated metal lines sitting on top of the sacrificial layer of SiO_2. The width of these metal lines ranges from 2 to 50 µm. The etching process has been carried out until the lines with largest width have been completely removed by the undercut. This ensures that also spiral inductors, which have a track-width ranging from 10 to 40 µm, are effectively released.

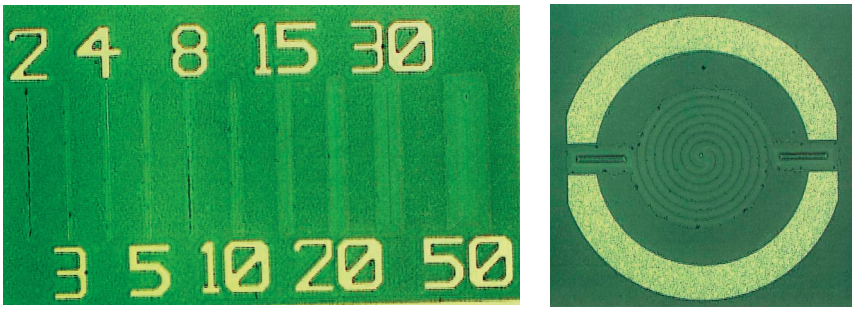

Figure 3.15 : Optical micrograph of the cell containing test lines completely washed away due to under-etching of SiO_2 (left), and a single-metal level device detached from the wafer (right). The HF VPE process has been carried out for 45 minutes imposing a temperature of 40°C to the substrate.

The efficiency of the releasing method using HF VPE is witnessed by optical images showing a test cell with all its metal lines washed away (see Figure 3.15 (left)), and a single-metal level spiral inductor with a track-width of 20 µm, that has been completely detached, except for the larger ground ring surrounding the coil (see Figure 3.15 (right)).

The etching rate of SiO_2 has been observed to be slightly faster at the centre of the wafer, where the largest test lines are completely detached after 40 minutes. Therefore, the process duration has been extended for an extra 5 minutes in order for the structures closer to the wafer edge to be also released.

SEM inspections have not revealed any stiction phenomena on devices with a diameter smaller than 500 µm. The moderate tensile stress measured on blanket Al thin-films (see paragraph 3.1.4) contributes in a large extent to avoid the structure from sticking onto the substrate or curling upwards. On the other hand, some of the devices with diameter greater than 500 µm have been observed to be locally pulled down to the substrate. However, it has not been possible to conclude whether the cause of the failure was stiction or a microgravity effect. Figure 3.16 shows SEM images of one of the fabricated free-standing planar spiral Al inductors separated from the substrate by means of an air-gap of 4 µm. It can also be noted that the metal has not been affected during the long exposition to HF vapor.

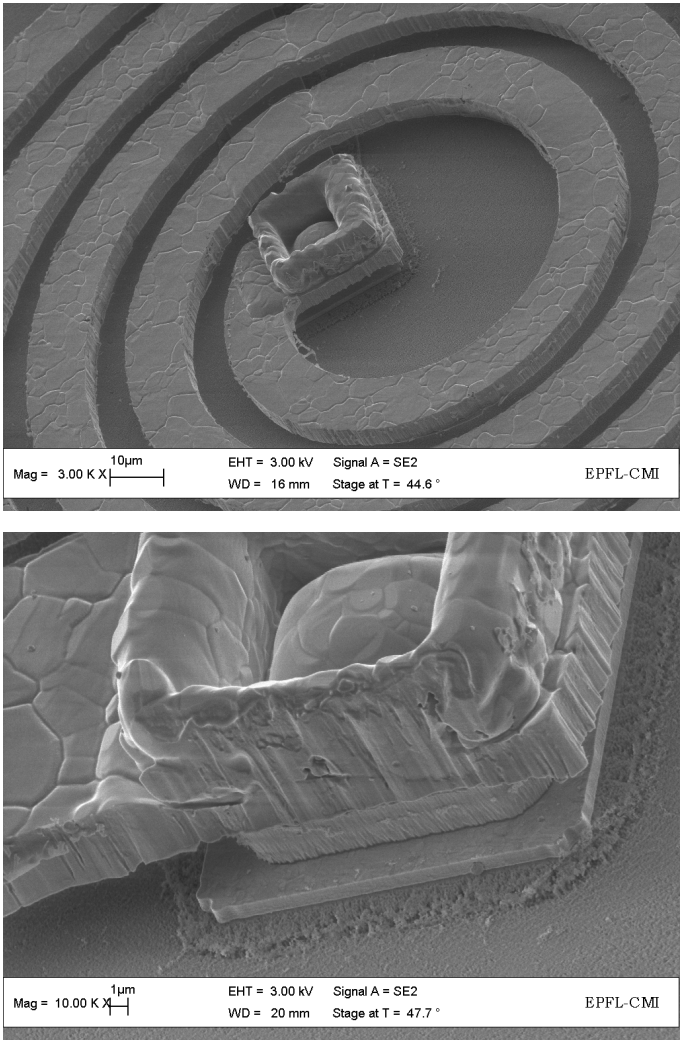

Figure 3.16 : SEM close-up views showing a suspended planar inductor separated from the substrate by means of a 4 µm-thick air-gap.

3. 4 Summary

Three simple, low-thermal budget and cost-effective micromachining processes developed for the fabrication of high-Q planar spiral inductors dedicated to RF applications have been presented. All the steps involved in the developed processes occur at low temperature (T_{max} < 150°C), except for the preliminary thermal oxidation of silicon substrates, thus making these microdevices potentially post-CMOS compatible.

The first process based on sputter deposited and dry-etched Al films has demonstrated vertical structures exhibiting aspect ratio up to 1.33 for film thickness up to 8 µm. The ability to form vertical patterns with high aspect ratio is an essential issue for creating minimum spacing between adjacent tracks of an inductor, and hence maximizing the total inductance per unit area through an enhanced magnetic coupling, as predicted by analytical or empirical expressions for the calculation of inductance of planar inductors. The quality of the deposited Al films has been characterized in terms of resistivity and residual stress. The moderate tensile stress measured (e.g., less than 40 MPa for a 8 µm-thick film) is an important issue for the integrity and reliability of these films. Moreover, DC measurements have pointed out that films with thickness exceeding 1 µm exhibit resistivity values only 10% away compared to the reported value for the bulk metal. Although this study specifically addresses inductors, the promising results issued from the dry-etching of thick Al films could also be exploited for fabricating other classes of RF passive components, such as transformers or interdigital capacitors. For these applications, the achievement of high aspect ratio structures is of paramount importance either for maximizing the coupling between primary and secondary coils, or for increasing the capacitance per unit area. As a general remark, the proposed planar geometry enables the devices to withstand violent mechanical shocks and vibrations and simplifies the packaging procedure.

The second process based on silver electroplating into polymer molds has enabled the fabrication of spiral inductors with a thickness of 12 µm. The upper limit of the achievable metal thickness is imposed by the thickness of the photoresist film used as mold. The measured resistivity of the electroplated silver is 10% higher compared to the value of the bulk metal. It has been shown that the electroplated patterns are characterized by a rounded profile. This can be attributed to the loss of width of the mold walls, that results in a shape slightly curved inward rather than vertical. As a main consequence, the spacing between adjacent tracks of an inductor is reduced by about 4 µm compared to the gap of the mask layout.

Finally, the third process based on a maskless selective etching of a sacrificial SiO_2 layer by means of vapor HF, has demonstrated the fabrication of planar spirals suspended over an air gap of 4 μm. The fabrication issues have been very promising because no stiction has occurred on those devices with a diameter up to 500 μm. The success of the presented process strongly relies on the fact that thick Al layers exhibit low tensile stress, thus preventing the spiral from curling up or from collapsing onto the substrate. An additional factor increasing the attractiveness of this process is that Al films have been observed to be substantially unaffected by corrosion in vapor HF environment. On the contrary, Al films would have been severely attacked in liquid HF or BHF solutions.

3. 5 References

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CHAPTER 4

RF CHARACTERIZATION OF INDUCTORS

THIS chapter presents an empirical study of the performances of planar spiral inductors. The goal of the study is to characterize the inductor performances and to see how these are related to materials issues and layout parameters. The different trends issued from the analysis of experimental data will constitute the basis for the establishment of accurate and scalable design rules enabling the fabrication of optimized inductors tailored for a desired inductance value.

The usual procedure undertaken for characterizing the performances of RF inductors involves the measurement of scattering parameters (S-parameters), the computation of impedance and Q-factor and, successively, the matching of measured data through simulations using an equivalent electrical model whose parameters describe the inductor behavior as a function of frequency. The elements used for the matching of measured data are commonly referred to as the *extracted parameters* and the fitting procedure itself is known as *parameter extraction*.

4. 1 RF measurement

On wafer two-port S-parameters have been measured using an Agilent N5230A network analyzer, a Karl-Süss probe station and Süss-Rosenberger ground-signal-ground (g-s-g) coplanar probes with a pitch of 100 µm. A standard short-open-load-through (SOLT) calibration is performed before the session of device measurement. Each inductor is measured from 30 MHz to 10 GHz in linear scale. During the measurement, the wafer is left at a floating potential onto the prober chuck. Measured S-parameters of one-port devices are then converted to impedance, Z_{11}, using (4.1). Open structures are also measured in order to de-embed the inductance measurement from the parasitics associated to the probing pads.

$$Z_{11} = Z_0 \cdot \frac{1 + S_{11}}{1 - S_{11}} \tag{4.1}$$

Z_0 is the characteristic 50 Ω impedance of the system. The inductor Q-factor is taken as the ratio of imaginary part of the impedance, Im(Z), to the real part, Re(Z). As discussed in paragraph 2.1, this definition is meaningful when the inductor is operated below its self-resonance. The Q-factor can be expressed directly as a function of S_{11} parameter, using the following expression [1] :

$$Q = \frac{2 \cdot \left| Im(S_{11}) \right|}{1 - \left| S_{11} \right|^2} \tag{4.2}$$

4. 2 Modeling

This section presents the development of an equivalent wide-band model enabling the simulation of the inductor behavior as a function of frequency. Figure 4.1 illustrates the conventional Π-type model describing the impedance behavior of a two-port inductor on a lossy substrate. The elements constituting the equivalent model are indicated in the schematic cross-section of a planar spiral inductor represented in Figure 4.2. The physical meaning of the lumped elements is the following [2] : L_s and R_s represent the series inductance and series resistance

of the metal trace (i.e., spiral and underpass). The term C_s models the capacitive coupling due to the overlap between the spiral and the underpass. An additional contribution to C_s arises from the capacitive coupling due to fringing fields between adjacent tracks. However, it is reported that the latter contribution is generally overwhelmed by the spiral-to-underpass coupling [3]. In fact, since adjacent tracks are almost equipotential, they form a capacitance that stores a negligible amount of energy and in a first approximation its contribution to the total parasitic capacitance can be neglected. However, this assumption could not be valid any longer if the spiral thickness becomes comparable to the spacing between adjacent tracks. Therefore, one of the goals of the presented empirical study is to provide an insight on the effective role of the interturn capacitance.

The network composed by C_{ox}, R_{sub} and C_{sub} accounts for the parasitics associated to the lossy substrate. C_{ox} models the oxide capacitance between the spiral and the substrate; whereas, R_{sub} and C_{sub} represent the silicon substrate resistance and capacitance, respectively. Since low-loss substrates, such as HRS and Pyrex, have very large values of R_{sub}, this term can be omitted from the circuit. As a result, the impedance of the substrate network reduces to a single capacitance dominated by the smaller one between C_{ox} and C_{sub}. This resulting capacitance combines then in parallel with C_s. Under this assumption, the term C_s now accounts for the total parasitic capacitance of the inductor.

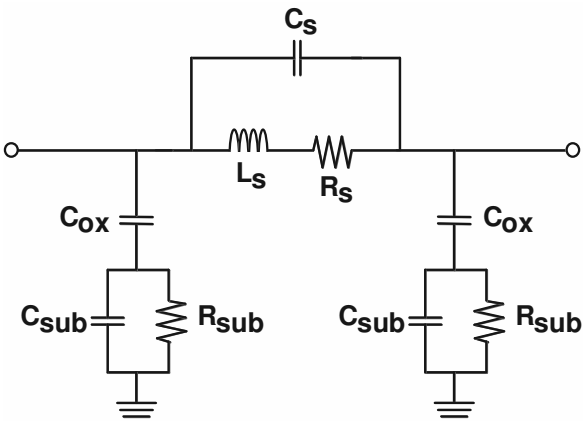

Figure 4.1 : Conventional Π-type equivalent model representing a two-port inductor on a lossy substrate.

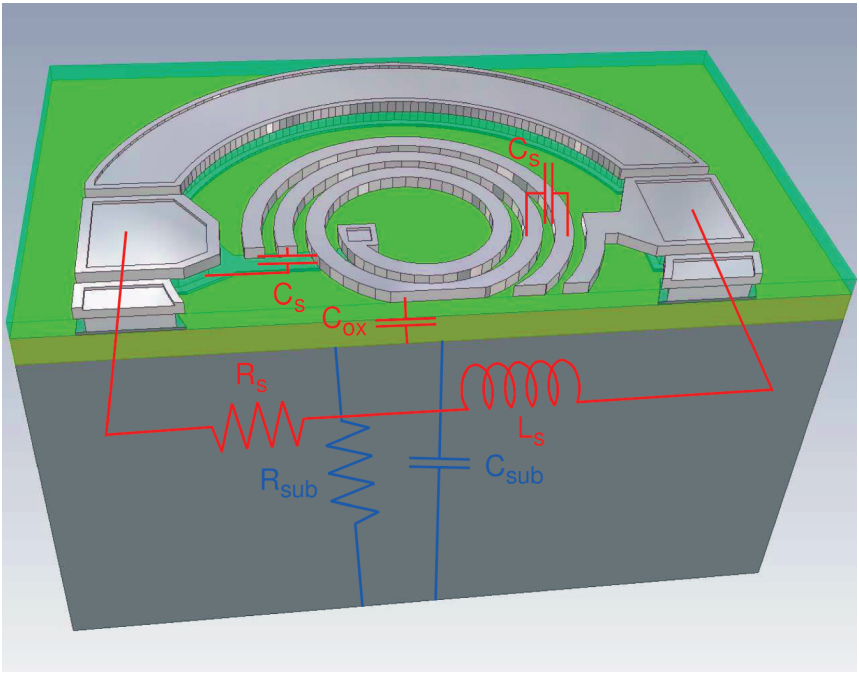

Figure 4.2 : Schematic cross-section of a two-port spiral inductor on a lossy substrate.

A major limitation of the classic Π-type model is the lack of a term describing the frequency-dependent increase of the metal resistance due to skin and proximity effect. The present work addresses this problem by developing an equivalent model that is capable to take into account the increase of the metal resistance, as well as the energy dissipation in the dielectric layers.

The proposed 6-element compact model used for the simulation of inductors on low-loss substrates is depicted in Figure 4.3. Here, a parallel network made of a resistor, R_f and an inductor, L_f is added in series to the main circuit. The purpose of the R_f-L_f network is to mimic the high-frequency increase of the conductor resistance [4, 5]. In addition, compared to the conventional Π-model, the proposed development presents a resistor R_d in series with C_s. The role of the term R_d is to account for the high-frequency dielectric losses occurring in the distributed capacitance. Since the proposed model is made of frequency-independent terms, it can be implemented on simulators such as Agilent's IC-CAP.

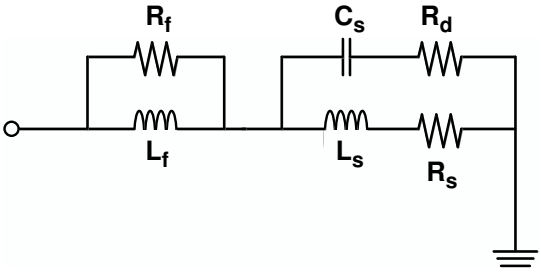

Figure 4.3 : Compact equivalent circuit based on frequency-independent elements used for simulating the behavior of a single-port inductor on a low-loss substrate.

The real and imaginary parts of impedance of the above circuit are given by the following expressions :

$$Re(Z) = \frac{\omega^2 R_f L_f^2}{R_f^2 + \omega^2 L_f^2} + \frac{R_s + \omega^2 C_s^2 R_d (R_s (R_s + R_d) + \omega^2 L_s)}{(1 - \omega^2 C_s L_s)^2 + \omega^2 C_s^2 (R_s + R_d)^2} \qquad (4.3)$$

$$Im(Z) = j\omega \frac{R_f^2 L_f}{R_f^2 + \omega^2 L_f^2} + \frac{L_s - R_s^2 C_s + \omega^2 C_s (C_s R_d^2 L_s - L_s^2)}{(1 - \omega^2 C_s L_s)^2 + \omega^2 C_s^2 (R_s + R_d)^2} \qquad (4.4)$$

The low-frequency approximation of (4.3) is dominated by the term R_s, as the other real terms are affected by the frequency. Hence, R_s represents the DC resistance of the spiral inductor. On the other hand, (4.4) indicates that at sufficiently low frequency, the imaginary part of impedance can be approximated by $\omega \cdot L_s$. This is because the first term on the right hand-side of (4.4), i.e., the one containing R_f and L_f, is usually a few orders of magnitude smaller compared to L_s. Therefore, L_s represents the equivalent inductance of the device. As the frequency increases, the other terms get more and more importance and Im(Z) departs from $\omega \cdot L_s$, as a consequence of the contribution of the parasitic capacitance, metal resistance and dielectric losses. Since the comparison of the performances of

inductors with different geometry and dimension is difficult, a *figure-of-merit* (FOM) has been defined :

$$FOM = Q_{max} \cdot L_s \tag{4.5}$$

where Q_{max} (or peak-Q) corresponds to the maximum value achieved by the Q-factor and L_s is the low-frequency inductance value extracted from the equivalent circuit. Based on the extracted parameters L_s and C_s, the following relationship has been used to calculate the self-resonant frequency, f_{SR} of those inductors having a self-resonance beyond the upper limit of the measured frequency range.

$$f_{SR} = \frac{1}{2\pi\sqrt{L_s \cdot C_s}} \tag{4.6}$$

Figure 4.4 represents the parameters used to describe the layout of a spiral inductor. These are, the outer diameter, D_{out}, the track-width, w, the track-to-track or inter-turn spacing, s, and the number of turns, n. The g-s-g pad for the RF measurement is shown on the left.

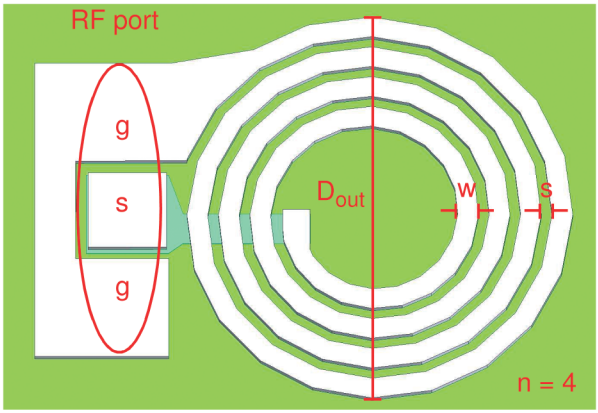

Figure 4.4 : Representation of the parameters used to describe the layout of a spiral inductor. The g-s-g pad for the RF measurement is also shown.

4. 3 Results and discussion

4. 3. 1 Equivalent model

The overall behavior of a measured inductor is compared to simulations issued from the proposed equivalent model (see Figure 4.3). The considered inductor is fabricated with a 12 µm-thick Ag spiral and is implemented on Pyrex substrate; its layout parameters are : D_{out} = 500 µm, w = 20 µm, s = 9 µm and n = 4. The measured versus simulated magnitude and phase of S_{11} are displayed in cartesian form (Figure 4.5.a) and in the Smith chart (Figure 4.5.b), respectively. The imaginary part of impedance divided by the angular frequency, Im(Z)/ω and the real part of the impedance, Re(Z) are plotted in (Figure 4.5.c). The value of the equivalent inductance, L_s extracted at low frequency from the curve Im(Z)/ω is 7.03 nH. Whereas the series resistance, R_s corresponding to the low-frequency value of the curve Re(Z) is 0.9 Ω. The whole set of extracted parameters is reported in Table 4.1. The self-resonant frequency, f_{SR} corresponds to the point where the inductor impedance is purely real. This occurs where Im(Z)/ω, and consequently the Q-factor, drop to zero. In this case f_{SR} is situated at 8.4 GHz. Finally, the inductor Q-factor is plotted in Figure 4.5.c. Initially, Q increases linearly because the reactance is increasing with frequency and the skin effect has not yet become noticeable. Soon, however, the metal losses due to skin and proximity effect become an issue. The Q still raises, but at a lesser rate and the slope gradually decreases. The flat part of the curve, where the Q attains its peak value, occurs as the series resistance and the reactance are changing at the same rate. Beyond this region, the parasitic capacitance and the ever more severe metal losses conspire to decrease the inductor Q-factor. Beyond the self-resonance the Q drops to negative values and the inductor impedance turns capacitive.

In general, simulated data are in excellent agreement with measurement all over the considered frequency range. The noisy behavior shown by measured data in the region where the Q-factor reaches its peak is due to the lack of accuracy in the measurement of the reflection coefficient, S_{11}. In fact, expression (4.2) shows the denominator is very sensitive to $|S_{11}^2|$, especially for values of S_{11} close to unity. Here, an error of few hundredths of dB results in a large variation of the calculated Q. It is therefore very hard to measure high-Q values using standard S-parameters techniques. This remark holds for the rest of the discussion of experimental data.

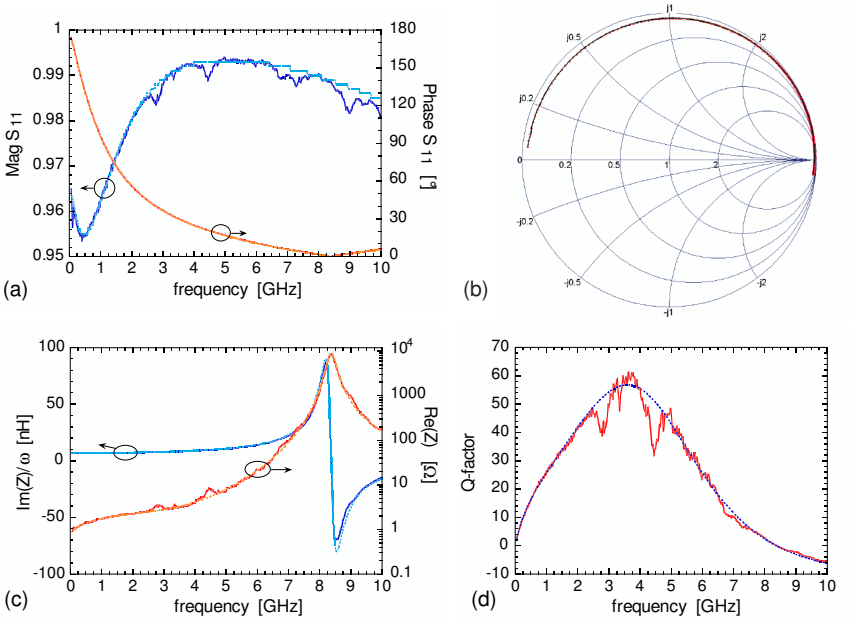

Figure 4.5 : Measured (full lines) and simulated data (dashed lines) of a 12 µm-thick Ag inductor fabricated on Pyrex. Magnitude (absolute values) and phase of S_{11} (a), Smith chart of S_{11} (b), Re(Z) and Im(Z)/ω (c), and Q-factor (d).

TABLE 4. 1 : SET OF EXTRACTED PARAMETERS CORRESPONDING TO THE SIMULATION OF THE AG INDUCTOR ON PYREX REPORTED IN FIGURE 4.5.

L_f [nH]	R_f [Ω]	L_s [nH]	R_s [Ω]	C_s [fF]	R_d [Ω]
0.27	1.35	7.03	0.9	51.4	14.4

4. 3. 2 Substrate type

Figure 4.6 and Figure 4.7 highlight the role played by the substrate resistivity on the Q-factor and Im(Z)/ω, for a set of inductors with identical layout (D_{out} = 500 µm, w = 20 µm, s = 6 µm and n = 3) and fabricated with a 3 µm-thick Al spiral. These inductors are implemented on three different substrates : Pyrex, high-

resistivity Si and doped Si, respectively. The corresponding performances and extracted parameters are summarized in Figure 4.8.

In general, the inductor fabricated on Pyrex exhibits considerably better performances in terms of Q_{max} and self-resonant frequency compared to the inductors fabricated on Si. Particularly, the 5.86-nH inductor on Pyrex achieves a Q_{max} of 37 at 4.2 GHz and a f_{SR} of 9.7 GHz; while the peak-Q of the 5.84-nH device on HRS is 22 at 3 GHz for a corresponding f_{SR} of 8.2 GHz. The 4.98-nH inductor on doped Si exhibits the poorest performances, with a Q_{max} of 10 at 1.4 GHz and a self-resonance of 7.4 GHz. The insulating nature of Pyrex suppresses energy dissipation through the substrate. In addition, the smaller relative permittivity of Pyrex ($\varepsilon_r = 4.6$) compared to Si ($\varepsilon_r = 11.7$) decreases the magnitude of the parasitic capacitance. As a consequence, the self-resonance is shifted toward higher values.

From Figure 4.8 it can be seen that the larger value of C_s corresponds to the inductor on doped Si. This can be attributed to the fact that in a more conductive substrate, the electric field lines terminate closer to the silicon surface due to the skin effect in the substrate, and therefore the effective substrate thickness decreases [6]. As a result, the parasitic capacitance increases and the self-resonance occurs at lower frequency.

The lower value of L_s shown by the inductor on doped Si can be attributed to image currents induced in the substrate that flow in a direction opposite to that of the current in the spiral. The resulting negative mutual coupling between these currents reduces the magnetic field, and lowers the overall inductance.

On the other hand, the term R_d drops as a function of the substrate resistivity. This is an indication of the more severe losses occurring in doped Si ($R_d = 95\ \Omega$) compared to HRS ($R_d = 35\ \Omega$) and Pyrex ($R_d = 18\ \Omega$).

The comprehensive trend of inductor performances as a function of the substrate type is shown in Figure 4.9. In general, for any given inductance value, devices fabricated on Pyrex exhibit larger Q-factors in the order of 40% and 70%, compared to devices implemented on HRS or on doped Si, respectively.

In conclusion, Pyrex appears as the most suitable substrate for fabricating high-performance inductors operating at several GHz. In addition, another advantage of Pyrex is represented by its low cost compared to high-resistivity Si wafers.

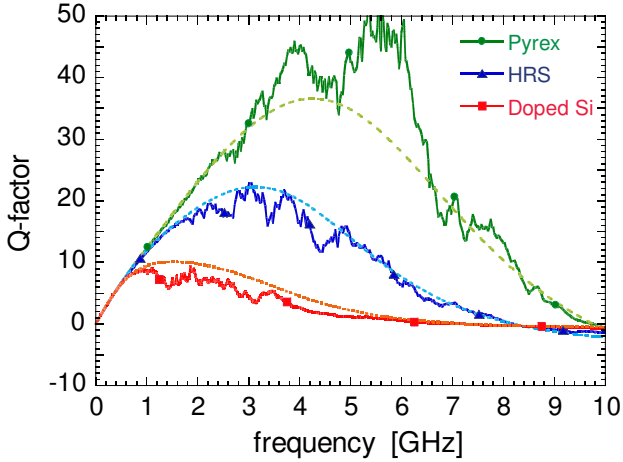

Figure 4.6 : Measured (full lines) and simulated Q-factor (dashed lines) for a set of inductors with a 3 µm-thick Al spiral and identical layout, fabricated on Pyrex, high-resistivity Si, and doped Si, respectively.

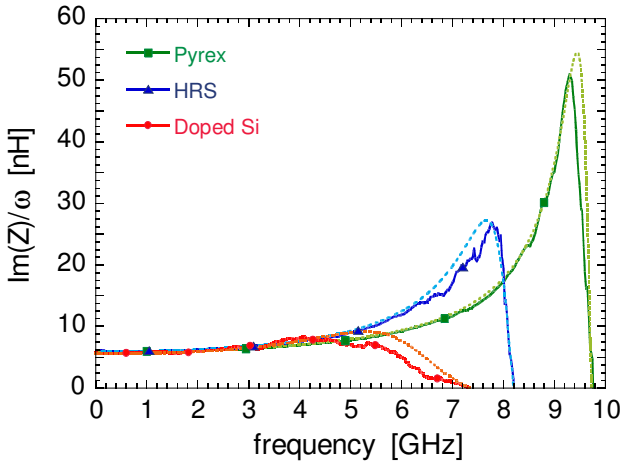

Figure 4.7 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) for a set of inductors with a 3 µm-thick Al spiral and identical layout, fabricated on Pyrex, high-resistivity Si, and doped Si, respectively.

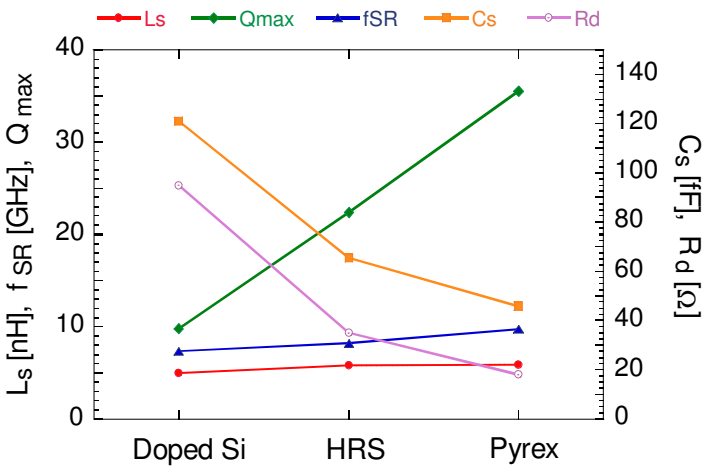

Figure 4.8 : Extracted parameters and performance outlook as a function of the substrate type for 3 µm-thick Al inductors with identical layout.

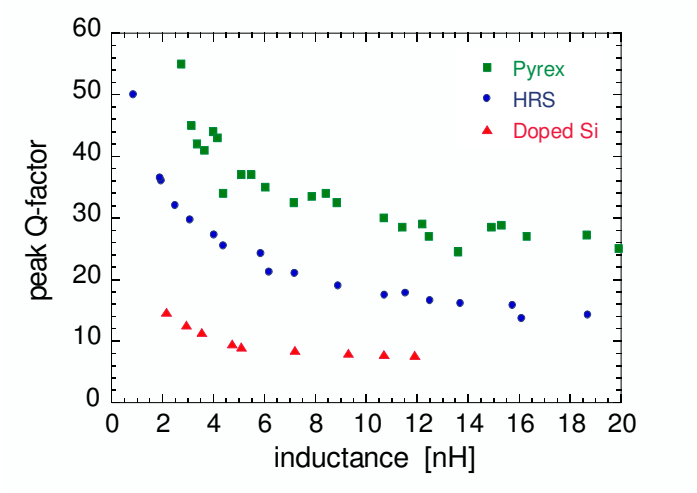

Figure 4.9 : Comprehensive outlook of the performances exhibited by 3 µm-thick Al inductors fabricated on Pyrex, high-resistivity Si, and doped Si, respectively.

4. 3. 3 Spiral conductivity

4. 3. 3. 1 Spiral thickness

This paragraph emphasizes the effect of the spiral thickness on the achievable performances by comparing a set of inductors fabricated on Pyrex with an identical layout (D_{out} = 400 µm, w = 20 µm, s = 6 µm and n = 3), but with a 4, 6 or 8 µm-thick aluminum coil. Figure 4.10 and Figure 4.11 show the trend of Q-factor and Im(Z)/ω, while Figure 4.12 summarizes the performances and the most relevant extracted parameters.

First of all, increasing the spiral thickness from 4 to 8 micrometers produces an effective drop of R_s of about 42%. This in turn allows for a significant improvement of both Q_{max} and $Q_{@2,4GHz}$ in the order of 20%. Moreover, a close look to the values of $Q_{@2,4GHz}$ reveals a more substantial improvement comparing the 4 to the 6 µm-thick inductor, than comparing the 6 to 8 µm-thick inductor. This stems from the effective saturation of the metal thickness, previously discussed (section 2.1), occurring when Al films approach a thickness of 8 µm.

On the other hand, the 4 µm-thick inductor has a slightly larger value of inductance (L_s = 3.55 nH) compared to the 8 µm-thick device (L_s = 3.44 nH). This is essentially due to geometrical reasons as, in general, a conductor with smaller cross-section displays a larger inductance because it generates a stronger external magnetic flux [2, 7], which in turn enhances the mutual magnetic coupling between neighboring conductors.

Furthermore, the term C_s remains practically constant on all the considered inductors. This means that a two-fold increase of the spiral thickness does not produce any significant increase of parasitic capacitance due to the fringing fields between adjacent tracks. This suggests that the effective capacitive coupling occurs mainly through the underlying Si dioxide and Pyrex substrate, rather than through the air. In fact, since the relative permittivity of SiO_2 (ε_r = 3.9) and Pyrex (ε_r = 4.6) is larger compared to the relative permittivity of air (ε_r = 1), the electric field lines couple more strongly through these dielectrics.

In conclusion, despite the proposed 8 µm-thick spiral inductors require a more challenging dry-etching process for their fabrication, the significant enhancement of Q_{max} and $Q_{@2,4GHz}$ justifies the use of such thick Al films.

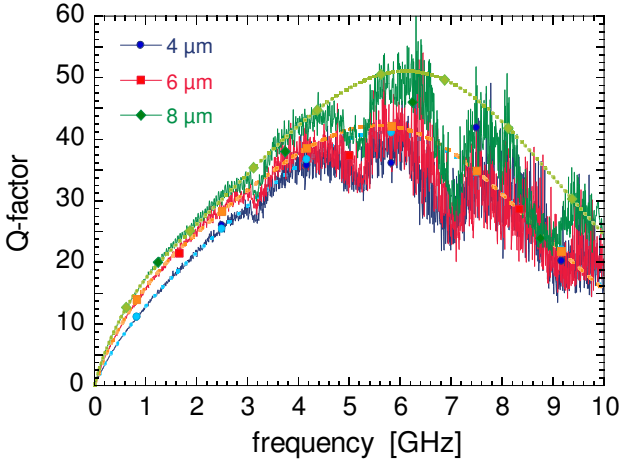

Figure 4.10 : Measured (full lines) and simulated Q-factor (dashed lines) as a function of the spiral thickness for a set of Al inductors with identical layout fabricated on Pyrex substrate.

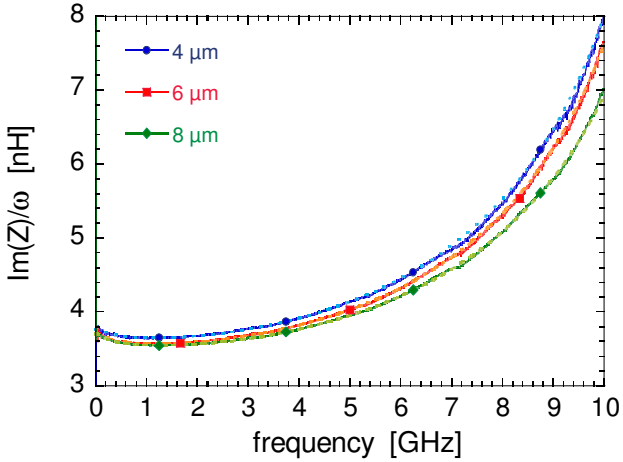

Figure 4.11 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) as a function of the spiral thickness, for a set of Al inductors with identical layout fabricated on Pyrex substrate.

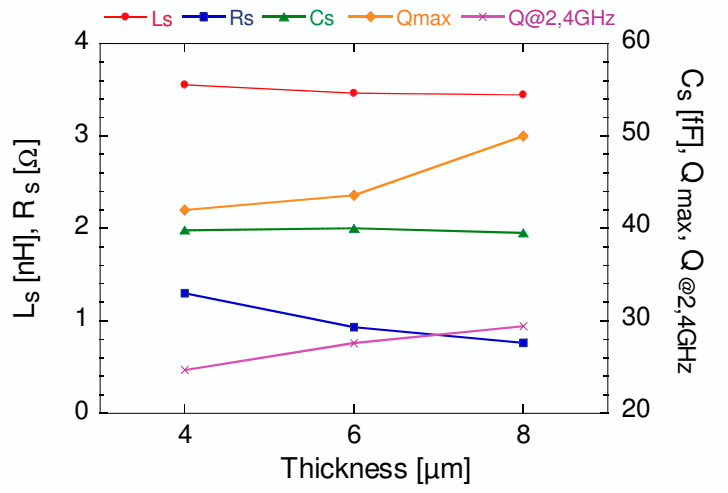

Figure 4.12 : Extracted parameters and performance outlook as a function of the spiral thickness for Al inductors with identical layout, fabricated on Pyrex substrate.

4. 3. 3. 2 Al versus Ag metallization

This paragraph compares the performances of two inductors fabricated with a 8 µm-thick Al and a 12 µm-thick Ag spiral, respectively. Both inductors have an identical layout (D_{out} = 400 µm, w = 20 µm, s = 6 µm and n = 4) and are implemented on Pyrex. The Q-factor curves are plotted in Figure 4.13, while Im(Z)/ω is displayed in Figure 4.14. The peak-Q and the $Q_{@2,4GHz}$ of the Ag inductor show an improvement of 20% compared to the Al inductor. This is directly related to the lower series resistance of the Ag inductor (R_s = 0.82 Ω) compared to its Al counterpart (R_s = 0.92 Ω).

On the other hand, the Ag inductor also exhibits a 8% higher series inductance (L_s = 5.09 nH) compared to the Al inductor (L_s = 4.68 nH). This stems from an enhanced magnetic coupling, that is very likely to be related to the unplanned reduction of the spacing left between electroplated structures (see paragraph 3.2.2).

As discussed in the previous paragraph, the thickness of the structures does not affect the parasitic capacitance. In fact, the extracted values of C_s differ less than 1%. Therefore, the lower self-resonance of the Ag inductor is only due to its larger series inductance.

The comprehensive trend of inductor performances as a function of the spiral conductivity is shown in Figure 4.15. Clearly, the inductors fabricated with thick electroplated Ag spirals show a substantial improvement of Q-factor because of the lower series resistance resulting from the combination of a higher metal conductivity and the increased conductor cross section. Although the skin effect confines moving charges to a thin portion near the conductor surface, the increased conductor thickness provides a larger cross section available for the conduction of charges. Consequently, the larger cross section multiplied by the coil length results in a significant increase of the useful area available for the current flow.

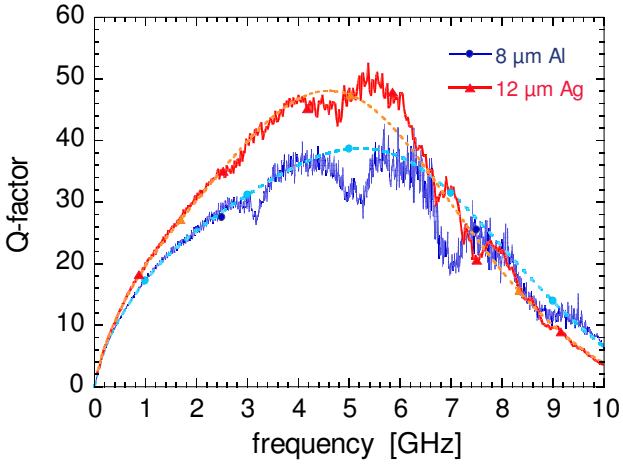

Figure 4.13 : Measured (full lines) and simulated Q-factor (dashed lines) of two inductors with identical layout fabricated with a 8 µm-thick Al or a 12 µm-thick Ag spiral, respectively. Both inductors are fabricated on Pyrex.

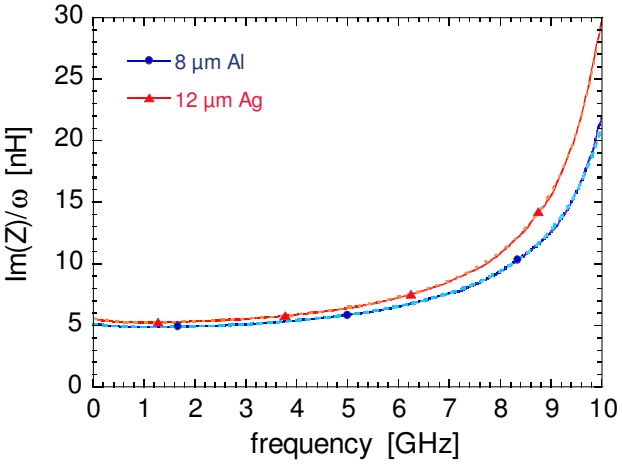

Figure 4.14 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) of two inductors with identical layout fabricated with a 8 µm-thick Al or a 12 µm-thick Ag spiral, respectively. Both inductors are fabricated on Pyrex.

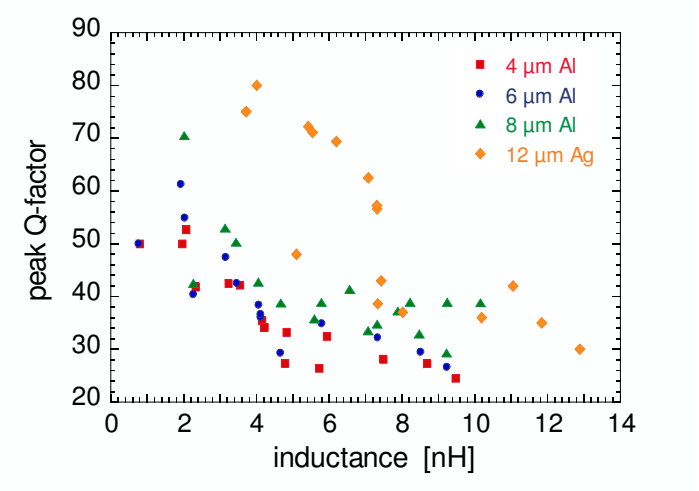

Figure 4.15 : Performance outlook as a function of the spiral conductivity. All inductors are fabricated on Pyrex substrate.

4. 3. 4 Layout parameters

4. 3. 4. 1 Number of turns

Figure 4.16 and Figure 4.17 highlight the trend exhibited by the Q-factor and Im(Z)/ω as a function of the number of turns. The reported set of inductors is fabricated with a 8 µm-thick Al spiral on Pyrex substrate. These devices share a constant D_{out} of 400 µm, w of 20 µm and s of 6 µm. The increase of the number of turns is done by progressively filling the spiral toward the centre. The outlook of the performances is summarized in Figure 4.18.

Basically, increasing the number of turns increases the series inductance of the coil, as a consequence of an enhanced contribution of self and mutual inductance. However, at the same time, the peak-Q drops because of the increased series resistance of the coil. The measured inductors exhibit values of Q_{max} situated between 22 and 70 for corresponding inductances of 6.0 and 2.02 nH, respectively. The self-resonant frequency is shifted progressively towards lower values when increasing n. This is primarily due to the increase of L_s and, in a lesser extent, to the increase of parasitic capacitance, C_s. Adding extra turns to the inductor not only raises the spiral length, but also increases the number of overlapping areas between the coil and the underpass. The net result is thus an increase of the parasitic capacitance due to coil-to-underpass and turn-to-turn coupling. However, all the presented inductors have a self-resonant frequency situated above 9 GHz, meaning that these devices could be operated up to that frequency.

Figure 4.18 shows that the equivalent inductance increases almost linearly up to 4 turns; whereas, adding extra turns, shows a weaker effect on L_s. In fact, since the innermost turns have a small periphery, their contribution to the total inductance is less marked. Nevertheless, these innermost turns contribute significantly to the high-frequency resistance since they suffer from more severe current crowding. This phenomenon is especially evident in the 6-turn inductor, where the slope of Q-factor decreases at a much faster rate compared to the inductors with less turns.

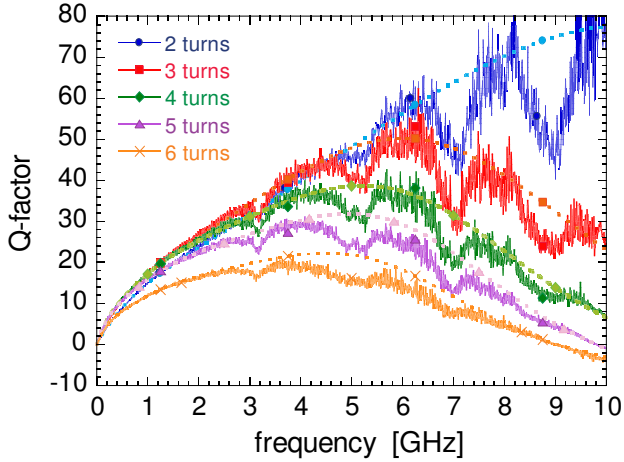

Figure 4.16 : Measured (full lines) and simulated Q-factor (dashed lines) as a function of the number of turns, *n*, for a set of 8 µm-thick Al inductors with identical outer diameter, fabricated on Pyrex substrate.

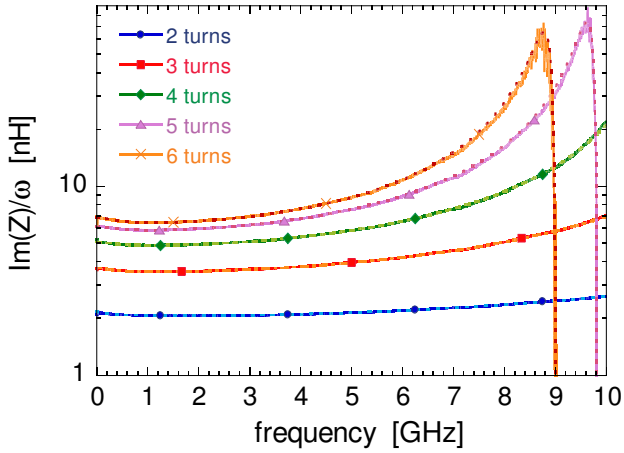

Figure 4.17 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) as a function of the number of turns, *n*, for a set of 8 µm-thick Al inductors with identical outer diameter, fabricated on Pyrex substrate.

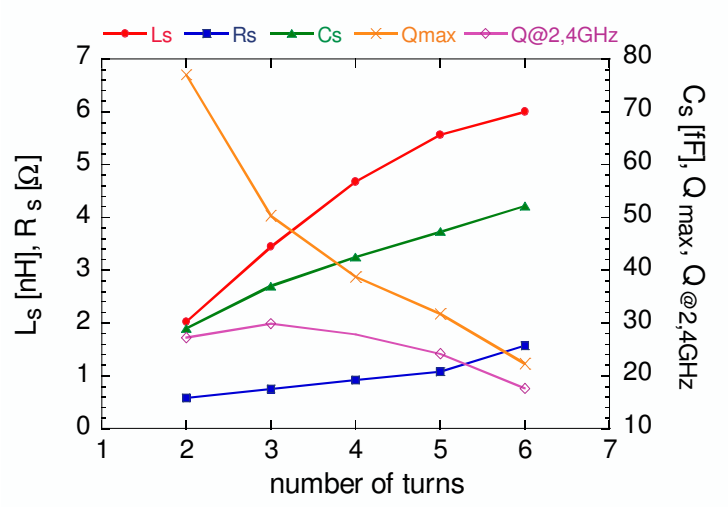

Figure 4.18 : Extracted parameters and performance outlook as a function of the number of turns, for a set of Al inductors with identical layout fabricated on Pyrex substrate.

4. 3. 4. 2 Outer diameter

Figure 4.19 displays the Q-factor as a function of the outer diameter for a set of four inductors having a constant *w* of 20 µm and *s* of 8 µm. The outer diameter and the number of turns have been adjusted in order to design a set of inductors with a constant coil length (l = 3620 µm). The reported set of inductors is fabricated with a 8 µm-thick Al spiral on Pyrex. Figure 4.20 summarizes the outlook of the performances and the extracted parameters.

All the presented devices display close inductance values. These are comprised between 3.37 and 3.96 nH. In addition, the values of series resistance, R_s (not displayed) are practically identical due to the same coil length. Nonetheless, the performance exhibited by these inductors differ significantly. As a general trend, the inductors with largest diameters, i.e., 600 and 440 µm exhibit the highest Q_{max} (41 and 45) and $Q_{@2,4GHz}$ (31 and 30). On the other hand, the two devices with smaller footprint, i.e., with a diameter of 370 and 340 µm, but with more turns, show a dramatic reduction of both Q_{max} (39 and 28) and $Q_{@2,4GHz}$ (17 and 24). Since the latter two inductors are filled with turns almost

up to the centre, they are more concerned by proximity effect, which is responsible for the high-frequency increase of the metal resistance and hence for the degradation of the achievable Q-factor.

Unlike R_s and L_s, the parasitic capacitance, C_s is considerably affected by the inductor footprint (see Figure 4.20). Particularly, C_s exhibit a linear increase as a function of the outer diameter, even though the number of turns (and thus the number of overlaps between the spiral and the underpass) is less for inductors with larger diameter. This demonstrates that the role played by the inter-turn coupling capacitance is far from being negligible. On the contrary, for inductors with few turns and large outer diameter the inter-turn coupling overwhelms the coil-to-underpass capacitance. Thus, for a constant coil length a larger inductor footprint determines a lower f_{SR}. However, in all cases f_{SR} is located well above 10 GHz.

In conclusion, for a given inductance value, the devices that perform better are those with a larger footprint and less turns, i.e., those presenting a more "hollow" spiral. However, since these devices also occupy a larger chip area, they may not always be the best choice for the circuit designer. In this case, a compromise between a high Q-factor and a limited size has to be found.

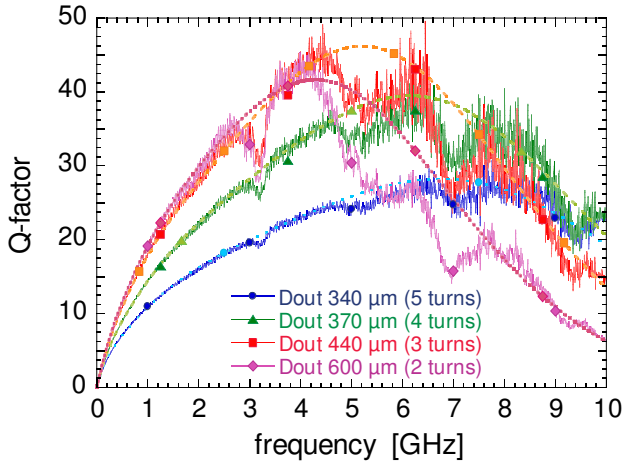

Figure 4.19 : Measured (full lines) and simulated Q-factor (dashed lines) as a function of the outer diameter, D_{out}, for a set of 8 µm-thick Al inductors fabricated on Pyrex substrate.

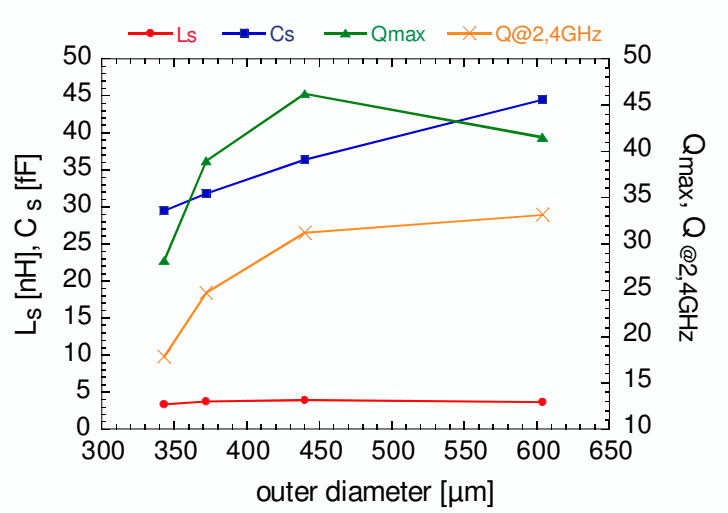

Figure 4.20 : Extracted parameters and performance outlook as a function of the outer diameter, for a set of 8 µm-thick Al inductors with identical coil length fabricated on Pyrex substrate.

4. 3. 4. 3 Track-to-track spacing

Figure 4.21 and Figure 4.22 highlight the trend exhibited by the Q-factor and Im(Z)/ω as a function of the track-to-track spacing, *s*. The reported inductors (D_{out} = 500 µm, w = 20 µm, and n = 4) are fabricated with a 3 µm-thick Al spiral on Pyrex. The outlook of the performances and extracted parameters is summarized in Figure 4.23. The reported inductors with s = 4 µm up to s = 18 µm exhibit peak-Q ranging from 34 to 38, and $Q_{@2,4GHz}$ between 28 and 25, for corresponding inductances of 8.7 and 5.8 nH, respectively. The series inductance, L_s is observed to decrease almost linearly as the track-to-track spacing increases. This is primarily due to the weaker mutual magnetic coupling between conductors [8, 9], and in a lesser extent, to a reduced self-inductance due to the shorter coil length. Similarly, an increase of s produces a significant decrease of C_s and results in higher self-resonances. This due to the mitigated capacitive coupling between conductors that become further spaced away. As a general trend, inductors with smaller inter-turn spacing are more attractive since they achieve higher inductance per unit area and display a better $Q_{@2,4GHz}$.

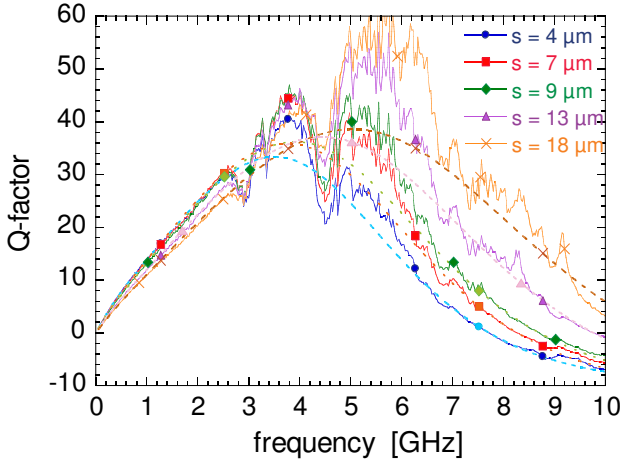

Figure 4.21 : Measured (full lines) and simulated Q-factor (dashed lines) as a function of the track-to-track spacing, *s*, for a set of 3 µm-thick Al inductors with identical layout fabricated on Pyrex.

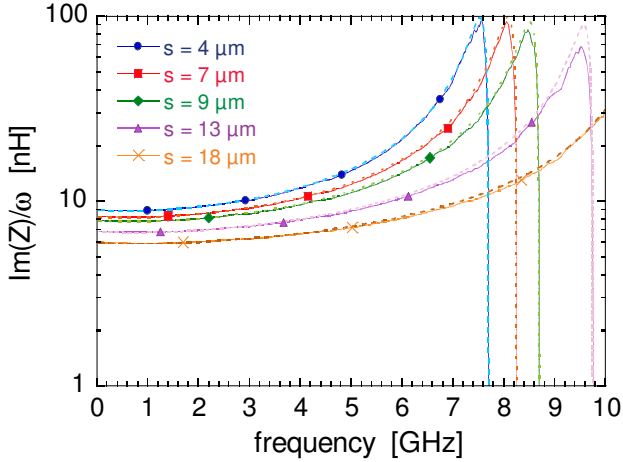

Figure 4.22 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) as a function of the track-to-track spacing, *s*, for a set of 3 µm-thick Al inductors with identical layout fabricated on Pyrex.

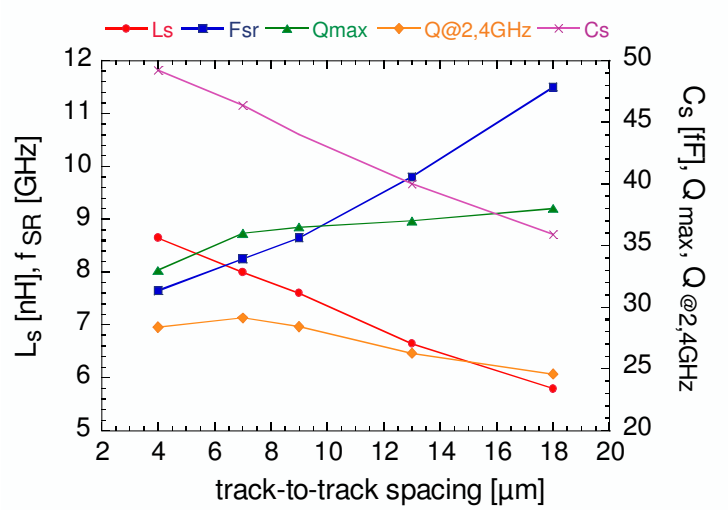

Figure 4.23 : Extracted parameters and performance outlook as a function of the track-to-track spacing, *s*, for a set of 3 µm-thick Al inductors with identical layout fabricated on Pyrex substrate.

4. 3. 4. 4 Track-width

The role of the track-width, *w* has been characterized by comparing a set of four inductors with a constant coil length (l = 3620 µm), track-to-track spacing (s = 8 µm) and 4 turns. Particularly, inductors with a track-width of 10, 20, 30 and 40 µm have been designed by adjusting the outer diameter in order to keep the same coil length. Consequently, an increase of the track-width results in a larger inductor footprint and in a decreased portion of void area at the center of the spiral. All the inductors have been fabricated with a 8 µm-thick Al spiral and have been implemented on Pyrex. Figure 4.24 shows the measured versus simulated Q-factor and Figure 4.25 displays measured versus simulated Im(Z)/ω. The outlook of the performances and extracted parameters is summarized in Figure 4.26.

A huge difference is observed by comparing the Q-factor curves of the four inductors. In fact, the inductors with narrower track-width (i.e., w = 10 and 20 µm) exhibit both a significantly larger peak-Q and $Q_{@2,4GHz}$ compared to inductors with wider tracks (i.e., w = 30 and 40 µm). Furthermore, by looking at the curves

of Im(Z)/ω (see Figure 4.25) and at the trend of L_s versus w (see Figure 4.26), it can be noted that inductors with narrower track-width display larger inductance. This is because a conductor with smaller cross-section generates more magnetic flux external to the conductor itself, which in turn improves the magnetic coupling and enhances the mutual inductance between adjacent tracks of the spiral [10].

As expected, the extracted values of series resistance, R_s decrease as w increases (see Figure 4.26). However, the obtained trend also emphasizes that the series resistance decreases at a slower rate compared to L_s. Consequently, L_s is the factor that dominates the slope of the Q-factor curve below the peak region.

Beside the lower value of inductance per unit length, the proximity effect can certainly be blamed for the worse performance shown by the inductors with larger track-width [8]. In fact, eddy currents generated by magnetic fields of neighboring conductors constrict the current flow toward the trace edges, thereby increasing the high-frequency series resistance, and ultimately vanishing the benefit brought by a larger conductor cross-section in decreasing the DC resistance.

In conclusion, for the considered constant value of coil length, inductors with narrow track-widths display a better figure-of-merit resulting from the combination of higher inductance and improved Q-factor. Moreover, they are also more attractive due to the smaller footprint. On the contrary, inductors with larger track-width display a lower inductance per unit coil length and are more prone to suffer from high-frequency resistance increase due to proximity effect.

In conclusion, very wide conductors should be used only for implementing inductors with few turns and with a large portion of void area at the center of the spiral.

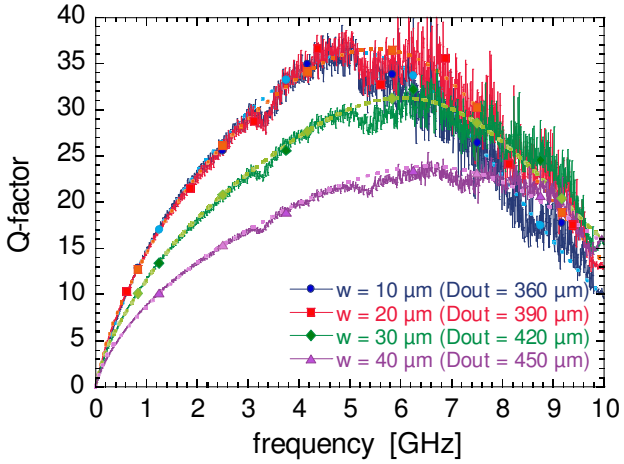

Figure 4.24 : Measured (full lines) and simulated Q-factor (dashed lines) as a function of the track-width, *w*, for a set of 8 µm-thick Al inductors on Pyrex with identical coil length, *l*, track-to-track spacing, *s*, and 4 turns.

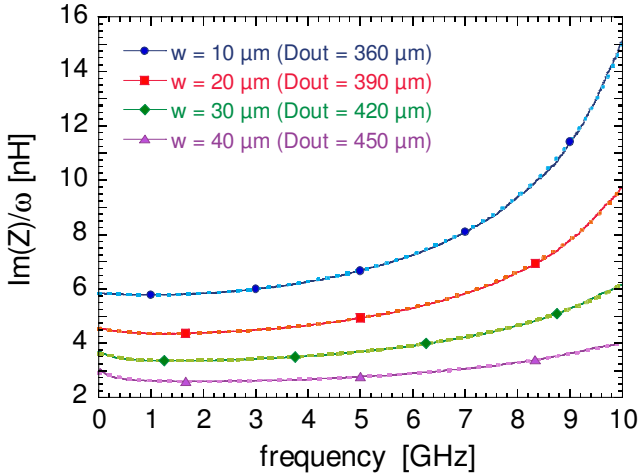

Figure 4.25 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) as a function of the track-width, *w*, for a set of 8 µm-thick Al inductors on Pyrex with identical coil length, *l*, track-to-track spacing, *s*, and 4 turns.

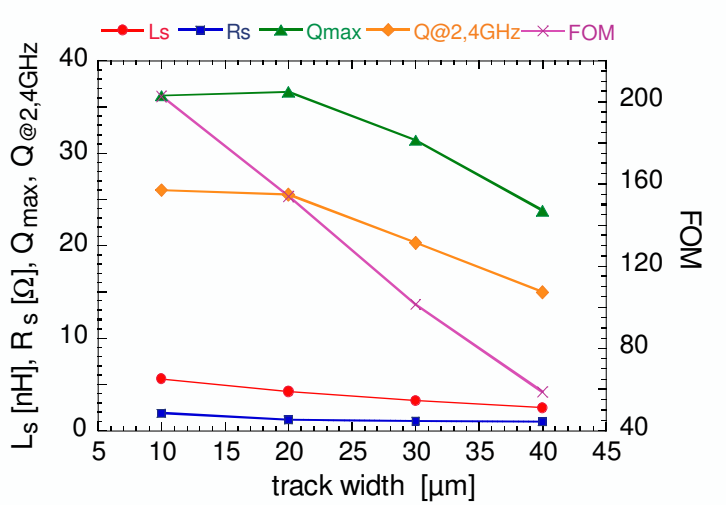

Figure 4.26 : Extracted parameters and performance outlook as a function of the track-width, *w*, for a set of 8 µm-thick Al inductors with identical coil length fabricated on Pyrex substrate.

4. 3. 4. 5 Coil shape

This paragraph addresses the study of inductor performances as a function of the polygonal shape of the coil. For this purpose, several inductors with different spiral layouts have been designed. Figure 4.27 shows the layout of a circular spiral inductor (designed with a polygonal coil of 40 sides) and a hexagonal spiral inductor. The following layout parameters are the same for each inductor : D_{out} = 450 µm, w = 20 µm, s = 8 µm and 5 turns. These device have been fabricated with a 8 µm-thick Al spiral on top of a Pyrex substrate. Figure 4.28 and Figure 4.29 emphasize the trend exhibited by the Q-factor and Im(Z)/ω as a function of the polygonal shape of the coil. The outlook of the performances is summarized in Figure 4.30.

For a given outer diameter, a spiral approaching a circular shape has a larger coil length, and consequently exhibits a greater total inductance per unit area. Particularly, the equivalent inductance remains almost constant for inductors with the largest number of sides, i.e., 40 (7.05 nH), 20 (7.0 nH) and 16 (6.95 nH), and

then drops for devices with less sides, i.e., 12 (6.58 nH), 8 (6.11 nH) and 6 (5.34 nH). It is also observed that, inductors approaching a circular shape exhibit in general better performances in terms of Q_{max}, $Q_{@2,4GHz}$ and figure-of-merit. However, they show a lower self-resonance because of the increased inductance and, in a lesser extent, due to higher inter-turn capacitance. On the other hand, spiral inductors with small number of sides suffer from a more severe resistance increase as a function of frequency because sharp corners constrict the high-frequency current flow to a reduced portion of the conductor width.

In conclusion, spiral inductors approaching a circular shape perform better compared to inductors with polygonal coils made up of few sides.

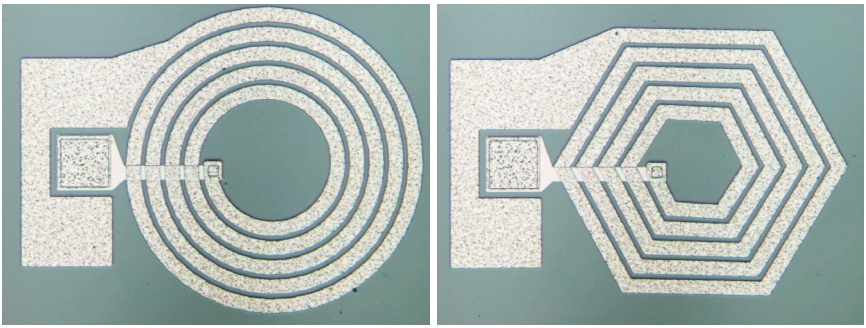

Figure 4.27 : Layout of a circular inductor designed with a polygonal coil shape of 40 sides (left), and layout of a hexagonal inductor (right). In Both cases, the following layout parameters : D_{out} = 455 µm, w = 20 µm, s = 8 µm and n = 5, are kept constant.

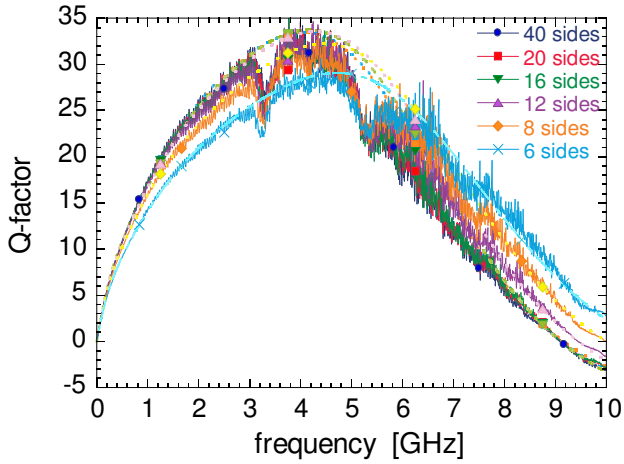

Figure 4.28 : Measured (full lines) and simulated Q-factor (dashed lines) as a function of the polygonal shape of the coil for a set of 8 µm-thick Al inductors fabricated on Pyrex.

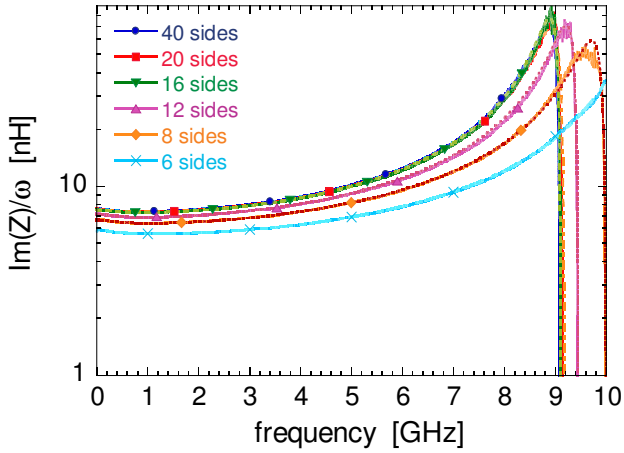

Figure 4.29 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) as a function of the polygonal shape of the coil for a set of 8 µm-thick Al inductors fabricated on Pyrex.

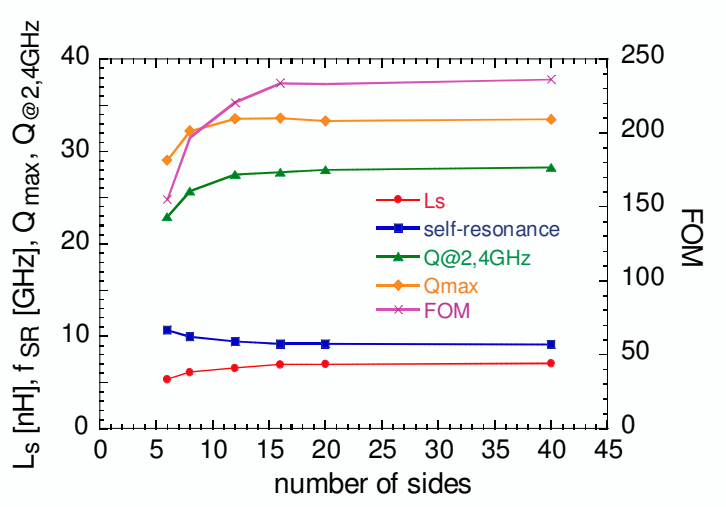

Figure 4.30 : Extracted parameters and performance outlook as a function of the number of sides constituting the polygonal shape of the coil.

4. 3. 4. 6 Spiral-to-underpass capacitance

This paragraph investigates the role played the parasitic capacitive coupling between the spiral and the underpass on the overall performances of spiral inductors. To do this, a set of inductors with identical layout (D_{out} = 400 µm, w = 20 µm, s = 6 µm and n = 4), but with an underpass width ranging from 10 to 40 µm, has been designed and fabricated with a 8 µm-thick Al spiral on Pyrex. Figure 4.31 shows the obtained Q-factor as a function of the underpass width; while, the performance outlook and extracted parameters are summarized in Figure 4.32.

The variation of the underpass width manifests its most prominent effect on the total parasitic capacitance, C_s, that increases gradually as the overlap between coil and underpass becomes larger. This results in a noticeable decrease of self-resonance, but is less significant, though still appreciable, on Q_{max} and $Q_{@2,4GHz}$. The extracted series resistance, R_s exhibits a decrease of 18% when comparing the inductor with 40 µm-wide underpass to its counterpart with 10 µm-wide underpass. This slightly enhances the $Q_{@2,4GHz}$ of the inductor with larger underpass. Based on the above considerations, the underpass width should be designed neither too narrow, nor too wide.

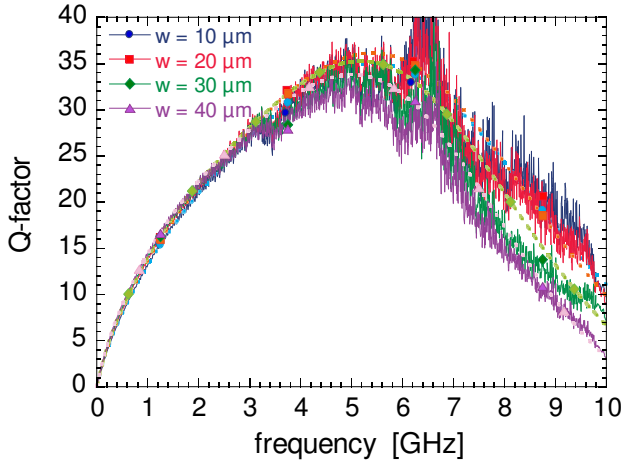

Figure 4.31 : Measured (full lines) and simulated Q-factor (dashed lines) as a function of the underpass width for a set of 8 µm-thick Al inductors fabricated on Pyrex, with identical layout.

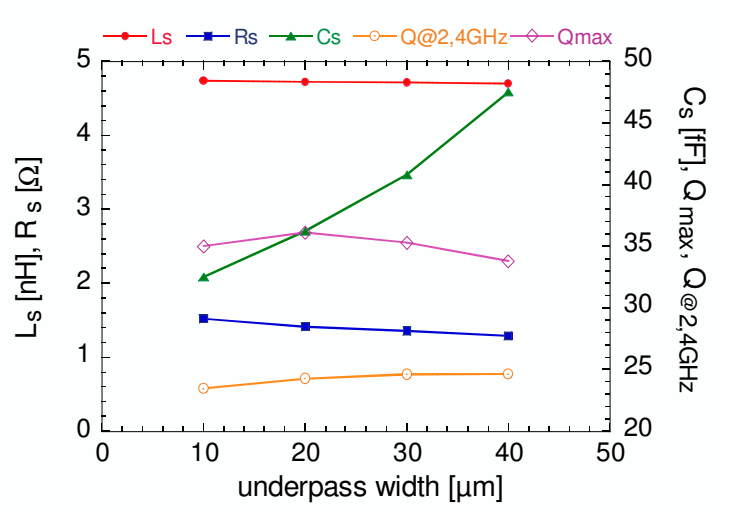

Figure 4.32 : Extracted parameters and performance outlook as a function of the underpass width for a set of inductors with identical layout.

4. 3. 5 Tapered inductor

This paragraph quantifies the performance improvement obtained on inductors having a tapered coil. Tapering consists in progressively narrowing the inner turns of a spiral inductor. Figure 4.33 shows the layout of a reference inductor having a constant track-width, w of 20 µm, and the corresponding tapered version in which the second turn has been narrowed by 2 µm, the third turn has been narrowed by 4 µm, and so forth in steps of 2 µm up to the innermost turn. Figure 4.34 and Figure 4.35 compare the measured Q-factor and Im(Z)/ω of a reference inductor versus its tapered version. Both inductors have same outer diameter (D_{out} = 350 µm), inter-turn spacing (s = 6) and number of turns (n = 4), and have been fabricated with a 8 µm-thick Al spiral on a Pyrex substrate.

The peak-Q and the $Q_{@2,4GHz}$ of the tapered inductor are 45 and 36, respectively. These performances correspond to a 12% and 17% improvement, respectively, over the corresponding values shown by reference inductor. In general, the significant performance improvement is primarily due to the increased inductance generated by the tapered inductor. The latter displays an inductance of 4.38 nH, that is 12% higher compared to the reference inductor (L_s = 3.86 nH). In fact, tapered tracks being longer and narrower they generate more self and mutual inductance and, hence, increase L_s. As a result, the higher inductance raises the slope of Q at low frequency. The Q enhancement is very significant, even though the series resistance of the tapered inductor (R_s = 1.15 Ω) is larger than the corresponding value of the reference inductor (R_s = 1.09 Ω). However, in this case, the increased series inductance overwhelms the larger series resistance. Moreover, adopting a tapered layout, the high-frequency increase of the metal resistance due to proximity effect is mitigated since the inductor presents a larger "hollow" area at the centre of the coil.

The parasitic capacitance of the reference inductor (C_s = 29.3 fF) is slightly higher than the one displayed by the tapered device (C_s = 28 fF). This is because the former presents a larger total area where the coil overlaps the underpass. In addition, the larger track-width contributes to increase the inter-turn capacitance.

The overall better performances achieved by several tapered inductors are highlighted in Figure 4.36. Here, the values of Q_{max}, $Q_{@2,4GHz}$ and figure-of-merit show a significant improvement compared to the corresponding performances of reference inductors.

In conclusion, the proposed layout improvement consisting in progressively tapering the coil of a spiral inductor has been demonstrated to be very effective in

enhancing the overall inductor performances. This type of layout is especially attractive whenever large inductance values are required (e.g. > 10 nH) altogether with a limited size budget.

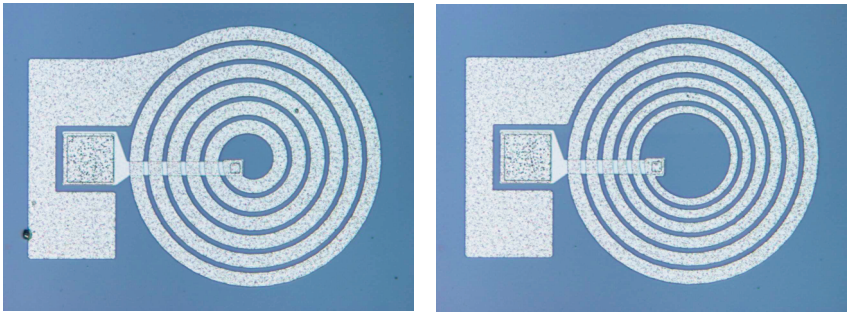

Figure 4.33 : Pictures showing the layout of a reference inductor with constant track-width of 20 µm (left), and the corresponding tapered version (right) in which each turn has been progressively narrowed in steps of 2 µm.

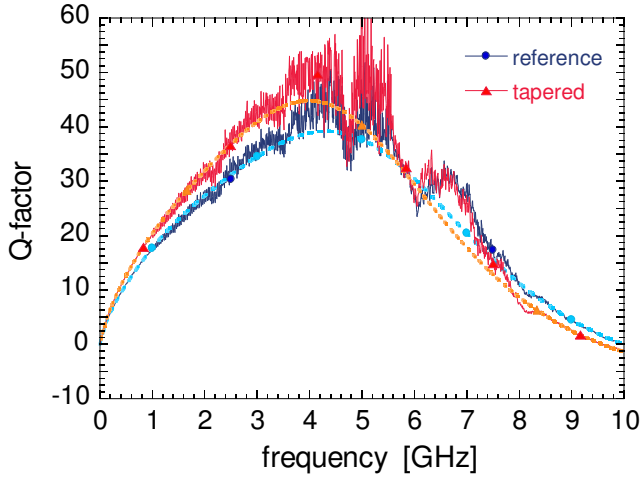

Figure 4.34 : Measured (full lines) and simulated Q-factor (dashed lines) of two 8 µm-thick Al inductors fabricated on Pyrex. One inductor has a coil with constant track width (reference), whereas the other one has a tapered coil.

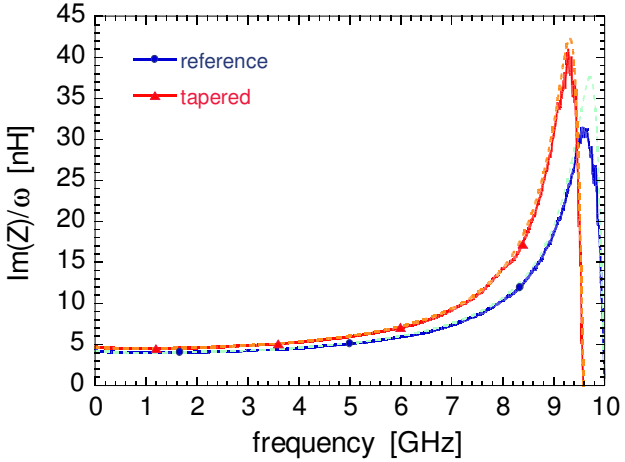

Figure 4.35 : Measured (full lines) and simulated Im(Z)/ω (dashed lines) of two 8 µm-thick Al inductors fabricated on Pyrex. One inductor has a constant track width, while the other one has a tapered coil.

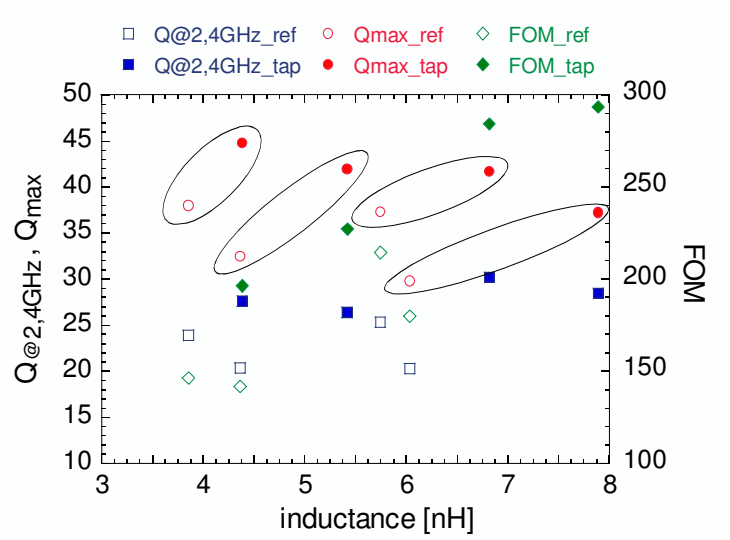

Figure 4.36 : Outlook of the performances exhibited by four couples (circled) of reference versus tapered inductors.

4. 3. 6 Suspended inductor

Figure 4.37 compares the Q-factor of a monolithic (i.e., the reference) versus a suspended inductor. Both devices have an identical layout (D_{out} = 300 µm, w = 15 µm, s = 6 µm, and n = 4) and have been fabricated on HRS with a 5 µm-thick Al spiral. The suspended inductor has been released from the substrate by the selective removal of a 4 µm-thick sacrificial layer of SiO_2, using the surface micromachining process presented in section 3.3.2.

Both the considered devices have almost identical values of series inductance and series resistance : L_s = 3.61 nH and R_s = 1.12 Ω for the reference, and L_s = 3.64 nH and R_s = 1.14 Ω for the suspended inductor. Initially, since their series resistances and inductances are the same, the curves of Q-factor are superimposed. However, at about 1.5 GHz these curves start to deviate. The suspended inductor shows a peak Q-factor of 30 at 5 GHz; while, the peak-Q of the monolithic inductor is 23.5 and occurs at a lower frequency, i.e., 4.4 GHz. The extracted values of series capacitance reveal that the suspended inductor, with C_s = 24.2 fF, suffer from a 20% lower parasitic capacitance compared to the monolithic inductor (C_s = 30.8 fF). This stems from the 4 times lower permittivity of air compared to the one of silicon dioxide. Above the corresponding peak-Q's, the curves of both inductors gradually decrease with the same slope. This is a possible indication of the fact that RF losses due to the distributed capacitance and substrate losses due to displacement currents, are substantially unaffected by the type of dielectric separating the spiral from the underpass. This is also witnessed by the values of the term R_d, which differ of less than 8%, having $R_{d\text{-}reference}$ = 106 Ω and $R_{d\text{-}suspended}$ = 98 Ω. Since the dielectric thickness, being it air or SiO_2, is very thin compared to the inductor footprint, the electric field lines leaving the spiral couple to the substrate in the same way regardless of the type of dielectric. Therefore, such an air-gap of 4 µm is not sufficient for overcoming substrate losses.

Figure 4.38 gives a general overview of the performances exhibited by pairs of monolithic versus suspended inductors. In all cases, the latter exhibit considerably higher peak-Q's and lower parasitic capacitance, thereby demonstrating the attractiveness of the proposed suspended inductors. The achievable performance could be further improved by providing a thicker air-gap. Particularly, this should be the case if these suspended inductors were to be implemented on top of doped Si wafers.

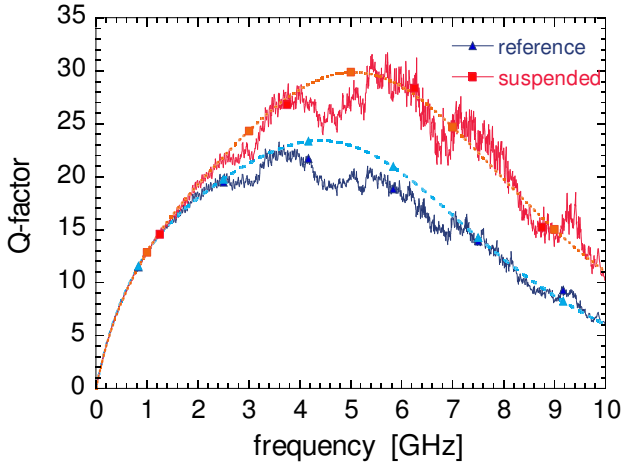

Figure 4.37 : Comparison of the Q-factor shown by a monolithic and a suspended inductor, respectively. Both inductors are implemented on high-resistivity Si and are fabricated with a 5 µm-thick Al spiral.

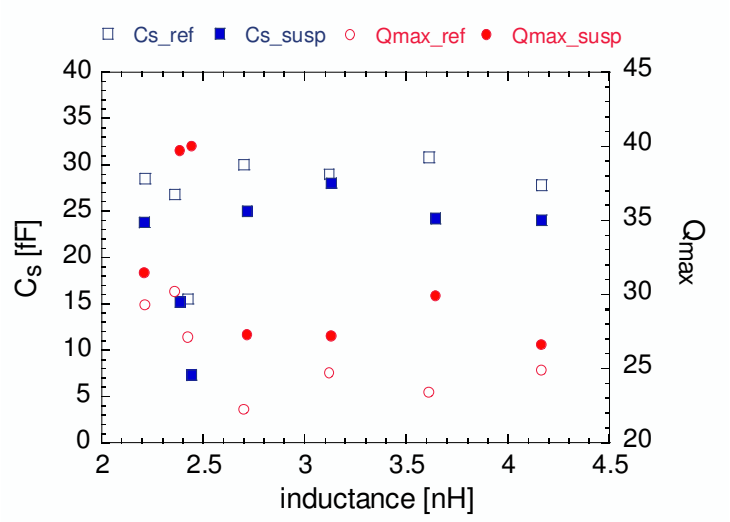

Figure 4.38 : Outlook of C_s and Q_{max} for monolithic versus suspended inductors.

4. 4 Performance outlook

A comprehensive performance outlook is presented in order to summarize this empirical study of planar spiral inductors. Data reported in this paragraph refer to 3 µm-thick Al inductors fabricated on Pyrex. In fact, this is the version of fabricated inductors which has been the most extensively characterized. These inductors have an outer diameter, D_{out} ranging from 400 to 600 µm and a number of turns, n comprised between 2 and 7. Moreover, they share some common layout parameters, i.e., w = 20 µm and s = 6 µm.

Contour plots are used in order to visualize the effects of n and D_{out} on the inductor performance. Figure 4.39 displays the contour plot of series inductance, L_s, while Figure 4.40 and Figure 4.41 represent the contour plots of peak Q-factor and self-resonant frequency, f_{SR}, respectively. The information contained on these plots will be exploited for the establishment of a set of layout parameters enabling the design of devices tailored for a given inductance value. As a further step, such optimized inductors will be used for implementing more complex RF circuits, such as lumped-element baluns (see Chapter 6).

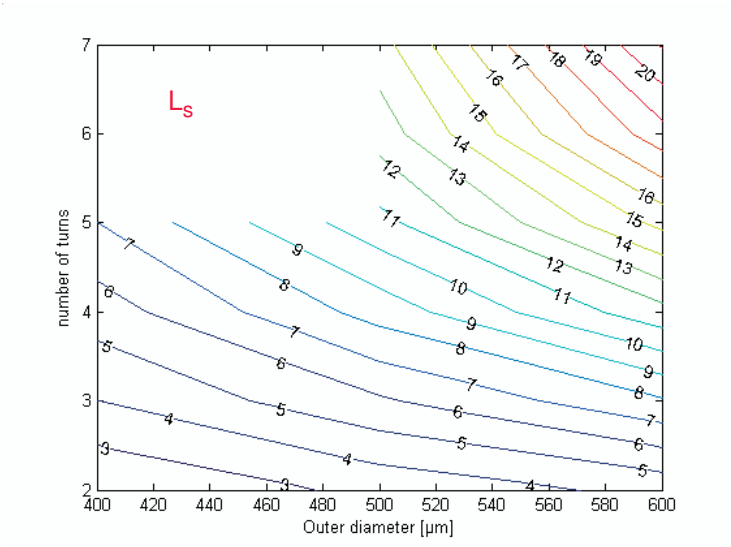

Figure 4.39 : Contour values of L_s as a function of n and D_{out}.

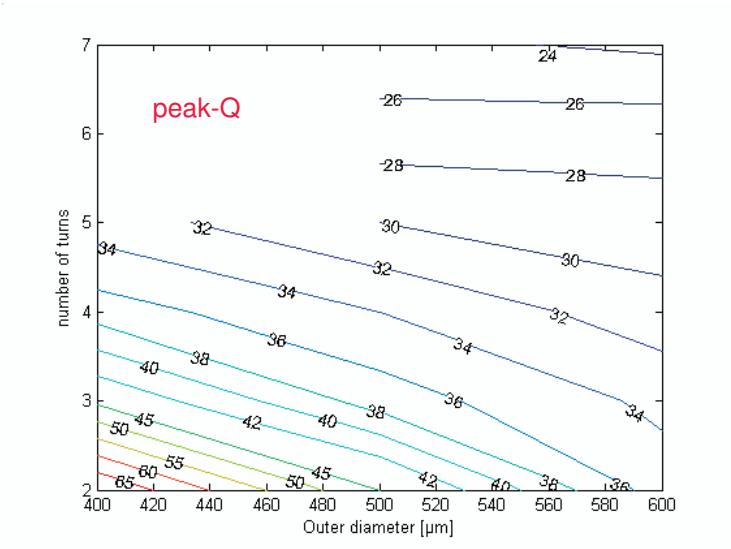

Figure 4.40 : Contour values of peak-Q as a function of n and D_{out}.

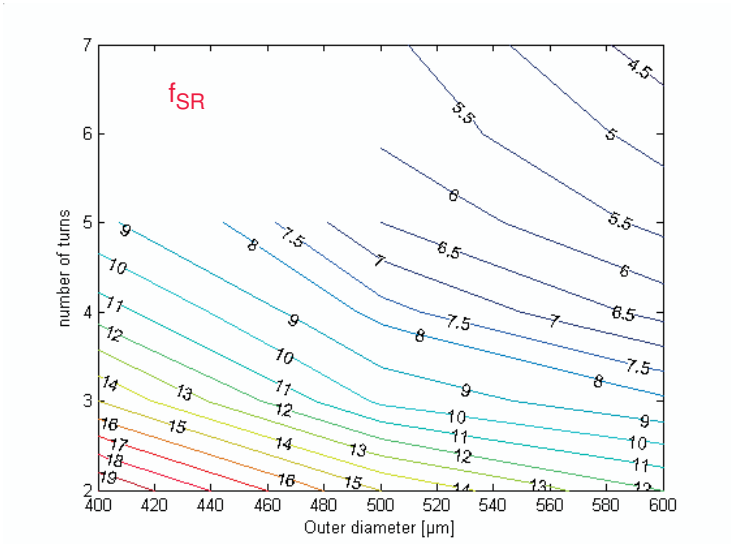

Figure 4.41 : Contour values of f_{SR} as a function of n and D_{out}.

4. 5 Design rules

Based on the characterization of the performances of spiral inductors as a function of the various layout parameters, the following general guidelines have been established in order to provide a help to the conception of optimized inductors operating at multi-GHz range.

- A spiral inductor should not be filled with turns up to its centre. Due to the generation of eddy currents at high frequency, the innermost turns of the spiral suffer from an enormous increase in resistance, while their contribution to the total inductance value is minimal. Eddy currents in a spiral inductor can be mitigated by adopting a “hollow” layout.

- For especially high inductance values, the inductor footprint should be kept minimum, in order to ensure that the self-resonant frequency is sufficiently higher than the operating frequency of the inductor. An inductor with a tapered layout represents an attractive solution for combining small size and large inductance per unit area.

- A spiral inductor approaching a circular shape is characterized by a larger conductor length per unit area. This in turn results in an increased inductance per unit area.

- The use of minimum spacing between adjacent tracks of an inductor allows for a tighter magnetic coupling. This in turn results in a significant increase of inductance. The concomitant increase of parasitic inter-turn capacitance due to fringing fields has been demonstrated to be of minor concern on the overall inductor performance.

- The width of the tracks of a multiturn spiral inductor should be limited. As a consequence of the skin and proximity effect, the center of a wide conductor is not used by the current flow. Therefore, excessively wide conductors are not efficient. Moreover, it has been pointed out that conductors with larger track-width generate less inductance per unit length. Very large track-widths should be used only for implementing inductors with 1 or 2 turns.

- The underpass should be neither too narrow, in order to keep the series resistance low, nor too wide, for limiting the parasitic coupling to the coil. An underpass width comparable to the track-width seems to be appropriate.

4. 6 References

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CHAPTER 5

EM SIMULATION OF INDUCTORS

THE GOAL of this chapter is to develop the necessary knowledge enabling to get fast and accurate matching of measured data of spiral inductors using electromagnetic simulations. The establishment of optimum simulation conditions will set up the basis for an efficient simulation of more complex and memory-demanding circuits, such as lumped-element baluns (see Chapter 6).

EM simulations presented in this work have been performed using Sonnet[1]. This software is based on an electromagnetic analysis engine called *em*. *Em* uses a modified method of moments analysis based on Maxwell's equations to perform a complete three-dimensional current analysis of arbitrary planar geometries, that includes both 3-D fields and 3-D currents. This is in contrast to 2.5-D analyses, which, while including full 3-D fields, allow only 2-D currents. Thus, a 2.5-D analysis does not allow via or any other vertical current. *Em* is a "full-wave" analysis engine, which means that it takes into account all possible coupling mechanisms. The analysis includes dispersion, stray coupling, discontinuities, surface waves, metallization loss, dielectric loss and radiation loss.

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1. Sonnet Software, Inc., 100 Elwood Davis Road, North Syracuse, NY 13212, USA. Website: http://www.sonnetsoftware.com

Em uses a surface meshing technique, i.e., only the surface of the circuit metallization is meshed. This is especially well-suited for the analysis of predominantly planar circuits, resulting in a much faster computation time compared to volume meshing techniques, such as those used for example in Ansoft's HFSS.

5. 1 Edition of a Sonnet project

The circuit to be analyzed is commonly referred to as the device under test, or DUT. The DUT is enclosed in a box, as shown in Figure 5.1.a, whose walls are assumed to be perfect electrical conductors (PEC), thereby imposing a boundary condition to the electric and magnetic fields. The box should be sufficiently large so as to prevent a capacitive coupling between the DUT and the conductive walls.

The DUT is connected to the box by one or more ports. The ports may be located either on box walls, or inside the box. Typically, when the ports are located on the box walls, fictive transmission lines are used for connecting the DUT to the ports, as shown in Figure 5.1.b. These transmission lines can be implemented as strips of lossless metal and they can also serve for providing a path to the ground. Since these transmission lines do not belong to the real DUT, their own admittance is successively eliminated from the simulated data by a de-embedding procedure. To do this, a reference plane is usually defined as the distance separating the port from the DUT, as illustrated in Figure 5.1.b by the arrow leaving the port on the left-side of the box.

Inside the box, the different levels of materials making up the real circuit, such as the substrate, dielectric layers, conductors and interconnects between different metallization levels, are defined and the corresponding material properties and thickness are specified. The substrate extends down to the ground plane represented by the bottom side of the box. Above the DUT a layer of air few millimeters thick extends up to the top side of the box providing the necessary electrical insulation.

The analysis starts by subdividing the circuit metallization into subsections, that are made up of cells. The cell is the building block used in the project editor and its size is specified by the user. In order for the results to be accurate, the cell dimension must be smaller than 1/20 of a wavelength.

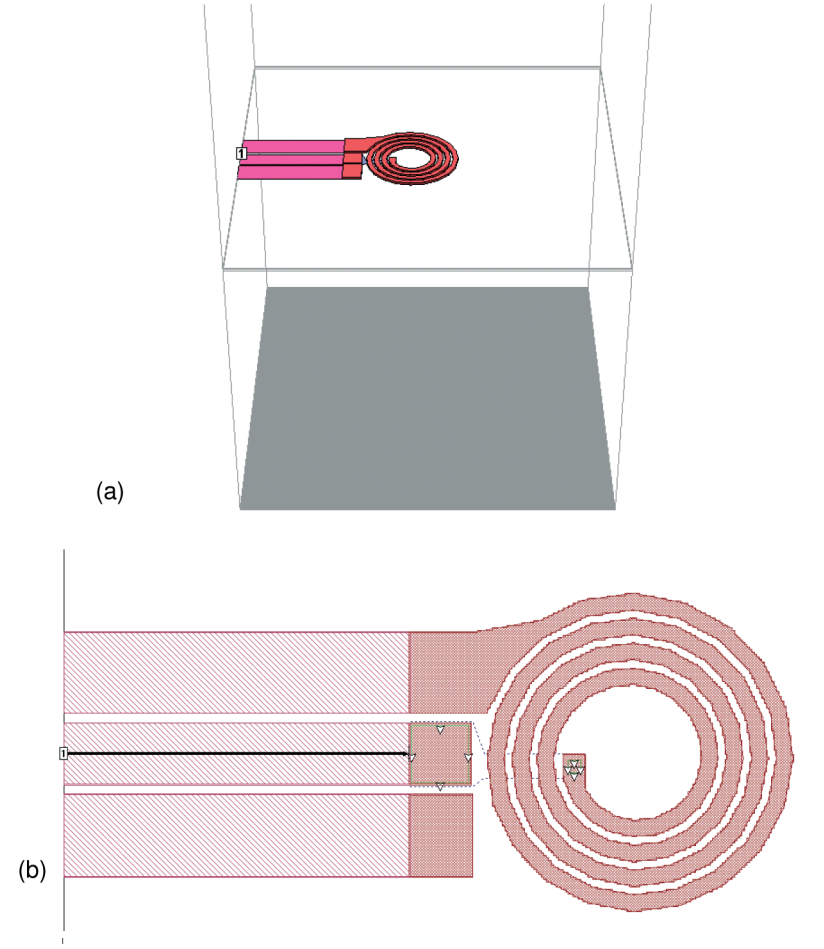

Figure 5.1 : The DUT is surrounded by a box, whose walls are defined as a perfect electrical conductors (PEC) (a). The corresponding 2-D layout shows the box-wall port on the left, transmission lines connecting the DUT to the port and to the box-wall for grounding, and the reference plane, indicated by the arrow, for which the de-embedding is carried out (b).

The order of magnitude of the "safe" wavelength can be estimated by taking the highest value of dielectric constant in the structure and the highest frequency at which the analysis is performed. The use of cells larger than 1/20 of λ usually

results in unacceptable errors due to incorrect modeling of the distributed effects across the cell. Assuming a dielectric permittivity of 12 and an upper frequency of 10 GHz, the value of the "safe" wavelength is about 400 μm. This value is about two orders of magnitude larger than the cell sizes typically used for simulating RF inductors.

The *em* engine calculates the tangential electric field generated on all the subsections, for a given current in a single subsection, then repeats the calculation for every subsection in the circuit, one at a time. In doing so, *em* effectively calculates the coupling between each possible pair of subsections in the circuit. Since one or more cells are automatically combined together to create subsections, the number of subsections is usually considerable smaller than the number of cells. This is an important aspect because the analysis solves an N x N matrix, where N is the number of subsections. Consequently, a small reduction in the value of N results in a large reduction of analysis time and memory. *Em* automatically places small subsections in critical areas where current density varies rapidly, but allows larger subsections in less critical areas, where current density is smooth or changing slowly.

Conformal mesh is a special case of subsectioning used to model polygons with long diagonal or curved edges. This technique groups together strings of cells following diagonal and curved metal contours to form long subsections along those contours. Whereas, the standard *staircase fill* results in numerous small x- and y-directed subsections, conformal mesh results in a few long conformal subsections. The main benefit of these larger sections is that they yield faster processing times with lower memory requirements.

Figure 5.2 shows an example of what the actual subsectioning technique looks like. The picture on the left hand-side is displayed using staircase fill; while, the picture on the right hand-side shows the result obtained using conformal mesh that enables a more efficient subsectioning procedure. Actually, conformal subsections have been used for meshing the coil only, while the pad not having curved edges is always meshed using standard staircase fill. The whole layout sectioned using staircase fill uses 15'538 subsections resulting in a file of 1'849 MB, that would lead to a prohibitively slow and memory-demanding analysis. On the other hand, the same DUT sectioned using conformal mesh cells generates a total amount of 1'417 subsections and a corresponding file of only 23 MB, hence requiring much less time and CPU memory.

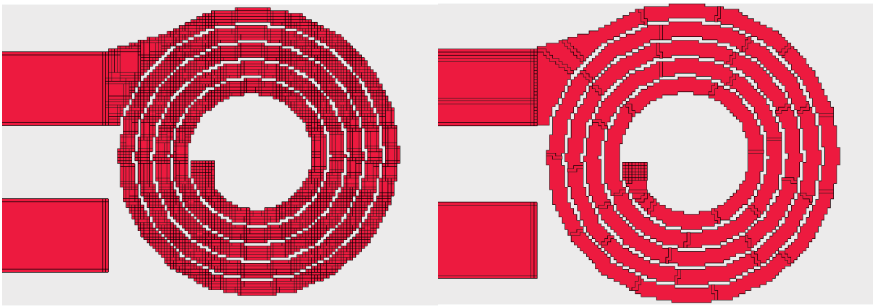

Figure 5.2 : Illustration of the subsectioning of a spiral inductor using either staircase fill (left) or conformal mesh (right).

The standard Sonnet model of metal loss uses the concept of surface impedance [1]. This concept allows planar EM simulators, such as Sonnet's *em*, to model real 3-D metal in two dimensions (zero thickness). This means that there is no difference between the top and the bottom side of the conductor. Although, this technique models the loss of the real 3-D metal fairly accurately, it does not model any change in the field distribution due to the metal thickness. This approximation is valid as long as the metal thickness is small with respect to the width of the line, the separation between lines, and the thickness of the dielectric.

One of the models provided by Sonnet for simulating the metallization is called *Normal metal* (NM). This model takes into account three parameters for simulating the metal losses, these are, the bulk conductivity, the metal thickness and the current ratio (CR). However, the metal thickness is used only in calculating loss due to skin effect, it does not change the physical thickness of the metallization in the circuit, that is still modeled as zero-thickness. The current ratio defines the ratio of the current flowing on the top surface of the conductor to the current flowing on the bottom surface. NM being a zero-thickness model, it does not take into account the sides of the conductor. Therefore, the current which flows on the sidewalls is ignored. A current ratio of unity is taken whenever it can be assumed that the current distribution is symmetrical with half of the current flowing on the top and half flowing on the bottom of the conductor.

The metal is considered to be thick when its thickness is comparable to other characteristic dimensions in the circuit, such as the conductor width or the gaps between conductors. In such cases, the use of *Thick metal* model (TM) is more

appropriate since it allows for the real modeling of the physical thickness of the conductor. When TM is used, the structure to be analyzed is appoximated by two or more infinitely thin sheets of metal. One sheet represents the top surface of the structure and a second sheet represents the bottom surface of the structure. Vias are placed automatically around the perimeter to represent the side-walls of the structure. Whenever more than two sheets are required, the interior sheets only supply a ring of current on the edge of the structure, as shown in Figure 5.3. If TM is used on conductors in extremely close proximity, the number of sheets should be increased in order to accurately model the side-to-side coupling between the conductors. Particularly, enough sheets should be used so that the spacing between sheets is less than the gap between conductors.

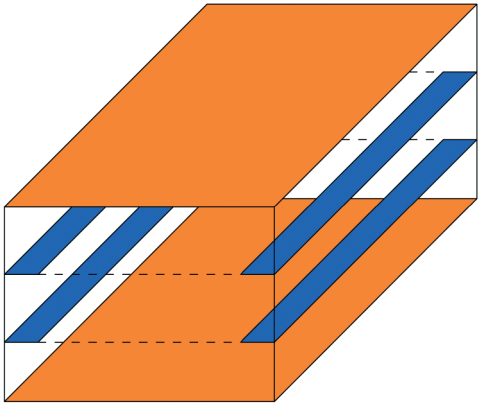

Figure 5.3 : Schematic cross section of a thick conductor modeled using TM with four sheets (NS = 4). The interior sheets are modeled only by a ring of metal located at the edge of the thick metal structure. The vias connecting sheets in different levels are not shown for clarity.

On the other hand, the total effective loss tangent of dielectric materials is calculated by *em* with the following relationship :

$$\text{Total loss tangent} = \tan\delta + \frac{\sigma_{diel}}{\omega \cdot \varepsilon_0 \cdot \varepsilon_r} \qquad (5.1)$$

where $tan\delta$ is the loss tangent of the dielectric, σ_{diel} is the dielectric conductivity, ω is the radian frequency, ε_0 is the free-space permittivity and ε_r is the relative permittivity of the dielectric. Therefore, tanδ has both a frequency-independent and a frequency-dependent term.

5. 2 Simulation results

EM simulations have been run on a Dell Precision PWS 380 workstation with a 3.2 GHz Intel® Pentium® processor and 2.0 GB of RAM. The analyzed DUTs have been imported in Sonnet in gdsII format generated from the CAD tool used to design the photolithography masks. This enables a straightforward comparison of measured data to simulations carried out on devices with identical layout.

5. 2. 1 Cell size

This paragraph addresses the role played by the cell size on the accuracy of the response and the time required for the analysis. The measured data of a 3 µm-thick Al inductor fabricated on HRS with the following layout parameters : D_{out} = 400 µm, w = 20 µm, s = 4 µm and 5 turns, have been compared to several simulated results obtained using cells with different size. Particularly, square cells ranging from 2 µm x 2 µm, up to 8 µm x 8 µm have been employed in different simulation runs. Since the considered inductor has an interturn spacing of 4 µm and a track width of 20 µm, the former is considered as the critical dimension of the DUT. All the simulations have been carried out using the same set of material properties and TM model with NS = 2. The values of resistivity and loss tangent of the HRS substrate taken for the simulation are ρ = 3.5 kΩ·cm and tanδ = 6.5%, respectively. Simulated data have been obtained with an adaptive band synthesis (ABS) frequency sweep. Typically, this type of analysis first calculates the exact solution at 5 to 10 discrete frequency points and successively returns several hundreds of values calculated at different frequencies by interpolation algorithms.

In general, the simulated curves of Q-factor displayed in Figure 5.4 are in good agreement with both the measured Q up to 1.5 GHz and with the self-resonance frequency, regardless of the cell size. This indicates that the simulation has predicted correctly the low-frequency increase of the metal resistance, which sets up the slope of the Q-factor curve, as well as the total parasitic capacitance, that defines the self-resonance. Nonetheless, the peak-Q values of the simulated curves

exhibit up to 10% difference depending on the chosen cell size. Another aspect that has to be mentioned is represented by the inaccurate matching provided by simulations above 8 GHz. This problem is common to all simulated results regardless of the cell size employed. For this reason, it could be related to a high-frequency dissipation mechanism (e.g., dielectric losses, surface parasitic conduction channel), which affects the real inductor, but that is not taken into account by EM simulation. However, further knowledge is needed in order to ascertain the origin of this discrepancy between measurement and simulation.

By looking at the curves of $\mathrm{Im}(Z)/\omega$ displayed in Figure 5.5 it is obvious that simulated results obtained with largest cell sizes (i.e., 7 µm x 7 µm and 8 µm x 8 µm) fail to match the measured behavior and yield unacceptable results. This is because these cells are much larger than the critical dimension of the circuit discussed earlier. On the contrary, convergence has been obtained for those simulations carried out with cell size of 6 µm by 6 µm and smaller. In fact, all the simulated curves have provided an accurate fit of measured data.

The trend reported in Figure 5.6 highlights the great difference in the calculation time as a function of the cell size. For example, the simulation performed using cell size of 6 µm x 6 µm (generating less than 1'000 subsections) has required about 1 min/freq, whereas the simulation carried out with smallest cells, i.e., 2 µm x 2 µm (generating about 3'000 subsections), has been more time-consuming, requiring 30 min/freq.

In summary, despite the analysis performed with largest cells allows for very fast calculations, typically few minutes per frequency, the poor accuracy obtained should discourage from using cells that are too large compared to the critical dimension of the circuit. On the other hand, when analyzing more complicated circuits, the choice of a too small cell size, may lead to prohibitively slow and memory-demanding analysis. Therefore, in such cases it is of primary importance to first identify the most critical dimension of the circuit and then set the cell size as close as possible to that critical dimension.

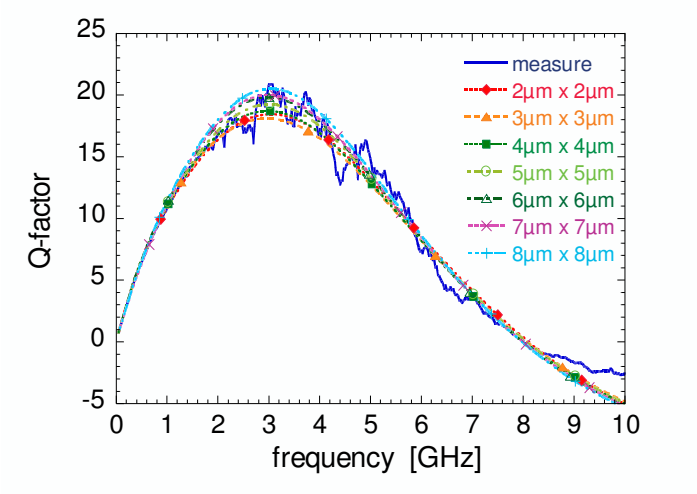

Figure 5.4 : Measured data of Q-factor (full lines) compared to simulations (dashed lines) carried out as a function of the cell size.

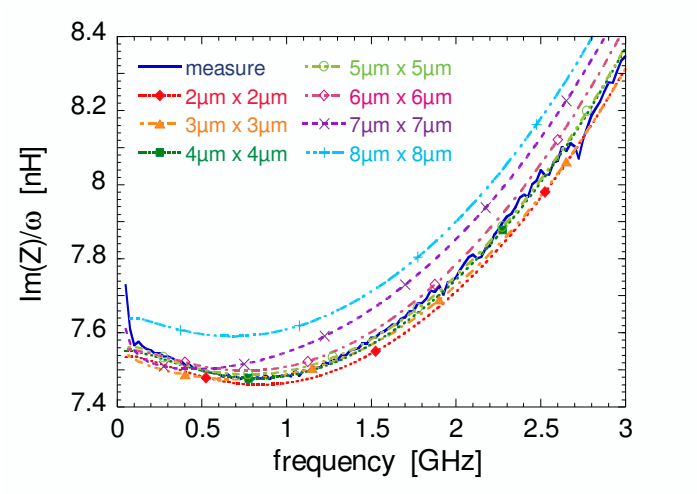

Figure 5.5 : Measured data of $\mathrm{Im}(Z)/\omega$ (full lines) compared to simulations (dashed lines) carried out as a function of the cell size.

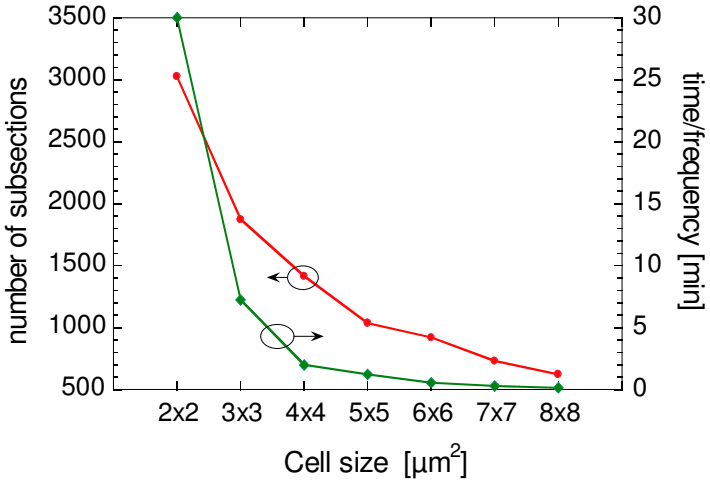

Figure 5.6 : Number of subsections and time required for the analysis of one frequency, as a function of the cell size used for simulating the DUT.

Figure 5.7 shows what the current distribution in a spiral inductor as a function of frequency looks like. These plots of current density in A/m are calculated at four discrete frequencies (i.e., 0.6, 3.0, 6.0 and 9.0 GHz) with a linear frequency sweep going from 0.6 to 9.0 GHz in steps of 0.6 GHz. Unlike the principle of ABS frequency sweep previously discussed, a linear sweep enables *em* to calculate the exact response at those frequencies specified by the user.

Already at 0.6 GHz the current density is no longer uniform across the spiral due to the proximity effect. The highest values of current density are found at the inner edges of the innermost turns. This effect becomes more pronounced as the frequency increases because the difference of current density between the inner and outer edges of the same turn becomes increasingly more important. By comparing the plots corresponding to 3.0, 6.0 and 9.0 GHz, it can be seen that the section effectively carrying the current flow becomes more and more reduced to a thin sheet near the conductor edge. Thus, the largest part of the conductor width sustains a small amount of current. This further emphasizes that at high-frequency, the inner turns of a spiral inductor are responsible in a large extent for the increase of total series resistance.

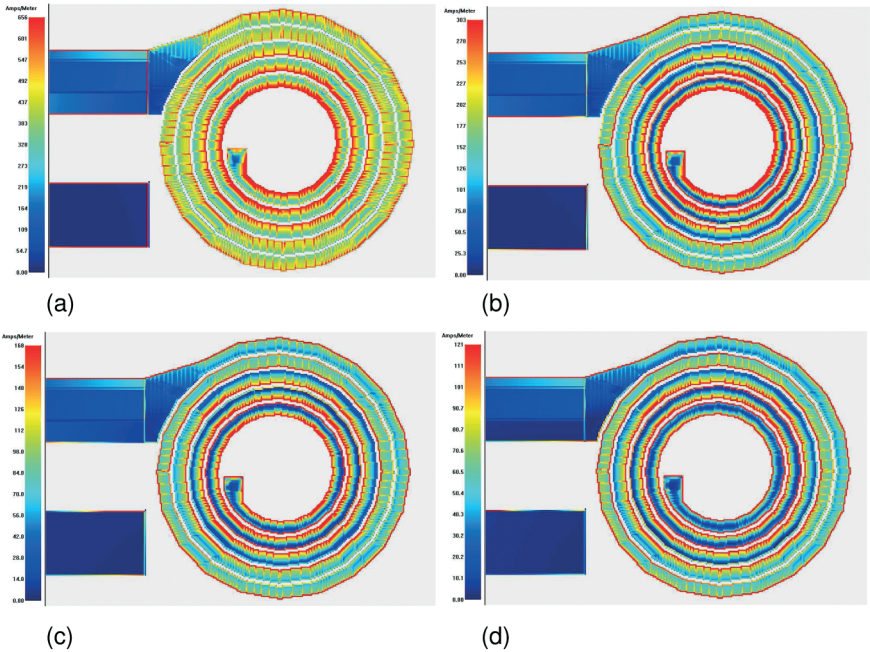

Figure 5.7 : Plots of current density in A/m, as a function of frequency : 0.6 GHz (a), 3.0 GHz (b), 6.0 GHz (c) and 9.0 GHz (d).

It is easy to imagine that this effect becomes even more severe when the spiral is filled with turns up to its centre. Therefore, this confirms that a spiral inductor with a hollow centre should be preferred to a spiral that is completely filled with turns.

5. 2. 2 Metal modeling

This paragraph characterizes the accuracy obtained using NM or TM for modeling the performance of a 8 µm-thick Al spiral inductor on Pyrex substrate. The values of resistivity and loss tangent of Pyrex taken for the simulation are $\rho = 1.25 \cdot 10^9$ Ω·cm and $\tan\delta = 4\%$, respectively. The layout parameters of the considered inductor are : D_{out} = 450 µm, w = 20 µm, s = 8 µm and 4 turns. The accuracy obtained with TM model has been further investigated by running several

simulations with a different number of sheets. The underpass of the inductor, due to its much smaller thickness compared to the skin depth of Al up to 10 GHz, is simulated using NM. All simulations have been performed using Conformal mesh and a cell-size of 4 µm x 4 µm. Such cell size has been chosen since it is the highest common factor of the track-width and inter-turn spacing.

Figure 5.8 and Figure 5.9 display measured and simulated data of Q-factor and Im(Z)/ω. The comparison of the simulated Q-factor curves points out that the use of NM for modeling such thick conductors completely fails to describe the reality. In fact, neither the simulated low-frequency Q-factor, nor the self-resonance show a reasonable agreement to measured data. This considerable discrepancy is also confirmed by looking at the low frequency curves of Im(Z)/ω. Here, simulated data obtained with NM model considerably overestimate the measured curve.

Unlike NM, the use of TM provides a much better accuracy. Particularly, as the number of sheets exceeds three, a rapid convergence of the simulated curves is obtained. This in turn provides a progressive improvement of the matching of low-frequency Q-factor, peak-Q and self-resonance. However, even the curve simulated with NS = 6 clearly overestimates the value of low frequency Im(Z)/ω. This important discrepancy of about 7% cannot be imputed to the intrinsic error of the simulation only. Possible other reasons that could be blamed are a lack of accuracy in the calibration procedure prior to RF characterization, or an interturn spacing on the real device larger than expected (i.e., $s > 8$ µm), that consequently lowers the mutual inductance between spiral tracks.

Figure 5.10 represents the number of subsections and calculation time required for the analysis of one frequency as a function of the type of model adopted. The number of subsections increases linearly with the number of sheets used in the TM model, while the calculation time per frequency follows a quadratic behavior. For example, the DUT simulated with NS = 2 (generating about 4'000 subsections) has required 3 min/freq, while the simulation run with NS = 6 (generating approximately 11'500 subsections) has required almost 35 min/freq. However, since the accuracy of the results is gradually improved by increasing the number of sheets, the present case suggests that the optimum compromise between calculation time and accuracy would be best met by choosing TM with NS = 4. The analysis run under these conditions generates less than 8'000 subsections and requires about 13 min/freq.

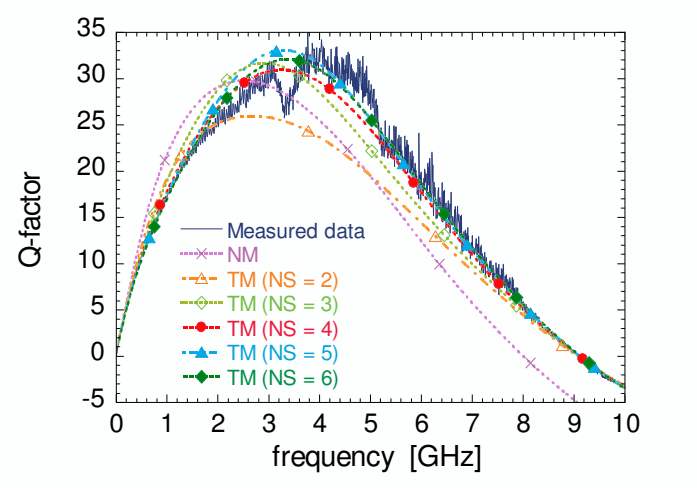

Figure 5.8 : Measured data (full line) of Q-factor compared to simulations (dashed lines) carried out as a function of the type of model used to simulate the spiral : Thick Metal versus Normal Metal.

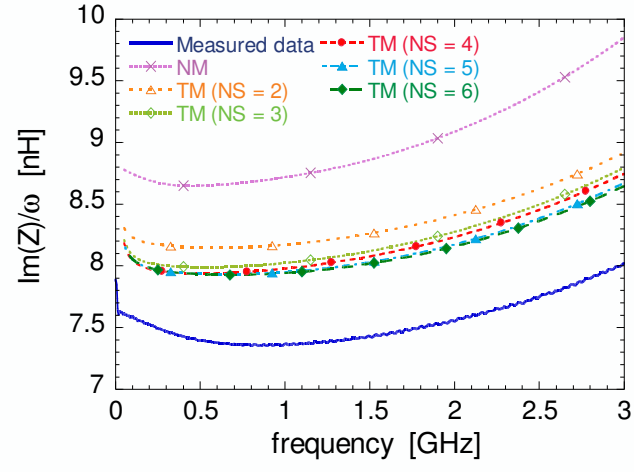

Figure 5.9 : Measured data (full line) of Im(Z)/ω compared to simulations (dashed lines) carried out as a function of the type of model used to simulate the spiral metallization : Thick Metal versus Normal Metal.

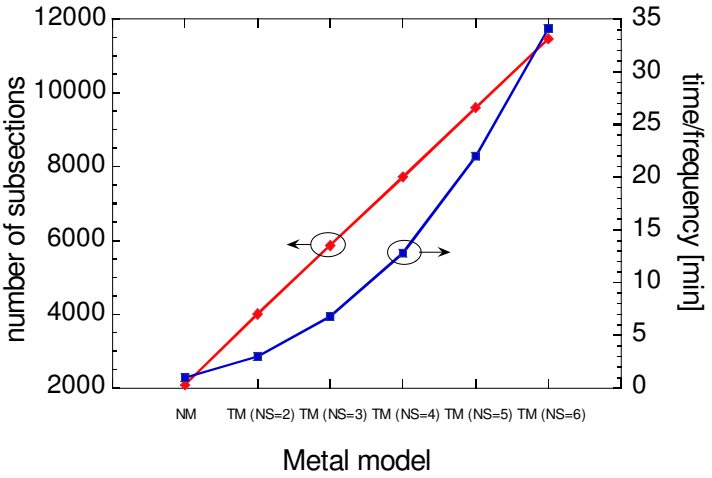

Figure 5.10 : Number of subsections and time required for the analysis of one frequency, as a function of the model used for simulating the spiral metallization.

5. 2. 3 Accuracy verification

The accuracy achievable by EM simulation has been further evaluated by comparing measured to simulated data of some inductors characterized by very different layout parameters, inductance, spiral thickness and implemented either on HRS or Pyrex. The material and layout parameters describing each of the considered devices are listed in Table 5.1. All inductors have been simulated using TM model. Particularly, the 3 µm-thick inductor on HRS (*Inductor 1*) has been simulated with NS = 2 and a cell size of 6 µm x 6 µm. The other two inductors having a 8 µm-thick spiral have been modeled using NS = 4. For simulating the tapered inductor (*Inductor 2*) a cell size of 3 µm x 3 µm has been employed, while for the square inductor (*Inductor 3*) the adopted cell size is 4 µm x 4 µm.

Figure 5.11 compares measured versus simulated Q-factor curves. In general, the simulated curves of the three considered inductors exhibit a good agreement with the corresponding measured data.

The curves of Im(Z)/ω are shown in Figure 5.12. Measured data of *Inductor 1* and *2* are very-well matched with simulations as witnessed by small discrepancies in the order of 1-1.5%. This is different for *Inductor 3*, where simulated data

overestimate the measure by about 6%. However, since *Inductor 2* and *3* belong to the same wafer, this more significant discrepancy can probably be attributed to a process variation decreasing the inductance value of *Inductor 3* (e.g., an inter-turn spacing, *s* larger than 8 µm), rather than to the lack of accuracy of the EM analysis.

TABLE 5.1 : MATERIAL AND LAYOUT PARAMETERS OF THE CONSIDERED INDUCTORS.

Device	Substrate	Spiral thickness [µm]	D_{out} [µm]	*w* [µm]	*s* [µm]	*n*
Inductor 1	HRS	3	500 (circular spiral)	20	6	3
Inductor 2	Pyrex	8	350 (circular and tapered spiral)	20 [a]	6	5
Inductor 3	Pyrex	8	640 [b] (square spiral)	20	8	5

a. The track-width of the outer turn is 20 µm, then the inner turns have been progressively narrowed in steps of 2 µm.
b. This value refers to the diagonal of the square spiral.

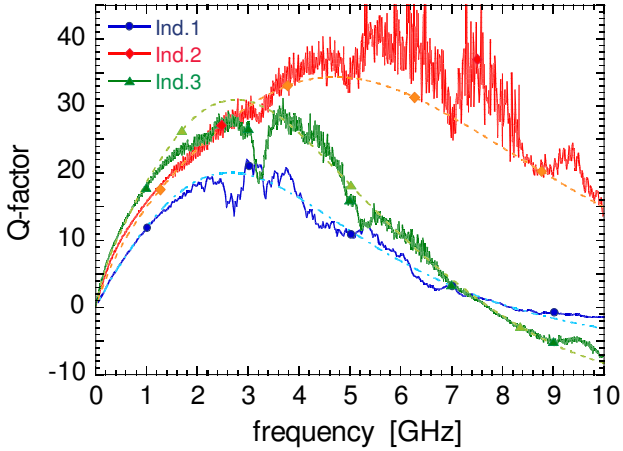

Figure 5.11 : Measured (full lines) versus simulated Q-factor (dashed lines) of three inductors with different layout and material parameters (see Table 5.1).

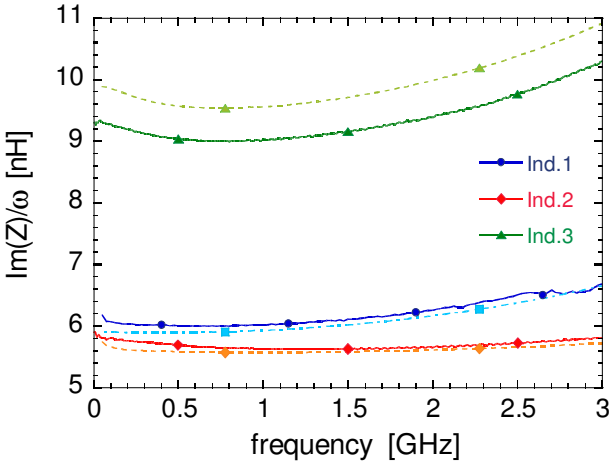

Figure 5.12 : Measured (full lines) versus simulated curves (dashed lines) of Im(Z)/ω for three different inductors.

5. 3 Spiral thickness effect

The goal of this paragraph is to evaluate through EM simulations the role played by the spiral thickness on the parasitic capacitance and series inductance of a spiral inductor. An inductor, supposed on Pyrex substrate, with the following layout parameters : D_{out} = 400 µm, w = 20 µm, s = 4 µm and 5 turns, has been considered. In total, five EM analysis have been run as a function of spiral thickness ranging from 1 up to 8 µm. TM model and a cell size of 4 µm x 4 µm have been used for all simulations. The number of sheets has been varied depending on the metal thickness. The default number of NS = 2 has been adopted form modeling the 1, 2 and 4 µm-thick spirals; whereas, NS = 3 and NS = 4 have been used for simulating the 6 and 8 µm-thick spirals, respectively, so as to maintain a constant ratio of thickness/NS.

Figure 5.13 shows that increasing the spiral thickness from 1 up to 8 µm progressively improves both the low-frequency Q-factor and the peak-Q. The most significant improvements are observed when the spiral thickness is increased from

1 to 2 µm and from 2 to 4 µm. Further thickening the spiral up to 8 µm still leads to an appreciable, though less marked, improvement of Q due to the saturation of the effective metal thickness, as shown by calculation in paragraph 2.1.1.

Above the peak-Q, the curves gradually merge together resulting in an almost identical self-resonant frequency located close to 10 GHz. This indicates that the contribution of the fringing fields between adjacent conductors to the total parasitic capacitance remains substantially unchanged even after a 8-fold increase of the spiral thickness. This confirms what has been argued in paragraph 4.3.3, i.e., that the capacitive coupling occurs mostly through the substrate and the dielectric layer of SiO_2 beneath the spiral, rather than through the air separating adjacent tracks of the inductor.

On the other hand, the curves of Im(Z)/ω displayed in Figure 5.14, point out that an increase of the metal thickness, ultimately results in a lower value of series inductance as it has already been observed and discussed in paragraph 4.3.3.

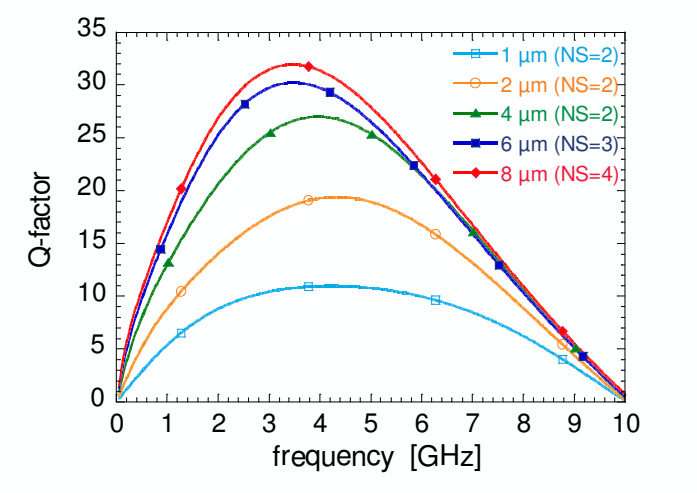

Figure 5.13 : Simulated curves of Q-factor as a function of the spiral thickness.

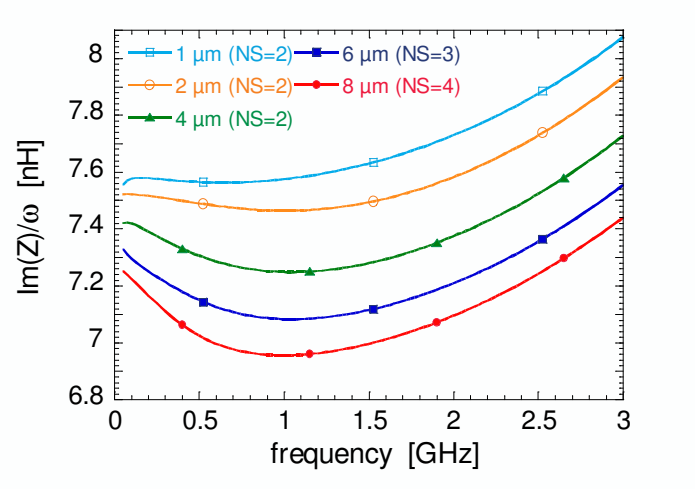

Figure 5.14 : Simulated curves of Im(Z)/ω as a function of the spiral thickness.

5. 4 Discussion

A good trade-off between accuracy and analysis time is represented by the choice of a cell size comparable to the critical dimension of the circuit. Typically, in the case of a spiral inductor, the critical dimension is represented by the inter-turn spacing, *s*. Whenever *s* is not a divisor of the track-width, *w*, the cell size should be chosen as the closest common factor of both *s* and a divisor of *w*. For example, considering a spiral inductor having $w = 12$ µm and $s = 7$ µm, in this case the most appropriate cell size would be 4 µm x 4 µm.

It has been demonstrated that the accuracy achieved when modeling thick conductors using TM model is very sensitive to the number of sheets used. Therefore, it is recommended to use a number of sheets exceeding the default value of two, at the expense of a longer analysis time.

The values of tanδ attributed to the dielectric layers (i.e., substrate and SiO_2), while not affecting the self-resonant frequency, have been observed to strongly influence the slope of the Q-factor curve beyond the peak-Q. Particularly, tanδ values close to 0% lead to very steep slopes, whereas increasing tanδ reduces the

slope and hence also the Q-factor at high frequency. In order to provide an accurate match of the measured Q-factor both at peak-Q and around the self-resonance, a relatively high value of tanδ has to be attributed to both HRS (tanδ = 6.5%) and Pyrex (tanδ = 4%) substrates. However, such values can hardly be imputed only to the dipole losses of the material. In fact, the reported values of tanδ for different dielectric materials rarely exceed 1% even in the GHz-range [2, 3]. Since by using HRS and Pyrex the bulk losses are considerably reduced, compared to doped Si, another dissipation mechanism has to be identified. Several studies focusing on HRS for high-frequency applications have pointed out that this type of substrate is prone to the formation of surface parasitic conduction channels [4-7]. When other dissipation mechanisms are eliminated this conduction phenomenon becomes noticeable. Particularly, it is reported that these surface channels build-up at the Si/SiO_2 interface as a result of either oxide contamination, interface states, or electrical biasing between a metal structure located above the oxide and the silicon [8]. Charges within the oxide attract free carriers near the substrate surface, thereby reducing the effective resistivity and increasing substrate losses. A similar parasitic phenomenon of surface conduction can be imagined for Pyrex too, because its bulk contains dopant species such as potassium and sodium ions.

From a more general point of view, EM simulation can be used to estimate the strength of parasitic phenomena, such as stray capacitances, inductances of transmission lines, or electromagnetic coupling between different elements in a circuit. This allows for a procedure of circuit optimization without recurring to several iterations of fabrication and measurement. However, the task of layout optimization through EM simulation is beyond the scope of the thesis.

5. 5 References

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CHAPTER 6

LUMPED-ELEMENT BALUNS

BALUNS have found a widespread use in wireless systems employing differential circuits [1, 2]. Particularly, they play a key role in double-balanced mixers [3-6], power amplifiers [7, 8], antennas and phase shifters. Basically, baluns provide conversion from an *unbalanced* or single-ended input to a *balanced* or differential output, or vice versa. Balanced outputs require that the input signal amplitude is equally splitted in half at the two output terminals altogether with a phase difference of 180° [9]. In general, the unbalanced input port and balanced output port impedances are different. Thus, baluns also need to transform impedance between input and output ports.

Since active baluns generally consume large DC power, passive baluns are preferred for low-power wireless applications. Passive balun architectures include the 180° hybrid-type [10, 11], the Marchand-type [3, 12] and the lumped-element filter-type. Traditionally, 180° hybrids or ring resonators are impractical for monolithic integration due to their large size. Marchand-type baluns implemented with quarter-wavelength coupled microstrip lines allows for integrated solutions. However, for wireless applications in the low GHz-range, the footprint of these distributed couplers becomes excessively large causing a significant waste of chip area. This issue can be addressed by adopting more compact topologies

represented by transformer-type circuits based on coupled nested spiral inductors [12-15], or by layouts based on discrete inductors and capacitors [16-19].

This chapter deals specifically with the latter class of baluns. The presented work involves design, simulation and characterization of lumped-element filter-type baluns obtained by co-integrating optimized inductors with metal-insulator-metal (MIM) capacitors so as to form low-pass and high-pass filter sections [20]. In general, MIM capacitors are preferred for implementing passive circuits since they achieve higher capacitance density per unit area compared to interdigital capacitors [21].

6. 1 State-of-the-art of lumped-element baluns

Baluns in RF circuits are often present as off-chip elements implemented using low-temperature cofired ceramic (LTCC) technology [21]. In fact, LTCC baluns exhibit superior performances compared to their integrated counterparts. Typical performances of commercial products, targeting the 2400-2500 MHz-band, are a minimum return loss of -12 dB at the unbalanced port, an insertion loss better than -0.9 dB, an amplitude and phase imbalance less than 0.45 dB and 0.2°, respectively [22].

Table 6.1 gives an overview of the state-of-the art performances exhibited by micromachined lumped-element baluns, such as those investigated in this work. Kim *et al.* [23] proposed a wideband balun for 5-GHz LAN applications fabricated on Si substrate with a 25 µm-thick SiO_2 layer for isolation, BCB low-K dielectric and 10 µm-thick electroplated Cu metallization. An insertion loss of 0.5-0.8 dB was reported altogether with an amplitude and phase imbalance of less than 0.3 dB and 2°, respectively, in the 5.2-5.8 GHz-band. The same technology was used by Jeong *et al.* [24] for fabricating a balun operating at 2450 MHz. An insertion loss of 0.5 dB, an amplitude imbalance of less than 0.3 dB and a phase imbalance of 3° were demonstrated. Chiou *et al.* [25] proposed a compensated high-pass/low-pass filter-type balun for implementing a double-balanced mixer. The measured insertion loss of both high-pass and low-pass sections was 4.4 ± 1.0 dB from 2.25 to 5.7 GHz, while the input return loss was -10 dB and the phase error was ± 5° across the band. Lin *et al.* [26] reported the development of a passive balun using spiral inductors and interdigital capacitors for a 2.4 GHz single-balanced diode mixer on Al_2O_3 substrates. The measured insertion loss was -4.7 dB, while the amplitude and phase difference were 0.4 dB and 3°, respectively, within the 1.9-

2.8 GHz-band. However, compared to the previous cases, the use of interdigital capacitors increases considerably the balun footprint. Recently, Kuylenstierna and Linnér [27] demonstrated a compact (620 x 650 μm^2) wide-band second order lattice balun implemented on GaAs. Over 90% bandwidth (1.5-3.5 GHz), a reflection loss better than -20 dB, and an insertion loss better than 1.0 dB, with a minimum of less than 0.6 dB at 2.5 GHz, were demonstrated. The amplitude and phase errors were less than 1.3 dB and 4°, respectively.

TABLE 6.1 : STATE-OF-THE-ART OF MICROMACHINED LUMPED-ELEMENT BALUNS.

Authors/year/ affiliation/ reference	Technology/ Substrate/ balun size [mm^2]	Operating frequency band [GHz]	Return loss [dB]	Insertion loss [dB]	Amplitude imbalance [dB]	Phase imbalance [°]
Kim et al., 2002, KAIST, Korea [23]	25 µm SiO_2 on silicon substrate, BCB interlayer, Cu electroplating (10 µm). Size : 1.5 x 1	5.2 - 5.8	NA[i]	- (0.5-0.8)	< -0.3	180 ± 2
Jeong et al., 2003, KAIST, Korea [24]	25 µm SiO_2 on silicon substrate, BCB interlayer, Cu electroplating (10 µm). Size : 1.85 x 1.2	2.4 - 2.5	-17 @ 2.45 GHz	-0.5	< -0.3	180 ± 3
Chiou et al., 1997, National Taiwan Uni, Taiwan [25]	Silicon substrate. Size : 1.5 x 2.7	2.25 - 5.7	< -10	-4.4[ii]	NA	180 ± 5
Lin et al., 2000, National Central Uni, Taiwan [26]	Al_2O_3 substrate. Size : 5.1 x 5.4	1.9 - 2.8	NA	-4.7[ii]	-0.4	180 ± 3
Kuylenstierna et al., 2005, Chalmers Uni of Technology, Göteborg [27]	GaAs substrate. Size : 0.62 x 0.65	1.5-3.5	< -20	-1.0 -0.6 @ 2.5 GHz	< -1.3	180 ± 4

i. NA : data not available.
ii. These values do not take into account the -3dB due to power splitting.

6. 2 Mixed-mode S-parameters

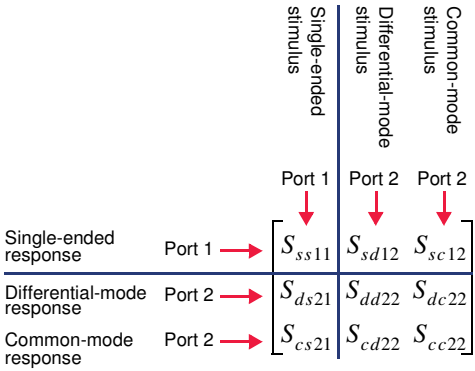
S-parameters are widely used for characterizing the linear response of high-frequency networks. The same advantages S-parameters have for two-port networks hold true for multiport and balanced network with few additions. For a two-port network the transmission parameters S_{12} and S_{21} are a measure of the complex insertion loss or gain through the device. The reflection parameters S_{11} and S_{22} describe the input and output mismatch loss, respectively. The S-parameter matrix of a multiport network must be expanded to n^2 elements, where n is the number of network ports.

The single-ended S-parameter matrix defined by (6.1) is difficult to interpret for circuits with balanced ports. Therefore, the S-parameter definition needs to be expanded to independently consider each mode in which a balanced device operates.

$$S_{std} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{6.1}$$

A generic three-port device with a balanced port can be described by wave quantities and S-parameters that refer to single-ended modes, as well as by parameters referring to differential and common modes. In 1995, Bockelman and Eisenstadt [28] introduced the so-called mixed-mode S-parameters to extend the classical single-ended power wave theory to the differential case. As in single-ended S-parameters, the voltages and currents defined on the balanced ports can be used to define a set of normalized power waves. The difference is that these new mixed-mode normalized power waves are now specific to a propagation mode, i.e., they address differential and common-mode operation, as well as the conversion between these two modes of operation.

The mixed-mode S-parameter matrix for a generic three-port device, with an unbalanced and a balanced port, is defined by (6.2). Single-ended and mixed-mode parameter descriptions of a device with one or more balanced ports are equivalent and mutually convertible.



(6.2)

Within the subscripts *xyij*, *x* and *y* stand for the letters *s* (single-ended), *d* (differential mode) or *c* (common mode); while, *i* and *j* denote the port numbers, 1 stands for the single-ended port and 2 stands for the balanced port. The order of letters and numbers has the same meaning as for single-ended S-parameters. The first letters and numbers (*x* and *i*) represent mode and number of the load port, whereas the second ones (*y* and *j*) stand for the source port mode and number.

The matrix relation between the mixed-mode S-parameters and the standard S-parameters is written as [29] :

$$S_{mixed-mode} = M \cdot S_{std} \cdot M^{-1} \tag{6.3}$$

with the *M* matrix defined as follows :

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} \sqrt{2} & 0 & 0 \\ 0 & 1 & -1 \\ 0 & 1 & 1 \end{bmatrix} \tag{6.4}$$

Additionally, *M* has the property $M^{-1} = M^{T}$. The transformation in (6.3) indicates that a change of basis has occurred between standard and mixed-mode S-parameters. This further indicates that the two sets of S-parameters are different

representation of the same device and that contain the same information about the device. The expressions of mixed-mode S-parameters are given below.

The term S_{ss11} accounts for the reflection loss at the single-ended port :

$$S_{ss11} = S_{11} \tag{6.5}$$

The term S_{ds21} describes the forward transmission characteristics when only the differential output signal is considered. Since this term considers power from both sides of the balanced pair, a loss of 3-dB no longer needs to be taken into account. The value of S_{ds21} determines the insertion loss for the single-ended to differential-mode conversion :

$$S_{ds21} = \frac{1}{\sqrt{2}}(S_{21} - S_{31}) \tag{6.6}$$

Therefore, a value of S_{ds21} as close as possible to zero dB is desirable.

On the other hand, the value of S_{cs21} determines the single-ended to common-mode transfer function :

$$S_{cs21} = \frac{1}{\sqrt{2}}(S_{21} + S_{31}) \tag{6.7}$$

A negative value in dB as large as possible of S_{cs21} is desirable because an ideal balanced device is optimized for operation in differential mode, thus any signal that is common (or in-phase) to both terminals is ideally rejected and does not pass through the circuit.

S_{dd22} accounts for the reflection loss at the balanced port under a differential-mode stimulus, it is expressed as :

$$S_{dd22} = \frac{1}{2}(S_{22} - S_{32} - S_{23} + S_{33}) \tag{6.8}$$

S_{cd22} describes the conversion of differential-mode waves into common-mode waves at the balanced port :

$$S_{cd22} = \frac{1}{2}(S_{22} + S_{32} - S_{23} - S_{33}) \tag{6.9}$$

S_{cc22} describes the reflection loss at the balanced port under a common-mode stimulus, it is given by :

$$S_{cc22} = \frac{1}{2}(S_{22} + S_{32} + S_{23} + S_{33}) \tag{6.10}$$

For 3-port networks, where $S_{12} = S_{21}$, $S_{13} = S_{31}$, and $S_{23} = S_{32}$ the mixed-mode parameters become reciprocals : $S_{ds21} = S_{sd12}$, $S_{cs21} = S_{sc12}$, and $S_{dc22} = S_{cd22}$. This further means that the conversion from balanced-to-unbalanced, or vice versa, is also reciprocal.

Both the amplitude and the phase imbalance at the differential output are important figures-of-merit for describing the characteristics of the balun. The amplitude imbalance is a measure of the difference in dB between the two outputs of the differential pair, it is defined as :

$$\text{Amplitude imbalance} = 20 \cdot \log \frac{S_{21}}{S_{31}} \tag{6.11}$$

The phase imbalance is a measure of the phase difference in degrees between the two differential outputs, it is expressed as :

$$\text{Phase imbalance} = 180° - \text{phase} \frac{S_{21}}{S_{31}} \tag{6.12}$$

Another figure-of-merit used for describing the quality of the balun is given by the common-mode rejection ratio (CMRR). This is defined as the ratio of the differential-mode gain to the common-mode gain :

$$\text{CMRR} = \frac{S_{ds21}}{S_{cs21}} \tag{6.13}$$

6. 3 Circuit simulation

As a first approach, several baluns have been simulated using a circuit simulator (Aplac) in order to evaluate their achievable performances in terms of the following characteristics : reflection loss at the single-ended port, S_{11}, amplitude and phase of the transmission parameters S_{21} and S_{31}, single-to-differential insertion loss, S_{ds21} and single-to-common transfer function, S_{cs21}. The comparison of simulated performances will thus help to identify the most attractive balun, that will be successively fabricated and characterized.

Figure 6.1 illustrates the four different layouts of lumped-element baluns that have been investigated. Basically, these are three-port circuits, where the terminal port 1 is connected to an unbalanced source of impedance Z_S, and the output terminals 2 and 3 are connected to a balanced load of impedance Z_L.

The circuit depicted in Figure 6.1.a is commonly referred to as the 1st order out-of-phase power splitter, it consists of two inductors and two capacitors. Due to its symmetry, the phase difference between ports 2 and 3 is 180° independent of frequency. This circuit is also known as the 1st order lattice balun [30]. Throughout this work it will be designated as the balun of type A.

Figure 6.1.b represents the balun of type B, which is constituted by four inductors and two capacitors. A high-pass Π-section using one series capacitor and two inductors shunted to ground connects ports 1 and 2, while a low-pass T-section using two series inductors and one shunt capacitor connects ports 1 and 3. Since low-pass filters support forward waves and high-pass filters support backward waves, a phase difference of 180° between ports 2 and 3 is achieved at the frequency of interest.

The pairs of filters making up the proposed balun can be substituted by the corresponding dual filters sections, thus giving rise to alternative balun topologies. The balun of type C is depicted in Figure 6.1.c. This is made of two inductors and four capacitors, it consists of a low-pass Π-section using one series inductor and two shunt capacitors, and a high-pass T-section made of two series capacitors and one shunt inductor.

A fourth layout of balun, called type D, is represented in Figure 6.1.d. This is composed of three inductors and three capacitors arranged in a low-pass T-section with two series inductors and one shunt capacitor, and a high-pass T-section made of two series capacitors and one shunt inductor, respectively.

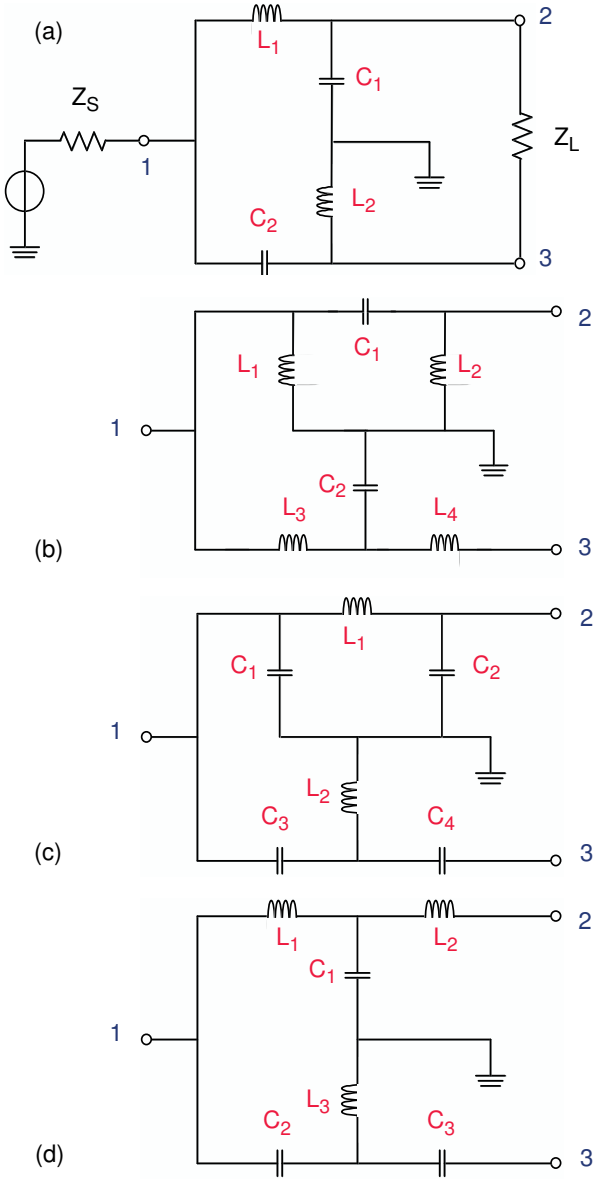


Figure 6.1 : Equivalent circuits of the proposed lumped-element baluns : type A (a), type B (b), type C (c) and type D (d).

The following relationships delineate the procedure adopted in order to determine the value of the lumped elements of the balun circuit. The balun is designed for operating in the ISM-band (2400-2480 MHz). Considering the center-frequency of this band, i.e., $f_0 = 2.44$ GHz, the radian frequency is given by :

$$\omega_0 = 2\pi f_0 \tag{6.14}$$

Then, the characteristic impedance of the balun is expressed as

$$Z_0 = \sqrt{Z_S \cdot Z_L} \tag{6.15}$$

where $Z_S = 50\ \Omega$ is the characteristic impedance of the single-ended source and $Z_L = 100\ \Omega$ is the characteristic impedance of the balanced load.

The nominal values of inductances and capacitances are then expressed with respect to the characteristic impedance of the balun and the radian frequency using (6.16) and (6.17), respectively.

$$L_0 = \frac{Z_0}{\omega_0} \tag{6.16}$$

The above expression yields for L_0 a value of 4.61 nH. Whereas, the value of C_0 calculated with the following expression :

$$C_0 = \frac{1}{\omega_0 \cdot Z_0} \tag{6.17}$$

yields a value of 0.92 pF. However, these nominal values of L_0 and C_0 do not take into account neither the parasitic capacitances associated to the pads and the inductors, nor the parasitic inductances due to the transmission lines connecting the lumped elements. Nonetheless, these parasitics have to be carefully accounted for in the design of the balun, so as to maintain suitable responses of both amplitude and phase imbalance. As a first approach, EM simulations have been performed for the sake of estimating the magnitude of parasitic coupling capacitances and inductances arising from the pads and interconnects, respectively. Particularly, very simple cases of parallel plate capacitors have been simulated in order to extract the magnitude of the capacitance between the pads.

On the other hand, transmission lines have been simulated in order to extrapolate the value of inductance per unit length. Furthermore, previous knowledge acquired from inductor characterization has been exploited for estimating the series resistance and the parasitic capacitance associated to the inductors. In Figure 6.2 the layout of balun of type B has been used as an instance for illustrating the various parasitics associated to the circuit. The physical meaning of these parasitics is the following :

- C_{p1} : input pad capacitance
- C_{p2} : output pad capacitance + parasitic capacitance due to L_2
- C_{p3} : parasitic capacitance on L_3
- C_{p4} : parasitic capacitance on L_4
- C_{p5} : parasitic capacitance due to C_2, L_3 and L_4
- C_{p6} : output pad capacitance + parasitic capacitance due to L_4
- L_{p1}, L_{p2}, L_{p3}, L_{p4}, L_{p5} : line inductance of the interconnects
- R_1 to R_9 : series resistances of the lumped elements and interconnects

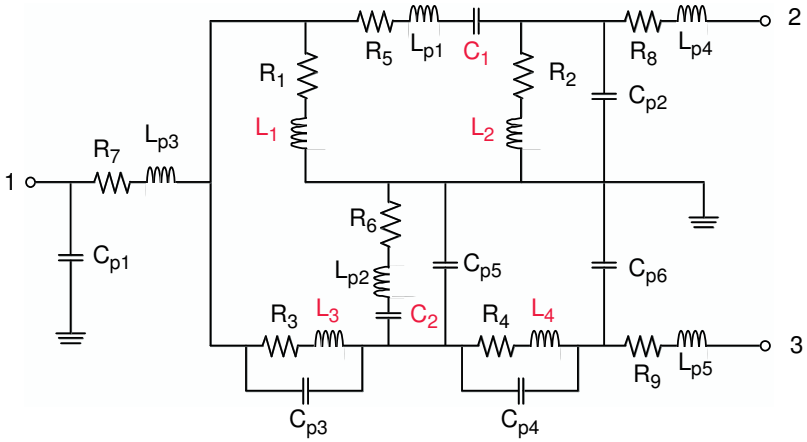


Figure 6.2 : Equivalent circuit of the balun of type B showing the parasitics capacitances, inductances and resistances associated to the pads, lumped elements and interconnects.

Once the different parasitics have been identified and their magnitudes estimated, these are used to tune the different values of the calculated discrete inductances and capacitances so as to counterbalance the effect of these parasitics. The tuning procedure has been realized using the following relationships :

$$C_1 = \frac{1}{\frac{1}{C_0} + \omega_0^2 \cdot L_{p1}} \tag{6.18}$$

$$C_2 = \frac{1}{\frac{1}{C_0} + \omega_0^2 \cdot L_{p2}} - C_{p5} \tag{6.19}$$

$$L_1 = \frac{1}{\frac{1}{L_0} + \omega_0^2 \cdot C_{p1}} \tag{6.20}$$

$$L_2 = \frac{1}{\frac{1}{L_0} + \omega_0^2 \cdot (C_{p2} - C_{p6})} \tag{6.21}$$

$$L_3 = \frac{1}{\frac{1}{L_0} + \omega_0^2 \cdot C_{p3}} \tag{6.22}$$

$$L_4 = \frac{1}{\frac{1}{L_0} + \omega_0^2 \cdot C_{p4}} \tag{6.23}$$

A similar procedure enabling to tune out the parasitics has been carried out on the other proposed baluns. As a further step, balun circuits including the parasitics have been simulated using Aplac.

Table 6.2 on page 19 summarizes the values of the relevant figures-of-merit obtained within the ISM-band (2400-2480 MHz). Figure 6.3 shows the behavior of the 1st order lattice balun (type A). The parameter S_{11} achieves a value of -19.7 dB at 2.44 GHz. The curves of S_{21} and S_{31} cross in a single point of value -3.65 dB situated precisely at 2.44 GHz. However, since both curves have a very steep slope, the amplitude imbalance become fairly severe away from the center frequency. The phases of S_{21} and S_{31} are -100 ± 2° and 74 ± 2°, respectively, hence leading to a phase imbalance of 6° within the frequency band of interest. The single-to-differential insertion loss expressed by the term S_{ds21} is better than -0.65 dB, while the single-to-common transfer function, S_{cs21} is less than -25 dB.

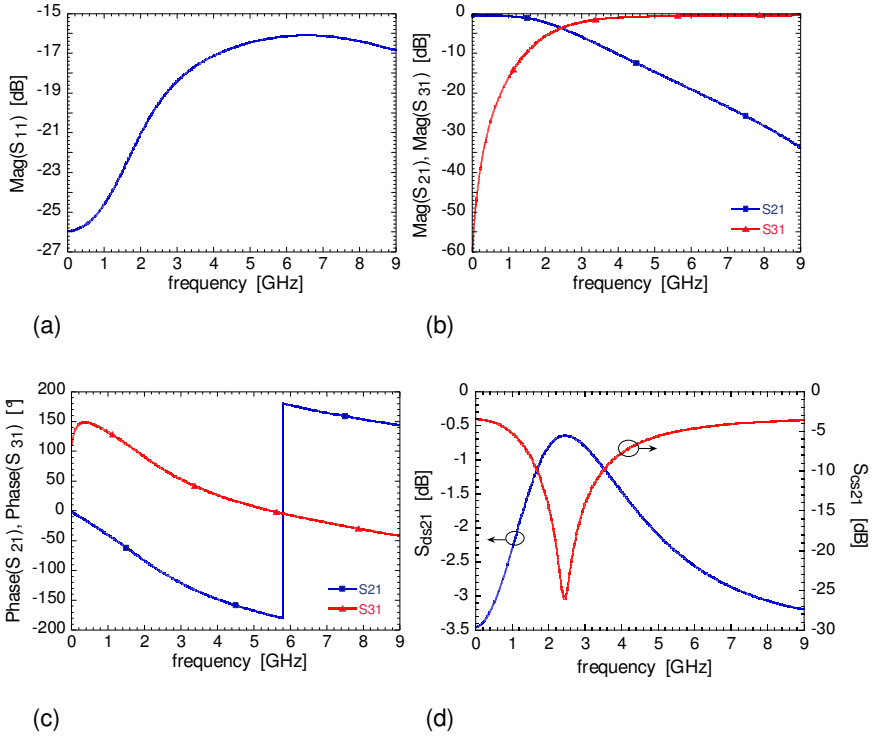


Figure 6.3 : Simulated characteristics corresponding to the balun of type A (1st order lattice-type) : magnitude of S_{11} (a), magnitude of S_{21} and S_{31} (b), phase of S_{21} and S_{31} (c), and magnitude of S_{ds21} and S_{cs21} (d), respectively.

Figure 6.4 illustrates the behavior of the balun of type B. S_{11} exhibits a sharp notch centered around 2.44 GHz, achieving values better than -25 dB . On the other hand, S_{21} and S_{31} display a nearly flat response across the frequency band of interest, thereby extending the useful bandwidth of the balun. S_{21} varies from -3.68 to -3.74 dB, while S_{31} varies from -3.72 dB to -3.69 dB. Since these values are very close, a nearly ideal amplitude imbalance (i.e., 0 dB) would be reached. The phases of S_{21} and S_{31} are 70 ± 2° and -111 ± 3°, respectively, thus determining a phase imbalance of about 1°. The single-to-differential insertion loss, S_{ds21} is better than -0.7 dB, while S_{cs21} ranges from -44 to -35 dB.

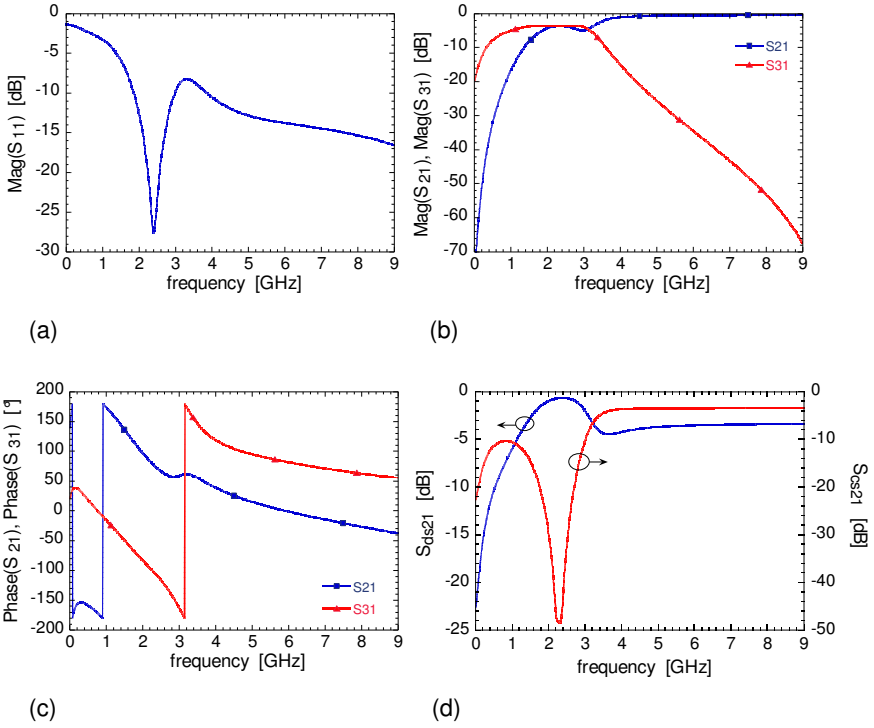


Figure 6.4 : Simulated characteristics corresponding to the balun of type B (4 inductors and 2 capacitors) : magnitude of S_{11} (a), magnitude of S_{21} and S_{31} (b), phase of S_{21} and S_{31} (c), and magnitude of S_{ds21} and S_{cs21} (d), respectively.

Figure 6.5 illustrates the behavior of the balun of type C. Like in the previous case, S_{11} exhibits a sharp notch centered in the frequency band of interest, displaying values comprised between -28 and -23 dB. Similarly, S_{21} and S_{31} also show a nearly flat response across the band. S_{21} varies from -3.69 to -3.74 dB, while S_{31} varies from -3.84 dB to -3.87 dB. These values ensure a theoretical amplitude imbalance of less than 0.2 dB. The phases of S_{21} and S_{31} are -99 ± 2.5° and 82 ± 3°, respectively, leading to a phase imbalance of about 1°. S_{ds21} is better than -0.79 dB, while S_{cs21}, is less than -40 dB.

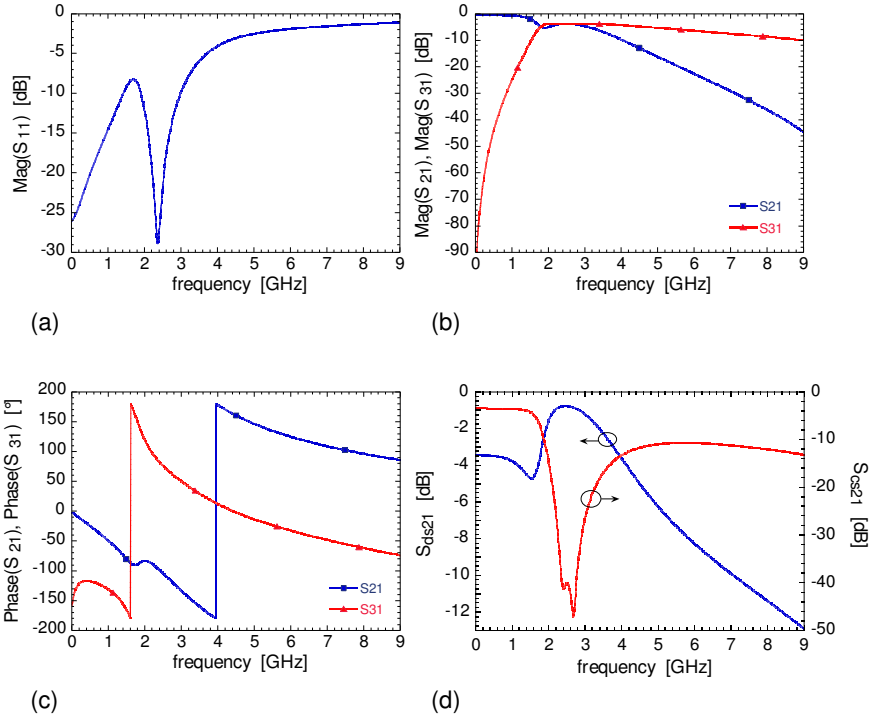


Figure 6.5 : Simulated characteristics corresponding to the balun of type C (2 inductors and 4 capacitors) : magnitude of S_{11} (a), magnitude of S_{21} and S_{31} (b), phase of S_{21} and S_{31} (c), and magnitude of S_{ds21} and S_{cs21} (d), respectively.

Figure 6.6 shows the behavior of the balun of type D. The reflection loss S_{11} is less than -8 dB all over the simulated frequency range. Moreover, in a similar fashion as for baluns of type B and C, S_{11} exhibits a notch centered in the ISM-band (2400-2480 MHz), with values better than -24 dB. However, when looking at S_{21} and S_{31}, it can be noted that the response in no longer flat, but two distinct bumps appear. Across the band of interest, S_{21} varies from -4.1 to -3.8 dB, while S_{31} varies from -3.5 to -3.7 dB. Compared to the baluns discussed earlier, these values of insertion loss ultimately result in a worse amplitude imbalance. The phases of S_{21} and S_{31} are -100 ± 2° and 82 ± 3°, determining a phase imbalance of about 2°. S_{ds21} is better than -0.78 dB, while S_{cs21} ranges from -29 to -38 dB.

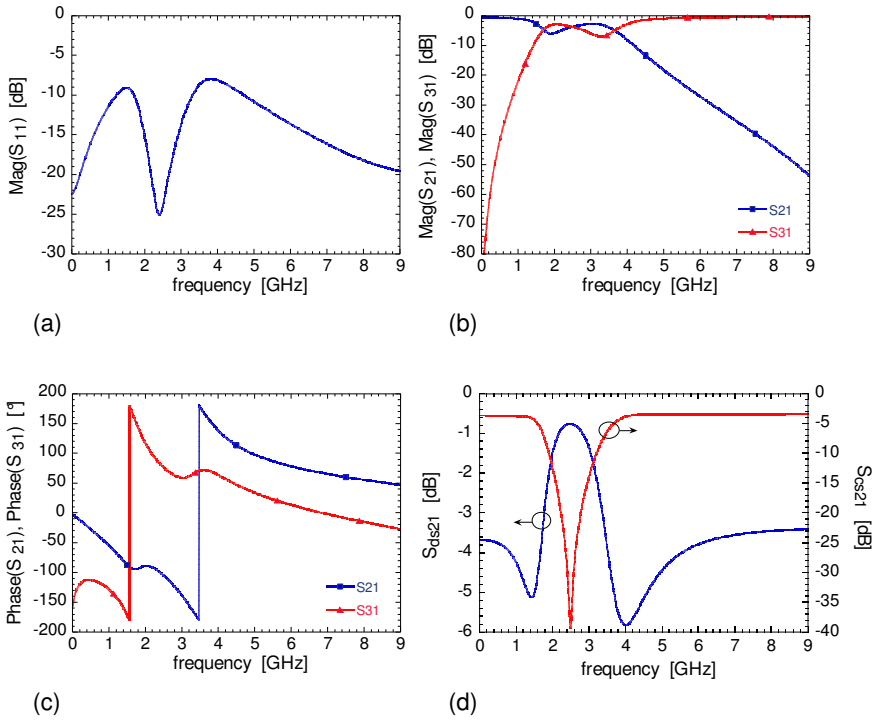


Figure 6.6 : Simulated characteristics corresponding to the balun of type D (3 inductors and 3 capacitors) : magnitude of S_{11} (a), magnitude of S_{21} and S_{31} (b), phase of S_{21} and S_{31} (c), and magnitude of S_{ds21} and S_{cs21} (d), respectively.

By comparing the simulated performances shown by the proposed baluns, some important considerations can be made. First of all, the curves of reflection loss at the single-ended port of the baluns of type B, C and D exhibit a sharp notch centered in the ISM-band (2400-2480 MHz), allowing for values of S_{11} in the order of -25 dB. In contrast, the balun of type A displays a value of S_{11} that is less than -20 dB. A value of S_{11} as negative as possible is highly desirable since it expresses the ratio of the energy reflected at the single-ended port versus the energy entering the device, hence, it is an indication of how good the impedance adaptation is.

The transmission parameters S_{21} and S_{31} corresponding to the baluns of type B and C, highlight a fairly flat response within the frequency band of interest. This in turn keeps minimum the difference in magnitude between these two parameters, thus potentially allowing for an excellent value of amplitude imbalance. On the other hand, the transmission parameters S_{21} and S_{31} of the baluns of type A and D, cross in a single point within the band and then rapidly separate, resulting in a worse amplitude imbalance compared to baluns of type B and C.

In general, the phase imbalance observed within the ISM-band (2400-2480 MHz), is less than 2° for the baluns of types B, C and D, and is about 6° for the balun of type A.

The simulated single-to-differential insertion loss, S_{ds21} of all the considered baluns is better than -0.8 dB. Particularly, from this point of view, the balun of type A, exhibiting a value of S_{ds21} = -0.65 dB, is the one that performs better. This stems from the fact that the insertion loss is mostly due to the DC resistance of the metal tracks, and the balun of type A, that is made up of only four discrete elements, features a shorter signal path between the input and output port. Consequently, the energy dissipated in the metallization is less compared to the other types of baluns constituted by six discrete elements. Moreover, the implementation of the balun of type A would results in a more compact layout.

Considering the parameter S_{cs21}, that accounts for the single-to-common mode transfer function, the baluns of types B and C are those showing the most promising performances, yielding values around -40 dB. Such low values of S_{cs21} ensure that a negligible amount of energy entering the single-ended port is converted into a common-mode signal at the balanced port.

Based on the considerations made so far, the baluns exhibiting the best performances are those of type B and C. However, since the balun of type C requires the implementation of four capacitors, its behavior is more sensitive to undesired process instabilities that could affect the nominal value of capacitance.

Such instabilities include, for instance, drifts in the deposition rate of dielectric films, or even modifications of the film quality that could lead to variations of the dielectric constant.

In conclusion, based on the trends issued from circuit simulations, the balun of type B appears as the most promising one in perspective of implementation by thin-film process. The fabrication and testing of the balun of type B is reported in the next paragraphs.

TABLE 6.2 : SIMULATED PERFORMANCES WITHIN THE ISM-BAND (2400-2480 MHZ) OF THE PROPOSED FOUR TYPES OF LUMPED-ELEMENT BALUNS.

Balun layout	S_{11} mag [dB] and *phase* [°]	S_{21} mag [dB] and *phase* [°]	S_{31} mag [dB] and *phase* [°]	S_{ds21} [dB]	S_{cs21} [dB]
Type A	-19.7 ± 0.1 *174 ± 3*	-3.6 ± 0.1 *-100 ± 2*	-3.7 ± 0.1 *74 ± 2*	-0.65	-25.9 ± 0.1
Type B	-26 ± 1 *124 ± 16*	-3.7 ± 0.02 *70 ± 2*	-3.7 ± 0.02 *-111 ± 3*	-0.7 ± 0.01	-40 ± 4
Type C	-25 ± 3 *-110 ± 30*	-3.72 ± 0.02 *-99 ± 2.5*	-3.86 ± 0.02 *82 ± 3*	-0.78 ± 0.01	-41 ± 0.5
Type D	-24.8 ± 0.4 *169 ± 7*	-4 ± 0.2 *-100 ± 2.2*	-3.6 ± 0.1 *82 ± 3*	-0.77 ± 0.01	-33 ± 5

6. 4 Fabrication

The baluns of type B have been fabricated using the 5-mask process involving Ag electroplating described in paragraph 3.2.2. The first thinner metal level (300 nm of Al) forms the underpass of inductors, as well as the bottom electrodes of MIM capacitors. The top 12 µm-thick Ag metallization implements inductor coils, top electrodes of MIM capacitors, transmission lines and the ground frame surrounding the whole circuit, respectively. A film 1 µm-thick of sputter deposited SiO_2 is used both as dielectric layer for the MIM capacitors and as isolation between underpass and spiral in inductors. Moreover, the proposed balun has been fabricated on Pyrex substrate in order to minimize RF losses. Figure 6.7.a shows the whole cell containing the fabricated baluns. In order to compensate the lack of

accuracy in the estimation of parasitics capacitances and line inductances, 51 baluns differing in the nominal values of their lumped inductors and capacitors have been designed. In addition, the zone at the top-right of the cell houses a series of single-port inductors and capacitors serving as reference for comparing the nominal values of capacitance and inductance assumed in the procedure of circuit simulation to the values obtained on these real devices by parameter extraction. Figure 6.7.b shows a SEM image of a fabricated balun having a footprint of 1.48 x 1.76 mm^2.

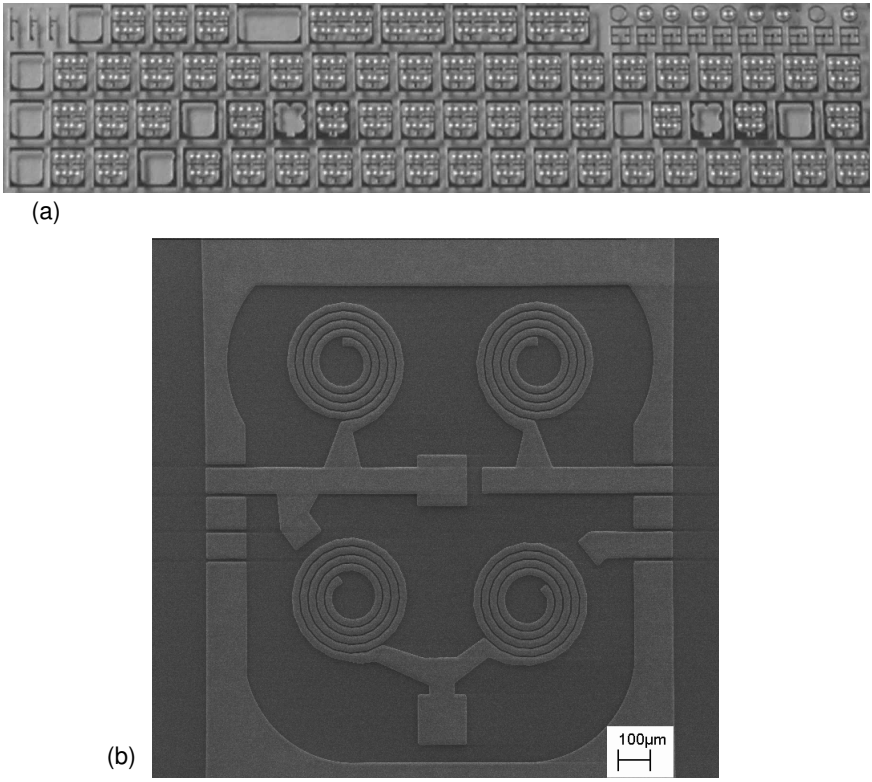


Figure 6.7 : Optical image of the cell containing the baluns, test inductors and capacitors fabricated on Pyrex substrate (a), SEM image of a fabricated balun with a total size of 1.48 x 1.76 mm^2 (b).

6. 5 RF characterization

6. 5. 1 Lumped elements assessment

The goal of this paragraph is to quantify the difference between nominal values of inductors and MIM capacitors and the effective values obtained from fabricated and characterized test devices.

Figure 6.8 compares the nominal inductances of three test inductors with 4 turns, $w = 20\ \mu m$ and $s = 6\ \mu m$, versus the values of L_s extracted with the equivalent circuit presented in paragraph 4.2. The extracted values of the characterized inductors are systematically higher than the nominal values. Particularly, this discrepancy ranges from 2.85 to 4.45%. Possible reasons that could be blamed for these values exceeding the expected ones are, firstly, the reinforced mutual coupling as a consequence of the reduced spacing left between adjacent electroplated tracks of inductors (see paragraph 3.3.2); and secondly, the inaccuracy inherent to the empirical procedure adopted for the prediction of inductance values (see paragraph 4.4).

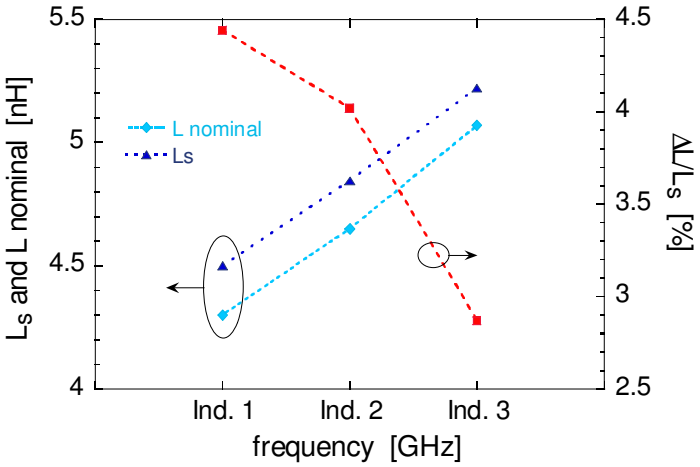


Figure 6.8 : Nominal values of inductance compared to the extracted values, L_s, and absolute error.

The well-known relationship for parallel-plate capacitors (6.24), has been used for calculating the area of the electrodes corresponding to a target value of capacitance.

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{t} \tag{6.24}$$

In the above relationship ε_0 is the free-space permittivity and ε_r is the relative permittivity of the dielectric film of SiO_2. The reported value ε_r = 3.9 corresponding to the thermal oxide has been assumed for the calculation. A is the area corresponding to the overlap between top and bottom electrodes, and t is the thickness of the dielectric layer separating the electrodes.

Figure 6.9 depicts the equivalent circuit describing the behavior of a MIM capacitor [31]. The physical meaning of the lumped elements is the following : R_s and L_s account for the series resistance and parasitic inductance of the electrodes, respectively. C_p is the equivalent capacitance of the device, that corresponds to the low-frequency value of the ratio 1/(ω·Im(Z)). Finally, R_p accounts for the losses of the dielectric film. Figure 6.10.a shows an example of measured versus simulated curves of 1/(ω·Im(Z)) for a MIM capacitor with a nominal value of 0.86 pF, while Figure 6.10.b displays the reflection parameter S_{11} plotted in the Smith chart. As the frequency increases, at some point the device impedance turns from capacitive to inductive as a consequence of the formation of parasitic inductance.

Figure 6.11 displays the nominal values of capacitance of five devices versus the corresponding extracted values of C_p. Here, the extracted values exceed the nominal values by 5.9 up to 6.5%. Possible reasons explaining this non negligible difference are, first of all, a bad calibration procedure of the network analyzer. Secondly, a dielectric thickness inferior to what has been planned. Third, a relative permittivity of SiO_2 that is higher than the value assumed for the calculation. Last, the effect of the fringing fields between top and bottom electrodes that add extra capacitance to the nominal value. However, this latter effect should contribute only marginally to the total capacitance value.

Since the sputtering rate of SiO_2 has been calibrated prior to the deposition on process wafers, it is very unlikely for the resulting film thickness to be about 6% inferior to the desired value of 1.0 µm.

On the other hand, a value of relative permittivity exceeding the reported one could arise from a different stoechiometry (i.e., a different Si/O ratio) compared to the one of thermal oxide. This reason seems to be the most plausible for explaining capacitance values higher than expected.

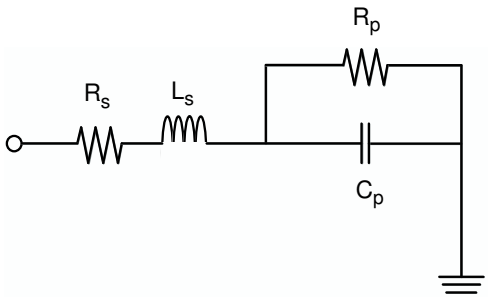


Figure 6.9 : Equivalent circuit of a metal-insulator-metal (MIM) capacitor.

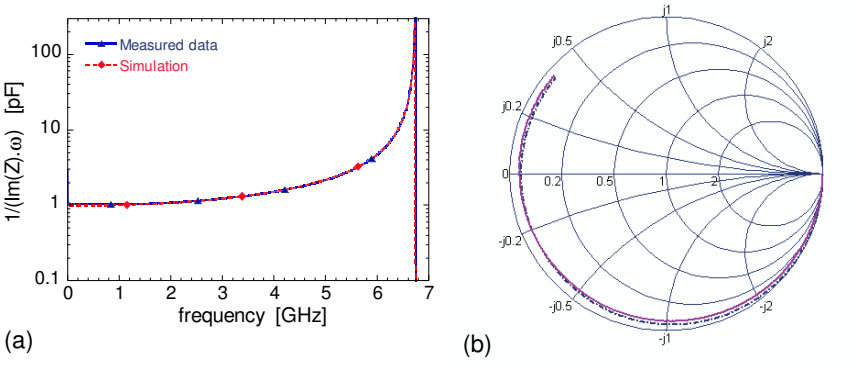


Figure 6.10 : Measured data (full lines) and simulated behavior (dashed lines) of $1/(\omega \cdot \mathrm{Im}(Z))$ (a), and reflection parameter, S_{11}, plotted on the Smith chart (b).

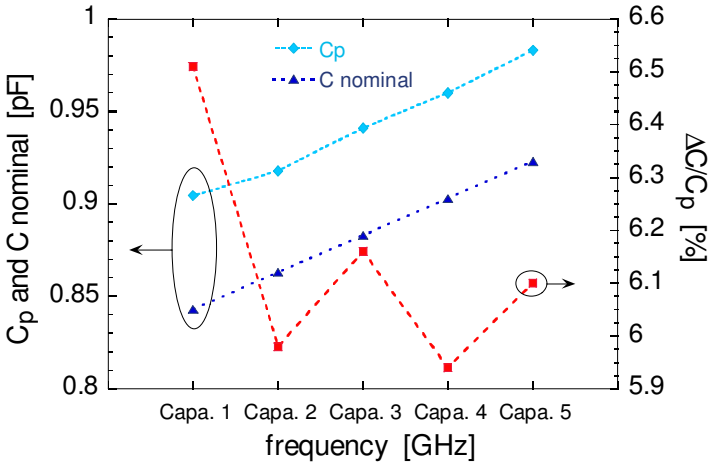


Figure 6.11 : Nominal values of capacitance compared to the extracted values, C_p, and absolute error.

6. 5. 2 Balun performances

This paragraph illustrates the typical performances exhibited by a balun of type B. Figure 6.12 shows the CAD plot corresponding to the characterized balun. The nominal values of the lumped inductors is 4.8 nH for L_1 and 5.0 nH for the other inductors, i.e., L_2, L_3 and L_4; whereas, the nominal value of the capacitors is 0.9 pF for C_1 and 0.86 pF for C_2.

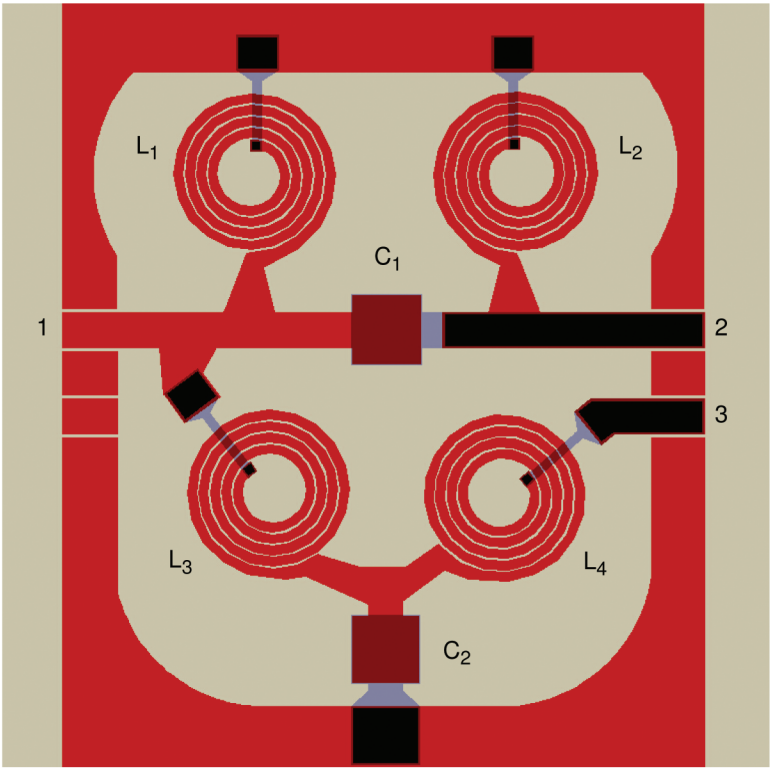


Figure 6.12 : CAD plot of the characterized balun of type B. The nominal value of the inductors is 4.8 nH for L_1 and 5.0 nH for the others; whereas, the nominal value of the capacitors is 0.9 pF for C_1 and 0.86 pF for C_2. The port number is also indicated.

The fabricated three-port baluns have been characterized using g-s-g-s-g probes. The S-parameter measurement has been performed form 300 KHz to 9 GHz in a linear scale of 1600 points. Subsequently, measured data have been treated with Matlab routines in order to compute the mixed-mode S-parameters.

Figure 6.13 shows the measured curve of the reflection loss at the single-ended port. Similarly to the behavior predicted by circuit simulation (see Figure 6.4), S_{11} exhibits a sharp notch allowing for very promising values of reflection loss. Particularly, S_{11} achieves a minimum of -36 dB at 2.3 GHz. Whereas, within the ISM-band (2400-2480 MHz), S_{11} spans from -25 to -20 dB, with a value at the center-frequency (i.e., 2.44 GHz) of -22.5 dB.

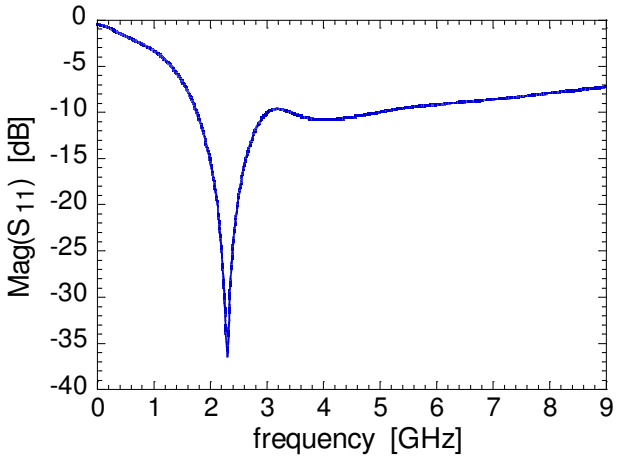


Figure 6.13 : Measured reflection loss at the single-ended port, S_{11}.

The amplitude and phase of the single-ended transmission parameters S_{21} and S_{31} are represented in Figure 6.14. Here, again, the measured characteristics are in good agreement with circuit simulations. S_{21} and S_{31} show fairly constant values of amplitude within the frequency band of interest, leading to a "smooth" amplitude imbalance. However, S_{21} is systematically lower than S_{31} all over the band. Particularly, S_{21} varies from -4.08 to -4.15 dB, while S_{31} spans from -3.68 to -3.7 dB.

Thus, it can be concluded that the transmission path from port 1 to port 2 is more prone to insertion loss than the path connecting port 1 to port 3. The phase of S_{21} is 68 ± 2°, and the phase of S_{31} is -112 ± 3°.

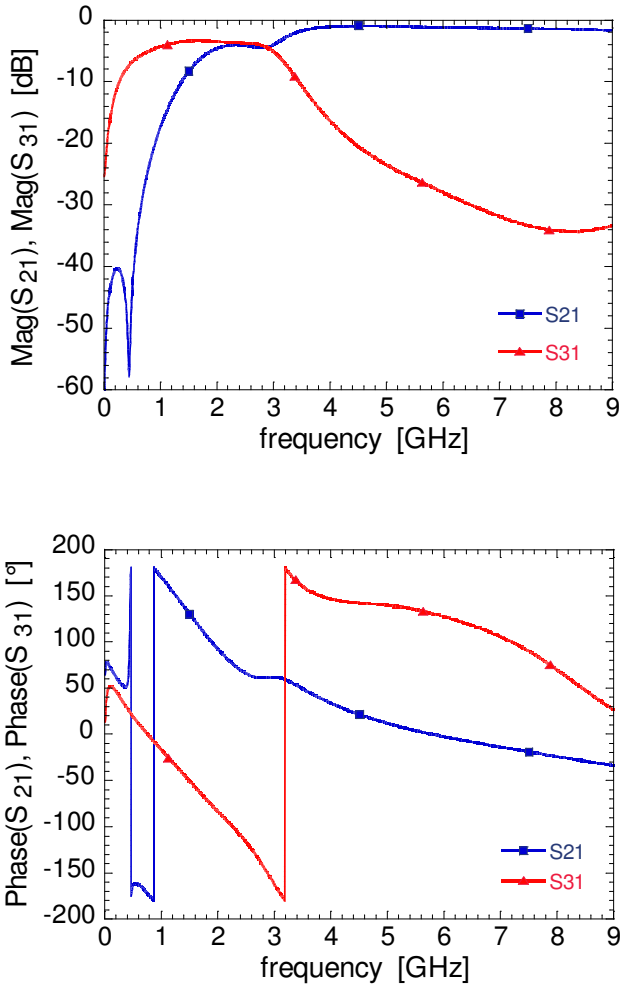


Figure 6.14 : Measured transmission parameters S_{21} and S_{31}: amplitude in dB (top) and phase in degrees (bottom).

Figure 6.15 shows the amplitude and phase imbalance plotted between 2 and 3 GHz. Within the ISM-band (2400-2480 MHz), the amplitude imbalance is 0.4 ± 0.02 dB, while the absolute phase error is less than 1.5°, achieving 0.1° at the center-band. However, it should be noted that the minimum of the amplitude imbalance, i.e., -0.38 dB, is obtained at 2.37 GHz.

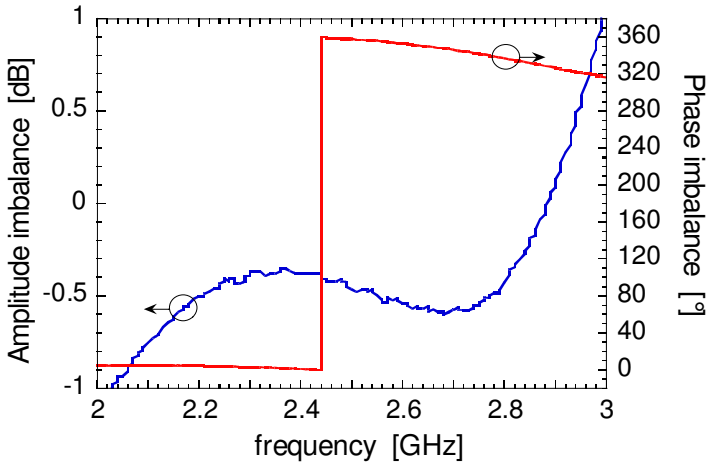


Figure 6.15 : Amplitude and phase imbalance.

The single-to-differential insertion loss and single-to-common conversion factor are plotted in Figure 6.16. The values of S_{ds21} and S_{cs21} corresponding to the ISM-band (2400-2480 MHz) are -0.9 ± 0.02 dB and -33.4 ± 0.2 dB, respectively. However, the minimum value of S_{ds21}, that is -0.85 dB, is achieved at 2.3 GHz, again revealing a non optimum match of the balun response with the target frequency-band.

The common-mode rejection ratio (CMRR) displayed in Figure 6.17 reaches its highest values in the ISM-band (2400-2480 MHz). These values range from 31.5 to 32.3 dB.

The mixed-mode S-parameters at the balanced port are represented in Figure 6.18. S_{dd22} accounts for the differential-mode reflection loss at the balanced port under a pure differential stimulus. A value of -22 dB at 2.44 GHz indicates a good

impedance adaptation. S_{cd22} describes the common-mode reflection loss at the balanced port under a pure differential stimulus. A value of -25 dB is achieved at 2.44 GHz. Such a large negative value in dB is an index of a good impedance adaptation and indicates that only a small amount of energy entering the device in differential-mode is converted into a common-mode signal response at the balanced port. This is a correct behavior for a device that is optimized for working in differential-mode. Finally, the parameter S_{cc22} describes the common-mode reflection loss at the balanced port under a pure common-mode stimulus. In this case, a value of -1.4 dB at 2.44 GHz is obtained. Such small value in dB means that the common-mode stimulus coupled to the balanced port is largely reflected. This again is a correct behavior.

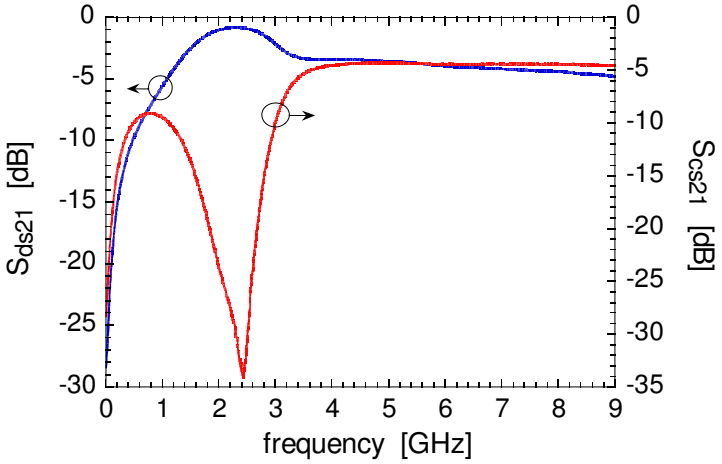


Figure 6.16 : Single-to-differential insertion loss, S_{ds21} and single-to-common conversion parameter, S_{cs21}.

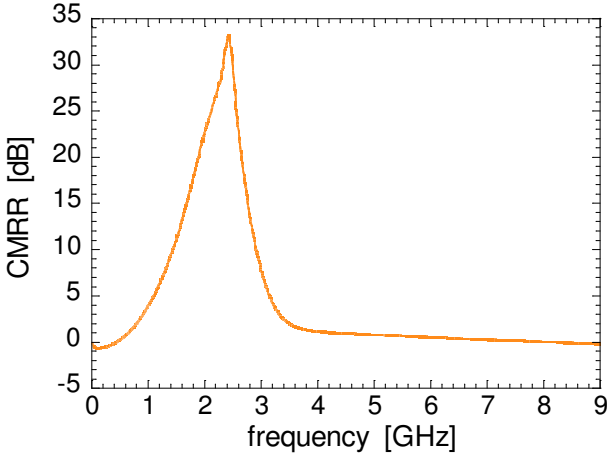


Figure 6.17 : Common-mode rejection ratio (CMRR).

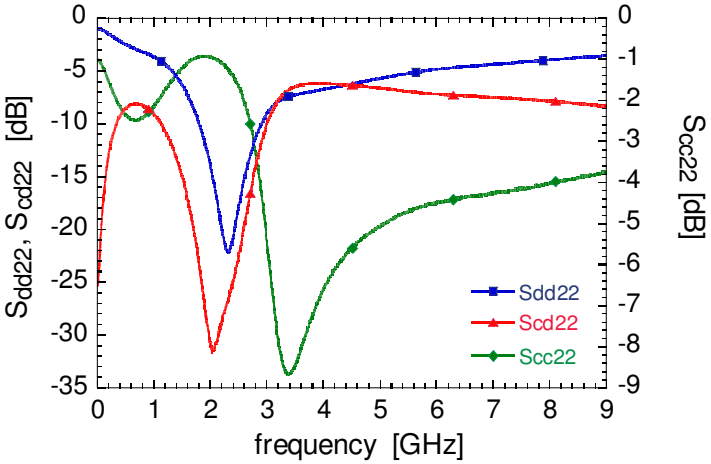


Figure 6.18 : Mixed-mode S-parameters at the balanced port : S_{dd22}, S_{cd22} and S_{cc22}.

6. 5. 3 Role of the capacitors

The next step is an investigation of the role played by the value of MIM capacitors on the overall behavior of the balun. This analysis is carried out by comparing a set of five baluns with identical nominal inductances, but with a value of capacitance that increases in steps of 10 fF. Table 6.3 lists the nominal values of the lumped inductors and capacitors. Thus, looking at Balun 1 and 5, the increase of the capacitance is 4.35% for C_1 and 4.54% for C_2.

Figure 6.19 highlights the behavior of S_{11} upon a variation of the capacitance values. Two major trends can be observed. Firstly, the higher the capacitance, the lower is the frequency corresponding to the notch of S_{11}. Balun 1 achieves its minimum of S_{11} at 2.3 GHz, whereas for Balun 5 the minimum of S_{11} is located at 2.22 GHz. Secondly, the increased capacitance raises the value of S_{11}, except in the case of Balun 3, thus resulting in a less good reflection loss.

On the other hand, the trends of S_{21} and S_{31} displayed in Figure 6.20, show that an increased capacitance produces less negative values of S_{21} and more negative values of S_{31}, thereby reducing the absolute difference between these two parameters and consequently improving the amplitude imbalance. Figure 6.21 confirms that the amplitude error at 2.44 GHz is indeed reduced from -0.5 dB for Balun 1 to -0.35 dB for Balun 5. On the contrary, the phase imbalance shows little variation being around 2-2.5° for all of the considered baluns.

The values of S_{ds21} displayed in Figure 6.22 are almost identical within the ISM-band (2400-2480 MHz); however, all the considered baluns achieve the minimum of S_{ds21} between 2.2 and 2.3 GHz. As shown in Figure 6.22, the minimum of S_{cs21} is well centered at 2.44 GHz. Here, the increase in capacitance produces better values of S_{cs21}. These range from -33 dB for Balun 1 to -35.5 dB for Balun 5.

TABLE 6.3 : NOMINAL VALUES OF THE LUMPED ELEMENTS.

Device	L_i [nH]	C_1 [pF]	C_2 [pF]
Balun 1	5.0	0.88	0.84
Balun 2	5.0	0.89	0.85
Balun 3	5.0	0.9	0.86
Balun 4	5.0	0.91	0.87
Balun 5	5.0	0.92	0.88

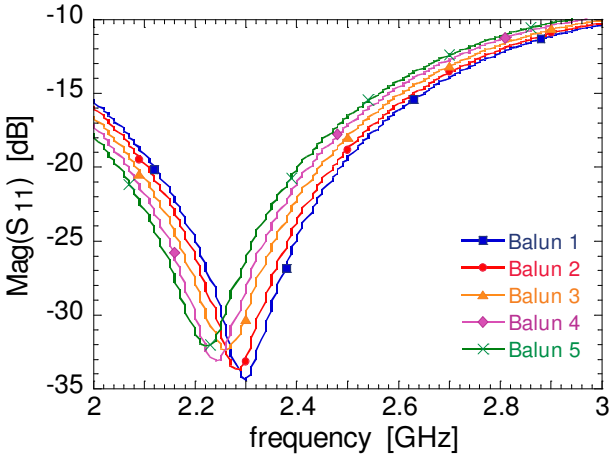


Figure 6.19 : Reflection loss at the single-ended port, S_{11}, as a function of different values of capacitance (see Table 6.3).

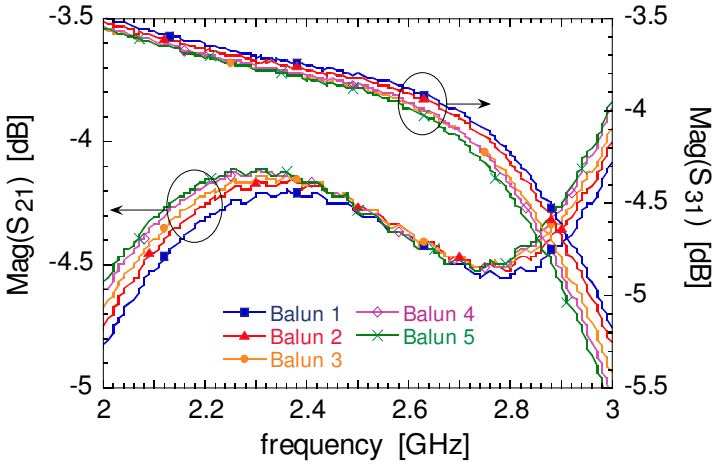


Figure 6.20 : Measured transmission parameters S_{21} and S_{31}, as a function of different values of capacitance.

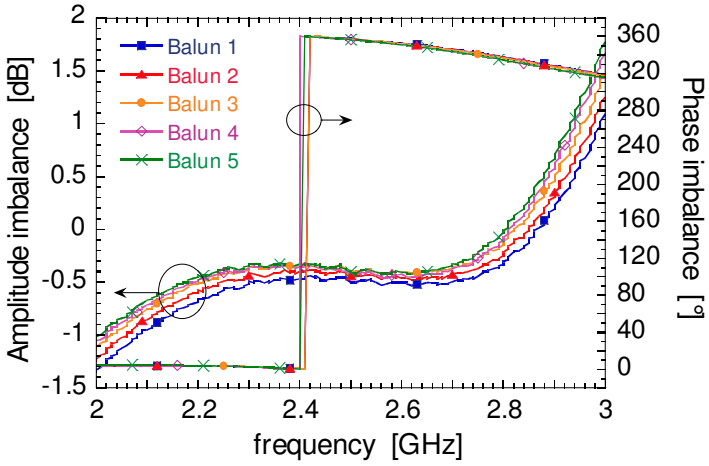


Figure 6.21 : Amplitude and phase imbalance, as a function of different values of capacitance.

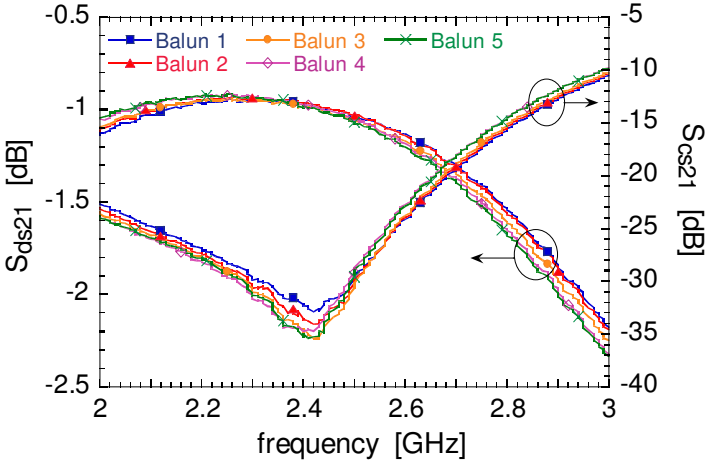


Figure 6.22 : S_{ds21} and S_{cs21}, as a function of different values of capacitance.

6. 5. 4 Role of the inductors

This paragraph provides an insight on the role played by the inductors by comparing the response of a set of three baluns with identical capacitance, but with different inductance. Table 6.4 lists the nominal values of the lumped inductors and capacitors. Balun 1 has four inductors with same inductance value of 4.25 nH, while Balun 3 has four 4.65-nH inductors. This corresponds to an increased inductance of 8.6%.

Figure 6.23 shows that the increased inductance has a significant effect on the return loss. S_{11} drops from -29 dB at 2.3 GHz for the Balun 1 to -45 dB at 2.27 GHz for the Balun 3. Hence, a higher inductance enhances the impedance adaptation of the balun. However, from a general point of view, the variation of inductance has been observed to be less significant on the other figures-of-merit describing the balun behavior.

When looking at the behavior of S_{21} and S_{31} (Figure 6.24), the Balun 2, with an intermediate value of inductance, is the one that performs better within the ISM-band (2400-2480 MHz). S_{21} is -4.1 ± 0.1 dB and S_{31} is -3.9 ± 0.1 dB.

Figure 6.25 shows that the amplitude imbalance is -0.6 dB and the phase imbalance is less than 3° for all the considered baluns.

The values of S_{ds21} and S_{cs21} are displayed in Figure 6.26. Balun 2 achieves a S_{ds21} of -0.8 dB at 2.44 GHz, that is 0.05 dB better than the other two baluns. On the other hand, the minimum value of S_{cs21} is -30.5 dB for all the baluns, even though the minimum is not achieved at the same frequency.

TABLE 6.4 : NOMINAL VALUES OF THE LUMPED ELEMENTS.

Device	L_i [nH]	C_1 [pF]	C_2 [pF]
Balun 1	4.25	0.91	0.87
Balun 2	4.35	0.91	0.87
Balun 3	4.65	0.91	0.87

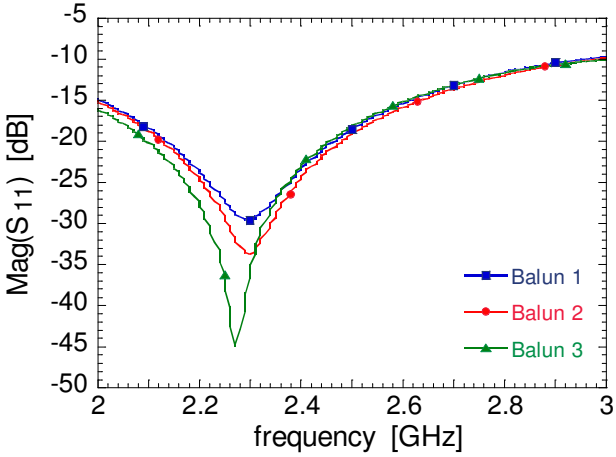


Figure 6.23 : Reflection loss at the single-ended port, S_{11}, as a function of different values of inductance (see Table 6.4).

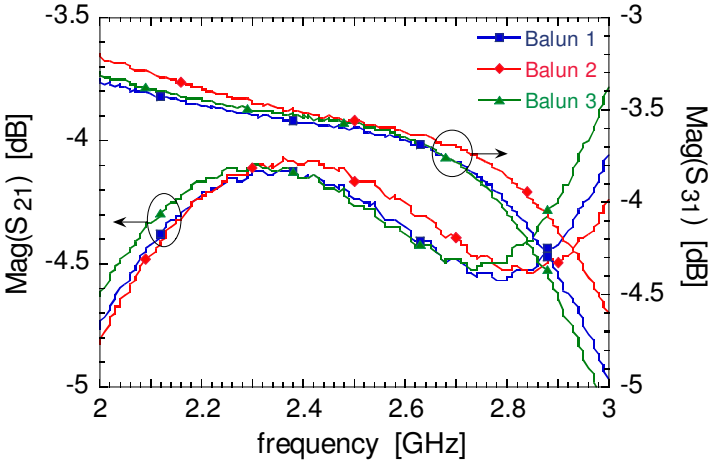


Figure 6.24 : Measured transmission parameters S_{21} and S_{31}, as a function of different values of inductance.

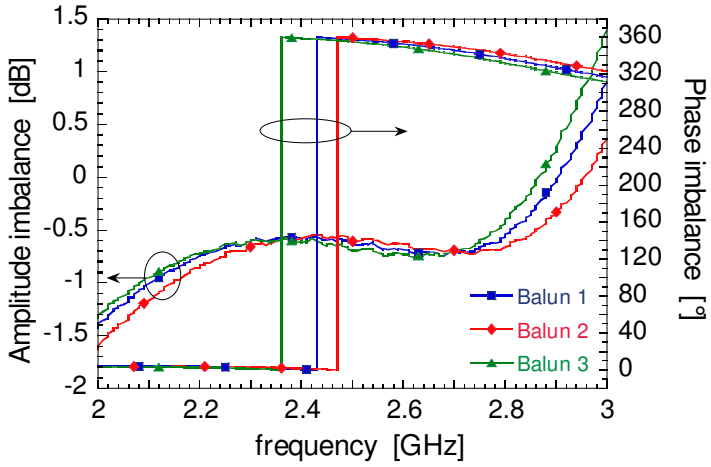


Figure 6.25 : Amplitude and phase imbalance, as a function of different values of inductance.

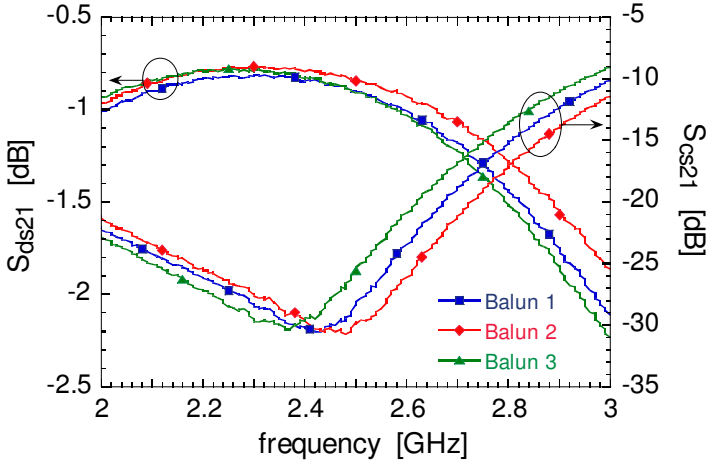


Figure 6.26 : S_{ds21} and S_{cs21}, as a function of different values of inductance.

6. 6 EM simulation

The measured performances of a fabricated balun have been compared to data issued from EM simulation. Figure 6.27 illustrates the 3-D layout of the simulated balun. This has been simulated as a three-port DUT using lossless transmission lines for connecting the box-wall ports to the DUT and for providing a ground path to the return signal. Thick metal model with NS = 3, has been used for simulating the metallization of the lumped inductors, capacitors and the transmission lines connecting these elements. Furthermore, in order to reduce the size of the analyzed file, Conformal mesh has been applied to inductors, while Staircase fill has been used for the other, essentially rectangular-shaped, metallization patterns. Normal metal has been applied to spiral underpasses, bottom electrodes of MIM capacitors and to the ground ring. The resulting file (1'229 MB) has been analyzed through an adaptive sweep and it has required 1 hour and 3 minutes for the calculation of one frequency. The computation of 12 discrete frequencies has required an overnight run.

The plots displayed in the next figures compare measured data versus simulated performances in terms of reflection loss, S_{11} (Figure 6.28), transmission parameters S_{21} and S_{31} (Figure 6.29), amplitude and phase imbalance (Figure 6.30), and S_{ds21} and S_{cs21} (Figure 6.31). In general, the simulated curves exhibit a reasonable agreement to measured data all over the considered frequency range.

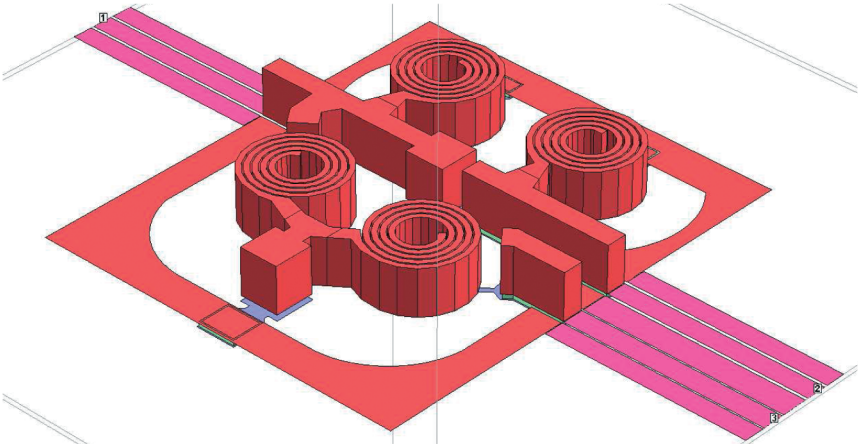


Figure 6.27 : Layout of the simulated DUT. Lumped elements have been modeled with TM (NS = 3), as highlighted by the non-zero thickness (not in scale).

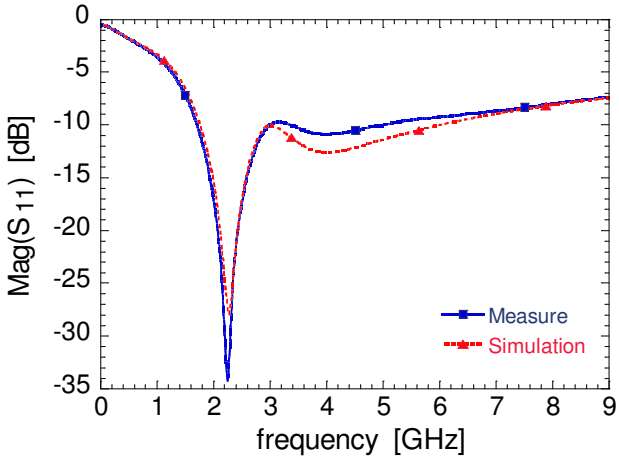


Figure 6.28 : Comparison of measured (full line) versus simulated (dashed line) reflection loss, S_{11}.

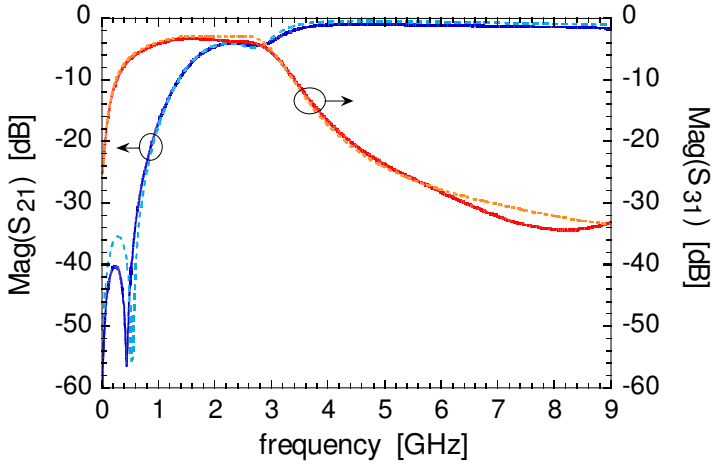


Figure 6.29 : Measured (full lines) versus simulated data (dashed lines) of the transmission parameters S_{21} and S_{31}.

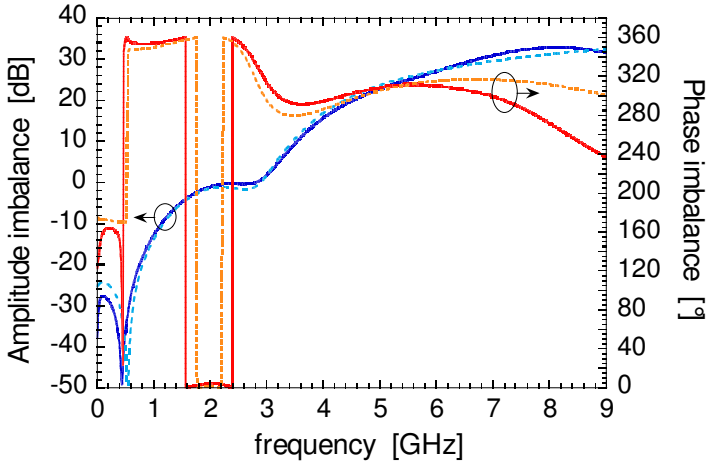


Figure 6.30 : Measured (full lines) versus simulated data (dashed lines) of amplitude and phase imbalances.

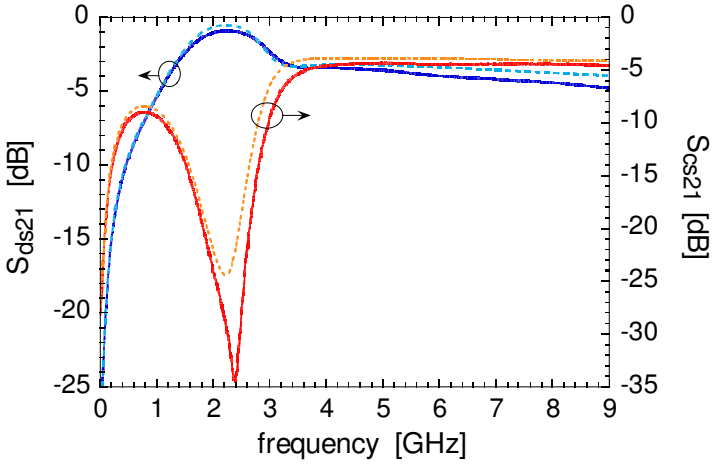


Figure 6.31 : Measured (full lines) versus simulated data (dashed lines) of S_{ds21} and S_{cs21}.

Table 6.5 summarizes the measured and simulated performances taken at 2.44 GHz. The incertitude given for each of these values covers the whole ISM-band (2400-2480 MHz).

TABLE 6.5 : MEASURED VERSUS SIMULATED PERFORMANCES WITHIN THE ISM-BAND (2400-2480 MHZ).

Data	S_{11} [dB]	S_{21} [dB]	S_{31} [dB]	Amplitude imbalance [dB]	Phase imbalance [°]	S_{ds21} [dB]	S_{cs21} [dB]
Measured	-20 ± 2 -34 @ 2.25 GHz	-4.23 ± 0.03	-3.82 ± 0.03	-0.41 ± 0.02	0.6 ± 2	-1.02 ± 0.03	-32 ± 2
Simulated	-20 ± 2 -28 @ 2.3 GHz	-4.38 ± 0.08	-2.9 ± 0.1	-1.4 ± 0.1	7 ± 2	-0.64 ± 0.04	-21.2 ± 0.6

The measured curve of S_{11} displays a notch centered at 2.25 GHz (see Figure 6.28). The corresponding simulated curve provides a good match and exhibits a minimum of S_{11} centered at 2.3 GHz. In order for the simulation to be accurate, ε_r of SiO_2 has been taken as 4.2, that is 7.7% higher than the reported value. In fact, earlier simulations run with $\varepsilon_r = 3.9$ (not presented in the report) have revealed a minimum of S_{11} centered around 2.4 GHz. This, again, emphasizes how the balun response is sensitive to a variation of capacitance. Despite the frequency corresponding to the minima of the measured and simulated curves of S_{11} is in excellent agreement, a significant difference in the notch amplitude is observed. The measured curve exhibits a minimum value of S_{11} of -34 dB, while the corresponding minimum of the simulated curve is -28 dB. As witnessed by behavior of the set of baluns discussed in paragraph 6.5.4, this discrepancy of amplitude could be imputed to the simulated inductance of the lumped inductors, which is lower compared to the inductance of the fabricated baluns. The inductors constituting the balun circuit have been simulated with an inter-turn spacing of 6 µm; however, as previously pointed out (see paragraph 3.2.2) the inter-turn spacing obtained on devices fabricated by Ag electroplating is actually less than 6 µm. This, in turn, leads to an enhanced value of inductance.

The simulated transmission parameters S_{21} and S_{31}, plotted in Figure 6.29, exhibit an opposite behavior with regard to measured data. Particularly, the

simulated S_{21} (-4.38 ± 0.08 dB) is slightly worse, within the ISM-band (2400-2480 MHz), than the measured parameter (-4.23 ± 0.03 dB); whereas, simulated values of S_{31} (-2.9 ± 0.1 dB) are significantly better than measured ones (-3.82 ± 0.03 dB). The higher insertion loss of the measured parameter S_{31}, could arise from the fact that the intrinsic resistance of the via-holes connecting the spiral to the underpass in the series inductors, plays an important role on the total DC resistance of the metallization and hence increases the measured insertion loss. The important gap between measured and simulated data of S_{31} in turn worsen the simulated amplitude imbalance (see Figure 6.30), as shown by the values reported in Table 6.5. The simulated phase imbalance within the frequency band of interest is also worse compared to the measured one (see Figure 6.30). Nonetheless, the simulated balun achieves the optimum phase imbalance at a lower frequency (i.e., 2.25 GHz).

A consequence linked to the optimistic value of the simulated transmission parameter S_{31} is that the simulated single-to-differential insertion loss, S_{ds21} (-0.64 ± 0.04 dB) is also better than the measured one (-1.02 ± 0.03 dB), as shown in Figure 6.31. On the contrary, measured values of S_{cs21} are better than -30 dB, whereas simulated values are around -21 dB.

6. 7 Summary

The measured performances exhibited by the proposed baluns targeting the ISM-band (2400-2480 MHz) can be summarized as follows : the reflection loss at the single-ended port, S_{11}, is better than -20 dB at 2.44 GHz, the amplitude and phase imbalance are 0.4-0.6 dB and less than 2°, respectively, the single-to-differential insertion loss, S_{ds21}, is comprised between -0.8 and -1.0 dB, and the single-to-common transfer function, S_{cs21}, is generally better than -30 dB. In general, these performances are comparable to those achieved by lumped-element baluns of similar type (see Table 6.1) and are slightly inferior compared to those exhibited by commercial LTCC baluns.

Based on the achieved performances, the developed lumped-element baluns are suitable for applications targeting the mentioned ISM-band with a bandwidth of 80 MHz. However, compared to commercial LTCC implementations, the proposed 6-element lumped baluns are rather narrow-band. This precludes their use in applications requiring, for example, a bandwidth of several hundreds of MHz. However, if this is the case, the bandwidth of lumped-element baluns can be extended by adopting filters sections of higher order. This specific issue has been

addressed by Kuylenstierna and Linnér [27], who demonstrated a second order lattice balun implemented with four T-filters (two low-pass sections and two high-pass sections), achieving a bandwidth of about 0.8 GHz. Furthermore, the coupled-coil transformer topology has been reported as an attractive solution for implementing compact and wide-band baluns, achieving a bandwidth of about 2 GHz [12, 14]. In the transformer topology, the coupled transmission lines are coiled into a spiral configuration, resulting in an increase of both the mutual inductance and capacitance between the coupled coils. Consequently, for the same lengths of conductor, the resonant frequencies of the spirals are significantly lower than those of straight lines.

6. 8 References

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CHAPTER 7

CONCLUSION AND OUTLOOK

A study addressing the essential issues of design, processing, simulation and characterization of RF inductors and baluns has been presented. The main theme of research concerning inductors has been focused at the improvement of the achievable performance, both from processing and design points of view. The necessary knowledge enabling the fabrication of high-performance inductors tailored for a given inductance value has been established. Optimized inductors have been successively used as building-blocks for implementing lumped-element balun circuits.

It has been pointed out that the Q-factor displayed by inductors implemented in standard CMOS processes is drastically limited by skin and proximity effect in the metallization and by various mechanisms that couple energy to the substrate. The technological constraints imposed by CMOS, such as the use of semiconducting Si substrates and finite metallization thickness, have been circumvented by recurring to micromachining processes, that tolerate the use of any kind of substrate and metal layers.

Resistive losses in the metal traces have been mitigated by providing thick metal films of Al or Ag and, from a layout perspective, by designing circular and hollow spirals. Spirals with a tapered layout have also been investigated for

reducing current crowding. On the other hand, substrate losses have been addressed by using HRS (3.5 kΩ·cm) or insulating substrates, such as Pyrex.

Al films with thickness ranging from 3 up to 8 µm have been sputter deposited at room temperature. These films have shown values of resistivity very close to the bulk metal (i.e., 2.62 µΩ·cm), for example a resistivity of 2.7 µΩ·cm has been measured on 8 µm-thick Al films. Moreover, such thick Al films have shown in-plane stress around 40 MPa. Al films have been patterned into spirals by dry-etching ICP using an anisotropic process based on Cl_2/BCl_3 chemistry. To the author's best knowledge, this is the first time that vertical patterns with aspect ratio up to 1.33 are demonstrated on 8 µm-thick Al films. The capability to achieve such high aspect ratios allows for the design of inductors with minimum track-to-track spacing. This in turn permits the maximization of the inductance per unit area through an enhanced mutual magnetic coupling.

Ag electroplating into molds of photoresist has made possible the fabrication of spirals up to 12 µm-thick. A resistivity of 1.8 µΩ·cm has been measured on such thick Ag films. This value is very close to the resistivity of the bulk metal (i.e., 1.72 µΩ·cm).

In addition to the low residual stress measured on sputtered Al films, this metal has been observed to be chemically inert when exposed to HF in vapor phase. These characteristics have been exploited for the fabrication of suspended (and potentially post-CMOS compatible) inductors. The crucial step of the process is the release of the Al spiral by selectively removing a 4 µm-thick sacrificial layer of SiO_2 using HF vapor phase etching. The developed process has been indeed very promising since sticking has not been observed on devices with medium or small footprint, i.e., with an outer diameter not exceeding 500 µm.

An empirical study of the achievable inductor performance has been conducted in order to shed light on the role played by the substrate, spiral conductivity and layout parameters. As a general trend, inductors fabricated on Pyrex achieve better performances in terms of Q-factor and self-resonance than their counterparts implemented on HRS. Particularly, peak-Q's exhibit an improvement of 30-40%, while f_{SR} raises by 1-2 GHz. This stems from the six order of magnitude lower conductivity and the halved dielectric constant of Pyrex. Another incentive to use Pyrex substrates is represented by its lower cost compared to HRS.

A Q-factor up to 50 at 4.5 GHz altogether with a self-resonance above 10 GHz have been exhibited by a 5 nH Ag inductor on Pyrex. In comparison, an inductor with identical layout fabricated with a 8 µm-thick Al spiral has shown a peak-Q of

38. Nonetheless, the better Q-factors allowed by thicker and more conductive Ag metallization are achieved at the expense of a more complicated process involving 5 steps of lithography, compared to the 3-mask process required for fabricating Al inductors. The role of the spiral thickness has been assessed by comparing Al inductors with identical layout and coil thickness ranging from 4 to 8 µm. A peak-Q of 52 and a $Q_{@2,4GHz}$ of 30 have been achieved by a 3.44 nH inductor with a 8 µm-thick spiral. These performances are considerably improved with regard to the same inductor fabricated with a 4 µm-thick spiral (peak-Q = 42, and $Q_{@2,4GHz}$ = 25). Ultimately, this justifies the use of such thick films and the more challenging dry-etching process required for the patterning of the spiral. Furthermore, measured data have emphasized that the spiral thickness has a negligible effect on the parasitic track-to-track capacitance. Tapering the spiral of the inductor has been demonstrated as an effective means for further boosting the overall performances from a layout perspective. A 8 µm-thick Al inductor on Pyrex with a tapered spiral has displayed a peak-Q of 45 for a corresponding inductance of 4.4 nH, while the corresponding reference inductor with same outer diameter and a constant track-width has shown a peak-Q of 40 and an inductance of 3.9 nH.

Suspended inductors have shown overall better peak-Q's and f_{SR} than their monolithic counterpart. This stems from the reduced parasitic capacitance due to the four times lower permittivity of air compared to SiO_2. However, in order to substantially mitigate substrate losses and to be able for example to successfully implement these suspended inductors on doped Si wafers, the air-gap separating the spiral from the substrate should be made much thicker, i.e., at least few tens of micrometers. This could be conceived by successively performing the following steps : SiO_2 deposition, via-holes opening, via-holes filling with Al, Al etching, SiO_2 deposition, SiO_2 planarization by CMP and repeating the cycle again starting with SiO_2 deposition. The proposed process would not require any extra mask.

An equivalent compact model based on frequency-independent elements has been developed for simulating the inductor behavior and extracting the relevant parameters, such as series inductance, L_s series resistance, R_s and parasitic capacitance, C_s. Measured data of inductors, regardless their geometry and material parameters, have been accurately matched all over the considered frequency range (i.e., 0.03-10 GHz).

In general, measured performances issued from RF characterization, challenge those exhibited by state-of-the-art monolithic or micromachined inductors with similar inductance values. However, the proposed planar geometry, while being rather simple to implement from a processing point of view, is also

inherently more robust than reported suspended or out-of-plane assembled 3-D architectures, can withstand violent mechanical shocks and vibrations and simplifies the packaging procedure of the final device.

Based on the various trends issued from RF characterization, a library of about 500 inductors, with inductance values ranging from 0.5 to 20 nH, has been established. Moreover, a set of general guidelines aiming at the improvement of the performances from a layout point of view has been delineated. The library constituted by inductor performances as a function of the layout parameters represents the cornerstone of the procedure for the design of inductors tailored for a given inductance value. The subsequent characterization of such tailored inductors has pointed out the achievement of inductance values falling within 4.5% of their nominal value.

EM simulation of inductors has been carried out in order to establish optimum conditions enabling an accurate matching of measured data. The knowledge acquired from this task has then enabled an efficient simulation of more complex and memory-demanding circuits, such as baluns.

As a further step of the research, lumped-element baluns targeting the ISM-band (2400-2480 MHz) have been simulated and designed by co-integrating optimized inductors with MIM capacitors. Baluns have been fabricated using the 5-mask process based on Ag electroplating. Different figures-of-merit have been adopted for evaluating the measured performances. The measured reflection loss, S_{11}, is generally better than -20 dB at 2.44 GHz. Typical values of amplitude imbalance within the frequency band of interest are 0.45-0.55 dB, whereas the phase imbalance is less than 2°. Moreover, the single-to-differential insertion loss, S_{ds21} ranges from -0.8 to -1.0 dB, and the single-to-common transfer function, S_{cs21} achieves values better than -30 dB. In general, the performances exhibited by the proposed baluns are comparable to those shown by micromachined baluns of similar type and are slightly inferior to those displayed by commercial discrete baluns implemented with LTCC technology. Although the obtained performances are suitable for applications targeting the mentioned ISM band, the proposed baluns are substantially narrow-band, meaning that their performances rapidly degrade outside the 80 MHz-passband.

7. 1 Outlook

All the fabrication steps involved in the developed processing routes occur at low temperature (T_{max} < 150°C). This makes possible the implementation of the proposed inductors directly on CMOS wafers. However, in this case, monolithic planar inductors would see their performance dramatically degraded from dissipation mechanisms linked to the semiconducting nature of Si. Ultimately, this would suppress the benefit brought by highly conducting Al or Ag spirals. A solution to make the proposed inductors post-CMOS compatible would be to fabricate them suspended over a thick air-gap, as discussed earlier. However, such a suspended architecture would raise important issues of long term mechanical reliability. An alternative solution capable of combining high-performance and robustness would be the implementation of inductors on a region of the Si wafer that has been altered in such a way to increase its resistivity. This local impedance modification could be realized either by the formation of porous Si or by proton implant. It is reported that both these techniques allow for an increase of resistivity up to 10^6-10^7 Ω·cm obtained on doped Si wafers. Furthermore, thick layers of BCB as low-K dielectric could also be used for providing an isolation between the inductor and the substrate.

Future studies of micromachined baluns should focus at further downscaling the balun footprint for reducing metal losses, at improving the overall performances, such as amplitude and phase imbalance, and at increasing the passband, for example by adopting higher order filter topologies. All these tasks can be accomplished by recurring to EM simulations.

High-performance micromachined inductors and baluns have been developed in a more general context of co-integration with other classes of RF MEMS, such as bulk acoustic wave (BAW) filters based on resonators made of piezoelectric AlN. One application than can be envisioned, is the on-chip integration of an inductor with a single BAW resonator in such a way to tune its resonant frequency and consequently extending the passband of the whole filter. On the other hand, baluns could be co-integrated with differential BAW filters present in the RF front-end of a transceiver for providing a single-ended to differential interface between different blocks of the circuit. The co-integration of baluns with BAW filters could be conceived either in monolithic or in hybrid form. In the former case, a micromachining process could be developed aiming at the fabrication of the balun above the filter level. Whereas the latter approach could be realized by recurring to flip-chip bonding.

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BIOGRAPHY

Patrick Carazzetti was born on May 7, 1976, in Locarno, Switzerland. He received the M.Sc. degree in materials science from the Swiss Federal Institute of Technology of Lausanne (EPFL), Switzerland, in March 2002. His master thesis was realized at the Ceramics Laboratory (LC), EPFL, under the direction of Prof. Paul Muralt. He dealt with the design, fabrication and characterization of surface micromachined resonators based on piezoelectric films of aluminum nitride (AlN).

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