An Asynchronous Delay Line for PAM Signal

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Synopsis

An asynchronous delay line for PAM signal having controlled delay capability is proposed. The delay line in a cascaded chain of identical memory cells. Each sample of the sequence of the input PAM signals passes or is shifted in particular cell depending on whether the succeeding cell is empty or not. A cell is composed of two memory capacitors with the peripheral control circuits. In this paper, especially, an example of the circuit for cell is shown and its several characteristics are discussed. At the end, some experimental results are given.

§ 1. Introduction

In the binary systems, some elastic memory units have been used to equalize with the different data-transmission systems having various data transfer rate. These are applicable to PAM systems by means of converting the signal to binary code, but the associated circuits to encode and decode become very complicated. Described in this paper[1] is a variable delay line dealing with PAM signal directly.

The delay line is composed of a cascaded chain of identical memory cells. It has many merits as follows.

(1) The delay time can be easily controlled by write pulse and read pulse without using any external circuits.

(2) The delay line has the ability of phase comparison.

(3) In case that one of write pulse and read pulse run over the other, the lack of signal is limited to only one. On the other hand, distortion and noise in each cell are accumulated in the output because of cascaded connection. Therefore, it is speciall ysuitable to the application requiring the memory of comparably small capacity. Some of the applications are synchronization, suppression of jitter, insertion or removal of the codes in PAM systems and so on. In the following chapters the principle and characteristics of the memory cells for the delay line will be made clear.

§ 2. Principle of memory cell

2.1 Majority decision logic circuit for PAM signal.

Fig. 1 (a) shows the composition of the
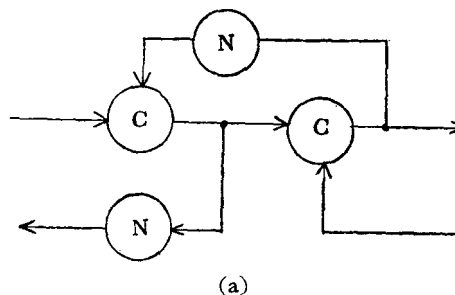
(a)

input 1	input 2	output
0	0	0
0	1	*
1	0	*
1	1	1

(b)

Mark * shows that out-put is remained unchanged.

Fig. 1 A memory cell for binary code.
  (a) Composition of cell.
  (b) Truth table.

memory cell in an asynchronous delay line for binary code and Fig. 1 (b) shows the truth table of the majority decision logic circuit used in the cell (C_1 element). Majority decision

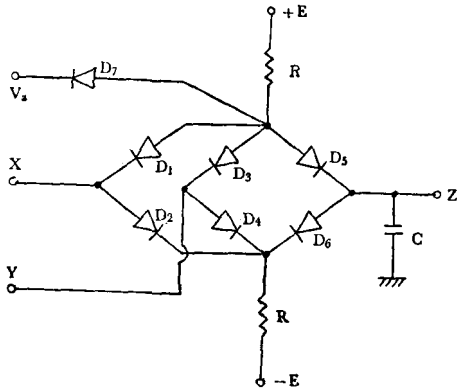logic circuit for PAM signal (C_m element) shown in Fig. 2 has the same logical function as C_1

Fig. 2 Basic majority decision logic circuit.

element. The input control signals X and Y take V_s or E ($V_1 > V_s$) and the input signal V_a varies the value between V_s and V_1. In the succeeding description, V_s and E correspond logically to 0 and 1 respectively. When X = Y = V_s the capacitor C is discharged to V_s through the transmission gate and Z is fixed to V_s. When one of X and Y becomes 1, Z is still remained to V_s, because the diode D_6 and D_1 or D_3 are cut off. If both X and Y becomes 1, charging of the capacitor C starts toward E and stops when Z coincides with the input PAM signal. Here, the storaged signal is not discharged, untill both X and Y becomes 0 (V_s) again. The signal X is synchronized with the leading edge of the input PAM signal. Accordingly, regarding X, Y and Z as the input 1, input 2 and out-put in the truth table of Fig. 1 (b) respectively, it is found that C_m element has the same logical function as C_1 element. The maximum time t_{rm} and t_{fm} required to charge and discharge PAM signal are given as Eq. (1).

$$t_{rm} = CRln\frac{E - V_s}{E - V_1} \\ t_{rf} = CRln\frac{E + V_s}{E + V_1} \Bigg\} \tag{1}$$

2.2 Improvement of input impedance of memory cell circuit

In the circuit of Fig. 2, the input impedance is determined by the current flowing through the diodes. In case of cascaded connection of

these cells, the input impedance of each cell becomes overload for the previous stage. Fig. 3
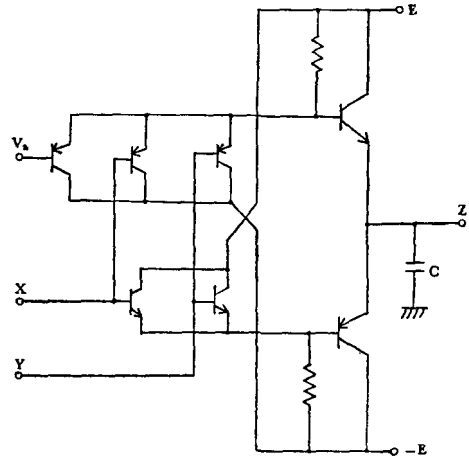

Fig. 3 Improved C_m element.

shows an improved circuit (C_m element) using transistors in place of diodes. In this circuit, the impedance is increased to β times without the sacrifice of the time constants to charge and discharge memory capacitor C.

2.3 Buffer amplifier

It is necessary to reduce the above-mentioned time constants for speeding up. One of the ways to achieve this purpose is to reduce the capacitance of the capacitor C and add a buffer amplifier with unity gain at the output. The simplest buffer amplifier using complimentary transistor is shown in Fig. 4. If α s of
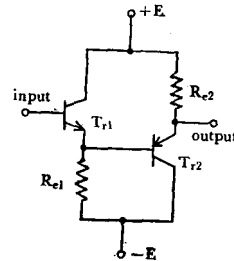

Fig. 4 Basic buffer amplifier.

both transistors are equal, the input impedance R_i is given approximately in Eq. (2).

$$R_i = \beta \frac{R_{e1} R_{e2}}{R_{e1} + R_{e2}} \tag{2}$$

However, in case of small capacitance, the discharge current through the impedance R_i
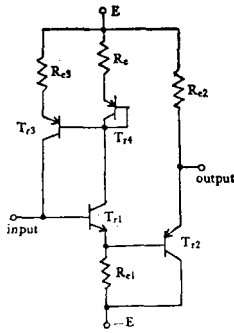
Fig. 5 Improved buffer amplifier.

can not be yet neglected. Fig. 5 shows an improved buffer amplifier, compensating the current flowing through R_i with the current flowing through transistor T_{r3}. T_{r4} is inserted to compensate the voltage between the base and the emitter in T_{r3} varied with the temperature. Fig. 6 shows the equivalent circuit.
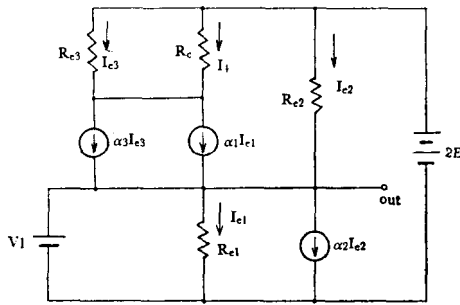

Fig. 6 Equivalent circuit of improved buffer amplifier.

The input impedance R_i' is shown in Eq. (3).

$$R_i' = \frac{1 - \dfrac{1}{\alpha_1}\left(1 + \dfrac{R_{e3}}{R_c}\right)}{\dfrac{1}{R_{e1}}\left\{1 - \dfrac{1-\alpha_1}{\alpha_3}\left(1 + \dfrac{R_{e3}}{R_c}\right)\right\} + \dfrac{1}{R_{e2}}\left\{1 - \alpha_2 \right.}$$

$$\left. - \dfrac{1-\alpha_2}{\alpha_3}\left(1 + \dfrac{R_{e3}}{R_c}\right)\right\} \tag{3}$$

Selecting the ratio R_{e3}/R_c so that the denominator of the equation above may be zero, R_i' becomes infinity. In the practical circuit, it is difficult to attain $R_i' = \infty$. But the larger input impedaece than that of the circuit shown in Fig. 4 can be easily performed.

2.4 Circuit of cell

One half of a cell (half cell) is composed of a C_m element, a buffer amplifier, a delay circiut and a signal detecting circuit. Fig. 7 shows the circuit of a memory cell for PAM signal. The PAM signal exists between V_0 and $V_1(>V_0)$, and in the absence of PAM signal, the input signal V_a is V_s. The signal detecting circuit, of which the threshold value is put between V_s and V_0, applies the binary control signal C_{out} and the output signal of the buffer amplifier S_{out} to the succeeding half cell. The control signal C_{out} takes V_s or E depending on whether PAM signal is memoried in the capacitor C or not. At the same time, the complement R_{out} of S_{out} is feed-backed to the
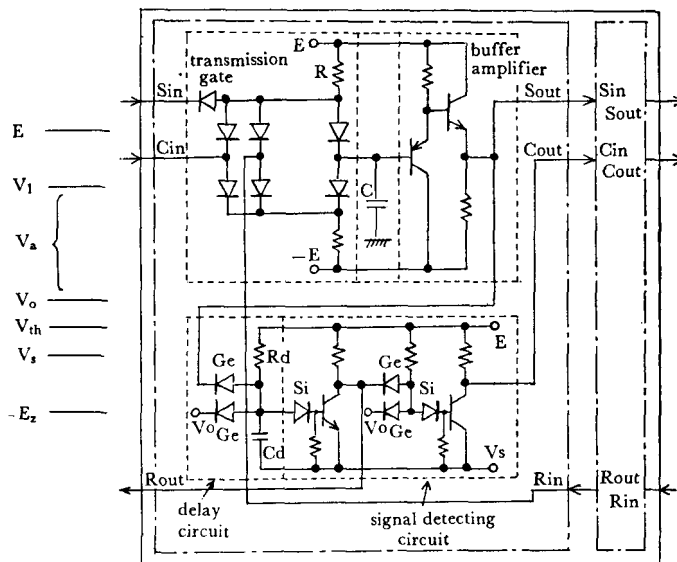

Fig. 7 Circuit of memory cell for PAM signal.

previous half cell as occupancy signal. Accordingly, the occupancy signal takes V_s or E depending on whether PAM signal is memoried in the half cell or not.   Here each signal level is set as above mentioned. When both R_{in} and C_{in} are E, the PAM signal at the input is stored in the capacitor C. The delay circuit ensures perfect memorying of the signal by delaying the output of the occupancy signal. A cell is composed of cascaded two half cells. When both cells are empty and the occupancy signal at the out put side is V_s, the PAM sign-

al is stored in the capacitor at the input side. At the same time the occupancy signal inhibits to transfer PAM signal to the cell at the output side. Becoming the occupancy signal E, the memoried signal at the input side is shifted to the cell at the out put side and the capacitor at the input side is discharged.   Fig. 8 shows the time chart of the signal transfer.   It is found that the memory cell has the same logical function as binary memory cell in Fig. 1.

§ 3. A variable delay line for PAM signal.

A variable delay line for PAM signal is composed of a cascaded chain of identical memory cells as shown in Fig. 9. Write pulse is given as the control signal C_{in} at input side and read pulse R_{in} at the out-put side seperately.   The sequence of sample hold signal are memoried or passed through, depending on whether the succeeding cell is empty or not. After reading of one sample hold signal, each sample hold value memoried in each cell is shifted toward the succeeding cell one by one. Delay time of PAM signal at the output equals to the time difference between write and read
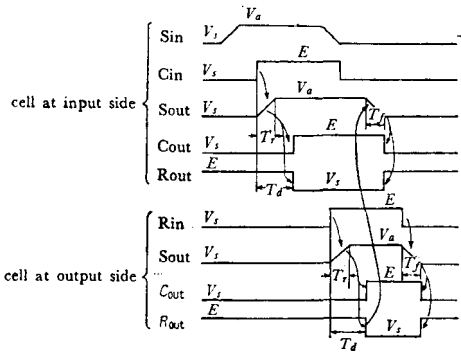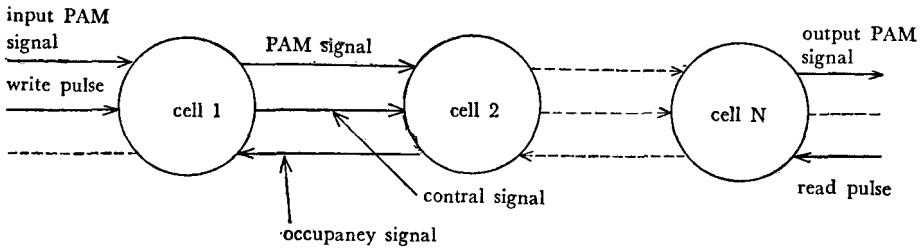

Fig. 8   Time chart of signal transmission.

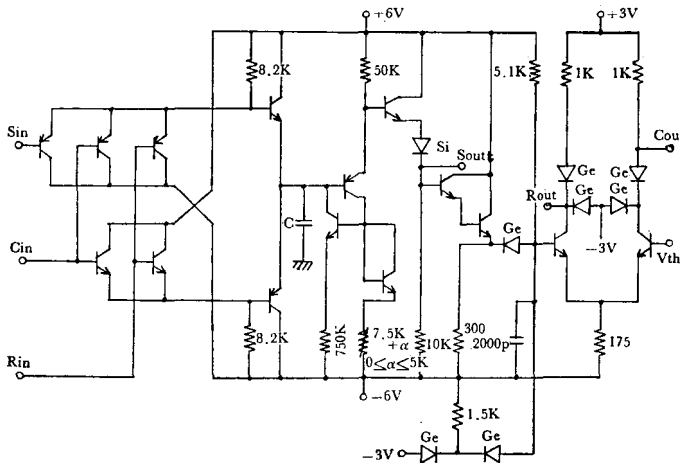Fig. 9   Composition of delay line for PAM signal.

Fig. 10   Test circuit of half cell.

pulses.

§ 4.   Test results and their discussion

4.1 Test circuit

Fig. 10 shows the circuit of the half cell used for test. In the transmission gate, silicon transistors are adopted for decreasing the power of the input PAM signal and the control signals. As a buffer amplifier, the emitter follower with high input impedence is used.   A

silicon diode is inserted to compensate the level shift of PAM signal passing through the transmission gate.

4.2 The characteristics of C_m element.

Fig. 11 shows the out-put waveforms to the various input PAM signals obtained in the experiment. In Fig. 12 the relationships
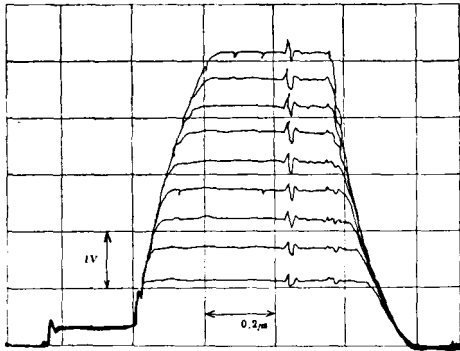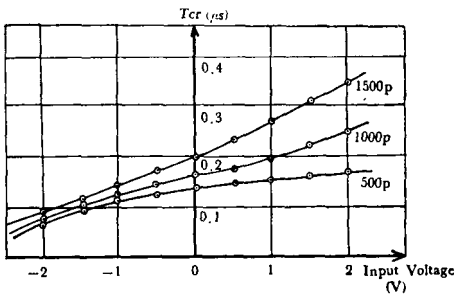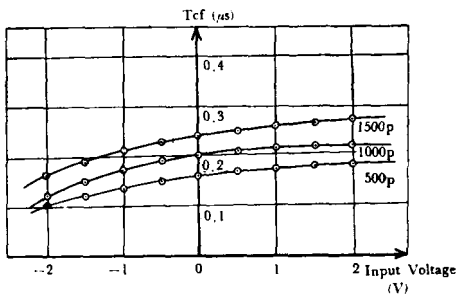

Fig. 11 Output waveforms to various PAM signal.

(a)

(b)

Fig. 12 Variation t_{cr} and t_{cf} to various input levels of PAM signal.
(a) t_{cr} (b) t_{cf}

between t_{cr} or t_{cf} and input level are shown, taking the capacitance of the memory capacitor C as a parameter. Both t_{cr} and t_{cf} increase with the capacitance of the capacitor C. The

difference of t_{cr} and t_{cf} is produced because of asymmetry of the zero level. The delay line containing the above-mentioned memory cells will be able to utilize for dealing with PAM signal in audio frequency.

4.3 Discussion of linearity.

One of the important character of the delay line is that the cell has the satisfactory linearity of the output to the input in the cell. Fig. 13 (a) and (b) show the output wave forms of the
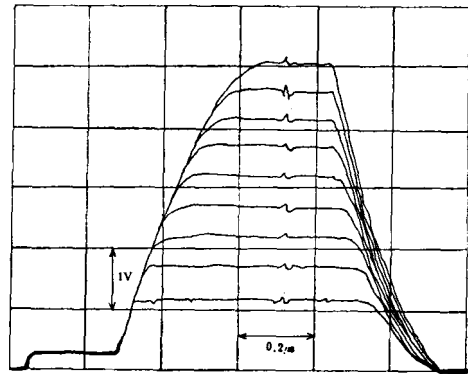

(a)
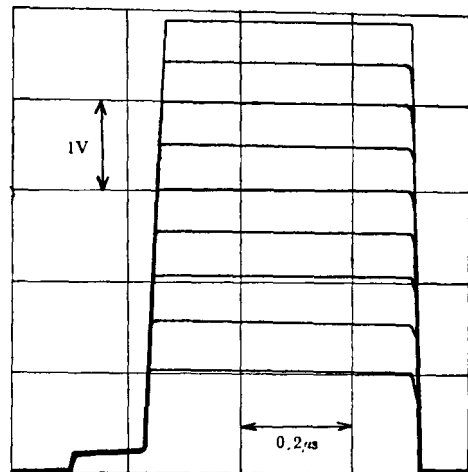
(b)

Fig. 13 Out-put waveforms.
(a) Waveform at short holding time.
(b) Waveform at the long holding time.

memory cell, the former is the wave-forms to be measured at the near of the short limit of the holding time and the latter is at the area of the long holding time. The results of the linearity test are shown in Fig. 14 (a) and (b). In case of the short holding time, good linearity with-in 3% is obtained. In case of the

Output Voltage (Volt)

(a)

Output Voltage (Volt)
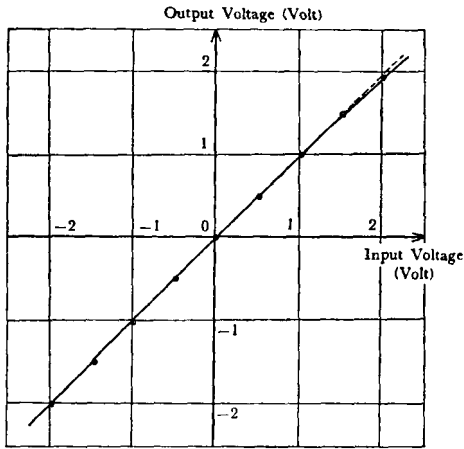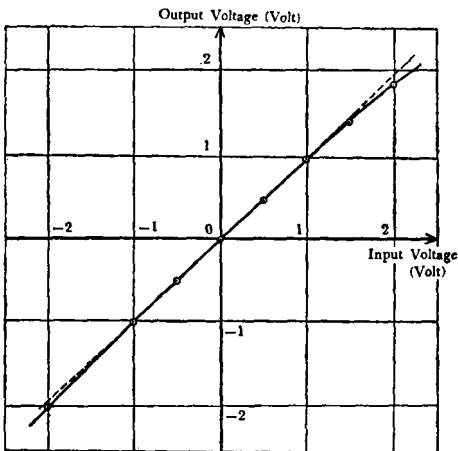
(b)

Fig. 14   Linearity
(a)   In case of holding time at lower limit.
(b)   In case of long holding time.

long holding time, the linearity is lightly inferior to the short holding time, because the charge of the capacitor is discharged through the input impedance of the buffer amplifier.

§ 5. Conclusion

In this paper, the composition, the principle and the experimental results of the memory cell in the delay line for PAM signal have been described.   From these results, the delay line composed of the above-mentioned memory cells shows our desired ability.   Especially, such a degree of the response will be sufficient to realize an elastic memory unit for the PAM signal at audio frequency.   By the more improvement of the linearity in the cell, more accurate delay line may be achieved.

The authers are grateful for the helps received from Sanyō Broad-casting Scientific Foundation.

References

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