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Hardware Design of Digital System with Remote-Diagnostic Capability

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Synopsis

In this paper, a hardware design of digital systems with remote-diagnostic capability is presented. We consider a method for testing a system T_1 on a module basis with a remotely installed systems T_2. In the testing mode, we set up a system (T_1-m,m') such that a module m of T_1 is replaced by an adapter A_1 connected to other adapter A_2 through a telephone line and the corresponding module m' of T_2 is connected to A_2. If the system (T_1-m,m') can simulate T_1 in the absence of any faluts, then it can test m' under a self test program. The main subject of this paper is to study the conditions of the system to be testable in the above sense.

At first, the remote diagnostic network based on the system in this paper, restrictions to the system configuration required to perform such a diagnosis and the operation of the diagnostic system are described. The second, the module structure to make above simulation possible is considered, representing the system configuration graphically. Finally, an example of the adapter is shown and the time consumed to diagnose is discussed.

One of our results is that a sufficiently large class of synchronous digital systems with few minor conventions is testable.

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1. Introduction

Recently, researches on the remote diagnosis for large-scale computers through a telephone line have begun in many laboratories, aiming at the establishment of the reliable and inexpensive maintenance network. Some maintenance networks have already been put into practice[1]. However, few reports in details about the remote diagnosis have been published.

On the other hand, we have considered[2] the possibility of the remote operation of two sub-systems closely coupled through a telephone line, aiming at the establishment of a convenient maintenance network for small-scale computers. It is assumed that these sub-systems are obtained by separating a stand alone system into two parts. An adapter is installed between each sub-system and the telephone line. The operation of the stand alone synchronous system only composed of combinational networks and clocked flip-flops can be simulated by that of two syb-systems coupled through the telephone line, with a few restrictions to the system configuration.

In this paper, we will consider the hardware design of a digital system with remote-diagnostic capability. Our remote diagnosis is performed on a module basis. A diagnostic system of the same type as user's ones is installed in a maintenance center. If a trouble happens in a user's system, modules are tested in turn by the diagnostic system as follows.

First, a module m_d is removed from the diagnostic system and the same module m_u in the user's system as m_d is connected to the diagnostic system in place of m_d through the telephone line and adapters. The diagnostic system is operated in the remote operation mode using m_u under a self test program. If the self test program detects any fault, m_u is concluded as a faulty module.

In chapter 2, an approach to the maintenance network based on above principle is described, and assumptions in the system configuration and the outline of the remote mode operation are discussed. In chapter 3, the module structure required for realization of this diagnosis is summarized. In chapter 4, we consider the structure of adapters.

2. Remote Diagnosis

2.1 Maintenance Network

In this paper, a digital system M is considered to be composed of modules m_{d1}, m_{d2}..... m_{dk} inserted into connectors on the back-wiring board. Then the system M will be denoted as $M=[m_{d1}, m_{d2}, \cdots m_{dk}]$.

Fault diagnosis means only to find out faulty modules in M. We are not concerned with internal components in the module, but the module's terminal behavior. Also, it is assumed for simplicity that there are no faults in the back-wiring board.

When a trouble happens in a user's stand alone system, the following procedure is frequently used to find out faulty modules. Suspected modules are replaced by new ones in turn and then the faulty module may be found out by running a test program. This is a simple method even a non-professional can use. The remote diagnosis in this paper is performed by extending above method to two sub-systems coupled through a telephone line. The faulty module may be found out, within capabilities of the test program, with a small amount of additional hardware, with rather a simple self test program and with a simple procedure.

A remote mode operation configuration ($M-m_d$, A_1, A_2, m_u) is depicted in Fig.1. A module m_d in M is replaced by an adapter A_1 and m_u is connected into another adapter A_2 which is linked

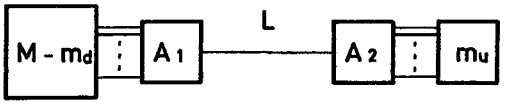


Fig.1 Remote mode operation configuration

to the adapter A_1 through a telephone line L. Adapters A_1 and A_2 can be the same except that A_1 uses a module extender with male connectors in both edges. If the configuration ($M-m_d$, A_1, A_2, m_u) can simulate M, then the operation of the configuration is called a remote mode operation (RM operation, for short), while the operation of the stand alone system M is denoted as SM operation (stand alone mode operation).

One of the main concerns in this study is to investigate the conditions of the module structure of the system M and the design of the adapter for the RM operation.

The remote diagnosis is performed as follows. Suppose that there are many users having stand alone systems M_j (j=1,2,...,p) and a maintenance center having a system M_t of the same type as M_j (see Fig.2). Usually, M_j is utilized independently according to each user's demand and M_t is always maintained to be ready for the maintenance of M_j. If any trouble happens in M_j, the user of M_j telephones to the engineer at the center. At first, the adapter A_2 will be tested in the configuration (—,A_1,A_2,—) if necessary. This is a simple test. In the maintenance center, a professional engineer estimates a faulty module m_{ui} and checks it by the following procedure.

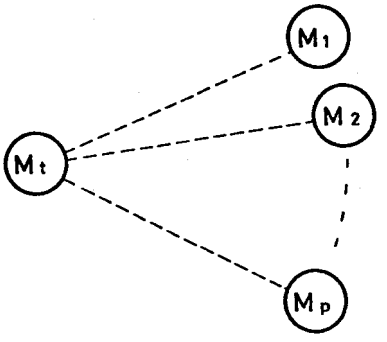


Fig.2 Maintenance network

a) he orders the user to remove m_{ui} from M_j, to plug it into A_2 and to connect A_2 to L.

b) he removes the module m_{di} of the same type as m_{ui} from M_t, plugs A_1 into M_t-m_{di} instead of m_{ui} and connects A_1 to L.

c) A system (M_t-m_{di}, A_1, A_2, m_{ui}) is operated (RM operation) under a test program. If there is any trouble in RM operation, m_{ui} can be concluded as a faulty module.

d) If no fault is detected in the step (c), then steps (a), (b) and (c) should be applied to other modules one by one, until it is detected.

By procedures (a) to (d), faulty modules may be identified. In this method, it is required for the test program of m_{ui} to check only if (M_t-m_{di}, A_1, A_2, m_{ui}) works properly or not, independently of m_{ui}, because M_t, A_1 and A_2 are assured in advance. This leads sometimes to a simpler test program compared to those programs which must take into account multiple faulty modules. This method may be good for

those systems in which there is no good correspondence between modules and testable logical functions. As a special case, if it has been ascertained that M(SM operation) has not worked correctly against the specific instruction, this instruction may be used as a temporal and convenient test program.

This method of diagnosis may be applicable to the maintenance network as shown in Fig.2. If more reliable diagnosis is required, two kinds of the RM operation can be used for the remote diagnosis as shown in Fig.3(cross diagnosis). In this case, especially, the presence of faults in M_j-m_{ui} can be also checked. Moreover, if necessary, the remote diagnosis can be performed between two users having the maintenance capability.

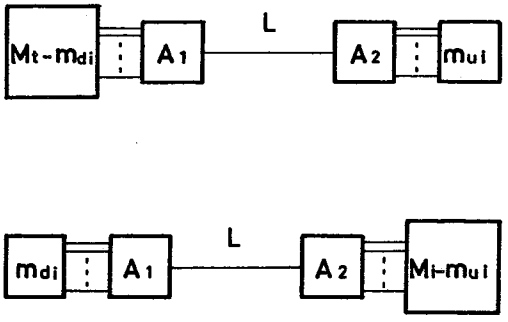


Fig.3 Two kinds of RM operation

2.2 System Configuration and Remote Mode Operation

The previous discussion implies that realization of the remote diagnosis requires to design the system capable of not only the SM operation but also the RM operation. It may be difficult however to consider the design method for general systems systematically, because the speed in the RM operation becomes lower than that in the SM operation and therefore additional design conditions are required beyond those in the SM operation. In this paper, to simplify considerations, a simple system M is assumed as follows.

(A1) M is a synchronous system, operating with a single phase clock pulse (hereinafter refered to as cp).

(A2) M is composed of only combinational logic circuits and flip-flops. These flip-flops act synchronizing with the cp and independently of its period. It means that only stable logical values at the outputs of the combinational logic circuits contribute to decide the next state of the system.

(A3) Components manufactured by any kind of techniques may be used

in M. For example, any one of TTL, NMOS and CMOS will do. Any scale of integrations in components (from discrete components to LSIs) may be also permitted. Especially, in LSI or MSI, if the assumptions (A1) and (A2) are satisfied only in input-output characteristics, internal configurations are out of the question.

To make both SM operation and RM operation possible, additional assumptions are required for the design of M as shown in items (A4) and (A5). These are assumed under the premise that the RM operation is performed by only transmissions of logical values between M-m_{di} and m_{ui}.

(A4) M is a modular system in which modules are plugged into the back-wiring board. Signals appeared on terminals of the back-wiring board are not analog ones but digital ones. This assumption shows that informations transmitted through L should be logical values.

(A5) The clock pulse generator (CPG, for short) should be externally disabled and in each module an input terminal should be prepared for this control. The control signal may be applied from the adapter to suspend CPG.

If M is designed to satisfy all the assumptions A1 to A5 and adapters are realized suitably, the RM operation can be performed by repeating the following two steps.

(Step 1) Logical values on the output terminals from M-m_{di} to m_{ui} and vice versa are transmitted to opposite sides through the telephone line and are applied to corresponding input terminals. Then, the adapter in each side compares logical values before and after the transmission in every output terminal. If these logical values do not coincide respectively, above process is repeated until they coincide. In this while, CPG in M is disabled through the input terminal explained in A5 and the application of cp from the adapters A_1 and A_2 is suspended.

(Step 2) One cp is applied to both M-m_{di} and m_{ui} respectively, after the release of the suspension of cp. In the side in which CPG is installed (the CPG is disabled), the cp is applied directly by the adapter, and in another side, the cp is applied from the adapter based on the command through the telephone line.

In the next chapter, the module structure of the system M will

be considered in detail, in order to make the RM operation possible.

3. Module Structure

3.1 Graphical Representation of the System

Fig.4(a) shows a simple example of a system M composed of two modules m_1 and m_2.

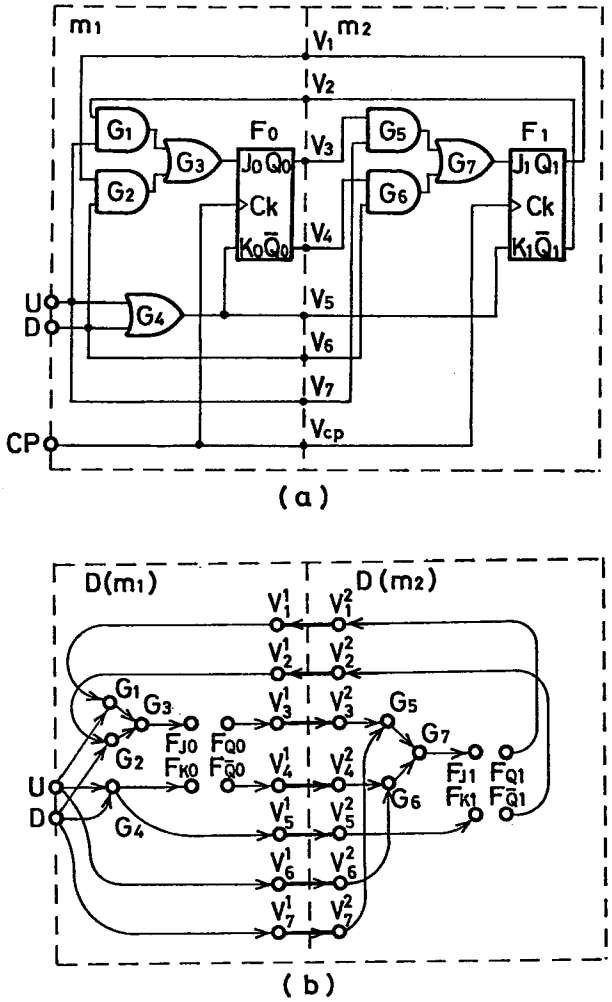


Fig.4 A simple example of system M

The points $V_1 \sim V_7$ and V_{cp} on the boundary between m_1 and m_2 correspond to connections through the back-wiring board. These points V_i (i=1,2,....7) are represented in Fig.4(b) as pairs of nodes V_i^1, V_i^2 connected by a thick edge with an arrow indicating the direction of information flow. Especially V_i^1 and V_i^2 correspond to terminals connecting m_1 and m_2 through the back-wiring board. In the RM

operation, information flows on these edges are accomplished by adapters and the telephone line. Flip-flops are represented in the graph by nodes representing input/output terminals and gates are also represented by nodes. The wiring between any two of flip-flops, gates and points V'_is is represented in the graph by a directed edge.

This graph shows information flows clearly during the time when outputs of all the flip-flops are kept invariable. In other words, it shows the situation when outputs of all the flip-flops are settled after the cp being disabled. Thus, the cp line is not depicted in Fig.4(b).

All the systems satisfying (A1) to (A5) can be represented by the graph as shown in Fig.4(b). Such a graph can be drawn by considering M equivalently to be composed of flip-flops and gates only.

If there is such a wired connection as that of gates with open collectors or tristate buffers, it may be represented in the graph by a node corresponding to the imaginary gate. If there is any bidirectional wiring, it is represented by a directed edge with bidirectional arrows. Power source lines, earth lines and clock pulse lines are out of discussions. Such graphs corresponding to M, $M-m_{di}$ and m_{ui} are denoted by D(M), D(M-m) and D(m) respectively.

Then, the following assumptions (A6) and (A7) may be set up with minor restrictions to practical cases.

(A6) Any one of gates and flip-flops are not separated into both sides of $M-m_{di}$ and m_{ui}.

(A7) There is no closed loop in D(M).

Next, the separability S(M,m) of $M-m_{di}$ and m_{ui} is defined as follows.

(D1) S_M is the maximum value of S_ℓ for every directed paths in D(M), where S_ℓ is the number of thick arrows existing in a directed path ℓ in D(M). This separability S(M,m) is well-defined by the assumption A7.

In this definition, the directed path is assumed to pass through each bidirectional edge once at most. This is based on the fact that the direction of the signal flow on a bidirectional wiring during every period of the cp becomes unidirectional.

3.2 Possibility of RM Operation

In the SM operation, logical values of inputs in each combinational circuit are propagated to its outputs through gates. Such actions are shown on D(M) as directed paths from initial nodes to terminal nodes. In order to perform the RM operation, it is necessary

to able to trace from initial nodes to terminal nodes on D(M-m) and D(m) along the same directed paths as in D(M) and in the same sequences as in D(M).

In general, D(M) consists of some weakly connected components. When D(M) is utilized to discuss the possibility of the RM operation, the number of these components may be reduced to one without loss of generality.

If there is not any wired connection in the original combinational circuit contained in M, it is possible without fail to trace from initial nodes to terminal nodes on D(M-m) and D(m) along the same paths as in D(M) and in the same sequences as in D(M). Because directions of thick arrows are fixed. That is, the RM operation is possible regardless of the way separated into modules. The maximum value of the number of times to transmit the logical values required to perform the RM operation in one period of cp is equal to S(M,m). The separability $S(M,m_2)$ of the example in Fig.4 is 1.

If there are some wired connections in the original combinational circuit, the graph is classified into two types according to whether any one of them is separated into D(M-m) and D(m) or not. If it is not separated, the RM operation is possible as above. If it is separated, the graph is classified into two sub-classes. One is the sub-class in which any node of wired connections is not divided and the other is the sub-class in which at least one of them is divided into two nodes.

An example is shown in Fig.5. In the former sub-class (see Fig. 5(b)), the number of edges relating to the wired connection in D(M-m) and D(m) is 3, while the RM operation is possible as above because directions of directed edges are always fixed. In the latter sub-class (see Fig.5(c)), the number of edges is 1, while it is required to perform the RM operation to determine the direction of the directed edge with bidirectional arrows (the transmission of logical values) by every cp. The direction is determined by adapters A_1 and A_2. The maximum value of the number of times to transmit logical values in one period of cp is also equal to S(M,m) in each case.

As results of above considerations, it has been shown that the RM operation is possible with conditions A1∿A7 only, as far as A_1 and A_2 have proper functions.

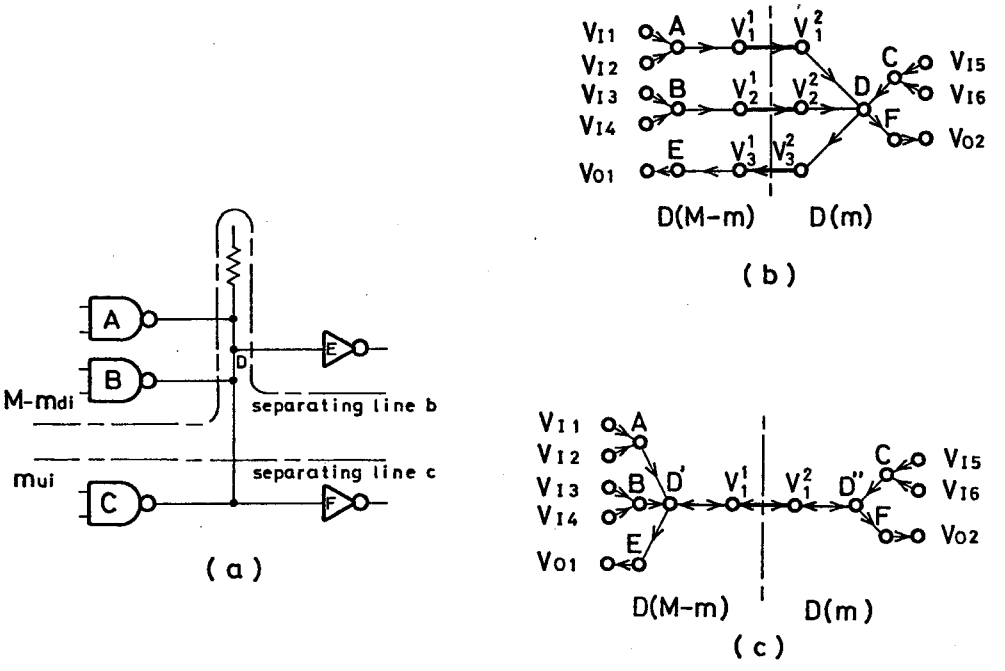


Fig.5 Separation of a wired connection

3.3 Relaxation of Restriction

All flip-flops in the system discussed in the previous section act perfectly synchronizing with the cp. They will be called synchronous flip-flops. However, in actual systems, those flip-flops are frequently utilized, which are not synchronized with the cp perfectly. For example, some flip-flops are enabled with some time-delay after the cp is applied. They are called non-synchronous flip-flops.

Assume that the system is allowed to be composed of such flip-flops and their control circuits as described below, in addition to assumptions (A1) to (A7).

(A8) Non-synchronous flip-flops may be operated synchronizing with signals delayed from the application time of the cp. Such flip-flops have not always terminals prepared for the cp. Above signals are given to flip-flops through various kinds of control circuits. Some of logical values at outputs of flip-flops fixed logical values and the clock pulse

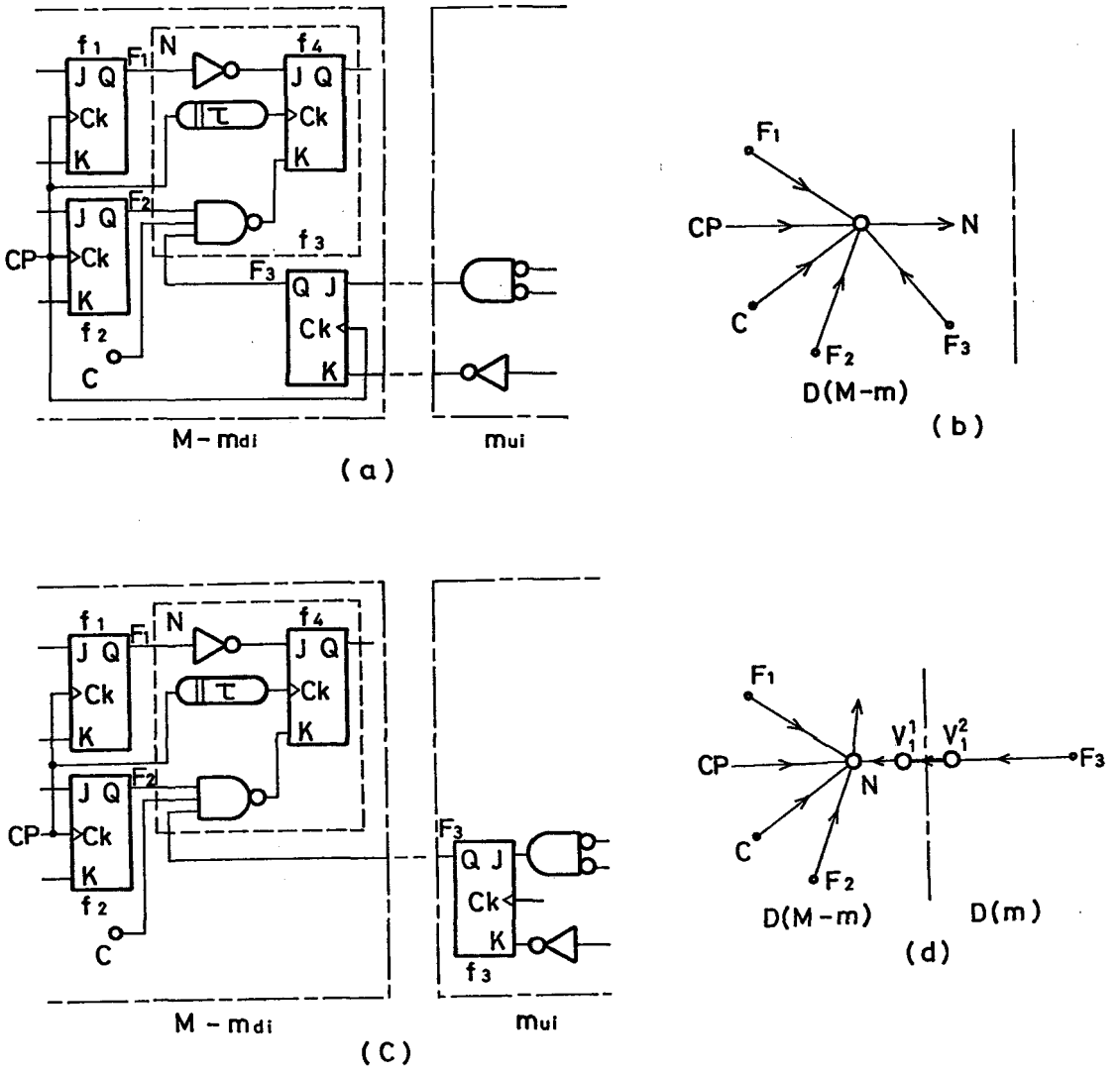
may be applied to input terminals of these control circuits. If control circuits are designed to make the SM operation possible, there are no restrictions in them except non existence of any memory element. Such a control circuit is hereinafter denoted briefly as an ICC (input control circuit). For example, the output of a monostable multivibrator or a non-synchronous flip-flop may be connected to the input of another non-synchronous flip-flop.

(A9) If the output of a non-synchronous flip-flop is connected to some of synchronous flip-flops directly or through various kinds of circuits except memory elements, logical values at inputs of these synchronous flip-flops should be settled before the application time of the next cp.

In this section, the system defined as above is again denoted as M. Non-synchronous flip-flops and their ICC's are denoted as $N_i (i=1,2,...q)$. The number of $N'_i s$ may be assumed to one (N) without loss of generality.

N is represented by a node in the graph. Let F denote a set of nodes correspond to outputs of synchronous flip-flops with edges directly leading to N and let C denote a set of nodes correspond to fixed logical values with edges directly leading to N. When M is separated into $M-m_{di}$ and m_{ui}, if all of N, C and F exist in the same side, results of discussions in the previous section are applicable. That is, the RM operation is possible. If they are separated, it is not always possible. Its possibility depends on the configuration of N and the way of the separation.

Let us show an example (see Fig.6). In case of the SM operation, the logical value at the input terminal k of the flip-flop f_4 will settle to a steady state, delayed by the propagation delay time τ after the application of the cp. If the circuit is separated as shown in Fig.6(a), N, C and F exist in $M-m_{di}$ side (Fig.6(b)), so that the RM operation is possible. If it is separated as shown in Fig.6 (c), N, C and F do not exist in the same side (Fig.6(d)), so that the RM operation is impossible. Because the logical value of the input terminal k of f_4 will not settle before the signal is applied to the terminal ck, that is, the operation may differ from the RM operation.



note : the circuit encircled by broken lines shows N.

Fig.6 Separation of an asynchronous circuit

4. Structure of Adapters and Speed in RM Operation

Some functions of adapters have been described locally. In this chapter, their whole functions are summarized and a design of the

adapter is explained. Finally, the speed in the RM operation is briefly discussed.

4.1 Functions of Adapters

The repetition rate of the cp in the RM operation decreases much more than in the SM operation, because the transmission rate of logical values between M-m_{di} and m_{ui} is restricted by the narrow band width of the telephone line. It is therefore basically required for adapters to control the repetition rate of the cp. In each module, an input terminal described in 2.2 (A5) is prepared for this control. When logical values on each pair of terminals (one for input, the other for output) agrees respectively, adapters in both sides of M-m_{di} and m_{ui} apply one cp through the input terminal in the module.

Some logical values on output terminals in M-m_{di} and m_{ui} may change after the application of the cp. These values are transmitted to corresponding input terminals in M-m_{di} and m_{ui} respectively by adapters. This procedure is repeated until each pair of logical values mentioned above agree respectively. Then, another cp is applied again to M-m_{di} and m_{ui}.

If there is any bidirectional line as shown in Fig.5(c), it is necessary for adapters to determine the direction to which the logical value is transmitted. In this paper, wired connections of open collectors and tristate buffers are taken into account as bidirectional lines.

In case of open collectors, if two logical values in M-m_{di} side and m_{ui} side are different, the transmission of the logical value should be directed from ON transistor side to OFF transistor side, otherwise the transmission is not necessary.

In case of tristate buffers, if either of two terminals coupled through the telephone line is at high impedance state, the transmission of the logical value should be directed from the side not at high impedance state to the other. If both are at high impedance state, the transmission is not necessary. If none of them is at high impedance state, the transmission should not be performed, because if logical values in M-m_{di} side and m_{ui} side are different, some tristate buffers may be burnt out. This case (a tristate buffer is ON and the other is OFF) can never occur in the normal SM operation, but this case could occur only on the way of the logical-value transmission phase in the RM operation. Therefore, the policy not to transmit the logical value of tristate buffers in that case

is safe and will not disturb the RM operation. The high impedance state is detected by I/O DTR (I/O detecter)[3].

Similar problems may arise in case that control circuits of tristate buffers in the wired connection are separated into M-m_{di} and m_{ui}. In this case, it is difficult to find out the suitable method to protect them, except the method separating M so that such conditions never occur.

4.2 A Design of Adapter

Fig.7 shows an example of the configuration of the adapter. Logical values on output terminals of M-m_{di}(m_{ui}) are read by μP (micro processor) and transmitted to m_{ui}(M-m_{di}) side in a serial form through SPC (serial-parallel converter) and MOD (modem) by μP. Next, logical values transmitted from m_{ui}(M-m_{di}) as the response to above transmission are read by μP through MOD and SPC, and compared with corresponding ones in REG(register) respectively. REG stores logical values given to M-m_{di}(m_{ui}). If any pair of logical values do not agree respectively, contents of REG are replaced by logical values transmitted from m_{ui}(M-m_{di}) and then above procedure is repeated until they agree. When they agree, μP instructs the removal of the suspension of the cp to CC(clock controller) in M-m_{di} (m_{ui}) side and the application of the cp to the adapter on the opposite side. CPG in CC controls so that it may be suspended again after the application of the cp. Programs for μP are stored in ROM.

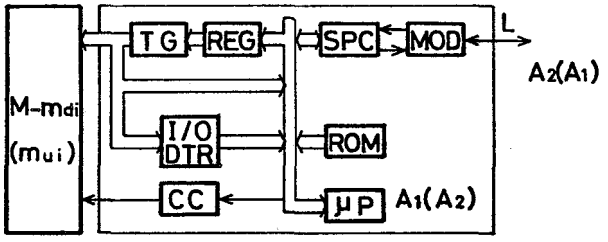


Fig.7 A configuration of adapter

Directions of transmissions on bidirectional lines between M-m_{di} and m_{ui} are determined as follows. In case of open collectors, TG(transmission gate) is realized by the same component as open collectors as shown in Fig.8. When the logical value on the terminal V_1(V_2) is read by μP, TG is closed under the control of μP through a

one bit flag R_1. The logical value should be transmitted from the low level side to the high level side, only when two logical values in M-m_{di} side and m_{ui} side are different.

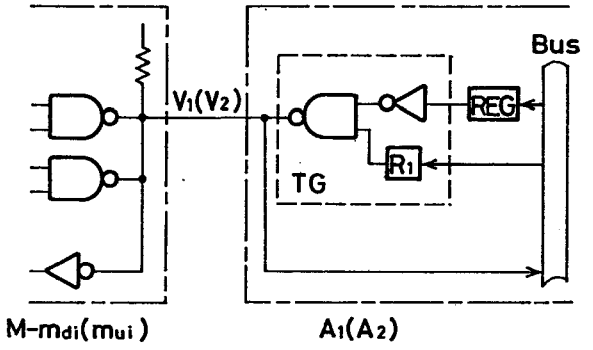


Fig.8 Transmission gate for open collector

In case of tristate buffers, TG and I/O DTR (I/O detecter) [3] can be realized as shown in Fig.9. High impedance state is detected by the degree of the change in the voltage on $V_1(V_2)$ before and after pulling up or pulling down of $V_1(V_2)$ through analog switches S_1, S_2. Pulling up or pulling down is instructed through a flag R_2 or R_3 by μP, respectively. All this while, TG is closed. The change

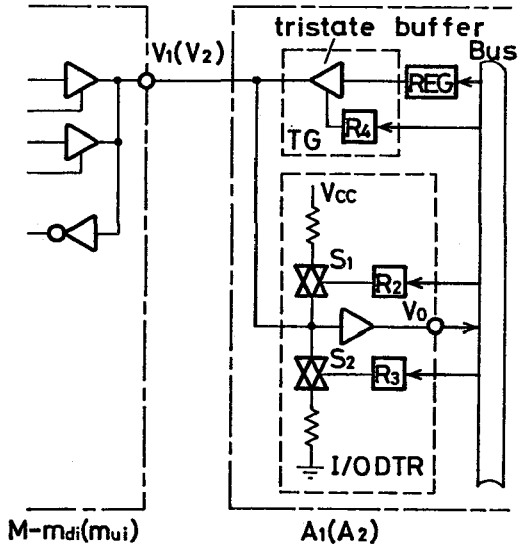


Fig.9 I/O detector for tristate buffer

in voltage is analyzed by μP. If the terminal $V_1(V_2)$ is at high impedance state, the logical value on the terminal V_0 will change from high to low or vice versa. If $V_1(V_2)$ is not at high impedance state, it will not change. The logical value on the terminal not at high impedance state should be transmitted to the terminal at high impedance state, only when either of two terminals is at high imperance state.

4.3 Speed in the RM Operation

One of the important problems in the RM operation is the decrease in the speed for the remote test. Here, principal parameters influencing on the speed in the RM operation are discussed.

The lowering facter D of the speed in the RM operation may be defined by the following formula.

$$D = \frac{\sum_{i=0}^{n} \sum_{j=1}^{S(M,m)} (A_{ij}+B_{ij})}{nT}$$

T : the period of the cp in the SM operation.

n : the number of cp's required to execute the test program.

A_{ij} : the operation time of the adapter at the jth transmission of logical values after the application of the ith cp.

B_{ij} : the transmission time on the telephone line at the jth transmission of logical values after the application of the ith cp.

T is determined by the specification of M at the SM operation and n is determined by the test program used. S(M,m), A_{ij} and B_{ij} are selectable in the design time. M should be separated into modules so that S(M,m) may be minimized. Then, in most cases, the number of times to transmit logical values will be minimized without sacrifices of other parameters.

Usually, A_{ij} is much smaller than B_{ij}, because the processing speed of the micro processor is much higher than the transmission rate of the telephone line. Thus, B_{ij} is another parameter selectable to decrease D effectively.

B_{ij} is equal to the product of the time consumed to transmit a

bit of signal on the telephone line and the number of bits to be transmitted. In order to decrease D, the number of bits per transmission should be decreased. Here, not only logical values of output terminals in the module, but also the command for the application of cp, start and stop bits of the transmission etc. are transmitted on the telephone line. According to our estimation, it will be most effective to transmit all signals in a predetermined order. If the small number of logical values change after every transmission, it will be more effective to transmit only terminal numbers on which logical values have changed.

5. Conclusion

We have considered the hardware design of a digital system with remote-diagnostic capability. Most of synchronous systems only composed of combinational networks and clocked flip-flops can be tested remotely with a few restrictions on the system configuration and the module structure. The system partially having asynchronous circuits can be also tested, if any of them are not separated into two or more modules. Adapters may be realized with simple hardware. The diagnostic speed may be reduced to some extent by minimizing the separability and the number of logical values transmitted. At present, the method is being evaluated by using experimental adapters.

This approach as it is may be applicable flexibly to the actual diagnosis. If the system configuration is extended to more general circuits, it will become more effective.

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