

Dynamic Design of a Tunnel Diode Transistor Combined Circuit

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Synopsis

The dynamic design of a tunnel-diode-transistor combined circuit and the applied pulse circuits are discussed. The combined circuit, in which a tunnel diode is connected in parallel with the collector junction of a transistor, is used. The dynamic design procedure is considerably simplified by describing the transient behavior of a tunnel diode with a set of approximate expressions and by the help of a self-analog simulator. This circuit is capable of carrying out both memory and majority logic operations, and serves as a basic unit for several different pulse circuits, such as a monostable circuit, a frequency divider, a ring counter, etc.

1. Introduction

Techniques which combine a tunnel diode with a transistor have been often used for high speed switching purposes. In such cases a tunnel diode is combined with a transistor in many different styles [1,2,3]. The circuit in which a tunnel diode is connected in parallel with the collector junction of a transistor arouses considerable interest. This circuit may be adopted in various pulse applications because of its flexibility, simplicity and various abilities, such as

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a memory, a majority logic, etc. The use of this circuit in the above fields is still attractive. From this point of view, simplifying its dynamic design is an important consideration.

The authors propose two points in this paper. They are:

(1) that the difficulties in the dynamic design of this circuit can be overcome easily by describing the transient behavior of a tunnel diode with a set of approximate expressions and by the help of a self-analog simulator [4] ; and (2) that this circuit is capable of carrying out both memory operations and majority logic operations and as a result it serves as a basic unit for several different pulse circuits, such as a monostable circuit, a frequency divider, a ring counter, an asynchronous delay line, etc. These applied circuits are available in practice.

Details are illustrated in order.

2. Basic Study [5,6]

The circuit treated here is shown in Fig.1. This circuit can be converted into a kind of pulse circuit with modifications of circuit parameters or by the addition of a few circuit elements and also can be used as a basic unit for pulse circuits of various kinds.

Such circuit are suitable for operation at a nanosecond and subnanosecond switching times. Here the basic problems in designing the circuit of Fig.1 are summarized below:

(1) In order to achieve high speed switching, it is advisable to select a tunnel diode with high figure of merit as well as a transistor with high cut-off frequency. However, such a tunnel diode demands larger peak current and as a result the current through a transistor increases. This means that the cut-off frequency of the transistor at the operating current level decreases. Besides, as the peak current of a tunnel diode increases, the input driving current should be increased by decreasing the input resistors. In such a case this circuit can not sometimes achieve the required logical functions, because its d-c characteristic is dominated by the nonlinear characteristic of the emitter-base resistance of a transistor.

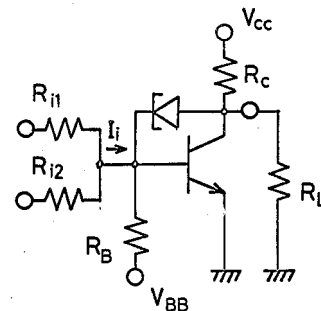


Fig.1 Basic unit

The value of the peak current I_p of a tunnel diode should be decided after the above considerations. With a commercially available germanium tunnel diode and silicon transistor, it is reasonable to select the value of I_p in the region of 2-4 ma.

(2) The value of the over drive factor $|\eta_i|$ is selected in the region of 2-3, in which this circuit may be driven most effectively, as found in the typical measured curves of Fig.2. Here the over drive factor is given by

$$\eta_i = \frac{I_i}{I_n} \tag{1}$$

where I_n in ma is one half of the difference between the peak current and the valey current of a germanium tunnel diode, and I_i in ma is the input current.

(3) The value of the emitter time constant τ_T of a transistor should be selected so as to keep the cost-to-performance ratio of this circuit as low as possible. The experimental values of the switching time $t_{dr}(f)$ against various values of τ_T/τ_D are plotted in Fig.3. Here τ_D is the equivalent time constant of the previously chosen germanium tunnel diode, the value of which is nearly equal to $25 \times C_p / I_n$. Then C_p in pF is the total capacitance of this circuit, as shown in the approximately equivalent circuit of Fig.4. From the curves of Fig.3, the value of the ratio τ_T/τ_D is selected within the following region,

$$0.5 < \tau_T/\tau_D < 2.0 \tag{2}$$

(4) The value of the load resistance R_L is selected so as to be greater than or equal to the lowest permissible value of R_L ,

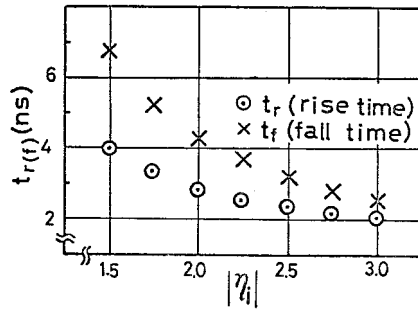


Fig.2 Effect of over drive factor on switching time

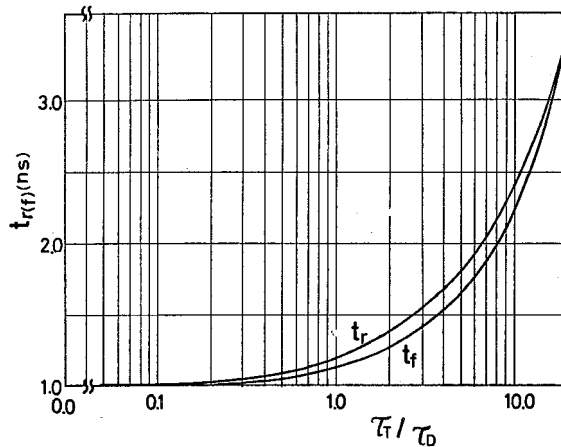
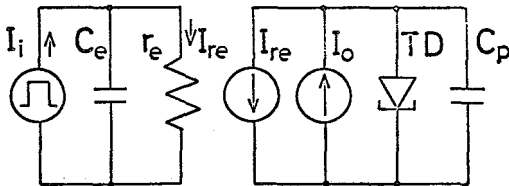


Fig.3 Experimental values of the switching time $t_{dr}(f)$ against various values of τ_T/τ_D

which in this case is about 50 ohms.

(5) When this circuit is used as a logical circuit, the voltages, $V_A + V_{be}$ and $V_B + V_{be}$, have one by one correspondence to two input levels, which are symbolized with '0' and '1'. Here V_A and V_B are the voltages at the tunnel diode terminals, when the operating points exist at A and B on the characteristic curve of Fig.5, respectively. And V_{be} is the voltage between the base and emitter of a transistor. The operating points of a tunnel diode will be decided corresponding to four possible combinations of the two input levels. The collector and base bias currents are adjusted so that a tunnel diode operates either at A or B when one of inputs is in high level and the other is in low level, and operates at A' or B' when both of inputs are in high level or in low level, respectively, and so that a transistor always operates on its active region. Here, because V_A and V_B are nearly equal to $V_{A'}$ and $V_{B'}$ respectively, the truth table as summarized in Table 1 is obtained.

Fig.6 shows an example of the circuit designed under the above conditions. On the basis of these



$$I_o = (I_p + I_v) / 2$$

$$\tau_T = C_e r_e$$

$$\tau_D = (C_p / C_d) \tau_D'$$

$$C_p = C_d + C_c + k \tau_T / R_L$$

τ_D' : time constant of tunnel diode

C_d : junction capacitance of tunnel diode

C_c : junction capacitance between base and collector terminals of transistor

k : coefficient showing the effect of R_L on dynamic response, $k = 0.7$ (experimentally determined)

Fig.4 Simplified equivalent circuit

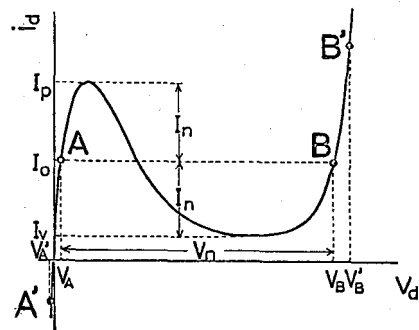


Fig.5 Operating points of tunnel diode.

Table 1 Truth table of basic unit

Z_{i1}	Z_{i2}	W_o
0	0	1
0	1	Z_o
1	0	Z_o
1	1	0

Z_{i1}, Z_{i2} : input

Z_o : output at present state

W_o : output at successor state

considerations, a method of the dynamic design of the above circuit will be described in detail later.

3. Dynamic Design

3.1 Utilization of Self-analog Simulator

An important work on dynamic design is to describe the transient response of a circuit to a given input pulse. In this case, a self-analog simulator is very available[4]. The desired circuit can be set up on such a self-analog simulator. Especially, it is convenient that the time-scale change can be accomplished in order to be apt to measure. Fig. 7 shows the self-analog simulator used here. The values of C_C , C_E' and C_D in Fig.7 are determined by the equations,

$$C_C = KC_C \quad (3)$$

$$C_E' = KC_{e'} \quad (4)$$

$$C_D = KC_D \quad (5)$$

$$T_T = KT_T \quad (6)$$

where K is the factor by which the speed of solutions is adjusted.

Here the emitter time constant T_T and the

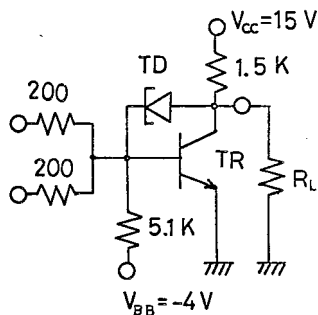
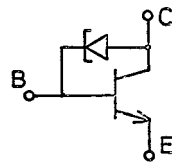
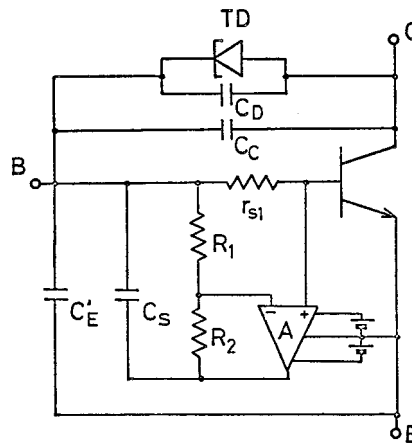


Fig.6 An example of basic unit



(a) original circuit



- C_D : junction capacitance of tunnel diode
- C_C : junction capacitance between base and collector terminals
- C_E' : junction capacitance between base and emitter terminals
- C_S : capacitor storing charge Q_S
- A: operational amplifier

(b) self-analog simulator

Fig.7 Scheme of self-analog simulator.

grounded emitter current gain β on the simulator are given by

$$T_T \approx \frac{R_1 + R_2}{R_1 + r_{S1}} \cdot \frac{r_{S1} C_S}{\beta} \tag{7}$$

$$\beta = \beta_0 \cdot \frac{R_1}{R_1 + r_{S1}} \tag{8}$$

where β_0 is the grounded emitter current gain of a transistor on real time. The value of C_S in Fig.7 is determined by Eq.(7). It is desired that the values of C_C, C_e', C_d and τ_T are measured on the basis of a charge controlled model.

As will be seen later, many of design parameters which are used to express the transient part of the output waveform are calculated from the experimental data obtained by means of the self-analog simulator.

3.2 Method for Dynamic Design

The above combined circuit has two stable states. The pulse width necessary for switching is closer to a switching time in the unit-step response of the circuit. This is because, if a narrower pulse is applied to the circuit, then the output waveform deteriorates, or if a wider pulse is applied to the circuit, then the maximum value of repetition rate is limited. Here a method for evaluating simply the transient response of the circuit to an input pulse whose width is equal to the above switching time is presented.

Fig.8 shows a typical transient response of the above circuit. Here $t_{dr}(f)$ is the length of time it takes the output to rise(or fall) to 50% of its full amplitude and $l_r(f)$ is the slope of rise (or fall). When the values of $t_{dr}(f)$ and $l_r(f)$ are normalized, then these two normalized values are used for expressing the output waveform.

First, to unify the transient responses of the circuit with different parameters, the voltage V , current I and time t are normalized in the form

$$v = \frac{V}{V_n} \tag{9}$$

$$\eta = \frac{I}{I_n} \tag{10}$$

$$\theta = \frac{I_n}{C_p V_n} \cdot t \tag{11}$$

Then the tunnel diode characteristic curve of Fig.5 can be normalized, as

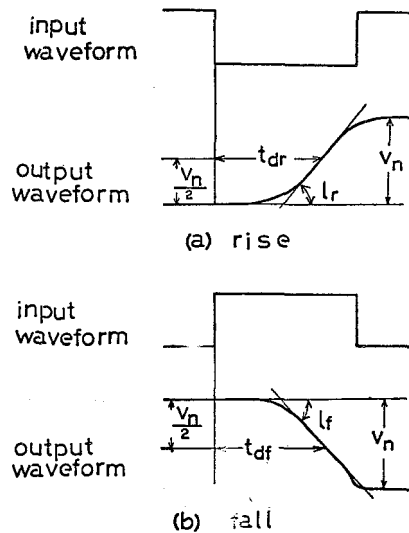


Fig.8 Typical transient response of basic unit.

shown in Fig.9. The values of $t_{dr}(f)$ and $l_r(f)$ also are normalized in the form

$$\theta_{dr} = \frac{I_n}{C_p V_n} \cdot t_{dr} \quad , \quad \alpha_r = \frac{C_p}{I_n} \cdot l_r \quad (12)$$

$$\theta_{df} = \frac{I_n}{C_p V_n} \cdot t_{df} \quad , \quad \alpha_f = \frac{C_p}{I_n} \cdot l_f \quad (13)$$

It is, however, difficult to describe $\alpha_r(f)$ and $\theta_{dr}(f)$ in the form of a simple function of device and circuit parameters, respectively, because of the extremely nonlinear characteristic of a tunnel diode. As previously stated the difficulty is overcome by some rough approximations.

The first approximation is that the characteristic curve of Fig.9 may be described near its valley point by

$$\eta_d = -1 \quad (14)$$

This depends on the fact that most part of the rise (or fall) time is occupied by the time it takes the switching locus on the tunnel diode characteristic curve to pass through the neighborhood of the valley point.

When the output voltage of V_0 is designated by v_0 in Fig.4, then the first derivative of v_0 with respect to θ_0 is given by

$$\frac{dv_0}{d\theta} = -\eta_{re} \eta_d \quad (15)$$

where η_{re} is obtained by normalizing the value of the dependent source current I_{re} in the circuit of Fig.4. When the output begins to rise (or fall), the value of η_{re} becomes nearly equal to $\eta_{ir}(f)$.

Therefore

$$\frac{dv_0}{d\theta} = -\eta_{ir}(f) + 1 \quad (16)$$

Thus α_r and α_f become, respectively,

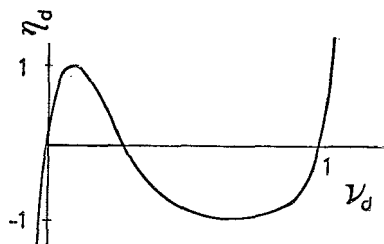
$$\alpha_r = -\eta_{ir} + 1 \quad (17)$$

$$\alpha_f = -\eta_{if} + 1 \quad (18)$$

The second approximation is that $\theta_{dr}(f)$ will be linearly related to the normalized emitter time constant θ_T by the equations,

$$\theta_{dr} = \theta_{dr_0}(\eta_{ir}) + g_r(\eta_{ir}) \cdot \theta_T \quad (19)$$

$$\theta_{df} = \theta_{df_0}(\eta_{if}) + g_f(\eta_{if}) \cdot \theta_T \quad (20)$$



η_d : normalized current of tunnel diode
 V_d : normalized voltage of tunnel diode

Fig.9 Normalized tunnel diode characteristic

where $\theta_{dr(f)_0}(\eta_{ir(f)})$ is the length of time it takes the response of the tunnel diode switch of Fig.4 to the dependent source, when it is considered to be stepwise, to reach 50% of its final value. Also $g_r(f)(\eta_{ir(f)}) \cdot \theta_T$ is the delay time induced by the effect of θ_T on the waveform of the above dependent source.

Then $\theta_{dr(f)_0}(\eta_{ir(f)})$ and $g_r(f)(\eta_{ir(f)})$ can be obtained by means of the self-analog simulator. These data are shown in Fig.10 and Fig.11.

In this manner, it is possible to determine the values of $\alpha_r(f)$ and $\theta_{dr(f)}$ by which the output waveform can be evaluated.

4. Applications

4.1 Monostable Circuit

A monostable circuit based on the above combined circuit is shown in Fig.12. The output terminal is connected to one of the input terminals through a delay line and a resistance R_f in series. When the monostable circuit in a quiescent state is triggered by a negative pulse, then it is initiated suddenly. It goes through the delay time τ_d of the delay line, after which it reverts to the initial state. The over drive factor by feedback currents depends on the sum of R_{i2} and R_f . Also, if the value of the input resistance R_{i2} is selected so as to satisfy the equation $R_{i2} + r_e = R_0$, where R_0 is the characteristic impedance of the delay line and r_e is the emitter resistance, then the impedance matching of the delay line to the basic combined circuit can be achieved.

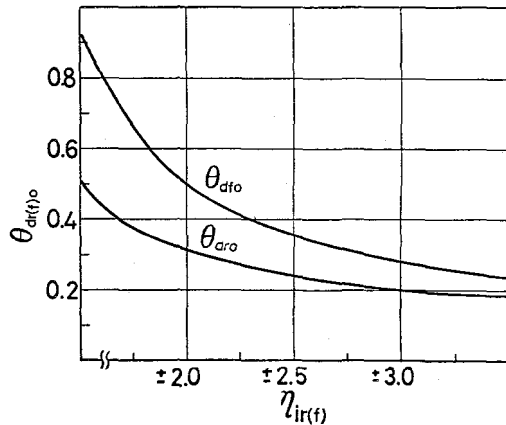


Fig.10 Value of $\theta_{dr(f)_0}(\eta_{ir(f)})$ obtained by means of self-analog simulator

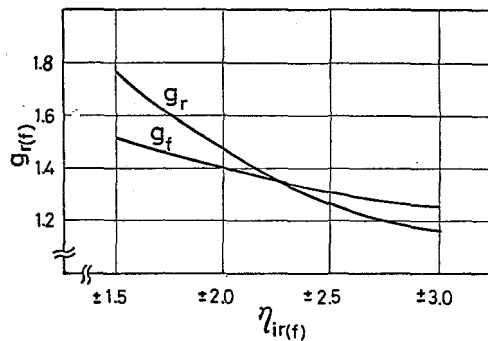


Fig.11. Value of $g_r(f)(\eta_{ir(f)})$ obtained by means of self-analog simulator.

Here the dynamic behavior of this monostable circuit is evaluated by using the dynamic design techniques described before. Fig.13 shows a typical response of this circuit to a square input, where the waveform of the output pulse is plotted with a solid line and that of the feedback pulse passing through the delay line is plotted with a broken line. Usually, these two waveforms are the same. Then the output waveform is determined by the use of the design parameters α_r , α_f , θ_{dr} and θ_h , where θ_h is the interval between the instant at which the leading edge of the feedback pulse reaches 50% of its final value and the instant at which the trailing edge of the output pulse reaches 50% of its final value. Therefore α_r , α_f and θ_{dr} can be calculated from Eqs.(17),(18) and (19). And then θ_h is given by

$$\theta_h = \theta_{df} \frac{1}{2(-\eta_{ir} + 1)} \tag{21}$$

where θ_{df} can be calculated from Eq.(20). This is because the leading edge of the feedback pulse reaches about 80% of its final value before the output pulse begins to fall. The output pulsewidth θ_w and the minimum repetition period θ_c are given by

$$\theta_w = \theta_d + \theta_h \tag{22}$$

$$\theta_c = 2\theta_d + \theta_{dr} + \theta_h + \frac{1}{2(-\eta_{if} + 1)} \tag{23}$$

where θ_d is the normalized value of the delay time τ_d of the delay line.

In this way, all parameters required for characterizing the dynamic behavior of the monostable circuit are determined. Fig.14 shows the measured values on real time and the values calculated from Eqs.(21) and (23). Fig.15 shows an example of the output waveform.

By means of the similar method, the dynamic behaviors of various pulse circuits based on the combined circuit may be simply determined.

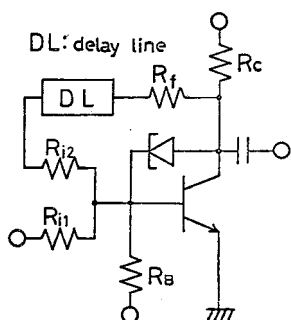


Fig.12 Monostable circuit

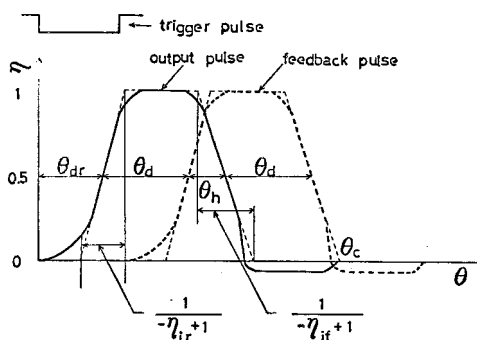


Fig.13 Typical waveform of monostable circuit.

4.2 Frequency Divider

If the delay time τ_d of the delay line is chosen so as to be much longer than the repetition period T of input pulses in the monostable circuit of Fig.12, then a frequency divider can be obtained. The

dividing ratio n is given by

$$n=1/(2N-1) \tag{24}$$

where N is the positive integer which satisfies the condition

$$(N-1)T \leq \tau_d \leq (N-\frac{1}{2})T. \tag{25}$$

Let us take an example of the actual circuit. When a delay line having a delay time of 163 nsec is used, a frequency divider having a dividing ratio of 1/33 at an input frequency of 100 MHz is obtained. Fig.16 shows the input and output waveforms.

4.3 Ring Counter

The above circuit also serves as a basic unit for a ring counter. It consists of the odd number of units in a ring. The ring counter of Fig.17 consists of three units. The output of the first unit is connected to the input of the second unit, the output of which is connected to the input of the third unit, in the similar manner

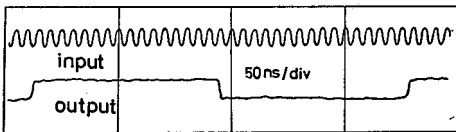
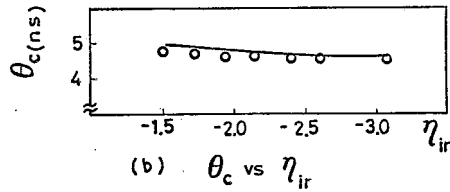
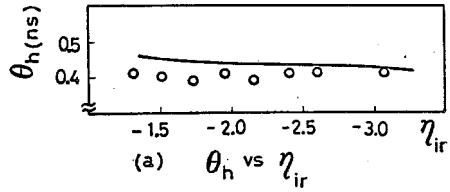


Fig.16 Output waveform of frequency divider.



o measured values in real time
 — calculated values

Fig.14 Comparison of experimental results with calculated ones.

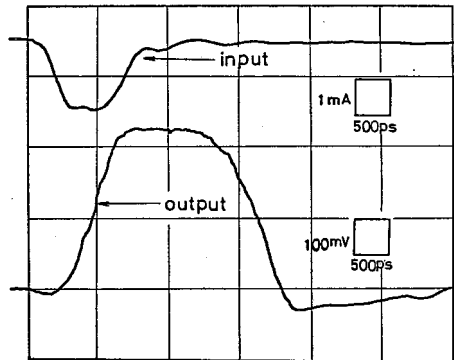


Fig.15 Output waveform of monostable circuit on real time

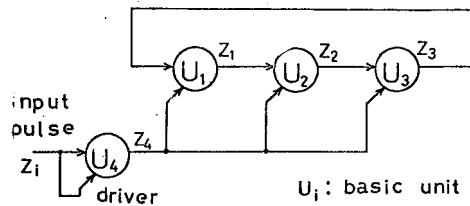


Fig.17 Scheme of ternary ring counter

the output of which is connected to the input of the first unit. The driver output is connected together to another input of each unit. The initial state of one unit is set so as to be different from that of the other. When the pulses to be counted are applied simultaneously to each unit, then only the state of one unit is changed by either leading or trailing edge of each input pulses. In this manner, the counter returns to the initial state every three pulse. Table 2 shows the truth table of such a ring counter.

The counter built as a trial can count 2×10^8 pulses per second. Fig.18 shows the input and output waveforms.

5. Conclusions

A method for the dynamic design of one of the circuits which combine a germanium tunnel diode with a silicon transistor and the applied circuits were illustrated in this paper. The conclusions can be summarized as follows:

- (1) The combined circuit serves as a basic unit for several different pulse circuits.
- (2) The applied circuits can operate at nanosecond and subnanosecond switching times as shown in some actual examples.
- (3) The transient behavior of the combined circuit and its applied circuits can be analyzed by the use of the delay time $\theta_{dr}(f)$ and the slope $\alpha_r(f)$, which can be expressed with a set of simple equations, respectively, by employed some approximations. The values of these parameters can be determined by substituting some data obtained by means of the self-analog simulator and some given values of device and circuit parameters into the above equations.

The method for the dynamic design described here is sufficient to

Table 2 Truth table of ternary ring counter

			Z ₄ = 0			Z ₄ = 1		
Z ₁	Z ₂	Z ₃	W ₁	W ₂	W ₃	W ₁	W ₂	W ₃
1	0	1	1	0	1	0	0	1
0	0	1	0	1	1	0	0	1
0	1	1	0	1	1	0	1	0
0	1	0	1	1	0	0	1	0
1	1	0	1	1	0	1	0	0
1	0	0	1	0	1	1	0	0

Z₁, Z₂, Z₃, Z₄: output of basic unit at present state

W₁, W₂, W₃: output of basic unit at successor state

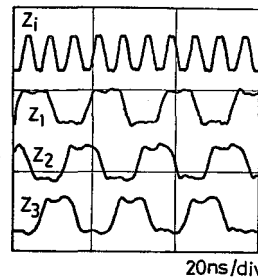


Fig.18 Output waveforms of ternary ring counter

the practical requirement. Since the above combined circuit may be used widely in various pulse applications.

Acknowledgment

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References

- [1] Y.C.Hwang, IRE Trans. Circuit Theory, Vol. CT-9(1962), 233.
- [2] Z. Kitamura, H. Terada, K. Omura and K. Tachibana, Trans. IECE, Japan, Vol. 53-C(1970), 31.
- [3] Z. Kitamura, H. Terada, K. Omura, K. Tachibana, K. Asada and T. Okamoto, Trans. IECE, Japan, Vol. 54-C(1971), 1071.
- [4] B.T. Murphy Bell Syst. Tech. J., Vol. 47(1968), 487.
- [5] Z. Kitamura, H. Terada, K. Omura, K. Asada and T. Okamoto, Trans. IECE, Japan, Vol. 53-C (1970), 418.
- [6] T. Okamoto, T. Misaki, K. Omura and Z. Kitamura, IEEE, S.S.C. Vol. 9 (1974)