Analysis and Design of Parallel Inverter Circuit with Parallel Inductive Load

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Synopsis

In this paper, the parallel inverter circuit with the load consisted of resistive load and constant reactive load in parallel, is analyzed taking into acount the d-c source reactance.

The circuit has a good voltage regulation for the variation of resistive load current, except the vicinity of no load.

The design method in using the results of analysis is also discussed.

§ 1. Introduction

In the parallel inverter circuit with transformer, the effects of transformer exciting reactance on circuit performance has been investigated[1]. Consequently, it is explained that some values of exciting reactance of transformer are usefull to improve the voltage regulatlon.

By using this characteristics, the parallel inverter circuit having a good voltage regulation can be designed.

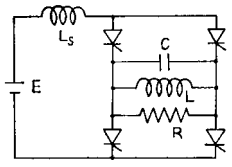

Fig. 1 Bridge type parallel inverter circuit with parallel inductive load.

§ 2. Asumptions and equivalent circuits

For the analysis of the circuit is shown in Fig. 1, following asumptions are introduced.

1) Resistances of reactor, d-c source, capacitor, etc. are negligible.

2) On the thyristor, leakage current in unconducting condition, voltage drop in conducting condition, turn-on time and reverse current at turn-off, are negligible.

3) The load is consisted of resistance R and constant indactance L that is connected in parallel.

4) The source current i_s is continuous.

5) The period in every half cycle is equal to t_0.

From these asumptions, the equivalent circuits of the circuit in Fig. 1 are given as shown in Fig. 2 (a), (b).

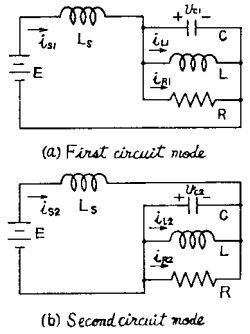

Fig. 2 Equivalent circuits of parallel inverter.

§ 3. Circuit analysis

From Fig. 2, following equations are introduced.

$$L\, di_S/dt + v_C = E \tag{1}$$

$$L\, di_L/dt = v_C \tag{2}$$

$$R\, i_R = v_C \tag{3}$$

$$C\, dv_C/dt = i_S - i_L - i_R \tag{4}$$

Eqs. (1)~(4) are rewritten in the operational matrix form as follows.

$$\begin{bmatrix} P & 1/L' \\ -1/C & P+1/RC \end{bmatrix}\begin{bmatrix} I' \\ V_C \end{bmatrix}=\begin{bmatrix} E/L_S \\ 0 \end{bmatrix}+P\begin{bmatrix} i'^{+0} \\ v_C^{+0} \end{bmatrix} \tag{5}$$

where, $i'=i_S-i_L$, $1/L'=1/L_S+1/L$, i'^{+0} and v_C^{+0} are initial values of i' and v_C. Solving Eq. (5) and transforming into the time function, we have

$$\begin{bmatrix} i' \\ v_C \end{bmatrix}=[\varphi]E+[\chi]\begin{bmatrix} i'^{+0} \\ v_C^{+0} \end{bmatrix} \tag{6}$$

where, $[\varphi]$ is a term related to the source voltage E, and $[\chi]$ is a term related to the initial conditions.

Substituting t_0, that is, the time interval of the first circuit mode or of the half cycle, into Eq. (6), we have

$$\begin{bmatrix} i'_0 \\ v_{CO} \end{bmatrix}=[\varphi_0]E+[\chi_0]\begin{bmatrix} i'^{+0} \\ v_C^{+0} \end{bmatrix} \tag{7}$$

where, i'_0 and v_{CO} are final values of i' and v_C in the first circuit mode.

The inverter circuit is a periodically interrupted circuit which is operated symmetrically. Therefore, in steady state, v_C and i_L are symmetrical waves, and the wave formes of i_S are same in both the first and the second circuit modes. Thus, $v_{CO}=-v_C^{+0}$, $i_{LO}=-i_L^{+0}$, $i_{SO}=i_S^{+0}$. From these relation,

$$i'^{+0}=i'_0+2\,i_{LO} \tag{8}$$

substituting Eq. (8) and $v_{CO}=-v_C^{+0}$ into Eq. (7), we have

$$\begin{bmatrix} i'_0 \\ v_{CO} \end{bmatrix}=([\boldsymbol{U}]-[\chi_0][\boldsymbol{A}])^{-1}\{[\varphi_0]E+[\chi_0]\begin{bmatrix} 2\,i_{LO} \\ 0 \end{bmatrix}\} \tag{9}$$

where, $[\boldsymbol{U}]$ is a unit matrix, and $[\boldsymbol{A}]$ is a transformation matrix as follows.

$$\begin{bmatrix} i'_0 \\ -v_{CO} \end{bmatrix}=[\boldsymbol{A}]\begin{bmatrix} i'_0 \\ v_{CO} \end{bmatrix}=\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}\begin{bmatrix} i'_0 \\ v_{CO} \end{bmatrix} \tag{10}$$

In the steady state, i_{LO} can be determined as follows. Since the relation $i_{SO}=i_S^{+0}$ is obtained,

$$L_S\int_0^{t0}\frac{di_S}{dt}\,dt=L_S\,[i_S]_0^{t0}=0 \tag{11}$$

Therefore, from Eq. (1)

$$\int_0^{t0} v_C\,dt=Et_0 \tag{12}$$

Then, from Eq. (2)

$$i_{LO}=\frac{1}{L}\int_0^{t0} v_C\,dt+i_L^{+0} \tag{13}$$

In Eq. (13), as $i_{LO}=-i_L^{+0}$,

$$i_{LO}=E\,t_0/2L \tag{14}$$

By the use of Eqs. (14), (9) and (6), the wave forms of v_C and i' in the steady state are obtained.

Now, the parameter Y, X_S, X, J_S, J and K are determined as follows. $Y=\omega C$, $X=\omega L$, $X=\omega L$, $J_S=YX_S$, $J=YX$ and $K=YR$. Where, ω is the angle velocity of the inverter driving frequency. Substituting these relations into Eqs. (14), (9) and (6), the wave forms of v_C are depicted in dimentionless form by the parameters of J_S, J and K, but the current i' can not be caluculated by these three parameters.

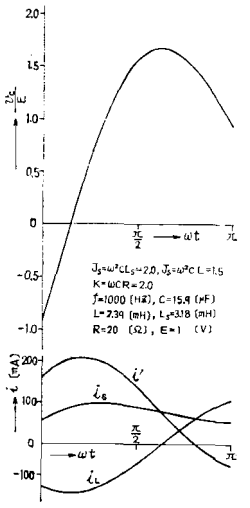

Fig. 3 Calculated example of wave forms.

The digital computer is used for the calculation. In Fig. 3, the caluculated example of wave forms is shown. In Fig. 4, the wave forms of v_C/E are shown, and minimam values of parameters $J_S=\omega^2CL_S$ in the wave forms with each same values of parameters $K=\omega\,CR$ and $J=\omega^2\,CL$, are corespond to boundary point where source current comes to be interrupted.

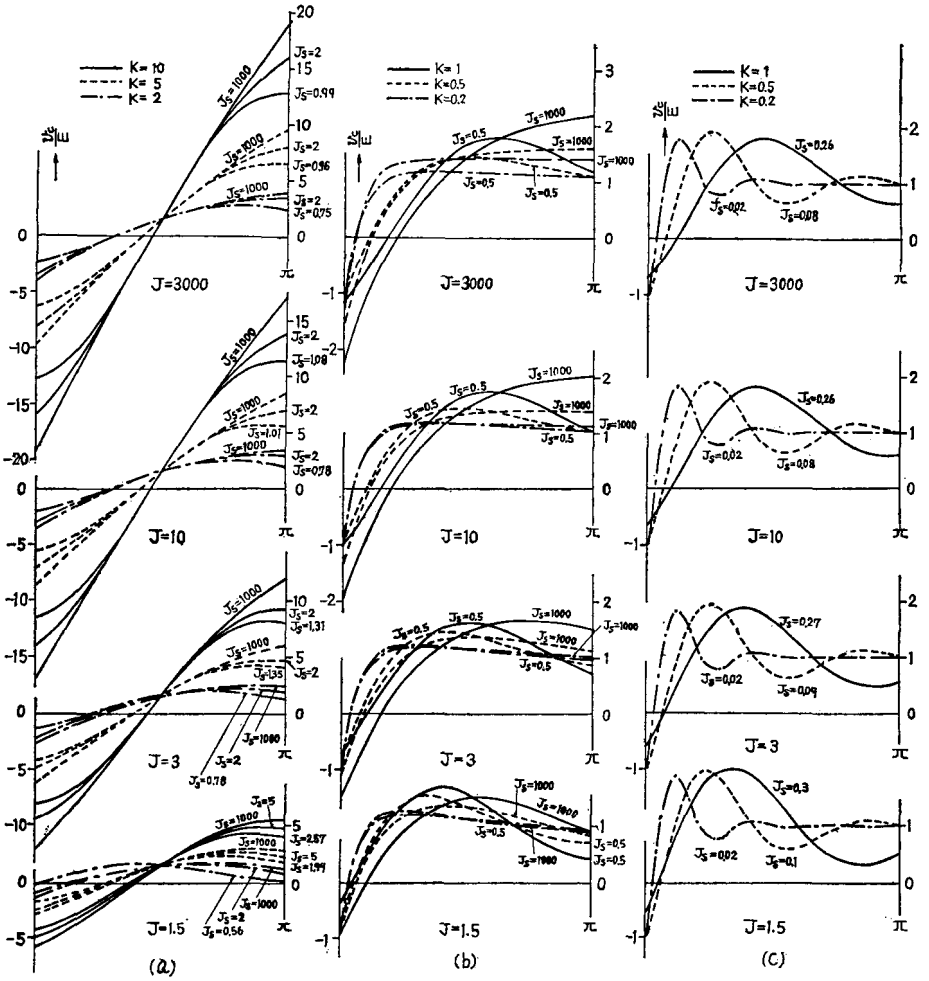

Fig. 4 Caluculated wave forms of capacitor voltage.

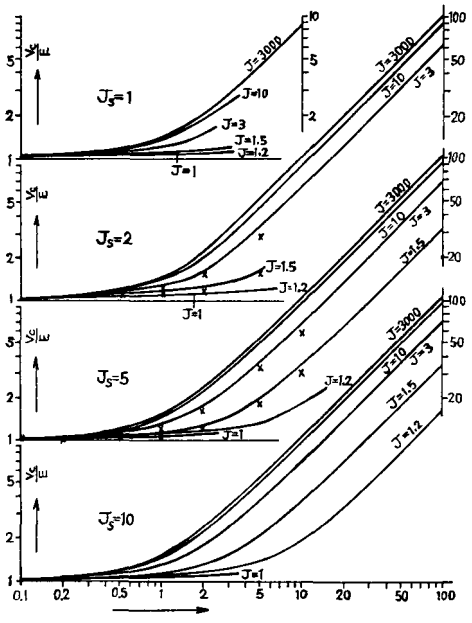

Fig. 5 Capacitor voltage in effective value.

The effective values of capactitor voltage V_c are shown in Fig. 5, only in the case that the source current is continuous. The boundary conditions which source current i_S is turned to interrupted condition from continuous, are shown in Fig. 6.

The mean value of source current I_S is determined as follows.

$$I_S = V_c^2/ER \tag{15}$$

§ 4. Experimental result

It is experimented on the circuit in Fig. 1. The reactor L_S and L are coreless. The water resistor is used as the load resistor. Substracting the voltage drops by the thyristor and the resistance of reactor L_S from the source voltage, the actual source voltage E is determined. The examles of wave forms of thyristor temminal voltage and source current are shown in Fig. 7

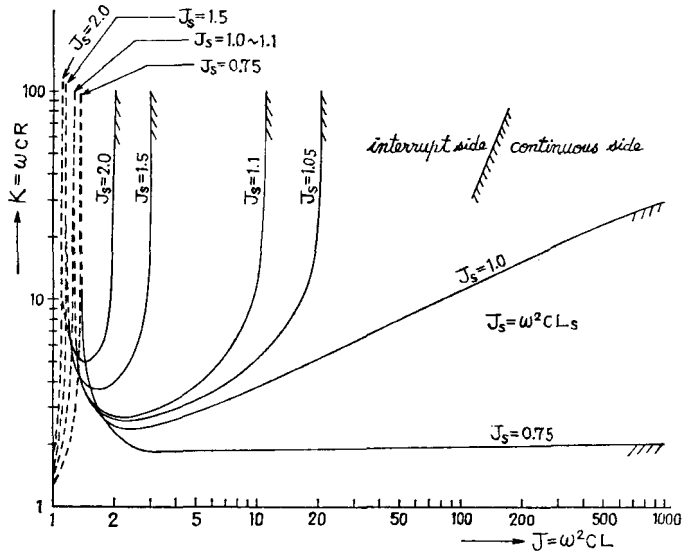

Fig. 6 Boundary lines where i_S comes to be interrupted.

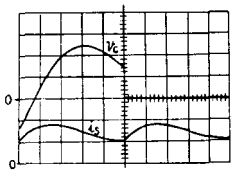

Fig. 7 Measured wave forms of thyristor voltage across A-K (upper side) and sourse current (under side).
(L, L_S : coreless reactor)
$J_S=\omega^2 GL_S=2.0$, $J=\omega^2 CL=1.5$, $K=\omega CR=2.0$, $f=1000Hz$, $C=7.5\mu F$, $L=5.07mH$, $L_S=6.77mH$, $R=42.4\Omega$, $I_S=1.3A$, $E=33.8$V, $V_C=38V$.

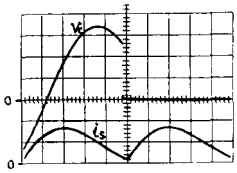

Fig. 8 Measured wave forms of thyristor voltage across A-K (upper side) and source current (under side).
(L, L_S : coreless reactor)
$J_S=\omega^2 CL_S=2.0$, $J=\omega^2 CL=1.5$, $K=\omega CR=5.0$, $f=1000Hz$, $C=7.5\mu F$, $L=5.07mH$, $L_S=6.77mH$, $R=106\Omega$, $I_S=1.0A$, $E=35V$, $V_C=53V$.

and Fig. 8. The experimental results of effective capacitor voltage V_C are shown in Fig. 5 by using $\times$ mark, when driving frequency $f=1000$ Hz, $C=7.5$ μF. The experimental results are similar to the caluculated.

§ 5. Design example

Next, the design example using the analyzed result, is shown. The specifications of the circuit are determined as follows, the circuit conection is as shown in Fig. 1, the driving frequency $f=360$ Hz, the out-put voltage in full load $V_C=30V$, the variation of load resistance $R=2\sim20\Omega$.

At the first, the parameter $J=1.5$ is picked up from Fig. 5, since regulation of the output voltage due to the variation of K, that is, the resistive load R, is relatively small. the parameter K is determined to $0.2\sim2.0$, proportional to the variation of R. In the case of $J=1.5$, $K=0.2$, it is necessary that the turn-off time of the thyristor is shorter than 38 μs, as shown from Fig. 4. From the relation $K=YR$, $Y=0.1$, accordingly $C=44$ μF, are determined. And from $J=YX=1.5$, $X=15$, accordingly $L=6.6$ mH, are determined. Taking $J_S=1.0$, that is, the value which sourse current is not interrupted by the variation of K, $L_S=4.4$ mH is determined.

The ideal characteristices of the circuit are as follows. On the full load, $E=28$ V is necessary to get $V_C=30$ V, since $V_C/E=1.06$ from Fig. 5. And then $I_S=16$ A from Eq. (15). On the minimum load, $V_C=32V$, since $V_C/E=1.15$. And then $I_S=1.85$ A. If the inductance L is infinitive, V_C is 58 V at the minimum load.

For the practical design, it is necessary to consider the voltage drop of the winding resistance R_S of the reactor L_S and the voltage drop E_{SCR} of the thyristor on conducting. For example, if $E_{SCR}=1\ (V)\times2$, $R=0.1\ (\Omega)$, the practical sourse voltage E' is $E+E_{SCR}+R_S I_S=32\ (V)$, V_C at minimum load is $(V_C/E)\times(E'-E_{SCR}-R_S I_S)=34.3(V)$.

The experimenntal result of the output voltage characteristices is shown in Fig. 9. In Fig. 9, the circuit characteristices without reactor L, and those with feedback rectifiers[2] and without reactor L, are shown in comparision. The reverse blocking times of thyristor on full load were about 40 μs for every type of circuits.

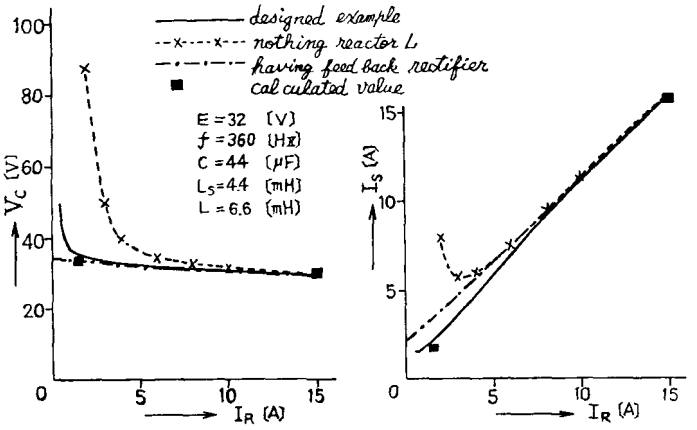

Fig. 9 Experimental result of designed example.

§ 6. Discussion

1) In steady state, the initial current $i_L{}^{+0}$ flowing in inductance L in every half cycle is caluculated by a simple formula. Therefore, the steady state operation of circuit is able to be solved by the second order simultaneous differential equation.

2) Concerning the wave forms and the effective value of output voltage, the measured value are similar to the caluculated, though, it is necessary to consider the voltage drops of thyristors and d-c souse reactor. As to souse current, the measured value is a little larger than the caluculated. This reason is supposed to be due to the losses of the capacitor C and the reactor L. Therefore, it is necessary to consider the efficiency of circuit elements, for better approximation.

3) There are many cases which the transformer is used in the side of the load. In these cases, the above mentioned circuit conditions are satisfied without the specified reactor L by making an air-gap in the core of transformer.

§ 7. Conculusion

The parallel inverter circuit with parallel inductive load is analyzed. Consequently, by connection of the reactor L, it is clarified that the voltage regulation of the inverter circuit is improved. The design example using the analyzed reults is shown, and the measured results of the design example, in which the voltage drops of the circuit elements are compensated, are to satisfy the specification.

It is concluded that the configuration is a usefull type of parallel inverter circuit.

Reference

1) S. Hayashi & others : J. I. E. E. **71** 145, 1970.
2) W. Mcmarry, D. P. Shttuck : Communication and Electronics 531, Nov. 1961.