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Convergence Acceleration and Accuracy Improvement in Power Bus Impedance Calculation With a Fast Algorithm Using Cavity Modes

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***Abstract*—Based on the cavity-mode model, we have developed a fast algorithm for calculating power bus impedance in multilayer printed circuit boards. The fast algorithm is based on a closed-form expression for the impedance Z matrix of a rectangular power bus structure; this expression was obtained by reducing the original double infinite series into a single infinite series under an approximation. The convergence of the single series is further accelerated analytically. The accelerated single summation enables much faster computation, since use of only a few terms is enough to obtain good accuracy. In addition, we propose two ways to compensate for the error due to the approximation involved in the process of reducing the double series to the single series, and have demonstrated that these two techniques are almost equivalent.**

***Index Terms*—Cavity-mode model, closed-form expression for fast calculation, power bus impedance, power bus resonance.**

I. Introduction

POWER bus resonances in a multilayer printed circuit board (PCB) are a problem, since the resonances not only cause radiated emission as electromagnetic (EM) interference, but also give rise to simultaneous switching noise as a signal integrity problem in high-speed digital circuits. Power bus noise suppression has thus become a major concern for electromagnetic compatibility (EMC) engineers engaged in high-speed PCB design. Fast and accurate estimation of the power bus noise early in a board's design cycle is desirable to ensure the signal integrity and EMC of the product. The main aim of our work has been to develop a modeling tool suitable for this purpose.

Current multilayer PCBs often use entire solid power-return (ground) plane pairs for DC power distribution (a power bus). With the continuous increase in clock rates, it seems reasonable to consider the power distribution system in PCBs as a dynamic EM system, in which the propagation effects are important. In fact, the power-return plane pairs in PCBs must be considered as a parallel-plate waveguide system. Most of the EM energy associated with the transient process remains captured within the two planes, which actually form an edges-open resonator; in other words, a patch antenna. Through various modeling methods, such as the distributed lumped-element equivalent circuit model [1], [2], the partial-element equivalent circuit (PEEC) approach [3], and numerical models based on the finite-element method [4] and finite-difference time-domain method [5] have been successfully applied to model power bus structures in PCBs. These models are relatively complex, and require a significant amount of computing time to achieve accurate results.

In addition to the above-mentioned models, a full cavity-mode model [6], [7] has also been used to characterize the rectangular power bus structure as a planar multiport microwave circuit [8], [9]. In the cavity-mode model, the input impedance of a port and/or the transfer impedance between two ports on a power bus can be expressed by a closed-form expression in a double infinite series. The double infinite series converges very slowly, though, particularly when used to calculate the self-input impedance for a small port dimension [10]. Usually, over a million terms must be computed to achieve good accuracy. As was done in the analysis of microwave planar circuits [11], the double infinite series can be reduced to a single infinite series by using a summation formula of a Fourier series under the assumption that the two-dimensional (2-D) port can be regarded as a 1-D port. Though the single series will take much less computation time than the double series, over a thousand terms still have to be computed to achieve good accuracy for the input impedance. In addition, an error occurs between the input impedances calculated using the double summation and those using the single summation. This error is due to the approximation involved in the process of reducing the double series to the single series.

In this paper, we propose a fast algorithm which can accelerate the convergence of the single infinite series [12], [13]. We have found that using just a few terms is sufficient to achieve good accuracy with the fast algorithm. Moreover, we show that the error between the double summation and the single summation can be compensated for in two ways. One is to subtract a "virtual" inductance term whose value depends only on the spacing between the two planes, regardless of the other board

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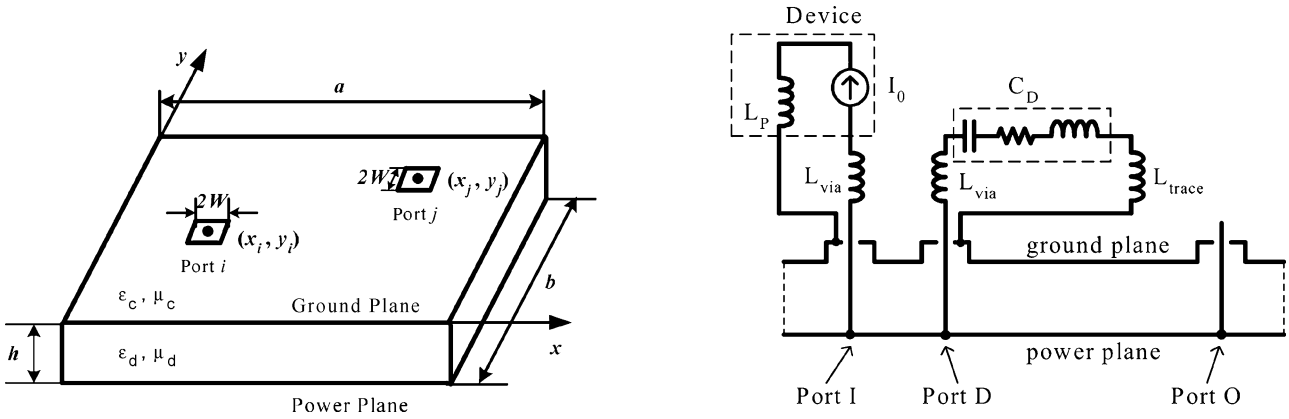

Fig. 1. Geometry of a rectangular power bus structure and its planar circuit model with external passive components and/or active devices.

dimensions and parameters. Another is to double the width of the 1-D port so that its circumference becomes equal to that of the corresponding 2-D port. We have found that these two techniques are almost equivalent to each other.

II. Cavity-Mode Model

The cavity-mode model is an analytical description of the impedance matrix (Z parameters) of a power bus structure (a bare board). The impedance matrix can be expressed in terms of the eigenfunctions and eigenvalues of the Helmholtz problem, by selecting a Green function [9] of the 2-D Helmholtz equation with the boundary condition of the second kind (the perfect magnetic conductor sidewalls), since most PCBs are electrically thin. Each "mode" in the Z-parameter expression corresponds to a pole in the impedance. The full-mode representation of the Z parameters of the power/ground plane structure is an infinite summation of modes, and results in an infinite number of poles.

A. The Double Summation

For a rectangular power bus structure with length a and width b (Fig. 1), based on the Green's function of the 2-D Helmholtz equation which satisfies the boundary condition of the second kind on the four sidewalls of the dielectric layer, the Z-matrix elements can be obtained as [6]–[9]

$$Z_{ij} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{\mathrm{j}\omega\mu_d h}{ab} \frac{C_m C_n \mathrm{sinc}^2(k_{xm}\mathsf{w})\mathrm{sinc}^2(k_{yn}\mathsf{w})}{k_{xm}^2 + k_{yn}^2 - \kappa^2} \times \cos(k_{xm}x_i)\cos(k_{yn}y_i)\cos(k_{xm}x_j)\cos(k_{yn}y_j) \quad (1)$$

where $\mathrm{sinc}(x) = \sin(x)/x$; $k_{xm} = m\pi/a$, $k_{yn} = n\pi/b$; x_i, x_j, y_i, and y_j are the coordinates of the center of the ith and jth ports in the x and y directions, respectively. w is much less than the wavelengths of interest and represents the port half-width (we assume for simplicity that the port sizes in the x and y directions for the ith and jth ports are the same); h is the dielectric thickness (spacing) between the power/ground planes; ω is the radian frequency; and $\mathrm{j} = \sqrt{-1}$. The constant $C_m = 1$ if $m = 0$, and $C_m = 2$ if $m \neq 0$. Similarly, $C_n = 1$ if $n = 0$, and $C_n = 2$ if $n \neq 0$.

The complex transverse wavenumber κ in the denominator of (1) is determined as we did in [12] and [13], and is given as

$$\kappa^2 = \omega^2\mu_d\varepsilon_d - \frac{\mathrm{j}2\omega\varepsilon_d Z_s}{h} \quad (2)$$

where μ_d and ε_d denote the permeability and permittivity of the dielectric, and the surface impedance Z_s of the imperfect conductor of the power/ground planes is given as in [14]

$$Z_s = (1+\mathrm{j})R_s, \quad R_s = \frac{1}{\delta_s\sigma_c}, \quad \delta_s = \sqrt{\frac{2}{\omega\mu_c\sigma_c}} \quad (3)$$

where R_s is the surface resistivity of the conductive layer, and δ_s is the skin depth of field penetration into the conductor. To obtain sufficiently accurate power bus impedance, both the dielectric and conductor losses must be taken into account. The dielectric loss naturally appears in the imaginary part of the dielectric constant $\varepsilon_d = \varepsilon_0\varepsilon_r$ ($\varepsilon_r = \varepsilon_{re} * (1 - j\tan\delta)$, $\tan\delta$: the loss tangent), while the conductor loss is incorporated into the surface impedance Z_s of the conductor.

B. The Single Summation

As Fig. 1 shows, a board mounted with active devices or passive components can be considered a multiport circuit network interconnected by the Z-matrix elements of the bare board. In principle, for a P port circuit network, the number of Z-matrix elements that need to be calculated is $P(P+1)/2$ due to the symmetry of the matrix ($Z_{ij} = Z_{ji}$), for each frequency of interest. The computation of the double summation in (1) is obviously time consuming, so it is not suitable for practical use if P is large. In addition, the double series is extremely slow to converge for the self-input impedance, because of the singularity of the Green function as the field point approaches to the source point. Therefore, we wanted to reduce the double series to a much more rapidly converging series through analytical techniques. Actually, by using a summation formula of a Fourier series [15]

$$\sum_{m=0}^{\infty} \frac{C_m \cos mx}{m^2 - \alpha^2} = \frac{\pi}{\alpha}\frac{\cos(x-\pi)\alpha}{\sin\pi\alpha} \quad (4)$$

we can reduce the double infinite series in (1) to a single infinite series [11], [12], and the resulting series is given as

$$Z_{ij} = \sum_{n=0}^{\infty} \frac{\omega\mu_d h a}{\mathrm{j}2b} C_n \cos(k_{yn}y_i)\cos(k_{yn}y_j) \times \mathrm{sinc}^2(k_{yn}\mathsf{w}) \frac{[\cos(\alpha_n x_-) + \cos(\alpha_n x_+)]}{\alpha_n \sin\alpha_n} \quad (5)$$

where $\alpha_n = a\sqrt{\kappa^2 - k_{yn}^2}$, and $x_\pm = 1 - (x_i \pm x_j)/a$.

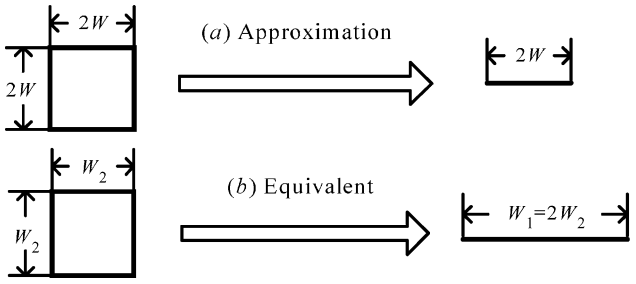

Fig. 2. (a) A 2-D port is directly reduced to a 1-D port under the approximation (6). (b) The error due to (6) can be compensated for by setting the circumference of the 1-D port equal to that of the 2-D port.

Notice that to obtain (5) from (1), we have made use of the approximation

$$\mathrm{sinc}^2(k_{xm}\mathsf{w}) \simeq 1. \tag{6}$$

This approximation physically means that the 2-D port is now regarded as a 1-D port, as shown in Fig. 2(a), and will result in an error between the results calculated by (1) and (5) for the input impedance. Note also that no approximation is involved in the reducing process for the port located at the edges with $x = 0$ or $x = a$, since in this case, the port itself is 1-D, rather than 2-D, as in the case of most microwave planar circuits where the patch is commonly fed by microstrip lines.

C. The Fast Algorithm

Looking at (5), it is clear that as long as $k_{yn}^2 > \kappa^2$ (α_n becomes imaginary), the series converges quite quickly, except for the case of $|x_\pm|$ being very close to unity. When $|x_\pm| = 1$ or $x_i = x_j$, the convergence is poor and thousands of terms are necessary. To speed up the convergence of the series in (5) for this case, the series may be written as

$$\sum_{n=1}^{\infty} \frac{\cos(ny)}{n^2} \frac{\cos(\alpha_n x)}{\alpha_n \sin \alpha_n} = \sum_{n=1}^{\infty} \frac{\cos(ny)}{n^2} \times \left[\frac{\cos(\alpha_n x)}{\alpha_n \sin \alpha_n} + \left(\frac{1}{\pi}\frac{b}{a}\right)\frac{1}{n} \right] - \sum_{n=1}^{\infty} \left(\frac{1}{\pi}\frac{b}{a}\right) \frac{\cos ny}{n^3} \tag{7}$$

where the second series on the right is rapidly converging, provided $|x|$ is equal or very close to unity, while the first series on the right is analytically summable with the help of [15]

$$\sum_{n=1}^{\infty} \frac{\cos(2nY)}{n^3} \simeq 1.202 + F(Y) \tag{8}$$

where $F(Y) = G(Y)$ for $0 \le Y \le \pi/2$ and $F(Y) = G(\pi - Y)$ for $\pi/2 \le Y \le \pi$. $G(Y)$ is given as

$$G(Y) = 2Y^2 \ln 2Y - 3Y^2 - \frac{Y^4}{18} - \frac{Y^6}{1350} - \frac{Y^8}{39690} - \frac{Y^{10}}{850500}. \tag{9}$$

Using this function, a fast algorithm can then be developed for calculating the Z-matrix elements. The expression for the self-input impedance element is given as

$$Z_{\mathrm{in}} = Z_1 + Z_2 + Z_4 + Z_6 + Z_7. \tag{10}$$

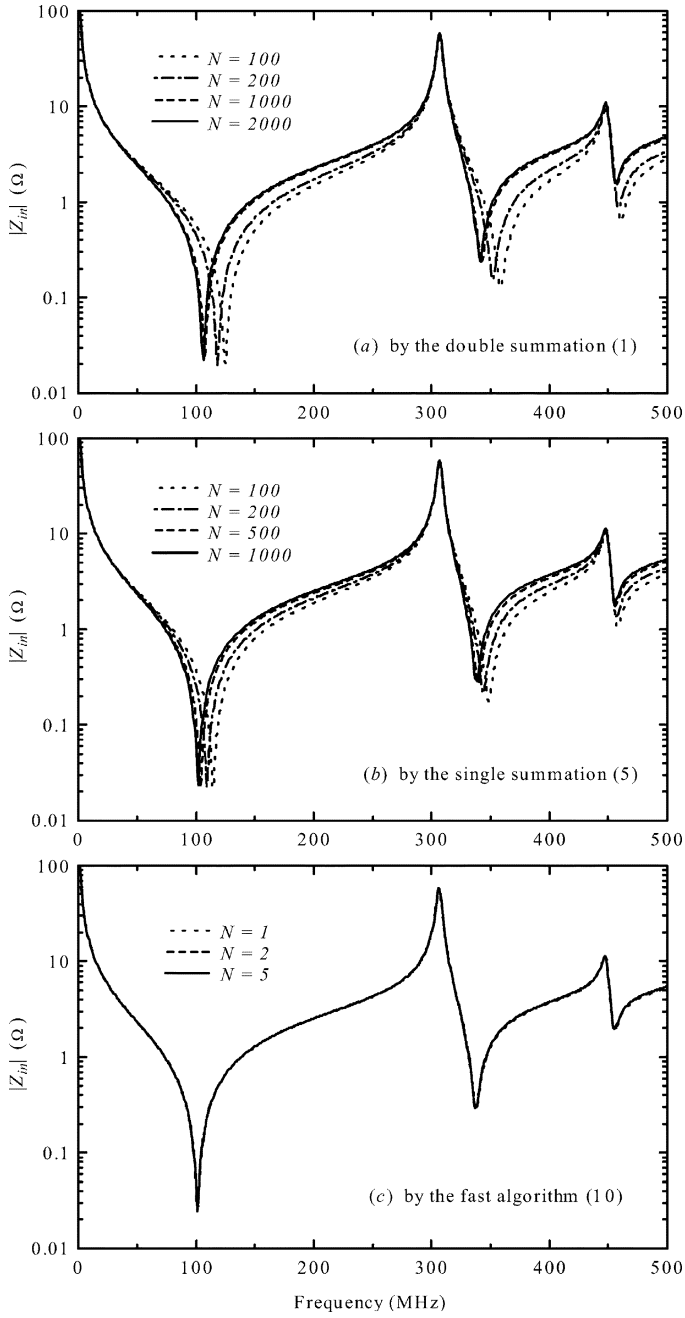

Fig. 3. Input impedance of a 237×162 mm board calculated by: (a) the double summation (1), (b) the single summation (5), or (c) the fast algorithm (10). N is the number of terms used in the calculations.

The detailed derivation of (10) and the definitions of terms can be found in the Appendix.

III. Results and Discussion

We performed numerical calculations to check the convergence and the accuracy of the fast algorithm. The infinite series in both (1) and (5) has to be truncated in practical calculations. The maximum number (for both $n_{\max}$ and $m_{\max}$ in the double series, and $n_{\max}$ in the single series) used in the calculation is denoted by N. The obtained results are considered to

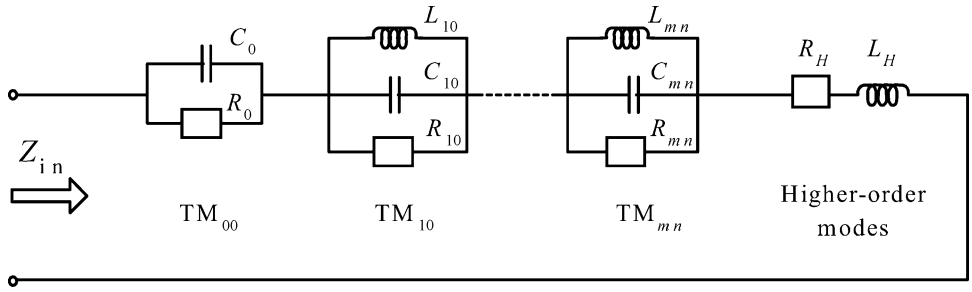

Fig. 4. Equivalent circuit for the input impedance of a power bus structure.

be the converged ones, when the relative error on the magnitude of the impedance calculated by truncating at N and at $N+1$, is less than 10^{-4}. The power bus is commonly fed by a coaxial probe or interconnected to active devices and passive components through circular vias, so the shape of a port is circular in practice, rather than square, as assumed in the cavity-mode model. The equivalent half-width of a square port can be determined as $\mathsf{w} = (\pi/4)\,\mathsf{r}$, where r is the radius of the corresponding circular port, assuming that their circumferences are equal to each other. In all of the following calculations, the conductor for the power/ground planes is considered to be copper of conductivity $\sigma_c = 5.92 \times 10^7$ [S/m]. The dielectric substrate between the two planes is assumed to be FR-4 glass epoxy of relative permittivity $\varepsilon_{\rm re} = 4.25$, with a loss tangent of 0.01 or 0.02.

We calculated the input impedance of a 237×162 mm power bus using the double series in (1), the single series in (5), and the fast algorithm in (10) with different numbers of terms for summation. The feed port was located at (40 mm, 59 mm) with the port dimension $\mathsf{w} = 0.1$ mm. The dielectric layer thickness between the power and the ground plane was 1.397 mm with a loss tangent equal to 0.01. The calculated results are plotted in Fig. 3(a)–(c). As discussed in [10], each cavity resonance peak is solely determined by one specific cavity mode, so the series converged quickly in the sense of achieving accurate cavity resonances. However, this fast convergence did not apply to the series resonances (the nulls). The first series resonance is caused by the board capacitance and the effective inductance contributed by all cavity modes, as shown by the equivalent circuit of Fig. 4 for the input impedance of a power bus structure. Adding more terms will shift the series resonance to a lower frequency, as observed in Fig. 3(a). To ensure the convergence of the series resonance frequency, $n_{\max}$ and $m_{\max}$ in the double summation had to be set to at least 2000, which led to a considerable computation time (about 21 min in an Alpha Station XP900 computer with 466 MHz CPU for 500 frequency points from 1 to 500 MHz). Though the computation time could be considerably reduced by using the single summation in (5) (about 1.1 s for $N = 1000$), we found that the convergence of the series resonance calculation was still poor, as shown in Fig. 3(b). This was due to the slow convergence of the series in (A4). To speed up the convergence of the series resonance calculation, we have developed a fast algorithm, as described in detail in the Appendix. As shown in Fig. 3(c), the convergence was greatly improved by the fast algorithm (10) (about 0.03 s for $N = 5$). For the present

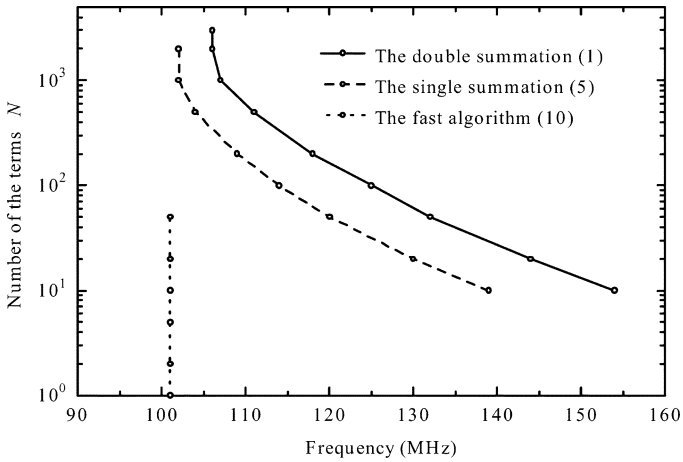

Fig. 5. Shift behavior of the first series resonance frequency in the input impedance shown in Fig. 3, as the number of terms used increases in the double summation (1), the single summation (5), or the fast algorithm (10).

case, over 1000 terms were needed in the single summation (5), but just two terms would be enough with the fast algorithm (10).

The effect of the number of the terms on the shift of the first series resonance frequency for the 237×162 mm board is plotted in Fig. 5, with either the double summation (1), the single summation (5), or the fast algorithm (10) used for the computation. Quick convergence for the series resonance calculation was achieved with the fast algorithm. The series resonance frequency estimated by the fast algorithm, however, was lower than the more accurate frequency provided by the double summation. The deviation or error regarding the series resonance frequency arises from the approximation (6) used in the process of reducing the double series to the single series, and is physically a result of overestimating the contribution from very high-order modes to the effective inductance. This suggests that the error can probably be compensated for by subtracting a "virtual" inductance term. Plotted in Fig. 6(a) are the imaginary parts of the input impedances for a 300×200 mm board with a dielectric thickness of 1.6 mm and a loss tangent of 0.02, estimated using either the fast algorithm (10) (the computation time was about 0.3 s for 3000 frequency points) or the double summation (1) (about 15 min). The board was fed at (15 mm, 15 mm) with the port half-width $\mathsf{w} = 0.6$ mm. The difference between the obtained results, that is the error due to the approximation (6), is plotted in Fig. 6(b). Except for a relatively large error around the cavity resonance frequencies, which arose from a slight de-

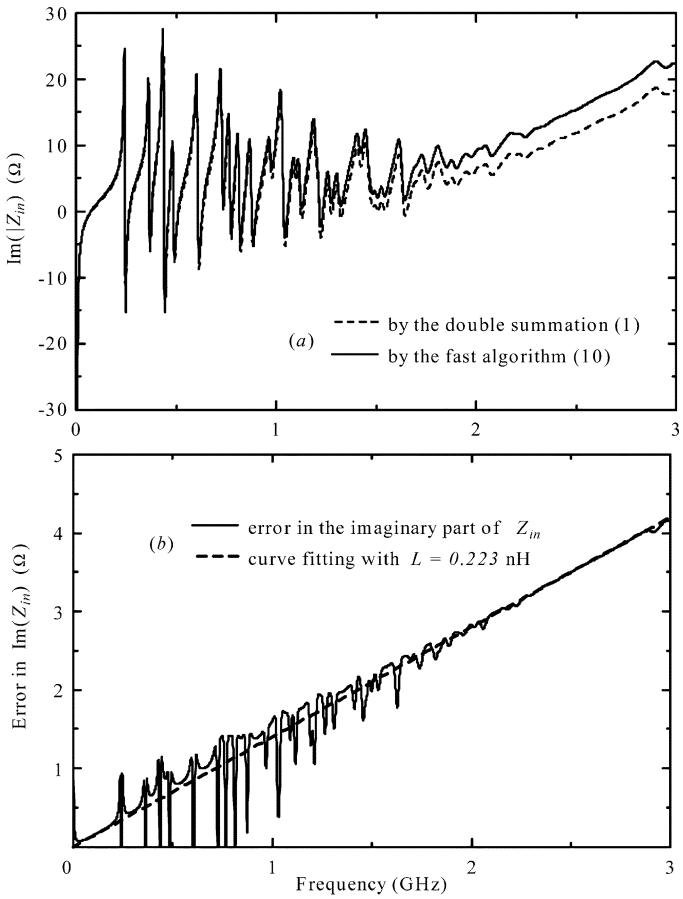

Fig. 6. Imaginary part of the input impedance for a 300×200 mm board. (a) Comparison and (b) error between the results calculated by the double summation (1) and the fast algorithm (10).

viation (less than 1 MHz) in the cavity resonance frequencies estimated by the fast algorithm (10) and the double summation (1), as well as from the sharp behavior of the cavity resonance peaks, the error can be well fitted by the impedance of an inductance term with its value equal to 0.223 nH.

A numerical study on various boards with different geometric and material parameters demonstrated that this "virtual" inductance was only proportional to the thickness h of the dielectric layer, and was almost completely unaffected by the other parameters. The expression for the "virtual" inductance term is then given as

$$L_h = \frac{0.223}{1.6} h = 0.139h \ (\text{nH}) \tag{11}$$

with h in millimeters.

It is well known that the inductive contribution observed at a port is strongly related to its dimensions. A wider port corresponds to a smaller inductive contribution. At high frequencies, the inductive contribution is usually determined by the circumference rather than the area of the port. For the inductive contribution from a 2-D square port of width w_2 and the inductive contribution from a 1-D linear port of width w_1 to be equivalent to each other, the relation $\mathsf{w}_1 = 2\mathsf{w}_2$ has to hold, as shown in Fig. 2(b). This suggests that the error due to (6) could also be compensated for by doubling the port dimension w in the fast algorithm. In Fig. 7, we compare the input impedance

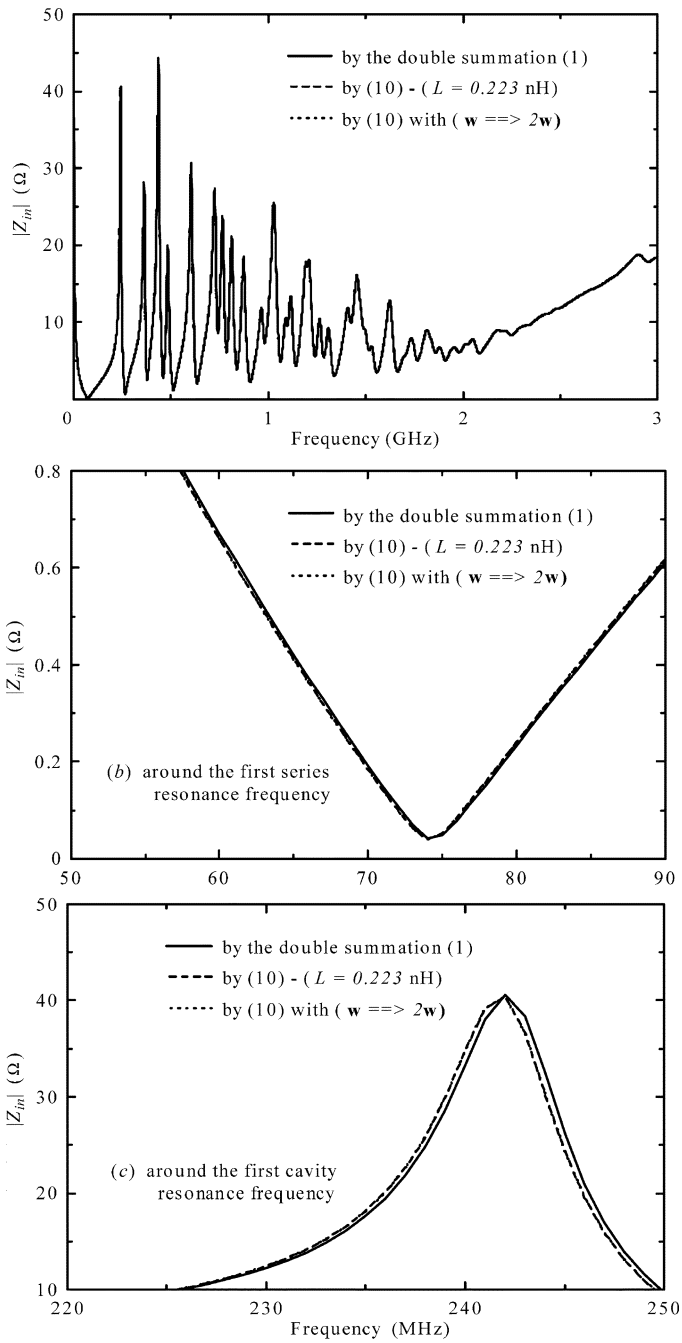

Fig. 7. Comparison of the input impedances calculated by three different schemes for the 300×200 mm board. (a) For frequencies up to 3 GHz. (b) Enlarged around the first series resonance frequency. (c) Enlarged around the first cavity resonance frequency.

calculated by the double summation with that obtained using the fast algorithm, compensated by either subtracting the "virtual" inductance term or doubling the port dimension w for the 300×200 mm board. The accuracy of the fast algorithm and the equivalence between the two compensation techniques were clearly demonstrated by the very good agreement among the results. The equivalence between the two compensation techniques is also proven analytically in the Appendix.

The merit of the fast algorithm is also discussed here for the transfer impedance between two ports at different locations (x_i, y_i) and (x_j, y_j). As described in Section II, the single series

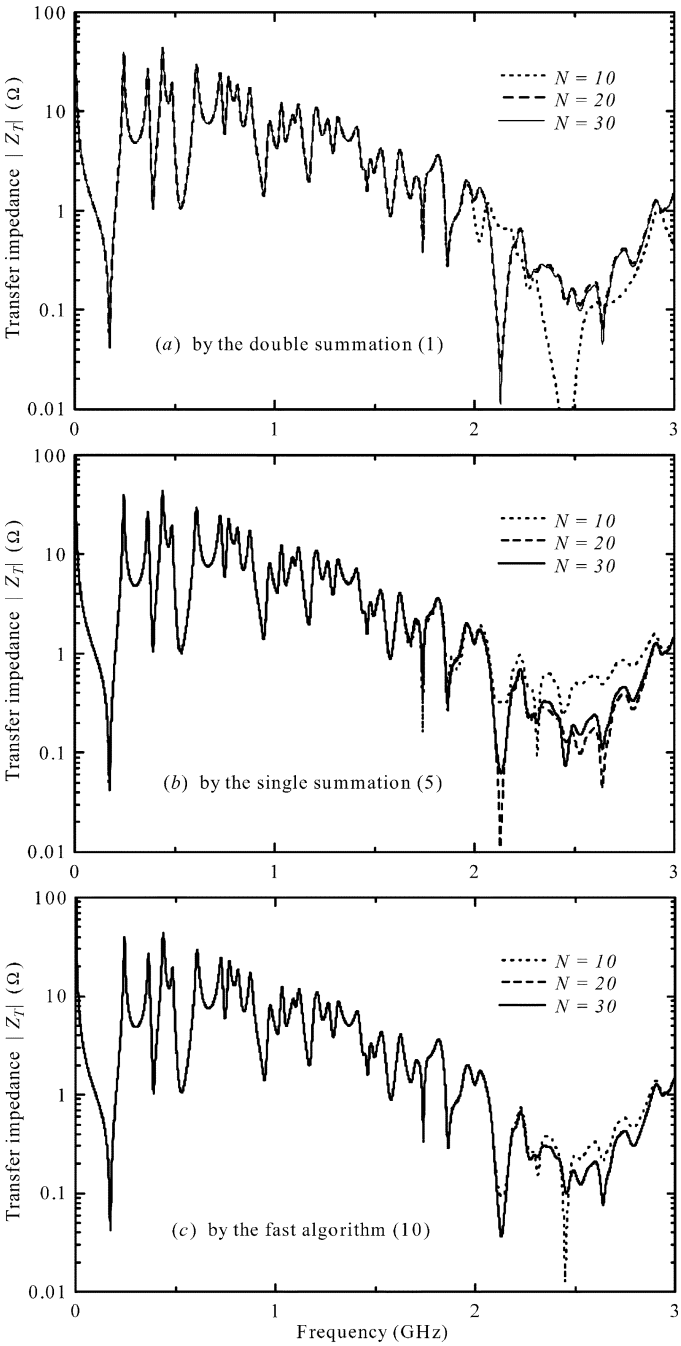

Fig. 8. Transfer impedance of the 300×200 mm board calculated by (a) the double summation (1), (b) the single summation (5), or (c) the fast algorithm. N is the number of terms used in the calculations.

in (5) is already rapidly converging as $x_i \neq x_j$. As $x_i = x_j$ (but $y_i \neq y_j$), using (7)–(9) seems to be a better way to achieve fast calculation. The transfer impedance between two ports located at (15 mm, 15 mm) and (15 mm, 185 mm) on the 300×200 mm board, calculated by the double summation (1), directly by the single summation (5), and by the fast algorithm [(5) together with (7)–(9)], is plotted in Fig. 8(a), (b), and (c) for the different numbers of terms used in the calculations. Though the double summation (1) enabled much faster convergence (the computation time was about 1.9 s for 3000 frequency points as $N = 30$) for the transfer impedance than for the input impedance shown in Fig. 3(a), the benefit of using the single summation (5) was still obvious (the number of terms that had to be calculated was reduced roughly from N^2 to N, and the computation time was about 0.27 s for $N = 30$). Using the fast algorithm [combining (7)–(9) with (5)], however, did not greatly improve the transfer impedance calculation, as shown in Fig. 8(b) and (c) (in Fig. 8(c), the computation was still about 0.27 s for $N = 30$). Finally, good agreement between the converged results (with $N = 30$) in Fig. 8(a) and those in Fig. 8(b) or (c) indicate that neither (6) nor the port dimension w significantly affected the calculated transfer impedance.

IV. Conclusion

We have developed a fast algorithm based on the full cavity-mode model for accurately calculating the power bus impedance in multilayer PCBs. The fast algorithm is based on a closed-form expression for the impedance Z matrix of a rectangular power bus structure. This expression was obtained by reducing the original double infinite series to a single infinite series under the approximation (6), and the computation of the single summation was further accelerated analytically. The convergence speed was greatly improved by the fast algorithm, particularly for the input impedance. For the example of Fig. 3, more than 1000 terms in the single summation (5) had to be computed to achieve good accuracy, but computation of only two terms was enough with the fast algorithm. Though use of (6) in the reducing process will result in an error between the results calculated by the fast algorithm and those calculated with the double summation, we found that this error can be compensated for by either subtracting a "virtual" inductance term or doubling the port dimension w. These two compensation techniques were found to be almost equivalent.

The fast algorithm presented in this paper is valid for a rectangular power bus structure. In addition, the fast algorithm, together with a segmentation method we previously reported, can be easily applied to more complicated power bus structures whose patterns consist of several segments of rectangles [16], [17] and/or right-angled triangles [18], and is also applicable to via-connected power bus stacks [19].

Appendix
Fast Algorithm for the Self-Input Impedance

The self-input impedance can be simply obtained from the transfer impedance by setting $i = j$ in (1) or (5). The expression for the self-input impedance is then given in the single series as

$$Z_{\text{in}} = Z_1 + Z_2 + Z_3 \tag{A1}$$

with

$$Z_1 = \frac{\omega\mu_d ha}{\mathrm{j}2b}\frac{[\cos(\alpha_0) + \cos(\alpha_0 x_+)]}{\alpha_0 \sin\alpha_0} \tag{A2}$$

$$Z_2 = \sum_{n=1}^{\infty}\frac{\omega\mu_d ha}{\mathrm{j}b}\cos^2(k_{yn}y_i)\mathrm{sinc}^2(k_{yn}\mathsf{w})\frac{\cos(\alpha_n x_+)}{\alpha_n \sin\alpha_n} \tag{A3}$$

$$Z_3 = \sum_{n=1}^{\infty}\frac{\omega\mu_d ha}{\mathrm{j}b}\cos^2(k_{yn}y_i)\mathrm{sinc}^2(k_{yn}\mathsf{w})\frac{\cos(\alpha_n)}{\alpha_n \sin\alpha_n} \tag{A4}$$

where $\alpha_n = a\sqrt{\kappa^2 - k_{yn}^2}$, $x_+ = 1 - 2x_i/a$. When $|x_+| \neq 1$, the series in (A3) should quickly converge, since the factor

$\cos(\alpha_n x_+)/\alpha_n \sin(\alpha_n)$ rapidly decreases as n increases. However, when $|x_+| = 1$ for the series in (A4), the convergence is not good, because

$$\lim_{n\to\infty}\left[\frac{\cos(\alpha_n)}{\alpha_n \sin(\alpha_n)}\right] \longrightarrow -\left(\frac{b}{n\pi a}\right). \tag{A5}$$

To speed up the convergence of the series in (A4), we rewrite the series as

$$Z_3 = Z_4 + Z_5 \tag{A6}$$

with

$$Z_4 = \sum_{n=1}^{\infty} \frac{\omega\mu_d h a}{\mathrm{j}b}\cos^2(k_{yn}y_i)\mathrm{sinc}^2(k_{yn}\mathsf{w}) \times\left[\frac{\cos(\alpha_n)}{\alpha_n \sin\alpha_n} + \left(\frac{b}{n\pi a}\right)\right] \tag{A7}$$

$$Z_5 = -\sum_{n=1}^{\infty} \frac{\omega\mu_d h a}{\mathrm{j}b}\cos^2(k_{yn}y_i)\sin^2(k_{yn}\mathsf{w}) \times\left[\left(\frac{1}{k_{yn}\mathsf{w}}\right)^2\left(\frac{b}{n\pi a}\right)\right] \tag{A8}$$

where the series in (A7) converges much faster than that in (A4), while the series in (A8) is analytically summable. Using the relation

$$8\cos^2(k_{yn}y_i)\sin^2(k_{yn}\mathsf{w}) = 2-2\cos(2k_{yn}\mathsf{w})+2\cos(2k_{yn}y_i) - \cos\left[2k_{yn}(y_i+\mathsf{w})\right] - \cos\left[2k_{yn}(y_i-\mathsf{w})\right] \tag{A9}$$

and making use of (7), we can express (A8) as

$$Z_5 = Z_6 + Z_7 \tag{A10}$$

with

$$Z_6 = -\frac{\mathrm{j}\omega\mu_d h}{4\pi}\left[\frac{F(\overline{\mathsf{w}})}{\overline{\mathsf{w}}^2}\right] \tag{A11}$$

$$Z_7 = \frac{\mathrm{j}\omega\mu_d h}{8\pi}\left[\frac{2F(y_+)}{\overline{\mathsf{w}}^2} - \frac{F(y_+ + \overline{\mathsf{w}}) + F(y_+ - \overline{\mathsf{w}})}{\overline{\mathsf{w}}^2}\right] \tag{A12}$$

where $\overline{\mathsf{w}} = \pi(\mathsf{w}/b)$, $y_+ = \pi(y_i/b)$ for $0 \le y_i \le (b/2)$, and $y_+ = \pi(1-y_i/b)$ for $(b/2) \le y_i \le b$. Thus, the final expression for the input impedance is given as

$$Z_{\mathrm{in}} = Z_1 + Z_2 + Z_4 + Z_6 + Z_7. \tag{A13}$$

As described in [10], the power bus structure can be simply modeled as an L_eC series branch below the first cavity resonance frequency, where $C(= \varepsilon_d ab/h$, given by (A2) as α_0, approaches zero at very low frequency) is the interplane capacitance, and L_e is the effective inductance contributed by all cavity modes. In other words, all terms in (A13) contribute to this effective inductance. However, as long as the port dimension w is small enough, compared with the board dimensions, the main contribution is made by Z_6 of (A11) and is approximately given as

$$L_e = \lim_{\mathsf{w}\to 0}\frac{Z_6}{\mathrm{j}\omega} = \frac{\mu_d h}{4\pi}\left[3 + 2\ln\left(\frac{b}{2\pi\mathsf{w}}\right)\right] \tag{A14}$$

for a port located away from the periphery of the board (that is, $|x_+| \neq 1$ and $y_+ \neq 0$). The remaining contributions from the other terms modify the main contribution. The contributions from Z_1 of (A2) and Z_4 of (A1) can almost be ignored. The contributions from Z_2 of (A3) and Z_7 of (A12) represent the part depending on the port location and the aspect ratio (b/a) of the board, but are insensitive to the port dimension w as if the port is not located on the edges ($|x_+| = 1$ or $y_+ = 0$) or the corners ($|x_+| = 1$ and $y_+ = 0$) of the board. The effective inductance is doubled at the edges and quadrupled at the corners, compared with that given in (A14), because of the contributions from Z_7 of (A12) for $y_+ = 0$ and/or Z_2 of (A3) for $|x_+| = 1$ (in this case $Z_2 = Z_3$).

As discussed in Section III, an error occurs as the double infinite series is reduced to the single infinite series. This error is due to the approximation (6) which results in an overestimation of the effective inductance L_e, since the 2-D port was regarded as a 1-D port. This error can be compensated for by either subtracting a "virtual" inductance term L_h, given in (11), or doubling the port dimension w in (A13). As stated above, doubling the port dimension w has almost no effect on the contribution to the effective inductance from the other terms in (A13), but does affect the contribution from Z_6 of (A11). According to (A14), doubling the port dimension w slightly decreases the effective inductance, and the amount of the decrease can be obtained as $(\mu_d/4\pi) * (2\ln 2) * h = 0.139 * h$ (nH) (with h in millimeters), which is exactly the same as given in (11). Therefore, whether a "virtual" inductance term is subtracted or the port dimension is doubled makes almost no difference. We should point out, though, that the compensation for a port located on the edges is not necessary, since in this case, it is better to consider the port itself to be 1-D rather than 2-D.

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