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A Practical Approach to Switching-Loss Reduction in a Large-Capacity Static Var Compensator Based on Voltage-Source Inverters

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Abstract— **This paper presents a simple method for reduction of switching and snubbing losses in a large-capacity SVC (static var compensator) consisting of multiple voltage-source square-wave inverters. The proposed method is characterized by a "commutation capacitor" connected in parallel with each switching device. The commutation capacitor allows the SVC to perform zero-voltage switching, and to reduce switching losses. The electric charge stored in the commutation capacitor is not dissipated, but regenerated to the dc-link capacitor. Moreover, a soft-starting method for the SVC is also presented to avoid forming a short circuit across the commutation capacitor during start up.**

Index Terms— static var compensators, reactive power, soft switching, zero-voltage switching.

I. Introduction

Static var compensators (SVC) consisting of multiple voltage-source inverters using GTO thyristors have been researched and developed for improving power factor and stability of transmission systems. SVCs have the ability to adjust the amplitude of the synthesized ac voltage of the inverters by means of pulse width modulation or by control of the dc-link voltage, thus drawing either leading or lagging reactive power from the supply.

Both high efficiency and high reliability are required for SVCs used in practical power systems. A pulse-width-modulated SVC [1]–[5], in which the dc-link voltage is controlled to remain at a constant value, can respond rapidly to a change in reactive power at the expense of increasing the switching and snubbing losses. On the other hand, a dc-link voltage controlled SVC [6]–[10], which is operated at a switching frequency of 50 or 60 Hz, produces reduced switching and snubbing losses, compared with an SVC based on PWM.

However, the switching and snubbing losses would not be negligible, as the required rating of the dc-link voltage controlled SVC is large. When the SVC draws a leading or lagging reactive power, the supply current leads or lags by 90° from the supply voltage. In other words, each voltage-source square-wave inverter used in the SVC is turned on or off at the peak of the supply current. A turn-off snubbing circuit commonly used in GTO inverters consists of a capacitor, a resistor and a diode. The snubbing capacitor is designed to suppress a surge voltage appearing at the peak current. Unfortunately, the electrical charge stored in the snubbing capacitor is usually consumed in the resistor. Various types of regenerative snubbing circuits [11]–[13] have been proposed to solve this problem, which regenerates the energy stored in the snubbing capacitor to the dc-link capacitor. However, it would not be expected to regenerate it with high efficiency because additional passive and active components are employed. Soft-switching techniques based on zero-voltage or zero-current switching have been introduced into voltage- and current-source inverters [14]–[22]. In order to achieve zero-voltage or zero-current switching, a resonant current flows through the switching device, or a resonant voltage is applied across the device. It is difficult to apply the soft-switching techniques to large-capacity SVCs because of increasing the current or voltage ratings of the switching devices. Such a complicated circuit spoils reliability of the SVCs in practical applications.

This paper proposes a simple method for reduction of switching and snubbing losses in a dc-link voltage controlled SVC. The method capable of achieving zero-voltage switching is characterized by a "commutation capacitor" which is connected in parallel with each switching device [10]. The commutation capacitor enables the switching device to be turned on or off at a zero-voltage condition, thus leading to reduction of surge voltage and switching loss without dissipation, unlike a conventional snubbing circuit. Parallel-connected capacitors to perform zero-voltage switching are also used in a soft-switching converter [14]–[19]. The commutation capacitor presented in this paper is similar to the parallel capacitor used in the soft switching converters, but it is different in terms of not requiring any additional resonant circuit or auxiliary switch. The supply current automatically discharges the electrical charge stored in the commutation capacitor, and regenerates it to the dc-link capacitor without superimposition of any resonant current or voltage. Therefore, connection of the commutation capacitor does not increase the current or voltage ratings of the switching devices, and it achieves high reliability of the SVC in practical use. Experimental results obtained from a laboratory setup rated at 10 kvar are shown to verify the viability of the operating principle of the commutation capacitor. Moreover, a soft-starting sequence, which performs the zero-voltage switching even during start up, is also presented and demonstrated in this paper.

II. System Configuration

Fig. 1 shows the experimental system of a 10-kVA static var compensator (SVC) consisting of four voltage-source square-wave inverters, a quad-series transformer and a dc-link capacitor. The system ratings and circuit parameters are shown in Table I. The dc links of the four voltage-source inverters are connected in parallel with the common dc-link capacitor of $C_{dc} = 500\ \mu$F. A starting resistor R_{dc} is connected to the dc-link capacitor via a switch SW_{dc}, which is used for the starting sequence discussed later. The ac ter-

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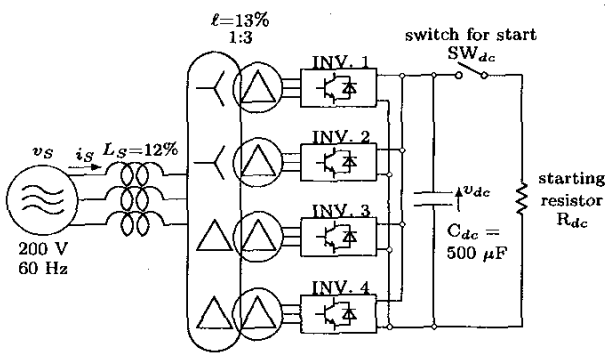

Fig. 1. Experimental system.

TABLE I
RATINGS AND CIRCUIT PARAMETERS

rated reactive power	Q	10 kvar
supply voltage (line-to-line)	V_S	200 V
supply frequency	f	60 Hz
dc-link voltage	V_{dc}	200 ~ 250 V
dc-link capacitor	C_{dc}	500 μF
unit capacitance constant [9]	UCC	1.3 mJ/VA
line inductance	L_S	1.3 mH (=12%)
leakage inductance	ℓ	1.4 mH (=13%)
commutation capacitor	C	1 μF
starting resistor	R_{dc}	1 kΩ

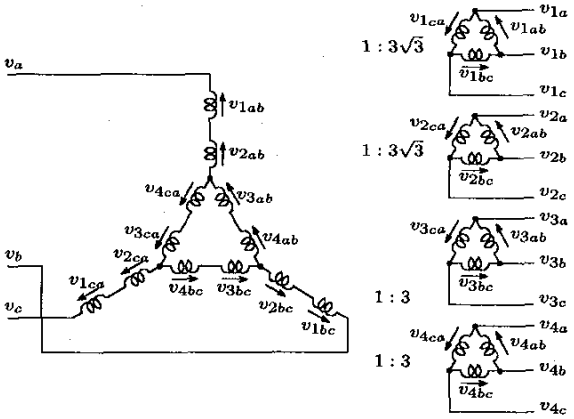

Fig. 2. Connection of quad-series transformer.

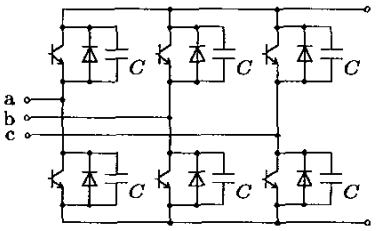

Fig. 3. Main circuit of inverter unit.

minals of the inverters are interfaced with the supply via the quad-series transformer. Fig. 2 shows the detailed connections of the quad-series transformer. The transformer consists of four three-phase transformers. The secondary windings of each transformer are connected in Δ, while the primary windings are separated phase by phase, and led out to six terminals. Although each inverter produces a six-step rectangular voltage waveform, the synthesized line-to-line voltage is formed as a 24-step waveform by applying a phase shift of ±7.5° to the supply voltage.

The SVC adjusts the dc-link voltage from 200 to 250 V in order to control an amount of reactive power. When the ac output voltage of the SVC lags to the supply, a small amount of active power flows from the supply to the dc-link capacitor, and the dc-link voltage rises up. Then the amplitude of the ac output voltage also increases, and thus the SVC draws a leading reactive power from the supply.

Fig. 3 shows the circuit configuration of each voltage-source inverter. A bipolar junction transistor integrated with an anti-parallel diode is used as a switching device in the following experiments. GTO thyistors, IGCTs or IGBTs would be used in a practical system. Each transistor is equipped with a commutation capacitor C in parallel, instead of a conventional snubbing circuit consisting of a capacitor, diode and resistor. The commutation capacitor enables the transistor to be turned on or off at zero voltage. Moreover, the electrical charge in C is not dissipated in any switching device or resistor but regenerated to the dc-link capacitor, so that a large capacitor can be employed to improve the turn-off capability of the switching device.

III. Commutation Capacitor

The commutation capacitor is similar to a loss-less snubbing circuit used in a high-frequency resonant inverter [23]. The loss-less snubbing capacitor enables the high-frequency resonant inverter to perform zero-voltage switching when the inverter is operated with a lagging power factor. On the other hand, the commutation capacitor allows the transistor to be operated with zero-voltage switching when a leading reactive power is drawn from the supply. However, the commutation capacitor differs from the loss-less snubbing circuit in terms of the amplitude of the current being turned off by the transistor. The power factor seen from the output terminals in the high-frequency resonant inverter may be near unity, while the power factor in the SVC is almost zero. The transistor is turned off near zero current in the high-frequency resonant inverter, whereas it is turned off at the peak of the inverter current in the SVC.

A. Operating Principle

Fig. 4 shows the operating principle of a commutation capacitor connected in parallel with each transistor. Fig. 4(a) is a simplified circuit for one phase of the inverter unit. Here, it is assumed that the dc link is two dc voltage sources $V_{dc}/2$, the neutral point of which is connected to the ground. A practical inverter has no connection of its dc link to the ground, and the ground current in this equivalent circuit in fact flows to the supply through the other phases.

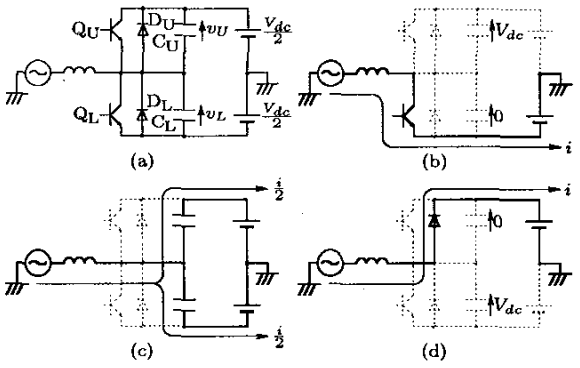

Fig. 4. Switching modes in commutation capacitor, (a) simplified circuit, (b) before, (c) during, and (d) after the commutation.

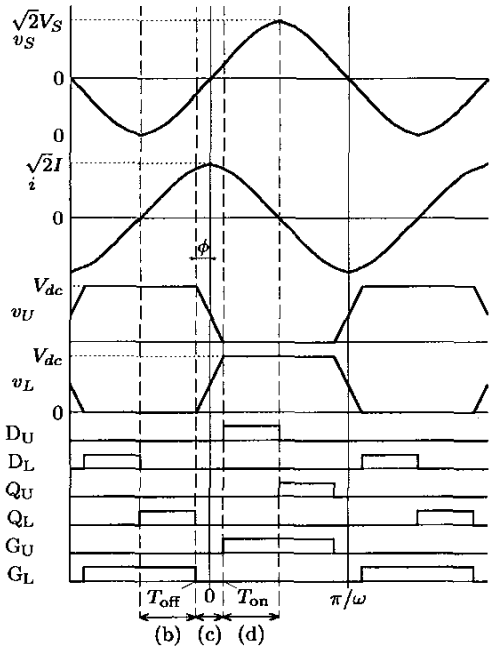

Fig. 5. Voltage and current waveforms in the voltage-source inverter equipped with commutation capacitors.

The voltage and current waveforms in the simplified circuit are shown in Fig. 5. At first, it is assumed that the lower transistor Q_L is conducting and the inverter current i is flowing through Q_L as shown in Fig. 4(b). The voltage across the upper commutation capacitor, v_U is the same as the dc-link voltage V_{dc} while the lower-capacitor voltage v_L is zero. The lower transistor Q_L can be turned off at zero voltage at the instant that the gating signal is removed from Q_L. During the commutation shown in Fig. 4(c), half of the inverter current $i/2$ flows through the commutation capacitor C_U and discharges C_U, and the other half charges C_L. When the upper-capacitor voltage v_U reaches zero and C_L is charged to V_{dc}, the free-wheeling diode D_U starts to conduct as shown in Fig. 4(d). The gating signal is provided to Q_U while D_U conducts. The upper transistor Q_U can be turned on under zero-voltage and zero-current condition after D_U turns off because the gating signal is continuously provided to Q_U.

The commutation capacitors enable zero-voltage turn-off, and zero-voltage and zero-current turn-on under the condition that the SVC takes a leading reactive power from the supply as shown in Fig. 5. If the SVC drew a lagging reactive power, the commutation capacitors would not work well because the inverter current would not discharge the commutation capacitors, and then the electrical charge would be shorted out at the instant the transistor is turned on. Therefore, the SVC equipped with the commutation capacitors should be operated so as to take a 90° leading reactive power, that is, to behave as a capacitor.

B. Design of Capacitance

The capacitance of the commutation capacitor should be designed to reduce the rate of voltage rise dv/dt at the peak value of the maximum inverter current. Since half of the inverter current flows through each commutation capacitor, the voltage across the commutation capacitor in Fig. 5(c) is given by

$$v_L = \frac{1}{2C}\int i\,dt, \tag{1}$$

where C is a capacitance value of the commutation capacitor. As shown in Fig. 5, $v_L = 0$ before $t = T_{\text{off}}$, while $v_L = V_{dc}$ after $t = T_{\text{on}}$. Equation (1) is represented as

$$V_{dc} = \frac{1}{2C}\int_{T_{\text{off}}}^{T_{\text{on}}} \sqrt{2}I\cos\omega t\,dt, \tag{2}$$

where I is the rms value of the inverter current i.

An amount of active power is drawn from the supply, and it is delivered to the dc link during the period of Fig. 5(d). On the contrary, the active power flows out to the supply during the period of Fig. 5(b), because the current direction is opposite to the supply voltage. Assuming that no power consumption occurs in the SVC, the conducting period of the transistor is equal to that of the free-wheeling diode: $T_{\text{off}} = -T_{\text{on}}$. The phase angle ϕ, at which the transistor is turned off, is given by

$$\phi = \omega T_{\text{on}} = \sin^{-1}\frac{\omega C V_{dc}}{\sqrt{2}I}. \tag{3}$$

Equation (1) is represented by the following equation.

$$v_L(t) = \begin{cases} 0 & (-\pi/\omega \le t < -\phi/\omega) \\ \dfrac{V_{dc}}{2} + \dfrac{I}{\sqrt{2}\omega C}\sin\omega t & (-\phi/\omega \le t < \phi/\omega) \\ V_{dc} & (\phi/\omega \le t < \pi/\omega) \end{cases} \tag{4}$$

The commutation capacitor is usually charged or discharged around the peak of the inverter current because the SVC can take only a leading reactive power. When the commutation period is much shorter than a period of the supply frequency, the inverter current i can be assumed as a constant value during the commutation. Therefore, the

rate of voltage rise, dv_L/dt is given by

$$\frac{dv_L}{dt} = \frac{\sqrt{2}I}{2C}. \tag{5}$$

The rated supply current of the 10-kVA laboratory setup used in the following experiments is 30 A, and the turn ratio of the quad-series transformers is 1:3. Thus, the rated rms current of each inverter is 10 A. The rate of voltage rise is designed to be $dv/dt = 7$ V/μs at the rated current where the commutation period of time is 30 μs, that is, ten times as long as the storage time of the transistor. The required capacitance value of the commutation capacitor is obtained from (5) as follows:

$$C = \frac{\sqrt{2} \times 10}{2 \times 7 \times 10^6} = 1.0\ \mu\text{F}.$$

Here, consider the capacitance of the commutation capacitor in a case of using a GTO thyristor rated at 6 kV and 6 kA, which is used around a dc-link voltage of 3 kV and a rms current of 2 kA. The capacitance scaled up for the GTO thyristor is

$$1.0 \times 10^{-6} \times \frac{2 \times 10^3}{10} \frac{250}{3 \times 10^3} = 17\ \mu\text{F}.$$

In general, the GTO thyristor is equipped with a snubbing capacitor of 6 μF. The scaled commutation capacitor is three times as large as that in the generally-designed snubbing capacitor. The voltage rise rate of the scaled commutation capacitor is

$$\frac{dv}{dt} = \frac{\sqrt{2}I}{2C} = \frac{\sqrt{2} \times 2 \times 10^3}{2 \times 17 \times 10^{-6}} = 83\ \text{V}/\mu\text{s},$$

while dv/dt in the generally-designed snubbing capacitor is given by

$$\frac{dv}{dt} = \frac{\sqrt{2}I}{C} = \frac{\sqrt{2} \times 2 \times 10^3}{6 \times 10^{-6}} = 470\ \text{V}/\mu\text{s}.$$

Note that dv/dt in the commutation capacitor is 1/6 of that in the generally-designed snubbing capacitor. The reason is that the inverter current flows through either upper or lower snubbing capacitor during commutation in the conventional snubbing circuit consisting of a 6-μF capacitor, a resistor and a diode, because the time constant decided by the 6-μF capacitor and the resistor is longer than the commutation period. If the snubbing capacitor were increased to 36 μF, that is, six times as large as the generally-designed capacitor, dv/dt could be reduced to 1/6, while the loss caused by the 36-μF capacitor is six times as large as that caused by the 6-μF capacitor. Installing a 17-μF commutation capacitor without causing any snubbing loss significantly improves the turn-off capability of the GTO thyristor for protection against overcurrent in line-to-line or line-to-ground faults.

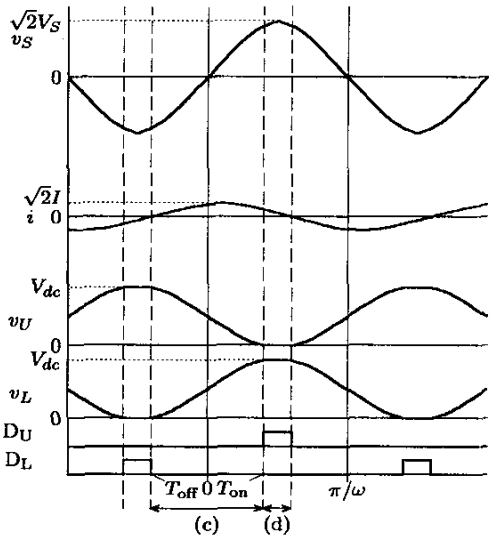

Fig. 6. Voltage and current waveforms in the case of connecting the starting resistor R_{dc}.

IV. Starting Method of the SVC Equipped with the Commutation Capacitor

In normal operation, the electric charge stored in the commutation capacitor is discharged by the inverter current, and it is not dissipated. However, if a transistor shorts out the charged commutation capacitor, a significant surge voltage and spike current may occur. Even when the SVC starts up, it is required to avoid such a short circuit of the commutation capacitor. Therefore, the following special sequence is developed to achieve zero-voltage-switching operation during the start up of the SVC.

A. Soft-Starting Sequence

No gating signal is provided to any transistor before start of the SVC. The six free-wheeling diodes form a diode bridge rectifier. Assuming that no power consumption occurs in the SVC, the dc-link capacitor is charged to the maximum line-to-line voltage of the supply. If a transistor were turned on, the transistor would short the commutation capacitor out.

At first, the starting resistor R_{dc} is connected with the dc-link capacitor. The voltage and current waveforms are shown in Fig. 6. The starting resistor works as a dc load for the diode rectifier, so that the dc-link voltage slightly decreases. Then each free-wheeling diode conducts only around the peak voltage of the supply to provide a dc current to the starting resistor R_{dc}. A gating signal can be provided to a transistor while the corresponding diode, which is connected in anti-parallel with the transistor, is conducting. Here no transistor shorts out the commutation capacitor because the voltage across the commutation capacitor is zero.

In the next step, the time period of providing the gating signal is extended as shown in Fig. 7. The transistor is turned on with zero-voltage and zero-current switching

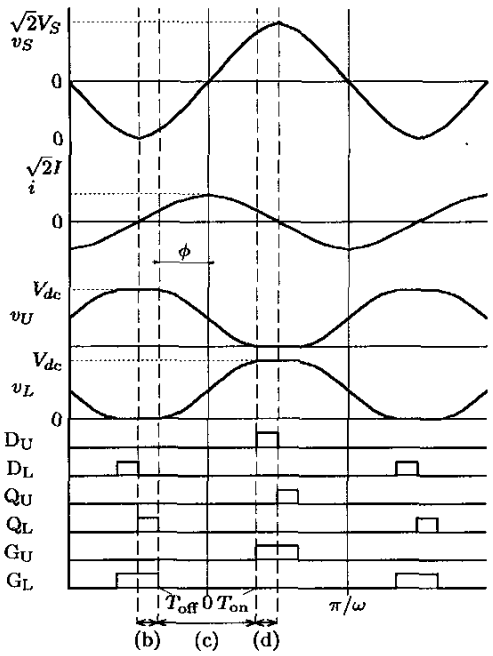

Fig. 7. Voltage and current waveforms during the starting sequence.

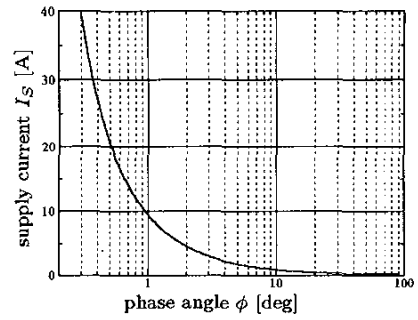

Fig. 8. Relationship between commutation angle ϕ and reactive power I_{Sq}.

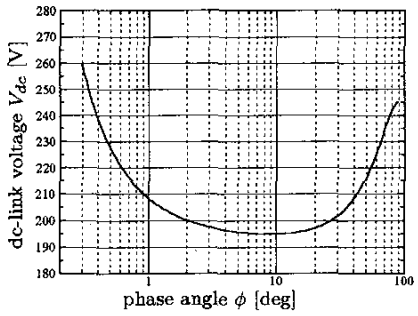

Fig. 9. Relationship between commutation angle ϕ and dc-link voltage V_{dc}.

as soon as the corresponding diode turns off, because the gating signal is continuously provided. Note that for example, lower capacitor voltage v_L in Fig. 7 is zero during the conducting period of transistor Q_L, so that removing the gating signal turns Q_L off with zero-voltage switching. Figs. 5 and 7 are the same, except for the turn-off timing of the transistor. Extending the conduction period of the transistor increases the conduction period of the diode, and then the operating condition approaches Fig. 5.

However, quick extension of the conducting period may cause flux saturation in the quad-series transformer due to producing a dc or low-frequency voltage in the inverter output. To avoid flux saturation, the turn-off timing should be gradually delayed from 90° to 0. After the delay angle reaches almost zero, the starting resistor can be detached from the dc link because the conducting period of the diode and transistor has already been established.

B. Controllable Range of Leading Reactive Power

Taking the commutation period ϕ into account, the fundamental component of the inverter output voltage in (4) is given by

$$V_f = \frac{2\omega}{\pi}\int_{-\pi/2\omega}^{\pi/2\omega} v_L(t)\sin\omega t\,dt = \frac{(2\phi+\sin 2\phi)I}{2\pi\omega C}. \quad (6)$$

The fundamental voltage at the primary side of the transformer is m/nV_f, where m is a number of series-connected inverters, and n is the turn ratio of the series-connected transformer. Disregarding the active power, the reactive-power component included in the supply current is obtained from the circuit shown in Fig. 1 as:

$$I_{Sq} = nI = \frac{m/nV_f - V_S}{\omega L_S}. \quad (7)$$

Applying (3) and (6) to (7) yields the reactive-power component I_{Sq} as follows:

$$I_{Sq} = \frac{2n^2\pi\omega C}{2m\phi + m\sin 2\phi - 2n^2\pi\omega^2 L_S C}V_S. \quad (8)$$

The dc-link voltage V_{dc} is given by

$$V_{dc} = \frac{2\sqrt{2}n\pi\sin\phi}{2m\phi + 2\sin 2\phi - 2n^2\pi\omega^2 L_S C}V_S. \quad (9)$$

Figs. 8 and 9 show the supply reactive current I_{Sq} and the dc-link voltage V_{dc} with respect to the phase angle ϕ. The circuit constants shown in Table I are used for this calculation. The minimum value of the dc-link voltage V_{dc} appears at $\phi = 9.8°$, which is about 195 V. In the range of $\phi < 9.8°$, I_{Sq} increases with the dc-link voltage V_{dc}, according to decreasing ϕ. The control characteristics are almost the same as those without commutation capacitors, and a feedback control of the reactive power allows a response as fast as 3 ms in this range.

However, V_{dc} increases with ϕ in the range of the phase angle $\phi > 9.8°$, whereas almost no change occurs in I_{Sq}. This is caused by the wave shape of the output voltage, which changes from trapezoid to sinusoid as shown in

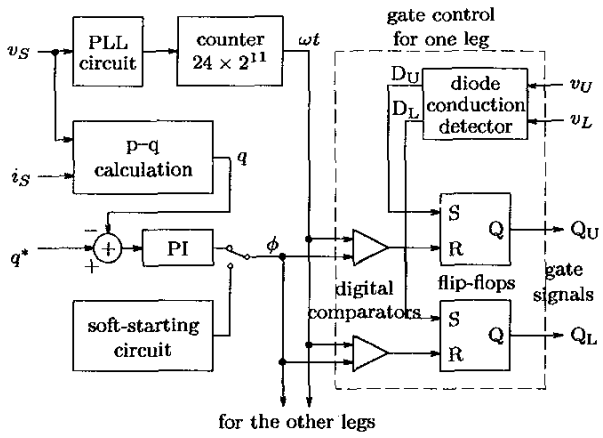

Fig. 10. Block diagram of control circuit.

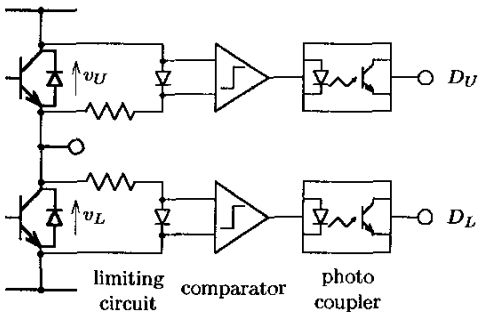

Fig. 11. Diode conduction detector.

Figs. 5 and 6. Irrespective of the rise of the dc-link voltage V_{dc}, the fundamental output voltage V_f is almost constant. Thus, a wide control of ϕ is required to adjust the reactive power in this range, which may cause a flux saturation in the quad-series transformer and/or instability in feedback control. The experimental setup introduces feedback control in the range of $\phi < 10°$, thus resulting in stable control of a leading reactive power in a range from 3% to 100%.

V. Control Circuit

Fig. 10 shows a block diagram of the control circuit. A PLL (phase-locked loop) circuit with a 16-bit counter is used to generate the phase information ωt. The PLL circuit produces a pulse train of 3 MHz, which is used as a clock pulse for the counter. The counter in Fig. 10 consists of a cascade of an 11-bit binary counter and a 24-step counter, and the PLL circuit synchronizes the counters with the supply frequency.

A gate controller for one leg consists of two 16-bit digital comparators, two flip-flops, and a diode conduction detector. The diode conduction detector shown in Fig. 11 detects a negative voltage across the transistor, that is, an on-state voltage of the free-wheeling diode, when the diode is conducting. The diode conduction detector consists of a specially-designed comparator and a photo coupler for isolating the control circuit from the main circuit. Each

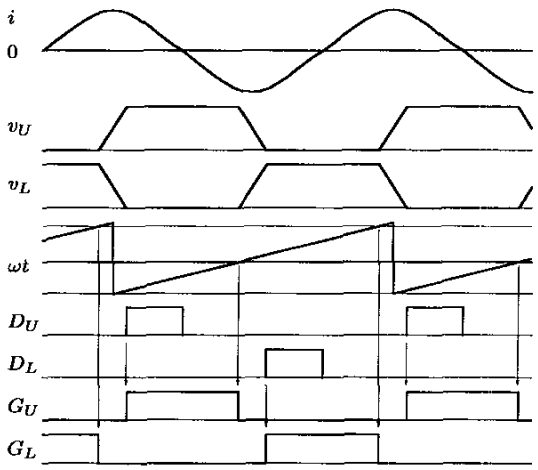

Fig. 12. Internal signals inside the gate controller.

comparator is equipped with a resistor and diode aimed at limiting the input voltage while the corresponding transistor is not conducting.

Fig. 12 shows an internal signal inside the gate controller. The digital comparator decides the turn-off timing for the corresponding transistor by means of comparison of the phase information ωt with the phase-shift reference ϕ. On the other hand, the turn-on timing comes from the diode conduction detector. Each flip-flop is reset by a turn-off signal from the phase control circuit, and set by the conduction signal of the corresponding free-wheeling diode as shown in Fig. 12. The turn-on timing for the transistor is not controlled by the control circuit but decided by the conduction state of the free-wheeling diode. This is one of the simplest and most reliable ways to avoid the short circuit of the commutation capacitor.

Either the PI controller or the soft-starting circuit provides the phase reference ϕ to the gate controller. The reactive power drawn by the SVC is controlled by a feedback loop based on the instantaneous reactive power theory [1]. The angle ϕ is set to 90° before starting SVC, and gradually approaches 0 in the soft-starting sequence. The PI controller is disabled to avoid the so-called "wind-up phenomenon" during the starting sequence, and it is enabled after the starting sequence is completed.

VI. Experiment Results

Figs. 13-16 show experimental waveforms. The SVC takes a leading reactive power rated at 10 kvar in Fig. 13, and takes a leading reactive power as small as 0.7 kvar in Fig. 14. Since the upper commutation capacitor voltage v_{1aU} is a rectangle wave shape, the 24-step voltage wave shape appears in the line-to-line voltage generated by the SVC, v_{ab} in Fig. 13. The synthesized voltage v_{ab} is almost sinusoidal in Fig. 14 because v_{1aU} has a trapezoidal shape. This means that the commutation capacitors have an additional ability of reducing higher-order harmonics. Note that all the transistors are turned on or off around the peak

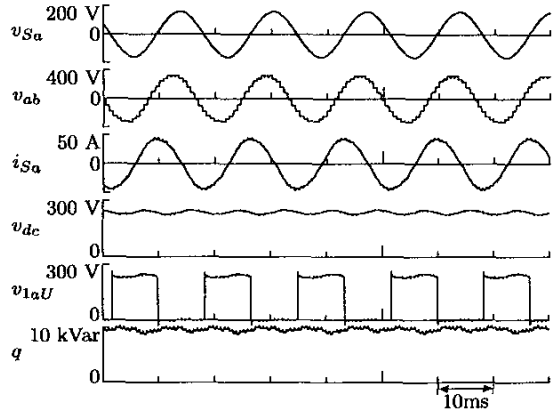

Fig. 13. Experimental waveforms when the SVC takes a leading reactive power rated at 10 kvar.

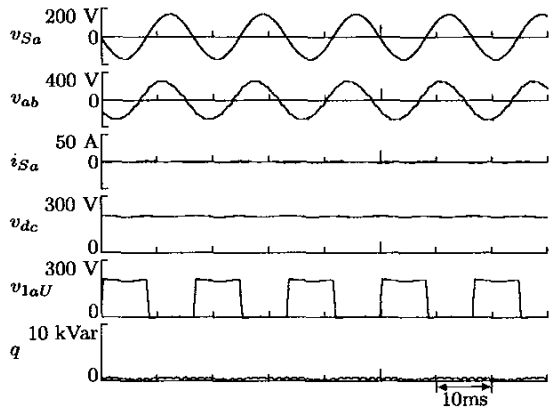

Fig. 14. Experimental waveforms when the SVC takes a leading reactive power as small as 0.7 kvar.

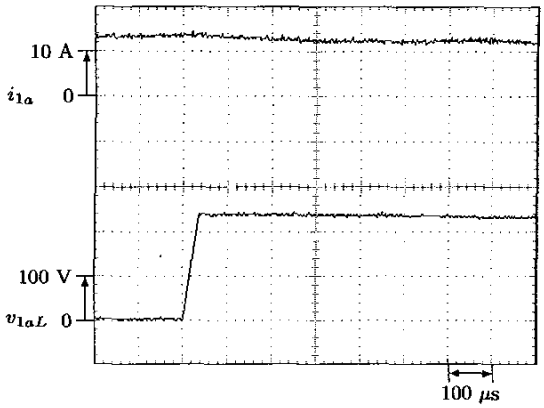

Fig. 15. Close-up waveforms under the 10-kvar operation.

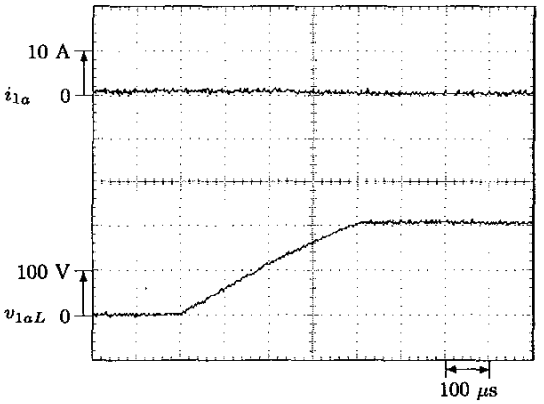

Fig. 16. Close-up waveforms under the 0.7-kvar operation.

of i_{Sa}. Large switching losses and stresses may occur in the transistors if any soft-switching technique is not applied to the inverters.

Figs. 15 and 16 are close-up waveforms of the inverter current i_{1a} and the lower commutation capacitor voltage v_{1aL}. After the transistor is turned off, the commutation capacitor voltage v_{1aL} gradually rises up and reaches 230 V in Fig. 15. The commutation period is 35 μs which is much longer than the turn-off or rising time inherent in the transistor, so that the switching losses and stresses are reduced.

Fig. 17 shows experimental results in soft starting. The dc-link voltage before start up is about 260 V in (a) when the starting resistor ($R_{dc} = 1$ kΩ) is connected to the dc link. No gating signal is provided to any transistor, but each free-wheeling diode conducts for 4 ms around the peak of the supply voltage. As the phase angle ϕ is decreased, the dc-link voltage v_{dc} gradually decreases, as shown in (b) and (c). The conducting periods of both diodes and transistors are increased, and the v_{1aL} approaches a rectangle waveform. In Fig. 17(d), the SVC completes the starting sequence, and runs in a normal operating condition. The starting resistor can be removed from the dc link after the starting sequence. The proposed starting sequence allows the SVC to start up without short circuit of the commutation capacitors.

VII. Conclusion

A new soft-switching technique using "commutation capacitors" has been proposed for a large-capacity SVC based on voltage-source square-wave inverters. The experimental results obtained from the 10-kVA laboratory setup show such an advantage of the proposed method as a significant reduction of surge voltage and switching loss without dissipation of the electrical charge in the commutation capacitors. In addition, the soft-starting sequence for the soft-switching SVC is also proposed and a controllable range of reactive power is theoretically derived.

The proposed soft-switching technique has a simple circuit configuration and does not increase the current or voltage ratings of the switching devices. Therefore, it is suitable for large-capacity SVCs required to draw a leading reactive power from the supply.

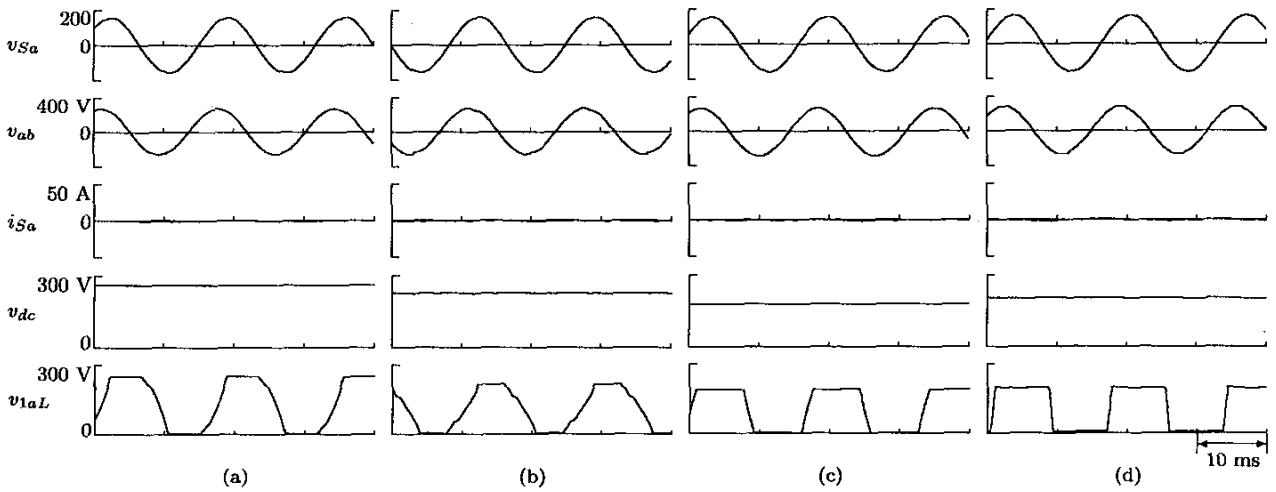

Fig. 17. Experimental waveforms in starting sequence, (a) before start, (b) $\phi = 60°$, (c) $\phi = 30°$, and (d) the starting sequence is completed.

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