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Fabrication of a logic gate circuit based on ambipolar field-effect transistors with thin films of C_{60} and pentacene

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Abstract

Ambipolar field-effect transistor (FET) devices were fabricated with a heterostructure of C_{60} and pentacene, and their p- and n-channel field-effect mobilities were studied as a function of thickness of pentacene thin-films. The observed dependences of the μ values were interpreted in terms of the morphology of the thin films and the band structure of C_{60}/pentacene heterostructure. A complementary metal-oxide-semiconductor (CMOS) circuit was fabricated by integration of two ambipolar FETs, aiming at realization of a new CMOS inverter circuit composed of FETs with the same device structure. The gain of 4, the threshold voltage of 85 V, and the complex output characteristics were explained on the basis of the properties of the component FET devices.

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1. Introduction

Field-effect transistors (FETs) with thin films of fullerenes have been extensively studied owing to their potential applications towards next-generation electronic devices [1-10]. The fullerene FET device, first fabricated with thin films of C_{60} by Haddon et al. [1], showed n-channel properties with a field-effect mobility μ of 0.08 – 0.30 $cm^2\ V^{-1}\ s^{-1}$, and it was raised to 0.56 $cm^2\ V^{-1}\ s^{-1}$ by a recent measurement of FET-properties under 10^{-9} Torr [4]. The highest μ value among the p-channel FETs with thin-films of organic molecules is 1.5 $cm^2\ V^{-1}\ s^{-1}$ in a pentacene FET [11].

A combination of two independent C_{60} and pentacene FET devices led to a complimentary metal-oxide-semiconductor (CMOS) inverter circuit [5]. The CMOS circuits are incorporated into various types of chips such as memories and microprocessors owing to their low-power consumption, good-noise margin and ease of design [12,13]. The importance of CMOS logic gate circuits lies in the FET devices with thin films of organic molecules, which enable realization of computer chips with flexibility, portability, and shock-resistance. An ambipolar FET device with a heterostructure of C_{60} and pentacene that we have recently fabricated showed μ values as high as 10^{-3} – 10^{-2} $cm^2\ V^{-1}\ s^{-1}$ [10]. For further application of these CMOS circuits, simpler and easier processes for fabrication are needed, and one of the possibilities is a proper use of ambipolar FET devices as their components, because such a circuit can be realized with only one type of ambipolar FET device.

The present letter reports on our measurement of the dependence of the μ values on the thickness of pentacene thin-films in C_{60}/pentacene heterostructure FET devices in order to clarify the relationship between the device structure and the ambipolar properties. Furthermore, we have fabricated a CMOS inverter circuit by integration of two ambipolar FETs on SiO_2/Si substrate to study the output characteristics of the inverter circuit based on their FET properties.

2. Experimental

Schematic representations of heterostructure FET devices of C_{60} and pentacene are shown in Fig. 1. All FET devices fabricated take the middle–contact device structure. Details of fabrication of the FET device were described elsewhere [10]. The channel length L and the channel width W of the device were 30 and 2500 μm, respectively. The characteristics of the FET devices and CMOS inverter circuit were measured at 10^{-6} Torr and 300 K. The FET properties were measured in the p- and n-channel measurement modes shown in Fig. 2(a). The absolute value of the leak current produced by applying the gate voltage V_G, $|I_G|$, was always below 0.2 pA at $|V_G| < 120$ V. The I_G never affected the drain current, I_D, and the insulating behavior of SiO_2 was steadily maintained. The diffusion of C_{60} and pentacene into the SiO_2 layer by annealing was deemed negligible, because $|I_G|<$ 0.2 pA after annealing of the device at 140 ˚C for 6 d.

3. Results and discussion

3.1. I_D - V_{DS} plots of C_{60}/pentacene heterostructure FET device

Plots of the I_D *vs.* drain-source voltage V_{DS} for the C_{60}/pentacene heterostructure FET device (Fig. 1(a)) are shown in Figs. 2(b) and (c). In the p-channel mode, the $|I_D|$ increases supra-linearly with increasing $|V_{DS}|$ at low values of $|V_G|$, and it decreases with increasing $|V_G|$ up to 30 V, as shown in Fig. 2(b). The I_D – V_{DS} plots show typical p-channel enhancement FET properties at high $|V_G|$. In the n-channel mode, the I_D increases supra-linearly with increasing V_{DS} at low values of V_G (Fig. 2(c)). The I_D decreases with increasing V_G and reaches a minimum value at $|V_G| \approx 50$ V. Further increase in $|V_G|$ leads to the enhancement of I_D, and the I_D – V_{DS} plots show n-channel properties (Fig. 2(c)). The p- and n-channel field-effect mobilities, μ_p and μ_n, are estimated to be 3.7×10^{-2} and 5.8×10^{-3} $cm^2 V^{-1} s^{-1}$, respectively, using the general formula for the linear region [13]. Thus, the ambipolar FET properties are observed in the device structure shown in Fig. 1(a).

The energy levels of Au/pencene/C_{60}, shown in Fig. 3(a), are drawn following Refs. [14] and [15]. The Fermi level, ε_F, is very close to the valence band of pentacene, while the ε_F is also close to that of the conduction band of C_{60}. Therefore, the injection probability of the hole in pentacene should be higher than that of electron, leading to the p-type behavior in the pentacene thin-films. On the other hand, the injection probability of electron in C_{60} should be higher than that of the hole. This leads to the n-type behavior in the C_{60} thin-films. Consequently, the ambipolar FET property in the C_{60}/penetacene heteostructure FET device originates from the n-channel conduction in the C_{60} thin-films and the p-channel conduction in the pentacene thin-films.

The pentacene/C_{60} FET device (Fig. 1(b)) also exhibited ambipolar FET properties after annealing. The μ_p and μ_n values were 3.1×10^{-5} and 1.9×10^{-3} $cm^2 V^{-1} s^{-1}$, respectively. This μ_p value of the present FET device was smaller by three orders of magnitude than that in the FET device shown in Fig. 1(a). This observation can be accounted for by the fact that the bottom-contact type pentacene FET exhibits lower FET properties than the top contact-type FET.

3.2. Thickness dependence of μ_p and μ_n in C_{60}/pentacene heterostructure FET device

The dependences of μ_p and μ_n on the thickness of pentacene in the C_{60}/pentacene heterostructure FET device (Fig. 1(a)) are shown in Fig. 3(b); the thickness of C_{60} thin-films was fixed to 80 nm for all the samples. The FET devices without annealing showed only p-channel properties, and the μ_p was independent of the thickness of the pentacene thin-film. The μ_p for the FET devices with smaller thickness of pentacene than 20 nm decreases rapidly by annealing the device at 120 ˚C for 18 h, as shown in Fig. 3(b). This decrease can be explained by the assumption that the pentacene grains are sparsely distributed in the channel region by sublimation of pentacene by annealing. The sublimed pentacene seems to be intercalated into the spatial sites of C_{60} thin-films on the pentacene thin-films. The sparse distribution of pentacene grains suppresses the hopping of the carriers between the crystalline grains because of a decrease in the overlap between the orbitals, leading to the lowering of the μ_p. No such sparse distribution of pentacene occurs in the channel region of the FET devices with larger thickness of pentacene thin-films even if parts of pentacene were sublimed by annealing, i.e., the μ_p should not decrease in the FET device. Actually, the μ_p value remained almost constant before and after the annealing of the FET device with large thickness of pentacene thin-films.

The μ_p value of the FET device after the annealing decreases with decreasing the thickness of pentacene thin-films below 25 nm, as shown in Fig. 3(b). The μ_p value is leveled above 25 nm. The pentacene grains should be more sparsely distributed because of the sublimation caused by the annealing, when the thickness of the pentacene thin-films is decreased. This should lead to the decrease in the μ_p value.

The annealing produced the n-channel FET properties in the FET device. The n-channel properties are associated with the C_{60} thin-films. The μ_n value shows a maximum in the FET device with 25 nm thickness of pentacene, and the μ_n decreases by one order of magnitude in the FET device with 17 nm thickness of pentacene. This finding is ascribed to the lowered flatness of interface between the thin-films of pentacene and C_{60} owing to the intercalation of pentacene into the spatial sites of the C_{60} thin-films. The low flatness should lead to the trapping of electron carriers. On the other hand, the μ_n value decreases by one order of magnitude when the thickness of pentacene increases to 40 nm. As seen from Fig. 3(c), the large accumulation of electron occurs in the channel region of the C_{60} thin films caused by a large band bending when the thickness of the pentacene thin-films is small, while only small accumulation of electrons is expected owing to a small band bending when the thickness is larger. If this is the case, the V_T in the n-channel operation should increase with increasing thickness of pentacene. In fact, the V_T increases from 100 to 180 V with increasing thickness from 25 to 40 nm. Thus, the lowering of the field effect on the C_{60} thin-films due to the large thickness of pentacene leads to the decrease in the μ_n.

3.3. CMOS inverter circuits composed of two C_{60}/pentacene heterostructure FET devices

A CMOS inverter circuit was fabricated with two ambipolar C_{60}/pentacene FETs (Fig. 1(a)). A schematic representation and a picture of the circuit are shown in Figs. 4(a) and (b), respectively. Two FETs are named devices I and II, as shown in Fig. 4(a). The plots of I_D –

V_{DS} were measured individually for these devices in the normal p- and n-channel measurement modes (Fig. 2(a)). The μ_p and μ_n values for device I were 3.1×10^{-1} and 2.3×10^{-5} cm^2 V^{-1} s^{-1}, respectively, while those for device II were 3.1×10^{-1} and 4.0×10^{-5} cm^2 V^{-1} s^{-1}, respectively. The I_D – V_{out} plots for these devices are shown in Fig. 4(c). The I_D – V_{out} plots were obtained from the I_D – V_{DS} plots in the p-channel mode for device I, and from the I_D – V_{DS} plots in the n-channel mode for device II. The V_{out}- V_{in} plot (Fig. 5(a)) can be predicted for this inverter circuit from the intercepts of the I_D – V_{out} plots (Fig. 4(c)) for these devices at the same V_{in} value. The predicted I_D – V_{out} plot (Fig. 5(a)) shows a rapid decrease in V_{out} at high V_{in} .

As shown in Fig. 4(a), the source of device II is grounded, while that of device I is connected to a power supply, V_{DD}, of 120 V. The experimental output characteristics shown in Fig. 5(b) were measured by the way represented in Fig. 4(a). The consistency between the predicted (Fig. 5(a)) and the experimental (Fig. 5(b)) output characteristics implies that these two FET devices operate properly in this CMOS circuit. The V_{out} value of $\approx$90 V at V_{in} < 80 V was observed, while the V_{out} of ~30 V was observed at V_{in} > 90 V. Thus, no vanishing of V_{out} was observed in this CMOS circuit even at high V_{in}. This feature can be ascribed to the fact that neither device I nor II is ever fully switched off because the CMOS circuit consists of two ambipolar FETs, as in the CMOS circuits reported in Ref. [7]. The gain and the threshold voltage of this circuit, V_{TIC}, were 4 and 85 V, respectively. This high V_{TIC} originates from the threshold voltage $|V_{Tp}|$ of 46 V for the p-channel FET property in device I, and the high threshold voltage V_{Tn} of 51 V for the n-channel FET property in device II. In this case, the V_{TIC} is expected to lie between 51 and 74 V.

The CMOS circuits with the same ambipolar FETs are expected to be useful for a simple and low-cost fabrication process of electronic devices, although the use of ambipolar FET devices leads to a lowering of gain because of a background current flowing through this circuit. A slight increase in V_{out} was observed with increasing V_{in} at $V_{\text{in}} < 80$ V. This finding directly reflects the fact that depletion of the hole occurs in device II at $V_{\text{in}} < 70$ V. Furthermore, a slight increase was observed again at $V_{\text{in}} > 110$ V being due to the depletion of electron in device I. The V_{out} and V_{in} values in this circuit are high because of the low C_0 and the thick layer (420 nm) of SiO_2. Such high values of V_{out} and V_{in} should be decreased by using either a high ε_x or a very thin insulating layer.

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Figure captions

Fig. 1. Cross sectional views of C_{60}/pentacene FET devices. (a) A thin film of C_{60} is deposited on a thin film of pentacene, and (b) a thin film of pentacene is deposited on a thin film of C_{60}.

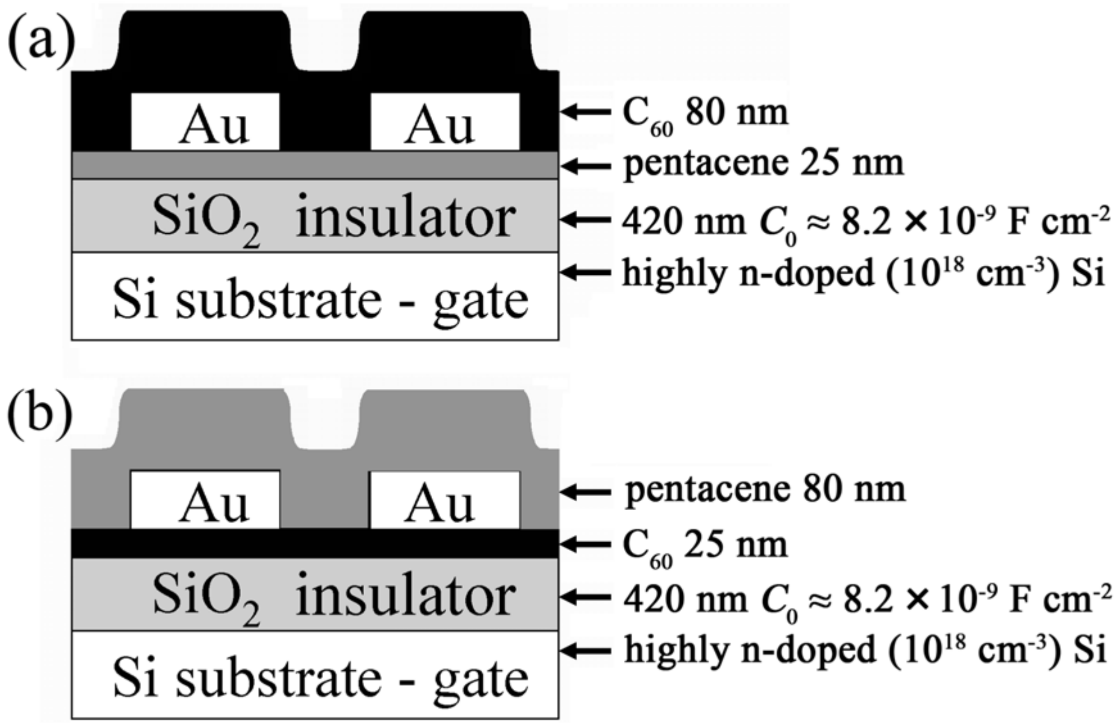
Fig. 2. (a) Schematic representation of p- and n-channel measurement circuits. I_D -V_{DS} plots of the C_{60}/pentacene heterostructure FET device measured in (b) the p-channel measurement-mode and (c) the n-channel measurement mode. The FET device was annealed at 140 ˚C for ≈ 6 d under vacuum of 10^{-6} Torr before the measurements of FET properties.

Fig. 3. (a) Energy band diagrams of the C_{60}, pentacene and Au electrode. (b) Dependences of μ_p and μ_n on the thickness of pentacene thin-films for the C_{60}/pentacene FET device. ●: μ_p before the annealing of the device. ◆: μ_p and ■: μ_n after the annealing of the device at 120 ˚C for 18 h. (c) Band bending of energy levels in the FETs with different thicknesses of pentacene thin-films at positive V_G.

Fig. 4. (a) Schematic representation and (b) picture of CMOS inverter circuit. (c) I_D – V_{out} plots for devices I and II after the annealing of the CMOS chip at 140 ˚C for 18 h, where $V_G = V_{in} - V_{DD}$ and $V_{DS} = V_{DD} - V_{out}$ for device I, and $V_G = V_{in}$ and $V_{DS} = V_{out}$ for device II. Very low-I_D region is shown to clarify the properties at high V_{in}

in the right figure of (c), where plots drawn with the same color correspond to those for the same V_{in}, and the intercepts at the same V_{in} are drawn by large closed circles.

Fig. 5. (a) Theoretical V_{out}- V_{in} plot obtained from the intercepts of the I_{D} – V_{out} plots shown in Fig. 4(c). (b) V_{out} – V_{in} plot measured for the CMOS inverter after the annealing at 140 ˚C for 18 h. The V_{out} -V_{in} plot shown in (b) was directly measured using the circuit shown in Fig. 4(a).



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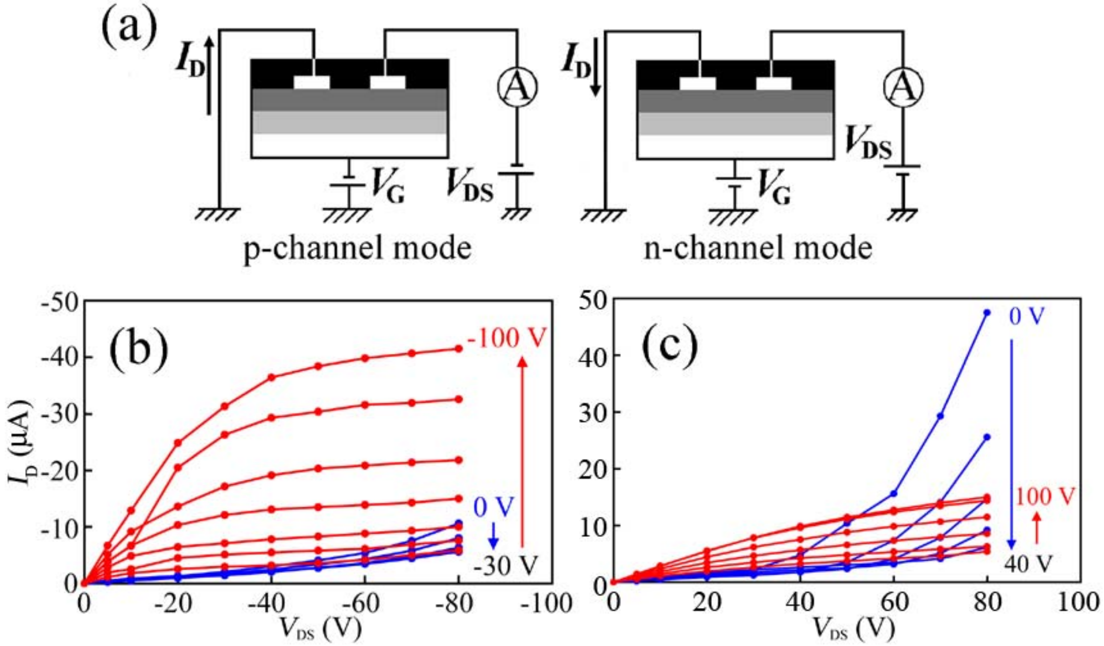

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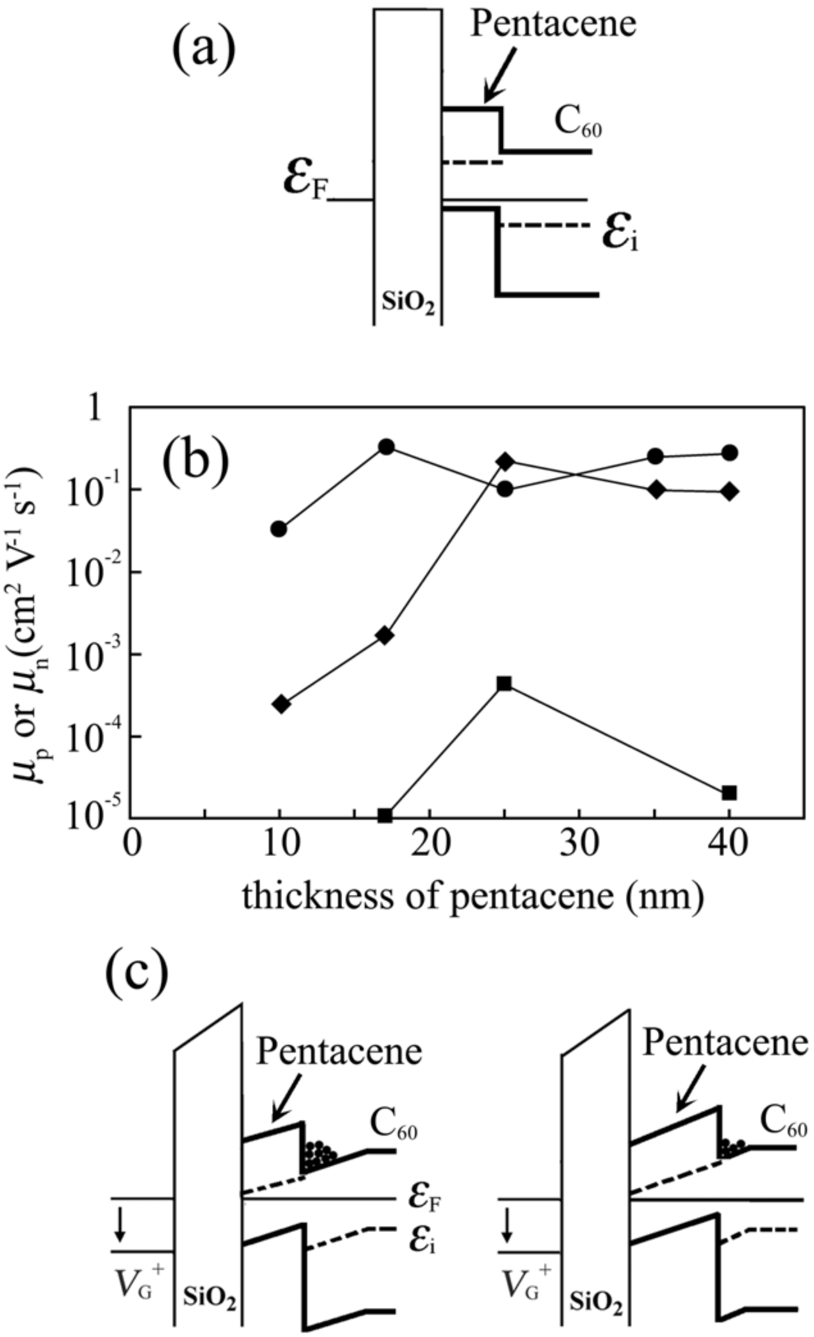

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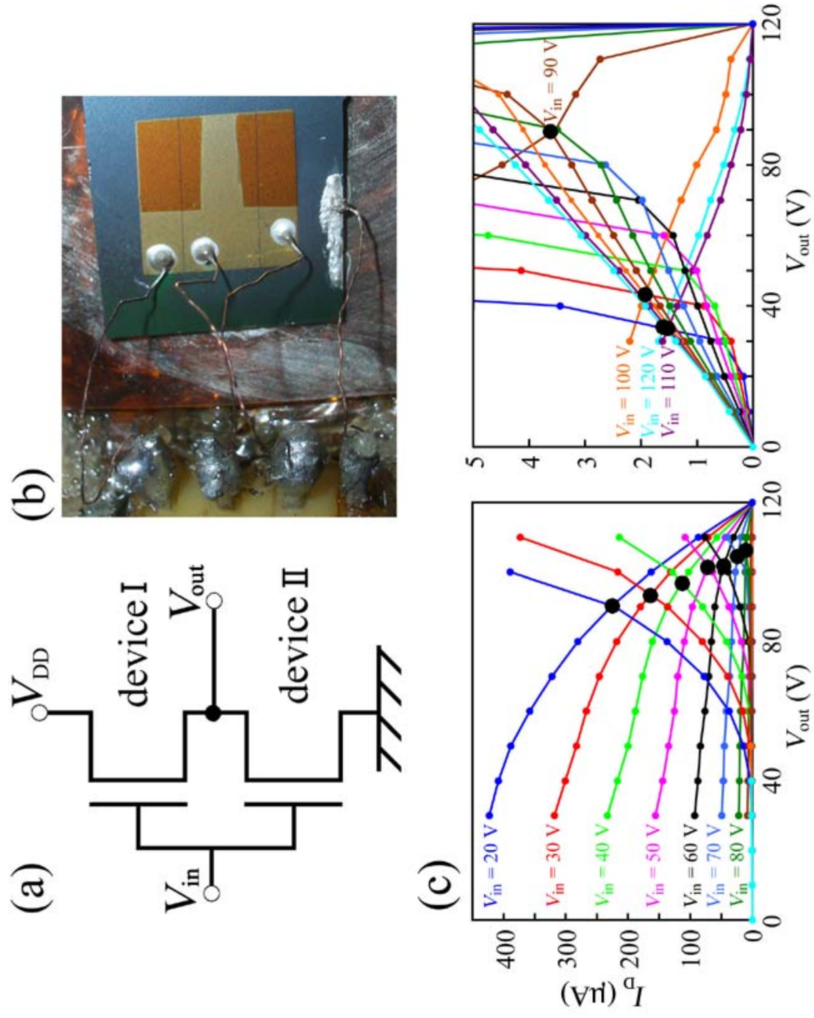

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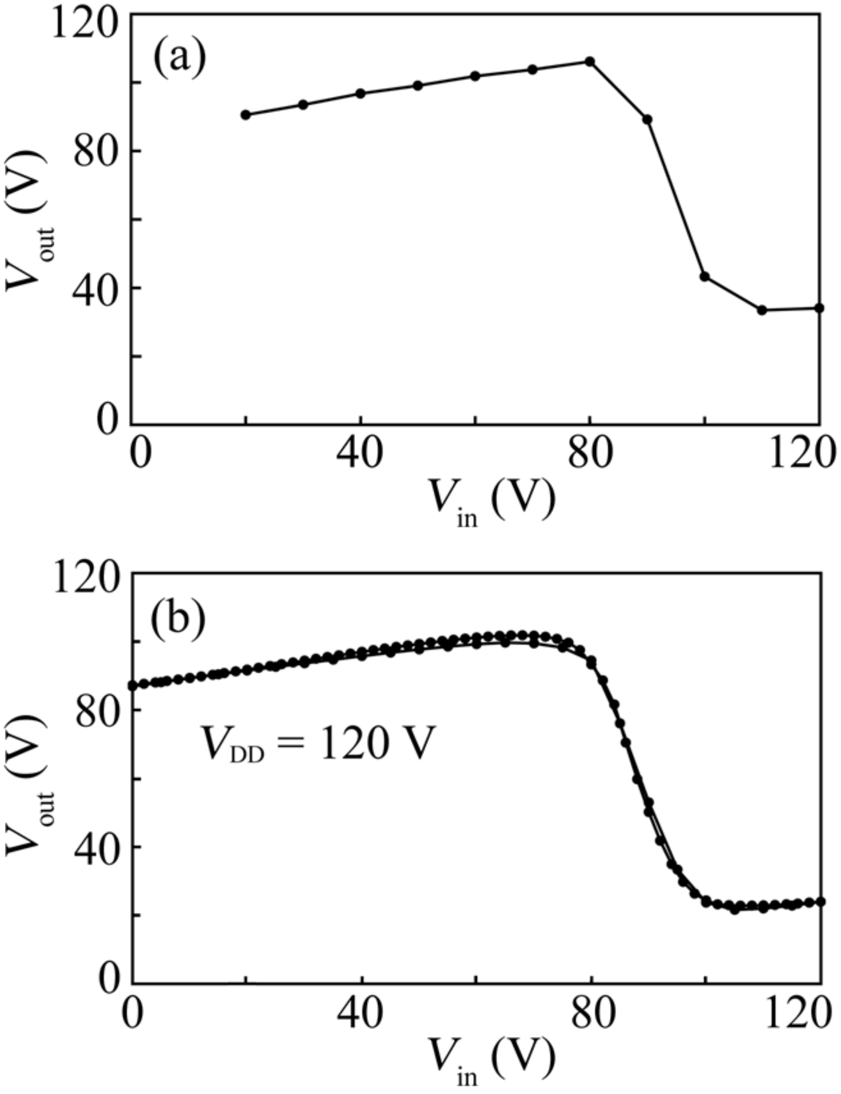

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