Engineering

Electrical Engineering fields

Okayama University *Year* 1998

A 2-MHz 2-kW voltage-source inverter for low-temperature plasma generators: implementation of fast switching with a third-order resonant circuit

Hideaki Fujita
Okayama University

Hirofumi Akagi
Okayama University

A 2-MHz 2-kW Voltage-Source Inverter for Low-Temperature Plasma Generators: Implementation of Fast Switching with a Third-Order Resonant Circuit

Hideaki Fujita, *Member, IEEE*, and Hirofumi Akagi, *Fellow, IEEE*

***Abstract*—This paper presents a specially designed third-order resonant circuit intended to achieve fast switching operation for a voltage-source series-resonant inverter using four MOSFET's. The third-order resonant current superimposed on a sinusoidal load current helps to quickly charge or discharge the output capacitance of each MOSFET. This results not only in a reduction of the commutation period which is required to turn the MOSFET on and off, but also in an improvement of the displacement factor at the output of the inverter. Moreover, the third-order resonant circuit acts as a low-pass filter to suppress the parasitic oscillation between line inductance and stray capacitance. The viability and effectiveness of the third-order resonant circuit is verified by a 2-MHz 2-kW prototype inverter developed for a low-temperature plasma generator.**

***Index Terms*— High-frequency inverter, low-temperature plasma, output capacitance, power MOSFET.**

I. Introduction

LOW-TEMPERATURE plasma has been applied to surface treatment processes for metallic parts, semiconductor materials, and so on [1]. A high-frequency strong magnetic field produces low-temperature plasma from low-pressure gas and sustains it. A high-frequency power supply of 2–10 kW is required to generate the magnetic field in a frequency range of 2–13.56 MHz, which is too high for conventional semiconductor devices to perform their switching operations. A linear amplifier using bipolar junction transistors (BJT's) or vacuum tubes has been applied to high-frequency power supplies for plasma generators at the expense of efficiency and size.

The emergence of fast switching devices such as power MOSFET's and static induction transistors (SIT's) has made it possible to implement high-frequency inverters for induction heating and plasma discharge surface treating applications [2]–[10]. However, a voltage-source inverter using MOSFET's has the following difficulty of operating at more than 1 MHz: turning a MOSFET on forms a short circuit of an electric charge stored in its inherent output capacitance, thus resulting in increased switching losses. The short circuit induces a voltage surge and current spike phenomenon as a result of the resonance between the output capacitance and a line inductance. To avoid the short circuit, each MOSFET should be turned on after finishing the discharge of the output capacitance. This contributes to degrading the displacement factor at the output of a high-frequency inverter operated at more than 1 MHz because the commutation period, which is required to completely discharge the output capacitance, can no longer be negligible. Operating the inverter at a poor displacement factor is accompanied by increased voltage and/or current ratings, so that the inverter efficiency goes down. Moreover, a nonnegligible difference exists in the output capacitance among four MOSFET's used in a single-phase H-bridge voltage-source inverter. This may induce differences in the rise time of each MOSFET and in the magnitude of voltage surge appearing across each MOSFET. Connecting a lossless snubber capacitor in parallel with each MOSFET results in adjustment-free operation without voltage surge, although the displacement factor at the output of the inverter also decreases as the capacitance of the snubber capacitor is increased.

This paper proposes an approach for improving the high-frequency performance of a voltage-source series-resonant inverter using four MOSFET's for very high-Q induction heating applications. This inverter is characterized by connecting a third-order resonant circuit at its ac terminals, which enables the output capacitance of each MOSFET to be discharged more quickly. This results not only in a reduction of the commutation period, during which all the four MOSFET's and diodes remain off, but also in an improvement of the displacement factor at the output of the inverter. The minimum commutation period is as short as the rise or fall time of the MOSFET. Experimental results obtained from a 2-MHz 2-kW voltage-source series-resonant inverter for a low-temperature plasma generator, along with analytical results, verify the viability and effectiveness of the third-order resonant circuit introduced in this paper.

Paper IPCSD 98–58, presented at the 1997 Industry Applications Society Annual Meeting, New Orleans, LA, October 5–9, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript released for publication July 27, 1998.

The authors are with the Department of Electrical Engineering, Okayama University, Okayama, 700-8530 Japan.

Publisher Item Identifier S 0093-9994(99)00448-X.

II. Switching Operation Considering the Output Capacitance of MOSFET

Fig. 1 shows the simplified circuit of a voltage-source series-resonant inverter, and Fig. 2 depicts the switching modes in it, considering the output capacitance of each

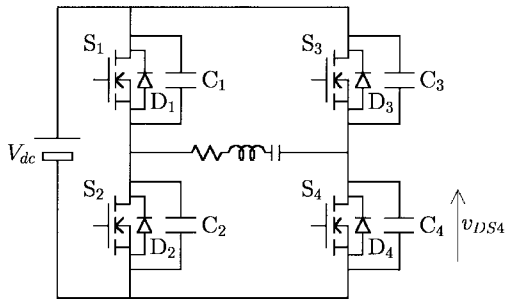


Fig. 1. Simplified circuit of the voltage-source inverter with a series-resonant circuit.

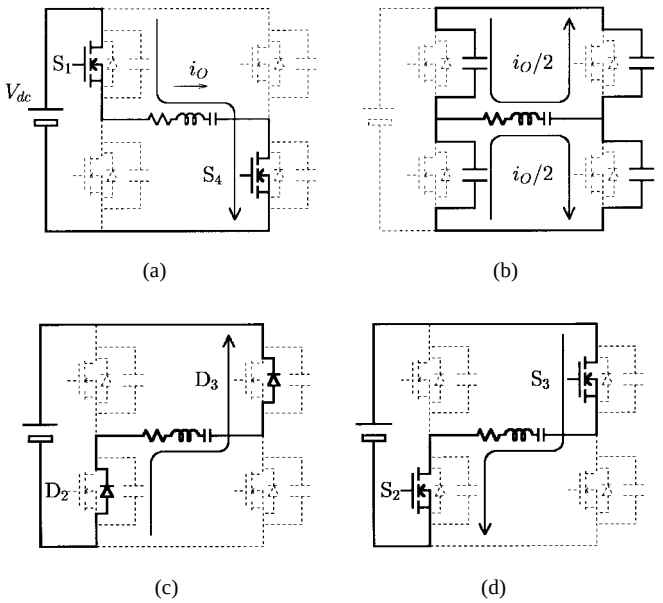


Fig. 2. Switching modes in the voltage-source inverter with a series-resonant circuit. (a) Before commutation. (b) During commutation. (c) After commutation. (d) After load current direction change.

MOSFET. Before commutation, MOSFET's S_1 and S_4 are conducting, and the direction of the load resonant current is $i_O > 0$, as shown in Fig. 2(a). Under the conditions, the voltages across output capacitors C_1 and C_4 are zero, while those across C_2 and C_3 are equal to the dc-link voltage V_{dc}. Turning S_1 and S_4 off starts the commutation process, and the switching mode changes to Fig. 2(b). During commutation, the load resonant current discharges C_1 and C_4 while it charges C_2 and C_3. When the voltages across C_1 and C_4 reach V_{dc} and those across C_2 and C_3 become zero, freewheeling diodes D_2 and D_3 start to conduct as shown in Fig. 2(c). After the direction of i_O changes, S_2 and S_3 conduct as shown in Fig. 2(d). Note that the gate signals are provided S_2 and S_3 prior to the mode change from Fig. 2(c) to Fig. 2(d) in order to perform zero-voltage and zero-current switching. This means that a time interval, which is known as the commutation period, is required for the discharge of the output capacitance. In addition, the inverter should be operated with a lagging displacement factor. If S_2 and S_3 are turned on before completing the discharge, the voltages across S_2 and S_3 go down to zero, while those across S_1 and S_4 being off

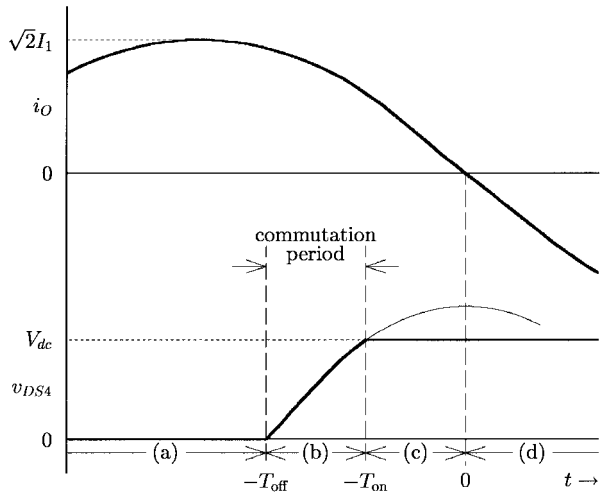


Fig. 3. Voltage and current waveforms.

go up to V_{dc} quickly. As a result, C_2 and C_3 are shorted out through S_2 and S_3, respectively. Thus, a large amount of current spike, which is a sum of the discharge currents of C_2 and C_3 and the recovery currents of D_1 and D_4, would flow through S_2 and S_3 being turned on. A surge also appears in the drain-to-source voltage due to the resonance between the output capacitance and the line inductance. To avoid such a short circuit, S_2 and S_3 should be turned on after completely discharging the output capacitance. This contributes to degrading the displacement factor of the high-frequency inverter operated at more than 1 MHz, because the commutation period required for the discharge can no longer be neglected as the operating frequency increases.

Fig. 3 shows the waveforms of the inverter output current i_O and the drain-to-source voltage v_{DS4}, taking into account the output capacitance of each MOSFET. Assuming that the direction of i_O changes at $t = 0$ and the rms value of i_O is I_1, i_O is represented as

$$i_O = -\sqrt{2} I_1 \sin \omega t. \tag{1}$$

Note that S_1 and S_4 are turned off at $t = -T_{\text{off}}$, and freewheeling diodes D_2 and D_3 start to conduct at $t = -T_{\text{on}}$. Since half of the load current $i_O/2$ flows through the output capacitance of S_4 during commutation *(b)*, the drain-to-source voltage v_{DS4} is given by

$$v_{DS4} = \frac{1}{C_{oss}} \int_{-T_{\text{off}}}^{t} \frac{i_O}{2}\, dt = \frac{\cos \omega t - \cos \omega T_{\text{off}}}{\sqrt{2} \omega C_{oss}} I_1 \tag{2}$$

where C_{oss} is the output capacitance of the MOSFET. This implies that v_{DS4} has a peak value at $t = 0$ and that the peak value can be adjusted by the turn-off leading time T_{off}. The drain-to-source voltage v_{DS4} is required to reach V_{dc} before $t = 0$ to avoid the short circuit of the output capacitance. Thus, the minimum value of the turn-off leading time $T_{\text{off-min}}$ is given by

$$T_{\text{off-min}} = \frac{1}{\omega} \cos^{-1} \left\{ 1 - \frac{\sqrt{2} \omega C_{oss} V_{dc}}{I_1} \right\}. \tag{3}$$

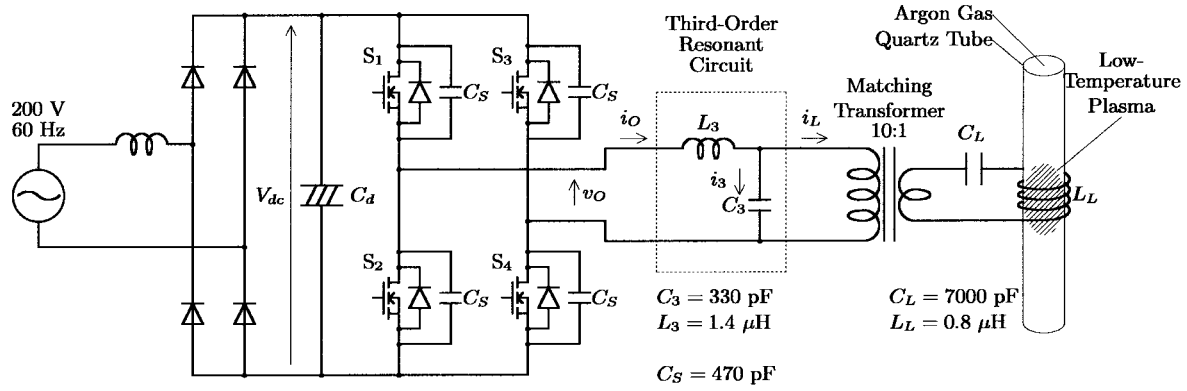


Fig. 4. System configuration.

TABLE I
RATINGS AND ELECTRICAL CHARACTERISTICS OF MOSFET (2SK2057)

		symbol	ratings	units
drain-to-source voltage		V_{DS}	500	V
gate-to-source voltage		V_{GS}	±30	V
drain current	DC	I_D	20	A
	pulse	I_{DP}	80	A
on-state resistance		$R_{DS(ON)}$	0.24	Ω
input capacitance		C_{iss}	3000	pF
output capacitance		C_{oss}	830	pF
switching times	rise time	t_r	25	ns
	turn-on delay	t_d(on)	60	ns
	fall time	t_f	55	ns
	turn-off delay	t_d(off)	280	ns

When S_1 and S_4 are turned off at $t = -T_{\text{off}-\min}$, and S_2 and S_3 are turned on at $t = 0$, all the MOSFET's and diodes achieve zero-voltage switching without forming any short circuit. Moreover, no recovery current flows in the freewheeling diodes because no diode conducts during the commutation. The turn-off leading time T_{off}, however, should be tuned for each leg due to a nonnegligible difference in the output capacitance among the four MOSFET's. In practical applications, it is difficult to individually adjust the turn-off timing T_{off} for every MOSFET. Connecting a lossless snubber capacitor in parallel with each MOSFET results in adjustment-free operation, although the displacement factor at the output of the inverter also decreases as the capacitance of the snubber capacitor is increased.

III. SYSTEM CONFIGURATION

Fig. 4 shows the system configuration of a 2-MHz 2-kW voltage-source inverter for a low-temperature plasma generator. The main circuit of the inverter is a single-phase H-bridge voltage-source inverter using four MOSFET's (2SK2057: TOSHIBA). The ratings and electrical characteristics of the MOSFET's are summarized in Table I. The body diode of the MOSFET is used as a freewheeling diode, so that no external diode is connected. A lossless snubber circuit connected to each MOSFET consists of only a 470-pF capacitor without any resistor or diode. The main series-resonant circuit is connected to the ac output of the inverter through a specially designed third-order resonant circuit and a step-down transformer with a turns ratio of 10:1.

A third-order resonant inductor L_3 is directly connected in series between the inverter and the transformer, while a third-order resonant capacitor C_3 is connected in parallel with the primary windings of the transformer. The resulting third-order resonant current superimposed on a sinusoidal load current helps to achieve quick charge/discharge of the output capacitor of each MOSFET.

When the third-order resonant circuit is disconnected, a parasitic resonant current flows whenever the commutation occurs, because the lead inductance and the winding capacitance of the transformer constitute a resonant circuit. The third-order resonant circuit acts as a low-pass filter for frequencies higher than the third-order harmonic frequency. The steep change in v_O occurs in the left of the third-order resonant circuit, whereas a slow change occurs in the right. The third-order resonant circuit, therefore, has the value-added function of suppressing such a parasitic resonance.

The main series-resonant circuit consists of a water-cooled seven-turns coil L_L and a high-frequency mica capacitor C_L. A quartz tube filled with argon gas, the diameter of which is 50 mm, is inserted into the resonant inductor L_L. A high-frequency magnetic field produced by the 2-MHz resonant current establishes and sustains a low-temperature plasma in the quartz tube.

IV. FAST SWITCHING OPERATION USING THIRD-ORDER RESONANT CIRCUIT

The aim of the third-order resonant circuit proposed in this paper is to realize a fast discharge of the output capacitance by superimposing a third-order resonant current on the first-order (fundamental) load resonant current. The third-order resonant circuit allows the individual MOSFET's to perform fast switching without any voltage surge or current spike.

Fig. 5 shows voltage and current waveforms when the third-order resonant circuit is connected. Here, v_1 and v_3 are the fundamental and third-order harmonic voltages included in the inverter output voltage v_O, respectively. Note that v_O is a trapezoidal waveform, where the rise and fall times of each MOSFET and the commutation period are taken into account.

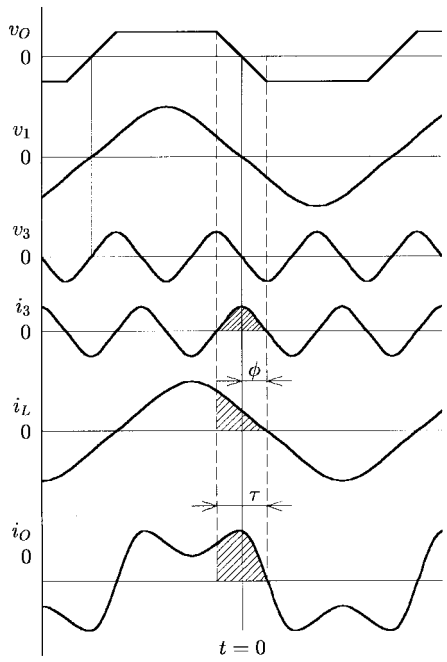


Fig. 5. Voltage and current waveforms in the third-order resonant circuit.

However, v_1 and v_3 in Fig. 5 are nearly equal to those under the assumption that the inverter output voltage is a square waveform, because the rise and fall times and the commutation period produce little effect on the fundamental and third-order harmonic voltages. Invoking the above assumption yields the following equations:

$$v_1 = -\sqrt{2}\frac{2\sqrt{2}V_{dc}}{\pi}\sin\omega t, \tag{4}$$

$$v_3 = -\sqrt{2}\frac{2\sqrt{2}V_{dc}}{3\pi}\sin 3\omega t. \tag{5}$$

The fastest dv/dt is achieved by placing the peak of the third-order resonant current at the zero voltage crossing. This needs a 90° phase shift between v_3 and i_3. The third-order component v_3 is in phase with v_1, since v_O is defined as shown in Fig. 5. Disregarding the resistance in the third-order resonant circuit leads to the third-order resonant current i_3 as follows:

$$i_3 = \sqrt{2}\frac{2\sqrt{2}V_{dc}}{3\pi(3\omega L_3 - 1/3\omega C_3)}\cos 3\omega t. \tag{6}$$

Note that the impedance to the right of the third-order resonant capacitor can be neglected in deriving (6), because the main resonant circuit exhibits a high-enough impedance for the third-order resonant frequency.

The third-order resonant current i_3 lags by 90° with respect to the third-order harmonic voltage v_3; in other words, i_3 reaches its peak value at the zero voltage crossing. The inverter output current i_O has a quasi-trapezoidal waveshape shown in Fig. 5 due to the superposition of the third-order resonant current i_3. This results in fast charge or discharge of the output capacitance because i_O is larger than the load resonant current i_L during the commutation. The third-order resonant current i_3 makes it possible to increase the current only during the commutation without any increase of the peak value of i_O, because the peak value of i_3 appears at the zero voltage crossing. The third-order resonant circuit i_3, therefore, should be tuned at a frequency slightly lower than three times as high as the operating frequency. Accordingly, the third-order resonant circuit acts as an inductive impedance which draws the third-order resonant current lagging by 90°.

V. Design Strategy of Third-Order Resonant Circuit

A. Design Strategy

The inverter output current i_O is a sum of the load resonant current i_L and the third-order resonant current i_3 given by

$$i_O = -\sqrt{2}I_1\sin(\omega t - \phi) + \sqrt{2}I_3\cos 3\omega t \tag{7}$$

where I_1 and I_3 are the rms values of the load resonant current i_L and third-order resonant current i_3, and ϕ is the phase difference between v_1 and i_L, so that $\cos\phi$ is the displacement factor at the output of the inverter.

The inverter output current i_O is required to charge or discharge the output capacitance C_{oss} and snubber capacitor C_S in the upper and lower arms during the commutation period τ. This requirement is represented as

$$2Q_C = 2(C_{oss} + C_S)V_{dc} = \int_{-\tau/2}^{\tau/2} i_O\, dt \tag{8}$$

where Q_C is the electric charge stored in C_{oss} and C_S. Accordingly, the amplitude of the third-resonant resonant current I_3 should be decided as

$$I_3 = \frac{3}{2}\,\frac{\sqrt{2}\omega Q_C + I_1\cos(\phi + \omega\tau/2) - I_1\cos(\phi - \omega\tau/2)}{\sin 3\omega\tau/2}. \tag{9}$$

In order to let the commutation finish at the instant that the load resonant current i_L is zero, the duration of the commutation period should be set to $\tau = 2\phi/\omega$. As a result, I_3 is obtained by

$$I_3 = \frac{3}{2}\,\frac{\sqrt{2}\omega Q_C + I_1\cos(\omega\tau) - I_1}{\sin 3\omega\tau/2}. \tag{10}$$

By substituting (10) into (6), the impedance of the resonant circuit with respect to the third-order resonant frequency Z_3 is determined as

$$Z_3 = 3\omega L_3 - \frac{1}{3\omega C_3} = \frac{2\sqrt{2}V_{\rm dc}}{3\pi I_3}. \tag{11}$$

One should choose an optimum value of C_3 and L_3 under a compromise or a tradeoff between a voltage drop across L_3 and a leading current flowing into C_3. If the capacitance value is large, the inverter would operate at a leading displacement factor. On the contrary, if the capacitance value is small, the inductance value of L_3 is large, which causes the nonnegligible voltage drop for the fundamental frequency.

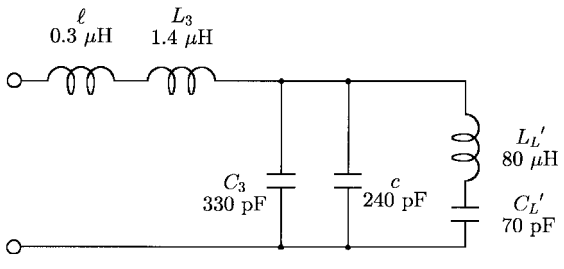


Fig. 6. Equivalent circuit of the third-order resonant circuit.

B. Evaluation in Experimental System

In the experimental system shown in Fig. 4, the resonant frequency of the load resonant circuit is 2.1 MHz, the rated resonant current is 9 A in rms value, and the dc-link voltage of the inverter $V_{\rm dc}$ is 200 V. Connecting a lossless snubber capacitor of $C_S = 470$ pF in parallel with each MOSFET, the electric charge stored in the output capacitance of the MOSFET and the snubber capacitor is given by

$$Q_C = (C_{oss} + C_S)V_{\rm dc} = 0.42\ \mu\text{C}.$$

The commutation period should be made longer than the rise and fall times of the MOSFET used. If the commutation is shorter, it would yield increased switching losses because the load resonant current would flow through the MOSFET's, even during the commutation period. Thus, the commutation period τ is set to $\tau = t_r = 55$ ns, which equals the fall time of the MOSFET used in the experimental system. From (10), the amplitude of the third-order resonant current is equal to 4.6 A in rms value. Thus, the resonant inductor and capacitor of the third-order resonant circuit L_3 and C_3 should be designed as $Z_3 = 16\ \Omega$. Assuming that $\phi/\omega = \tau/2$ in (10), the displacement factor at the output of the inverter, $\cos\phi$ equals 94%.

Fig. 6 shows an equivalent circuit when both third-order resonant and load resonant circuits are connected, taking into account the turns ratio of the matching transformer. The equivalent reactor L_L' of the load resonant circuit is equal to $L_L' = n^2 L_L$, and the equivalent capacitor C_L' equals $C_L' = C_L/n^2$, where n is the turns ratio of the matching transformer. The magnetizing inductance of the matching transformer can be ignored in Fig. 6 because the magnetizing current is too small at an operating frequency as high as 2 MHz. The leakage inductance in the matching transformer is also neglected because it is much smaller than L_L'.

A line inductance of $\ell = 0.3\ \mu$H exists between the inverter bridge and the matching transformer, and the matching transformer has a parasitic capacitance of $c = 240$ pF in its primary windings. Taking into account the line inductance and the parasitic capacitance, the third-order resonant reactor L_3 is set to 1.4 μH, and the third-order resonant capacitor C_3 to 330 pF. Thus, the resonant frequency equals 5.1 MHz. The impedance of the third-order resonant circuit is given by

$$3\omega L_3 - 1/(3\omega C_3) = 64 - 46 = 18\ \Omega.$$

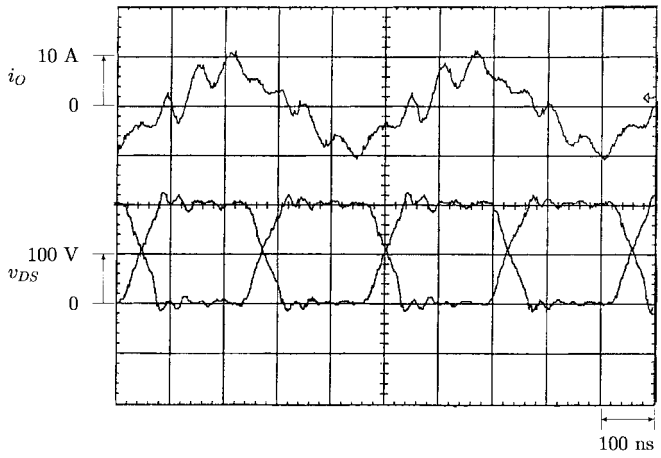


Fig. 7. Experimental waveforms in the case of disconnecting the third-order resonant circuit.

Thus, the leading current flowing into the third-order resonant capacitor is

$$\frac{2\sqrt{2}}{\pi} \times 200/(2\pi \times 2 \times 10^6 \times 330 \times 10^{-12}) = 0.7\ \text{A}$$

which is less than 1/10 of the load resonant current. The voltage drop appearing across the third-order resonant reactor L_3 is negligible because L_3 is only 2% of the load resonant reactor.

The effect of change in the operating frequency on the amplitude variation is discussed below. Assume that the load resonant current is decreased by 1/2, due to a frequency change. In this case, an increase in the operating frequency is only 1.7% because the load resonant circuit has a high quality factor of $Q = 50$ in the experimental system. The impedance of the third-order resonant circuit equals

$$3\omega L_3 \times 1.017 - 1/(3\omega C_3 \times 1.017) = 65 - 45 = 20\ \Omega.$$

This means that the variation in the third-order resonant current decreases by only 10%, even if such a large frequency change occurs, because the third-order resonant circuit is used in a frequency range where the circuit has an inductive impedance.

VI. Experimental Results

Fig. 7 show experimental waveforms in the case of disconnecting the third-order resonant circuit. The inverter output current includes an oscillating current of 15 MHz because of a parasitic resonance between the line inductance and the stray capacitance in the matching transformer. A surge appears in the drain-to-source voltage because the MOSFET's are turned on before the discharge of the output capacitance. In Fig. 7, both rise and fall times are about 80 ns, and the displacement factor is 88%.

Fig. 8 shows experimental waveforms in the case of connecting the third-order resonant circuit. Since the third-order resonant current is superimposed on the load resonant current, the inverter output current i_O has a quasi-trapezoidal waveshape without any parasitic oscillation. No surge appears in the drain-to-source voltage because the third-order resonant

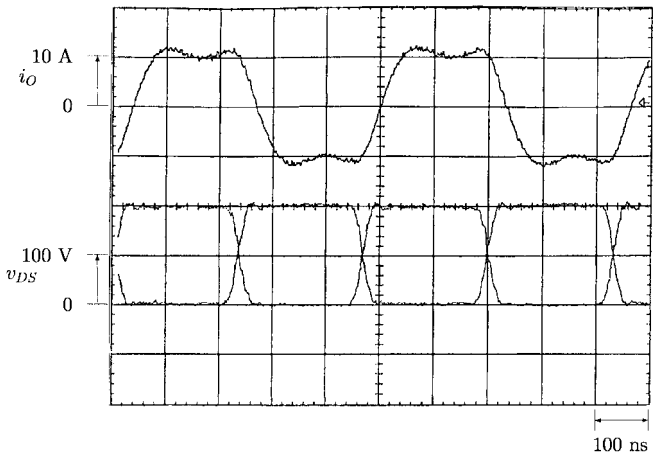


Fig. 8. Experimental waveforms in the case of connecting the third-order resonant circuit.

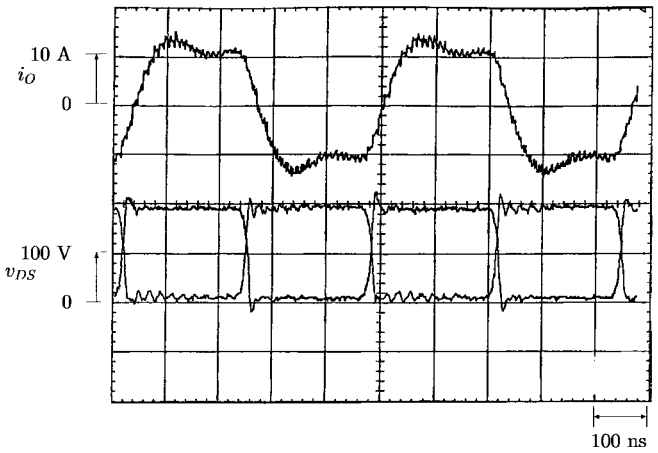


Fig. 9. Experimental waveforms in the case of disconnecting the lossless snubber capacitor.

current perfectly discharges the output capacitance before the corresponding MOSFET's are turned on. The rise and fall times are 40 ns in Fig. 8, which equals half of those in Fig. 7. This indicates that a displacement factor as high as 97% is achieved by connecting the third-order resonant circuit. The dc input power of the inverter is 1800 W, and the high-frequency output power is 1690 W. Thus, the inverter efficiency is 94%, which confirms that the inverter performs a zero-voltage switching operation, even at a frequency as high as 2 MHz.

Fig. 9 shows experimental waveforms when any lossless snubber capacitor is not connected. The rise and fall times in Fig. 9 equal 20 ns because the inverter output current i_O charges or discharges only the inherent output capacitance of each MOSFET. However, a surge appears in the drain-to-source voltage v_{DS}. Note that the voltage surge magnitude in one leg is different from that in the other leg because of the differences in the output capacitance between the two MOSFET's. Moreover, a small error of the turn-off time may produce a large voltage surge, compared with the case of connecting the snubber circuit. Thus, an adjustment of the turn-off time for each leg is required to reduce such a voltage surge. It is, however, difficult to perfectly adjust the turn-off time in a practical application.

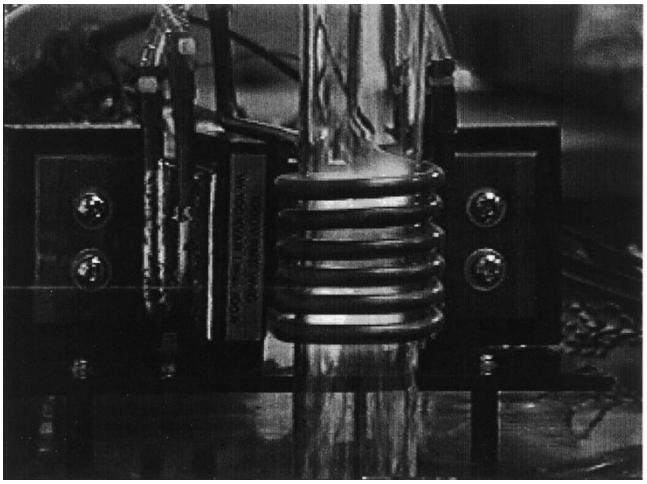


Fig. 10. Low-temperature plasma before flaming up.

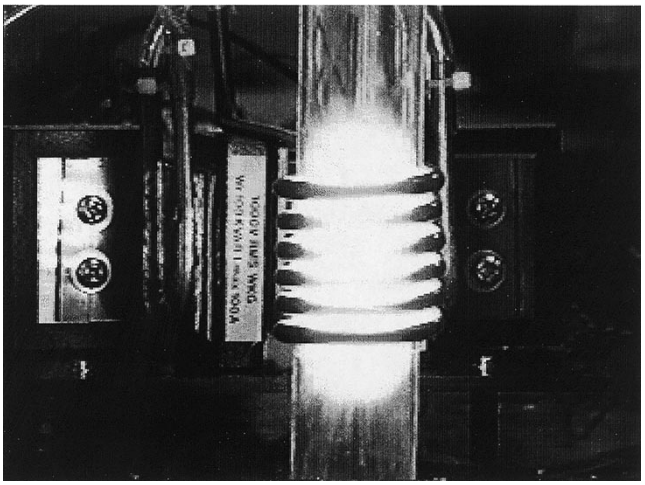


Fig. 11. Low-temperature plasma after the plasma becomes hot.

Figs. 10 and 11 show states of low-temperature plasma generated by the inverter. Low-pressure argon gas is injected in the quartz tube and the output power of the inverter is adjusted by varying the dc-link voltage in this experiment. After the plasma becomes hot, the quality factor of the main resonant circuit decreases from 40 to 10.

VII. Conclusion

This paper has proposed a voltage-source series-resonant inverter equipped with a third-order resonant circuit for the purpose of achieving a fast switching operation. The design strategy and practicability of the third-order resonant circuit have been discussed theoretically and experimentally. The third-order resonant current superimposed on a sinusoidal load current plays an essential role in achieving quick charge and discharge of the output capacitance of each MOSFET.

The main advantages of the proposed inverter equipped with the third-order resonant circuit appear to be the following.

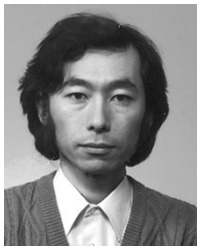
1) Experimental results show a switching operation as fast as 40 ns and a displacement factor as high as 97% with neither voltage surge nor current spike.
2) The connection of the third-resonant circuit only causes a slight increase in the rms current, but does not cause any increase in the peak current of the MOSFET.
3) The third-order resonant circuit has the value-added function of suppressing the parasitic oscillation which comes from the lead inductance and the parasitic capacitance existing in the matching transformer.
4) An inverter efficiency as high as 94% at 2 MHz is obtained from the experiments, owing to the proper zero-voltage switching operation.
5) The 2-MHz 2-kW prototype system has succeeded in generating the stable low-temperature plasma.

ACKNOWLEDGMENT

The authors would like to thank T. Okabe and K. Hirao, former graduate students in the Department of Electrical Engineering, Okayama University, for their support in these experiments.

REFERENCES

[1] H. U. Eckert, "The induction arc: A state-of-the-art review," *High Temp. Sci.*, vol. 6, pp. 99–134, 1974.
[2] S. B. Dewan and G. Havas, "A solid-state supply for induction heating and melting," *IEEE Trans. Ind. Gen. Appl.*, vol. IGA-5, pp. 686–692, Nov./Dec. 1969.
[3] W. E. Frank and C. F. Der, "Solid state RF generators for induction heating applications," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1982, pp. 939–944.
[4] S. Bottari, L. Malesani, and P. Tenti, "High frequency 200-kHz inverter for induction heating applications," in *Conf. Rec. IEEE PESC'85*, 1985, pp. 308–316.
[5] H. Akagi, T. Sawae, and A. Nabae, "130-kHz, 7.5-kW current-source inverters using static induction transistors for induction heating applications," *IEEE Trans. Power Electron.*, vol. 3, pp. 303–309, May 1988.
[6] T. Yokoo, H. Itho, and A. Sano, "High frequency inverters for induction heating equipment by using static induction transistors," in *Proc. PCIM*, 1988, pp. 101–108.
[7] P. P. Roy, S. R. Doradla, and S. Deb, "Analysis of the series resonant converter using a frequency domain model," in *Conf. Rec. IEEE PESC'91*, 1991, pp. 482–489.
[8] L. Grajales, J. A. Sabaté, K. R. Wang, W. A. Tabisz, and F. C. Lee, "Design of a 10-kW, 500-kHz phase-shift controlled series-resonant inverter for induction heating," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1993, pp. 843–849.
[9] H. Fujita and H. Akagi, "Pulse-density-modulated power control of a 4-kW, 450-kHz voltage-source inverter for induction melting applications," *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 279–286, Mar./Apr. 1996.



Hideaki Fujita (M'91) received the B.S. and M.S. degrees in electrical engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1988 and 1990, respectively.

Since 1991, he has been a Research Associate in the Department of Electrical Engineering, Okayama University, Okayama, Japan. His research interests are static var compensators, active power filters, and resonant converters.

Mr. Fujita was the recipient of First Prize Paper Awards from the Industrial Power Converter Committee of the IEEE Industry Applications Society in 1990, 1995, and 1998.

Hirofumi Akagi (M'87–SM'94–F'96) was born in Okayama-City, Japan, in 1951. He received the B.S. degree from Nagoya Institute of Technology, Nagoya, Japan, in 1974 and the M.S. and Ph.D. degrees from Tokyo Institute of Technology, Tokyo, Japan, in 1976 and 1979, respectively, all in electrical engineering.

In 1979, he joined the Department of Electrical Engineering, Nagaoka University of Technology, as an Assistant Professor. He later became an Associate Professor. Since 1991, he has been a Full Professor in the Department of Electrical Engineering, Okayama University, Okayama, Japan. In 1987, he was a Visiting Scientist at Massachusetts Institute of Technology, Cambridge, for ten months. From March to August 1996, he was a Visiting Professor at the University of Wisconsin, Madison, and then Massachusetts Institute of Technology. His research interests include ac motor drives, high-frequency resonant inverters for induction heating and corona discharge treatment, and utility applications of power electronics, such as active filters, static var compensators and FACTS devices.

Prof. Akagi has received eight society and committee Prize Paper Awards from the IEEE Industry Applications Society, including the First Prize Paper Award in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS for 1991. He is a Distinguished Lecturer of the IEEE Industry Applications and IEEE Power Electronics Societies for 1998–1999.