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CMOS Floating Gate Defect Detection Using I_{DDQ} Test with DC Power Supply Superposed by AC Component

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Abstract

In this paper, we propose a new I_{DDQ} test method for detecting floating gate defects in CMOS ICs. In the method, unusual increase of the supply current caused by defects is promoted by superposing an AC component on the DC power supply. Feasibility of the test is examined by some experiments on four DUTs with an intentionally caused defect. The results showed that our method could detect clearly all the defects, one of which may be detected by neither any functional logic test nor any conventional I_{DDQ} test.

1. Introduction

It is well known that most of the defects caused in CMOS logic ICs manufactured are short ones and open ones[1]. The open defects are further classified into stack-open ones and floating gate ones. The short defects and the stuck-open defects can be detected effectively by functional logic tests, so-called I_{DDQ} tests[2],[3], etc. The floating gate defects however cannot always be detected owing to the following reason[3]-[6].

Potential of the floating gate is apt to be affected by the environment surrounded[5],[7]. It may therefore vary according to the values of input vectors as if defect-free , and besides, quiescent supply current may scarcely increase as if defect-free. In other words, there can exist some defects which are detectable with neither any functional logic test nor any conventional I_{DDQ} test. Thus, it is an earnest request for test engineers to develop more powerful methods to be able to detect such defects.

From the background mentioned above, an I_{DDQ} test method with an externally applied electric field[8] was proposed. It intends to detect open defects by exciting the defective nodes with the electric field so that a large amount of abnormal supply current flows. It may be expected by use of the method that some of defects, which cannot be detected by any other method, turn detectable ones. Some class of floating gate defects is one of such defects. The detailed performance of the method however has not been known because it is on the way of development.

This paper proposes a new I_{DDQ} test method which has ability similar to one in the paper[8]. In our method, a sinusoidal signal superposed on the supply voltage is used in place of the electric field to excite the floating points. The test equipment is simpler and the effect of the sinusoidal signal on the floating point is more reliable.

In the next section, we describe the outline of our test method. In the succeeding section, we analyze the floating gate potential in order to make its principle clear. In the fourth section, feasibility of our test method is shown based on some experiments on four DUTs with an intentionally caused defect. In the fifth section, our method is compared with other conventional test ones. Finally, we conclude with a summary and our future works.

2. Test strategy

Figure 1 shows a CMOS inverter and its input/output characteristics. A high level input voltage v_H and a low level input voltage v_L are defined as $V_{iH} < v_H \leq V_{DD}$ and $0 \leq v_L < V_{iL}$, as shown in Figure 1(b), respectively. If the inverter is defect-free and the input voltage V_i is held within either of above ranges, quiescent supply current scarcely flows.

On the other hand, if it has any floating gate defect, the potential of the defective node is uncertain, and the defect cannot always be detected by conventional I_{DDQ} tests because of the following reason.

Figure 2 shows an equivalent circuit for an inverter with a floating gate defect, where C_D, C_G and C_I are stray capacitances from the floating node to the power supply source, the ground (GND) and the corresponding input terminal, respectively. As long as V_{DD} is held invariant and V_i is fixed to v_H or v_L, the potential of the defective node is determined by electrical charges stored on these capacitances. It

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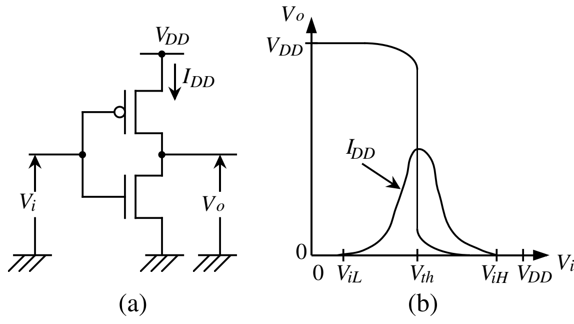

Figure 1. DC characteristic of CMOS inverter

scarcely changes within a second or a minute because of high leakage resistance. If such the potential is over either of the ranges(i.e. $V_{iL} < V_i < V_{iH}$), some supply current flows, while it is within either of them, little supply current flows. Thus, the defect cannot always be detected by the conventional I_{DDQ} tests.

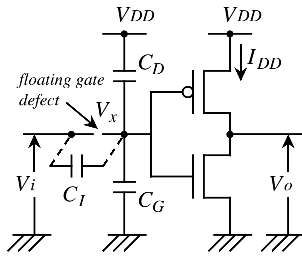

Figure 2. Equivalent circuit for inverter with floating gate defect

In order to make it detectable reliably by the I_{DDQ} tests, it is necessary to force the potential V_x of the defective node to bring into active region of the inverter. Figure 3 shows an a circuit which we developed for the purpose. Input terminals should be connected to the power supply node and the ground so that V_i is fixed to v_H and v_L, respectively. The C_I shown in Figure 2 is merged into C_D and C_G according to $V_i = V_{DD}$ and $V_i = 0$(GND), respectively. A sinusoidal component V_S is superposed on the DC supply voltage V_D. So, V_i also swings sinusoidally, promoting to make the complementally MOSFETs conduct. Thus, it is expected that our method can detect the defect more sensitively than conventional I_{DDQ} tests.

3. Analysis of floating gate potential

From Figure 3, V_x can be related to V_{DD} by

$$\frac{dV_x}{dt} = B\frac{dV_{DD}}{dt} \tag{1}$$

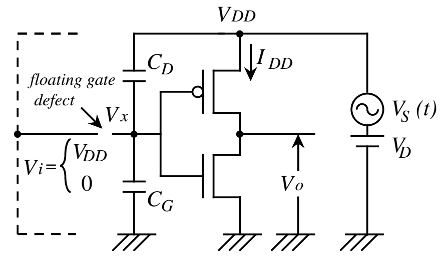

Figure 3. Test circuit

where $B = C_G/(C_D + C_G)$. The power supply voltage V_{DD} is given as

$$V_{DD}(t) = V_D + V_S(t) \tag{2}$$

where V_S is a sinusoidal signal shown in the following.

$$V_S(t) = A \sin \omega t = A \sin 2\pi f t \tag{3}$$

If the initial value of V_x is at v_0, we can obtain the following solution from the equation(1).

$$V_x = AB \sin 2\pi f t + v_0 \tag{4}$$

It is found from the equation above that V_x varies with the change of V_S sinusoidally.

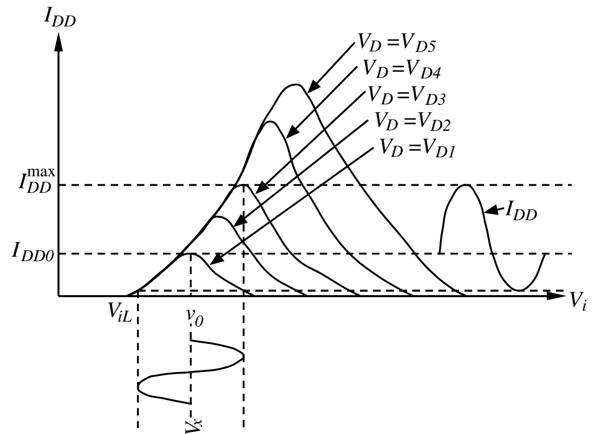

Figure 4. Static $V_i - I_{DD}$ characteristics with dynamic behavior of a defective inverter in case of $V_{iL} < v_0 \leq V_{th}$

Bold lines in Figure 4 shows static $V_i - I_{DD}$ characteristics of a CMOS inverter. The threshold voltage V_{th} and the peak supply current I_{DD}^{max} increase with the rise in $V_D(V_{D1} < V_{D2} < \cdots < V_{D5})$. All the curves trace almost the same locus as long as V_i in each curve is lower than the

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corresponding V_{th}. Accordingly, the boundary V_{iL} of the low level voltage is held constant, regardless of V_D.

The inverter which has the characteristics shown in Figure 4 is supposed to have a floating gate defect. The potential V_x given by the equation (4) is induced at the defective node, and some variable component appears in I_{DD} as shown on the right side. That is, if $V_{iL} < v_0 \leq V_{th}$, the peak supply current I_{DD}^{max} is higher than the quiescent one at $A = 0 (V_S = 0)$. Waveforms of V_x and I_{DD} for v_0 lower than V_{iL} are shown in Figure 5. The I_{DD} flows intermittently in synchronizing with V_S. It is apparent that if the defective node has a initial potential between V_{iL} and V_{th} as shown in Figure 4, the defect is detectable by both conventional I_{DDQ} method and our method. The defect of the DUT in such a situation as Figure 5 is however detectable only by our method, because little I_{DD} flows at v_0 less than V_{iL} if $V_S = 0$.

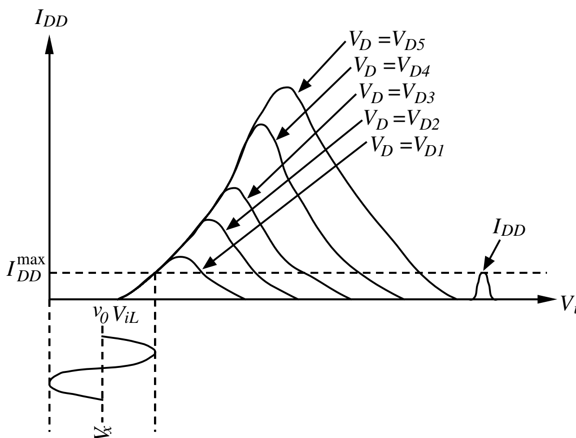

Figure 5. Dynamic behavior in case of $v_0 \leq V_{iL}$

For the DUT with a initial potential higher than V_{th}, the outline illustration of $V_i - I_{DD}$ curves can be obtained as Figure 4 opposed against I_{DD} axis. The criterion of the potential is the supply voltage V_D. The dynamic behavior in case of $v_0 \geq V_{iH}$ can be shown as Figure 6, which is given by opposing Figure 5. It is found that our method is also applicable to the case in the same way as Figure 5.

Thus, it is expected from above analysis that any floating gate defect can be detected by the proposed method regardless of values of v_0 and B, as long as A is selected to enough high value.

4. Experimental results

For the purpose of the experimental examination, we picked up four NAND gate packages TC4011BPs manufactured by Toshiba Co.. Each of them has four 2-inputs

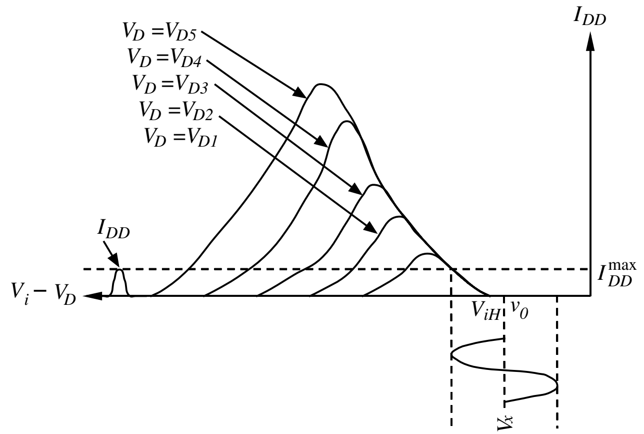

Figure 6. Dynamic behavior in case of $v_0 \geq V_{iH}$

NAND gates. We made up only one floating gate defect per package. That is, each DUT has only one defect differing from the others. Figure 7 shows the points of the defects by marking crosses (1)-(4) on a CMOS NAND circuit. Figure 8 shows them on the layout. We caused them by cutting the corresponding aluminum wires with FIB (Focused Ion Beam).

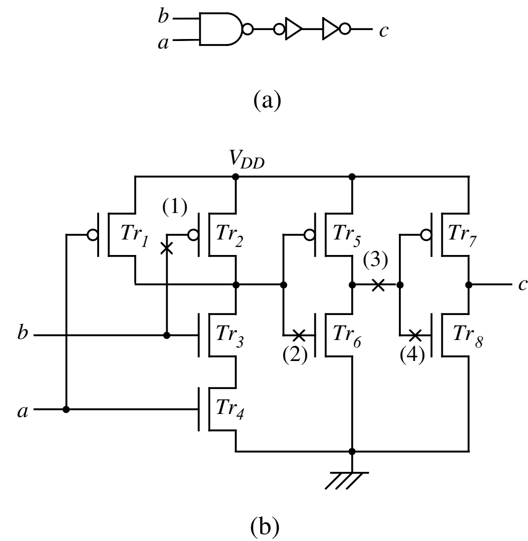

Figure 7. Defects shown on a CMOS NAND gate circuit(TC4011BP)

Figure 9 is the test circuit used in our examinations. Pin numbers 14 and 7 are for power supply and ground, respectively. $R(1.0k\Omega)$ is a resistor to measure the supply current I_{DD}. All the input pins of NAND gates except a faulty one

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were connected to the ground. For the inputs of the faulty NAND gate, the same test vectors as those in the paper[8] were given. For example, we used a test vector $a = v_H$, $b = v_H$ for the defect(1) in Figure 7(b), so that a current path from the power supply node to the ground may be generated.

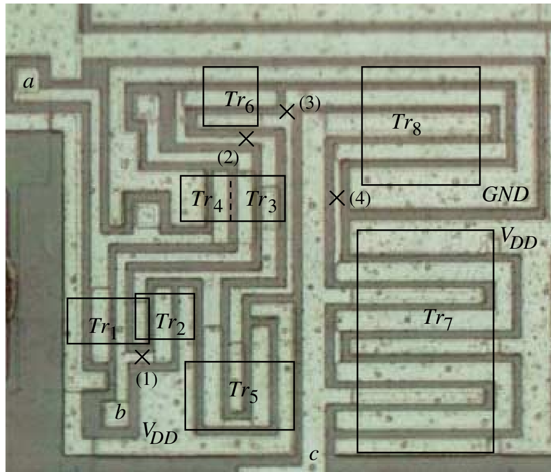


Figure 8. Four defects on the layout

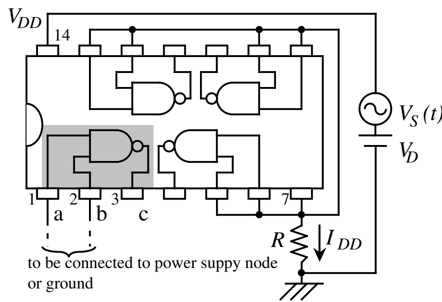
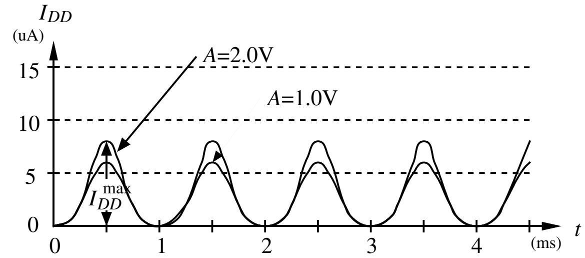


Figure 9. Experimental circuit

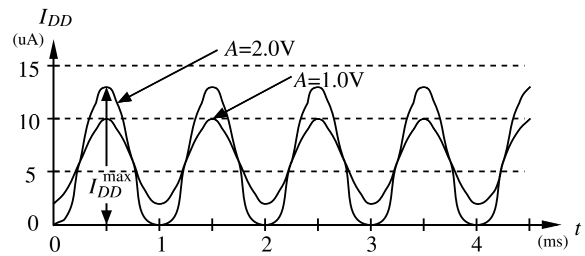
The results showed that we could detect all the defects by our method. That is, I_{DD} of each DUT abnormally increased with the test vector mentioned above. Waveforms are shown in Figure 10 (a),(b),(c) and (d) which correspond to the defects(1),(2),(3) and (4) shown in Figure 7, respectively. The I_{DD} in each DUT was measured at enough intervals to avoid influence of the last measurement. On the way of testing, the supply current I_{DD} oscillated synchronously with the AC component superposed.

The peak supply current I_{DD}^{max} in each case increases with the extension in the amplitude A of the sinusoidal component. Though it is smallest in case of the defect(1), it is much larger than the leakage current which is about $2\mu A$ in unfaulty TC4011BPs. It means that all the four floating gate defects can be detected by measuring the supply current.

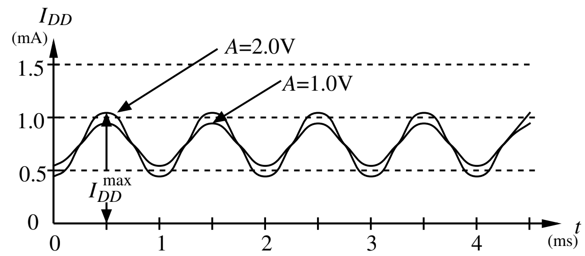
Though the frequency of V_s used in the results shown in Figure 10 was 1kHz, even 100Hz and 10KHz could almost get the same results. Maximum frequency depends on the DUT.



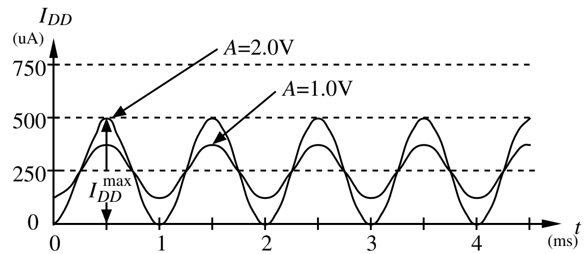
(a) *defect* (1), V_D = 6.0V, *f*=1kHz, *a*=*b*=v_H



(b) *defect* (2) , V_D = 6.0V, *f*=1kHz, *a*=*b*= v_H



(c) *defect* (3) ,V_D = 6.0V, *f*=1kHz, *a*=*b*=v_L



(d) *defect* (4) ,V_D = 6.0V, *f*=1kHz, *a*=*b*=v_H

Figure 10. Waveforms of I_{DD}

5. Consideration

In this section, we consider the results shown above in comparison with those of other test methods. Figure 11

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shows the relations between the amplitude A of the sinusoidal wave superposed and the peak supply current I_{DD}^{max}. The I_{DD}^{max} in each case increases in accordance with the increase of the amplitude A.

It also increases with the rise in V_D except for the defect(1). It is easily found from the results that the defects(2)∼(4) can be detected as abnormal rise in I_{DD} not only by our method but also by conventional I_{DDQ} test methods. On the contrary, the defect(1) can be detected only by our method, because I_{DD}^{max} increases not with V_D, but with A. We also examined that it cannot be detected by means of functional logic test. Those results are summarized in Table 1.

Table 1. Comparison with other test methods

defect no.	logic test	usual I_{DDQ}	our method
(1)	×	×	○
(2)	○	○	○
(3)	○	○	○
(4)	○	○	○

We will next discus why only our method can detect the defect(1). The defect(1) was made up by cutting the wire at the location much close to the gate of MOSFET Tr_2 as shown Figure 8. It seems therefore that the magnitude of C_I is rather large in comparison with C_D or C_G in Figure 2. This means that the action of Tr_2 is liable to be controlled by the potential of the input (the value of b) as if defect-free. Taking such a situation into account, we can understand the result of the defect(1) tabulated in Table 1 as follows. In the functional logic test, Tr_2 is in saturation state for the test vector $a = v_H, b = v_L$, resulting in no fault on appearance. In the usual I_{DDQ} test, the test vector $a = b = v_H$ is given, so that Tr_2 is in cut-off state, resulting in no fault($I_{DDQ} \simeq 0$). On the contrary, I_{DD} increases remarkably by the sinusoidal component in our test, resulting in fault.

6. Conclusion

In this paper we proposed a new I_{DDQ} test method for detecting floating gate defects in CMOS ICs. The feasibility of the test is examined by some experiments on four NAND gate packages having a defect intentionally caused. The experimental results showed that supply current could be induced synchronously with the AC component superposed on the DC power supply. It means that proposed method can detect floating gate defects rather easily than the paper[8]. It is expected our method is also applicable to stuck-open defects Our future work is applicability check for open defects of other kinds.

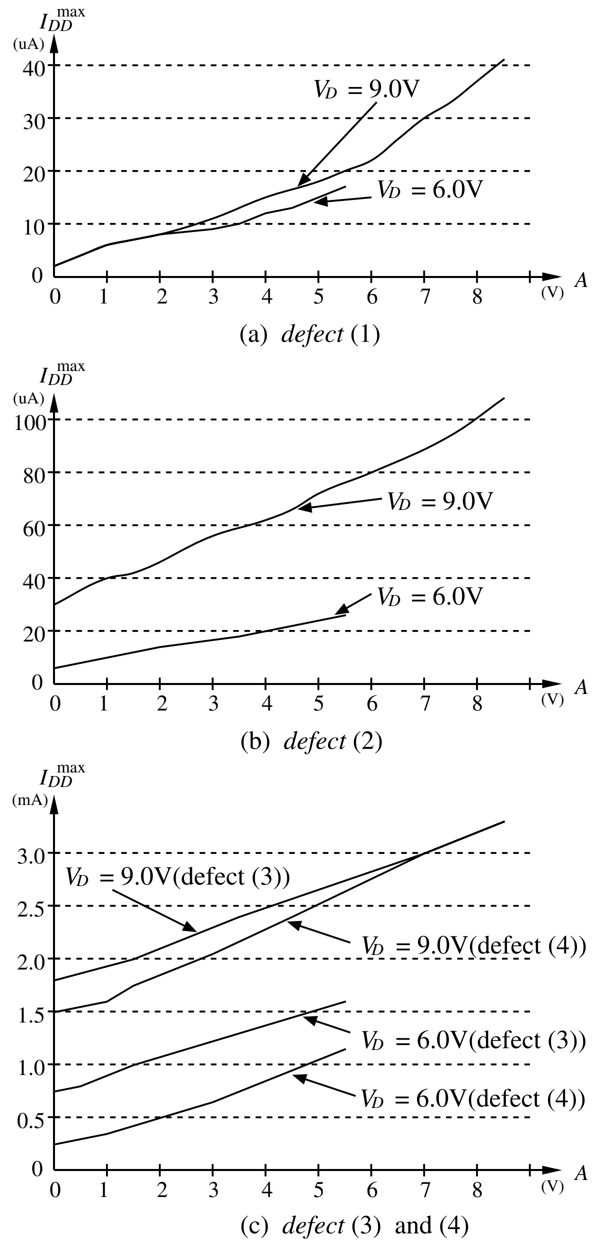

Figure 11. Effect of sinusoidal wave

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