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# Effect of Annealing and Hydrogen on Properties of Electrodeposited Platinum Electrode and Lead-Zirconate-Titanate Films for Ferroelectric Random Access Memory Applications

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The selection of capacitor electrode materials for the nonvolatile ferroelectric random access memory is one of the most important issues because capacitor electrical characteristics are strongly influenced by the electrode materials. The lower Pt electrode was electrodeposited on the Ti seed/Pt seed layer. Two different thicknesses of Ti seed layer (5 and 15 nm) were adopted, and lead-zirconate-titanate (PZT) was deposited on the electrodeposited Pt. The Pt crystal orientation with a 5 nm Ti seed layer is much better than that with a 15 nm Ti seed layer, and the deposited PZT shows much better crystal orientation. Due to better crystal orientation of the PZT layer in the case of a 5 nm Ti seed layer, a Pt/PZT/Pt capacitor well-saturated *D-V* hysteresis loop was obtained whereas little current was observed in the large electric field. With the 15 nm Ti seed layer, numerous several-μm-sized voids formed on the lower Pt electrode surface. With the 5 nm Ti seed layer, fewer voids formed on the lower Pt electrode surface. Glow discharge spectrometry measurement with a 15 nm Ti seed layer shows much higher H intensity than that with a 5 nm Ti seed layer, and the H peak coincides with the Ti peak. The H existing in the Ti seed layer must have transmitted into the PZT layer and deteriorated the PZT crystal orientation.
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Many efforts have been made toward realizing nonvolatile ferroelectric random-access memories (FeRAMs) in the past decade. Many reports have been published on the ferroelectric thin films such as $Pb(Zr,Ti)O_3(PZT)$ and $SrBi_2Ta_2O_9(SBT)$. The choice of electrode materials is one of the most important issues toward realizing these FeRAMs, since the electrical characteristics are strongly influenced by the electrode materials. Platinum (Pt),[1] ruthenium (Ru),[2,3] iridium (Ir),[4-6] and $SrRuO_3$[7] have been examined as the electrode materials and they were formed mostly by metallorganic chemical vapor deposition (MOCVD) and sputtering.

Pt, however, is possible to be electrodeposited by the wet method and electrodeposition is a low-cost process if compared to the MOCVD or sputtering. Saenger et al.[8] reported the process of submicrometer Pt electrodes by through-mask electrodeposition. Horii et al.[9] also reported the submicrometer Pt electrodes by electrodeposition. They both discussed the importance of a through-mask process with reactive ion etching (RIE), since Pt is very difficult to be etched with RIE. Unfortunately, few descriptions on the electrical characteristics have been reported in these former reports.[8-10]

A Pt electrode is conventionally formed by sputtering and many reports have been published.[11-15] Electrical characterization of FeRAM has been reported in these reports,[11-15] however the crystal structure of the Pt electrode and ferroelectric film has not been reported in detail. None of these reports[11-15] discuss the H (hydrogen) effect due to the Ti seed layer.

In this work, the Pt/PZT/Pt capacitor was formed with an electrodeposited Pt lower electrode. The *I-V* and *D-V* characteristics of the capacitor were measured and the electrical characteristics were discussed based on the process condition of the electrodeposited Pt lower electrode. Crystal structures of the Pt electrode and the detailed H effect due to the Ti seed layer were discussed.

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## Experimental

The silicon wafer surface consists of the $SiO_2$ buffer layer, the Ti seed layer (thickness = 5 or 15 nm), and the Pt seed layer (see Fig. 1). The $SiO_2$ layer was formed by CVD, and the Ti and Pt seed layers were formed by ion-beam sputtering. Ion-beam sputtering conditions of Ti and Pt seed layers are listed in Table I. Reaction pressure, sputtering time, output electric power, temperature, and their thickness are shown in the table. After cutting the wafer into a substrate size of $2 \times 2$ cm, the lower Pt electrode was electrodeposited on this Pt seed layer. The lower Pt electrode of 500 nm in thickness was electrodeposited for 5 min at $i = 100$ A $m^{-2}$ with stirring of 400 rpm. PRECIOUSFAB Pt 1000 Pt bath (Electroplating Engineers of Japan Ltd.) was used at bath temperature of 343 K. HZ-3000 of Hokuto-Denko Co., Ltd. was used as current source. Then the Pt electrodeposits were annealed in an infrared furnace (GFA-430V, Thermo Riko Co., Ltd.) under vacuum condition to improve the crystalline orientation. This annealed Pt electrodeposited layer with annealing acted as the lower electrode of the capacitor. Then the PZT layer was formed on the lower Pt electrode by MOCVD. The raw materials conditions are listed in Table II. MOCVD sources, temperature, and argon gas flow rate are shown in the table. Substrate temperature, oxygen gas flow rate, reaction pressure, and deposition time are also shown in the table. The upper Pt electrode was formed by sputtering and patterned by a lift-off pro-

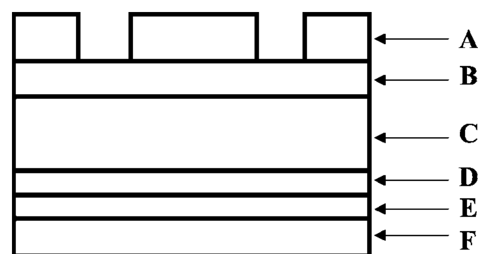


**Figure 1.** Schematic illustration of the capacitor. (a) Upper Pt patterned electrode; (b) PZT; (c) lower Pt electrode; (d) Pt seed layer; (e) Ti seed layer.

**Table I. Ion-beam sputtering conditions.**

| | Conditions of reaction | | | |
|---|---|---|---|---|
| | Lower Pt electrode | Upper Pt electrode | Ti Seed layer | |
| Reaction pressure | | 667 mPa | | |
| Sputtering time | 247 s | 165 s | 20 s | 60 s |
| Output | 1 kW | | 0.5 kW | |
| Temperature | 573 K | 298 K | 573 K | |
| Thickness | 150 nm | 100 nm | 5 nm | 15 nm |

cess. Figure 2a shows the lift-off process to form the patterned upper Pt electrode. Figure 2b is the photomask pattern. The Pt-PZT-Pt capacitor was finally fabricated by the formation of a patterned upper Pt electrode by the lift-off process and Pt sputtering. The surface morphologies of the deposits were observed by FE-SEM (Hitachi S-4300). The crystal structures of the Pt electrodeposition layer and the Pt seed layer were identified by X-ray diffraction analysis (Rigaku RAD-2VC, X-ray tube voltage = 40 kV, current = 30 mA). The concentration profiles of each element in the metal layer were measured by GDS (Glow Discharge Spectroscopy, HORIBA JY-6300F). Electrical properties of PZT capacitors were measured using a Sawyer-Tower circuit, a pulse generator (NF:WF1946), a digitizing oscilloscope (HP:54616B), and an electrometer (Keithley:6517).

## Results and Discussion

*Crystalline orientation of the lower Pt electrode*.— The degree of crystal orientation for the platinum electrodeposit layer and the platinum seed layer were examined by X-ray diffraction analysis. Figure 3 shows the result of relative X-ray integrated intensity by changing annealing temperature and time. The relative X-ray integrated intensity is the ratio of the diffraction intensity of an annealed Pt(1 1 1) specimen divided by that of a nonannealed one. Figure 3a is with 1 h annealing time. The relative X-ray integrated intensity is largest at 823 K annealing temperature. Figure 3b is with 823 K annealing temperature. The relative X-ray integrated intensity is the largest at 1 h annealing time. Therefore, the relative X-ray integrated intensity of the annealed specimen at 823 K for 1 h shows the largest relative X-ray integrated intensity, which is six times larger than that of the nonannealed one. We adopted the annealing condition of 823 K for 1 h in the following experiments.

Figure 4 shows the XRD patterns after deposition of PZT on the Pt electrode. Ti layer thickness was 5 nm for Fig. 4a and 15 nm for Fig. 4b, respectively. With 5 nm Ti sputtering layer (a), a very strong Pt(1 1 1) peak exists at about $2\theta = 40°$ and a weak Pt(2 0 0) peak exists at about $2\theta = 46°$. PZT(1 0 1) and PZT(2 0 0) peaks also exist at about $2\theta = 32$ and $47°$, respectively. With a 15 nm Ti sputtering layer (Fig. 4b), Pt(1 1 1), Pt(2 0 0), PZT(1 0 1), and PZT(2 0 0) peaks also exist, however their intensities are much weaker than those of Fig. 4a. Pt(1 1 1) intensity of Fig. 4a is about several tens of times larger than that of Fig. 4b and PZT(1 0 1) and PZT(2 0 0) intensities are about ten times larger.

**Table II. PZT layer formation conditions.**

| Raw material conditions Source | Temperature | Ar gas flow rate |
|---|---|---|
| $(C_2H_5)_3PbOCH_2(CH_3)_3$ | 313 K | 100 cm$^3$/min |
| $Zr(O\text{-}t\text{-}C_4H_9)_4$ | 303 K | 60 cm$^3$/min |
| $Ti(O\text{-}i\text{-}C_3H_7)_4$ | 303 K | 40 cm$^3$/min |
| Condition of reaction | | |
| Substrate temperature | | 723 K |
| $O_2$ gas flow rate | | 260 cm$^3$/min |
| Reaction pressure | | 667 Pa |
| Deposition time | | 30 min |

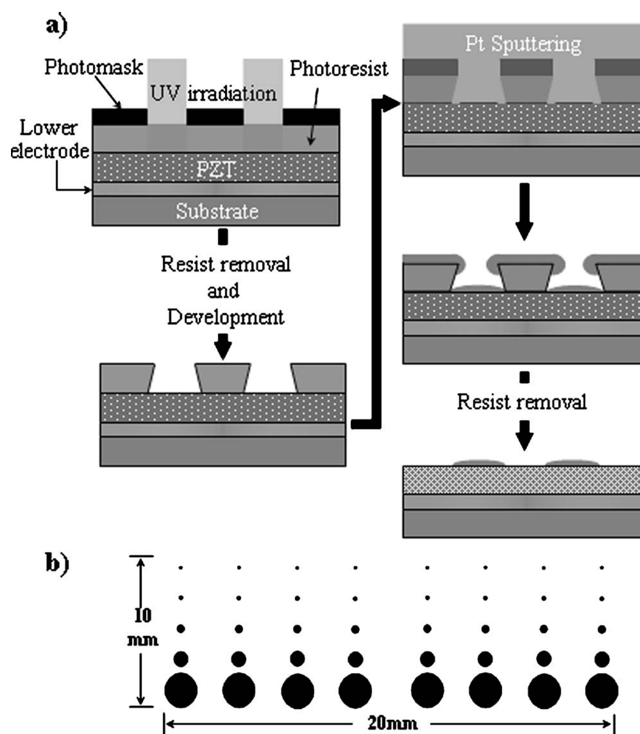


**Figure 2.** Schematic illustration of lift-off process to form patterned upper Pt electrode and the pattern. (a) Lift-off method process; (b) photomask pattern used in the lift-off process.

*Electric characteristics for the Pt/PZT/Pt capacitor*.— Figure 5 shows the electric characteristics of the Pt/PZT/Pt capacitor. Figure 5a illustrates the relationship between the electric displacement and applied electric field (*D-V* characteristics), and Fig. 5b the relationship between the current density and applied electric field (*I-V* characteristics) with both Ti seed layer thickness of 5 or 15 nm. The *D-V* characteristic of the Pt/PZT/Pt capacitor (Fig. 5a) indicated that a well-saturated *D-V* hysterisis loop was obtained with the 5 nm Ti seed layer and $\pm 12$ ($\mu$C cm$^{-2}$) electric displacement existed at an applied electric field of 0 (kV cm$^{-1}$). With the 15 nm Ti seed layer, the Pt/PZT/Pt capacitor barely showed a ferroelectric *D-V* hysterisis loop. As shown in Fig. 5b, the Pt/PZT/Pt capacitor with the 15 nm Ti seed layer shows a rapid increase in the current

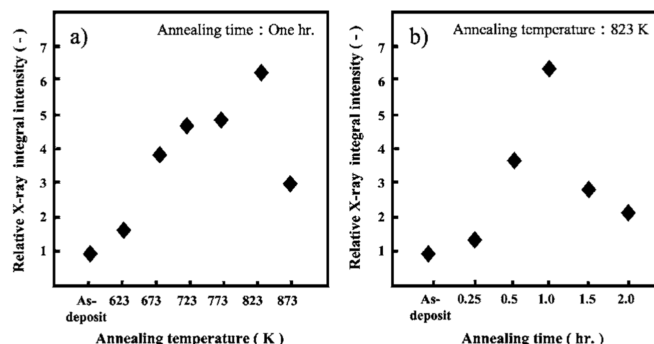


**Figure 3.** Effect of annealing of Pt (seed)/Pt (electrodeposit) substrate. (a) Relationship between annealing temperature and relative X-ray integral intensity; (b) relationship between annealing time and relative X-ray integral intensity.

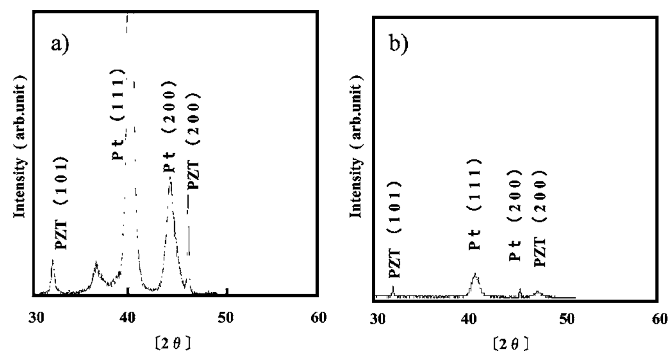

**Figure 4.** X-ray diffraction results of Pt(seed)/Pt(electrodeposit)/PZT capacitor. (a) With the 5 nm Ti seed layer; (b) with the 15 nm Ti seed layer.

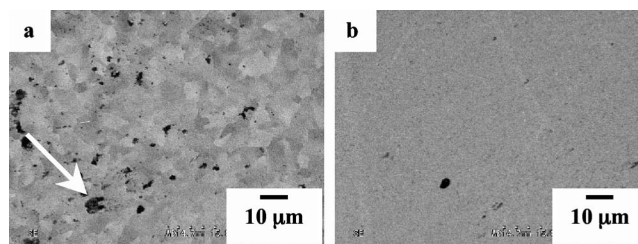

**Figure 6.** FESEM observation of the lower Pt electrode after annealing. (a) With the 15 nm Ti seed layer; (b) with the 5 nm Ti seed layer.

density at the applied electric field of ±20 kV/cm. The current density with the 5 nm Ti seed layer capacitor increases slowly with applied electric field even up to ±200 kV/cm. Accordingly, the Pt/PZT/Pt capacitor with the 5 nm Ti seed layer shows better electric characteristics than that with the 15 nm Ti seed layer.

*Annealing effect on lower electrode morphology and H concentration profile*.—Figure 6 is the FE-SEM images of the lower electrode surface annealed at 823 K for 1 h with a Ti seed layer thickness of 15 nm (Fig. 6a) and 5 nm (Fig. 6b), respectively. Figure 6a shows numerous several-μm-sized voids (see arrow in Fig. 6a), while there are many fewer voids and the surface is much smoother in Fig. 6b.

Figure 7 shows the concentration depth profiles of Ti and Pt seed layers without Pt electrodeposit (lower Pt electrode annealed at 823 K for 1 h). Figure 7a is the case with the 15 nm Ti seed layer and Fig. 7b is that with the 5 nm Ti seed layer. The sputtering time is shown as the $x$ axis and element intensity profiles are plotted as the $y$ axis. With (a) of the 15 nm Ti seed layer (Fig. 7a), Pt exists up to a sputtering time of 1.0 s and Ti exists up to 2.0 s. Si appeared after 2.0 s. The H peak coincides with Ti peaks. With (b) of the 5 nm Ti seed layer (Fig. 7b), Pt and Si intensities are almost the same as those in Fig. 7a. Ti and H intensities in Fig. 7b, however, are much smaller than those in Fig. 7a.

*Discussion on annealing effect and electrical characterization*.—Figure 8 shows a schematic illustration of hydrogen and the Ti seed layer. From the GDS result, the 15 nm Ti seed layer has much higher H intensity and the H peak coincides with Ti (Fig. 7a). Also, it is well known that Ti has the property of H storage.[16,17] Let us compare the Pt/PZT/Pt capacitor with the 15 nm Ti seed layer and with the 5 nm Ti seed layer based on the hydrogen reaction.

With the 15 nm Ti seed layer, numerous voids form on the lower Pt electrode, as was shown with an arrow in Fig. 6a. X-ray diffraction intensities of Pt(1 1 1), Pt(2 0 0), PZT(1 0 1), and PZT(2 0 0) become weaker than those with the 5 nm Ti seed layer (Fig. 4). The H peak intensity coincides with the Ti peak in the case of the 15 nm Ti seed layer (Fig. 7a). The hydrogen that existed in the Ti seed layer transmits into the lower Pt electrode and the PZT layer and their crystal lattices interstitially. These H atoms in the Ti seed layer cause voids in the lower Pt electrode (Fig. 6a), and X-ray diffraction intensities of Pt and PZT are weakened (Fig. 4b). Furthermore, *D-V* characteristics barely show a ferroelectric *D-V* hysterisis loop (Fig. 5a) and *I-V* characteristics show a large leakage current (Fig. 5b).

With the 5 nm Ti seed layer, the lower Pt electrode has fewer voids and the surface is much smoother than the lower Pt electrode with the 15 nm Ti seed layer (Fig. 6b). With concentration profile measurement, comparing with the case of the 15 nm Ti seed layer, a 5 nm Ti seed layer has smaller H intensity than 15 nm (Fig. 7). Also, the Pt(1 1 1) X-ray intensities of the 5 nm Ti seed layer are about several tens of times larger than 15 nm and PZT(1 0 1) and PZT(2 0 0) intensities are about ten times larger (Fig. 4). Due to the better crystal orientations of the ferroelectric PZT layer, a well-saturated *D-V* hysterisis loop was obtained (Fig. 5a) and the current density increases slowly up to ±200 KV/cm of applied electric field (Fig. 5b) with a 5 nm Ti seed layer Pt/PZT/Pt capacitor.

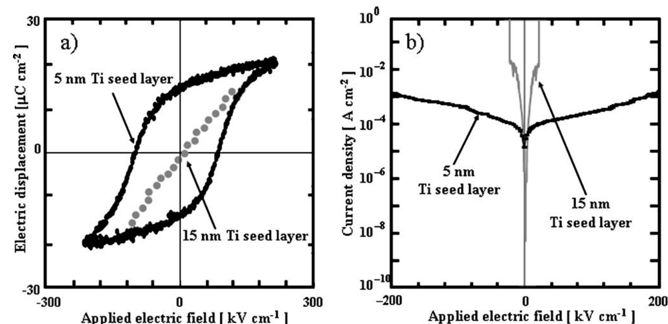

**Figure 5.** Electric characteristics of the Pt/PZT/Pt capacitor. (a) *D-V* characteristic of the capacitor; (b) *I-V* characteristic of the capacitor.

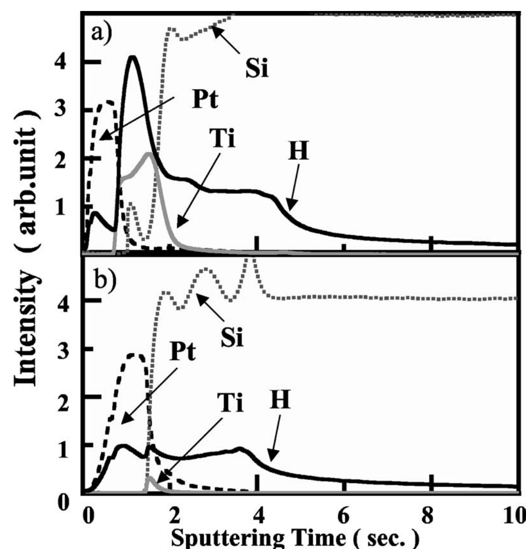

**Figure 7.** Concentration depth profile of elements measured by GDS. (a) With the 15 nm Ti seed layer; (b) with the 5 nm Ti seed layer.

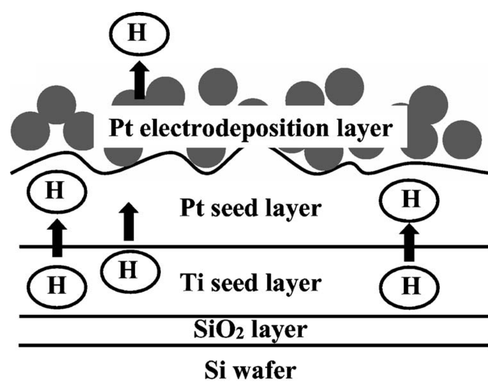


**Figure 8.** Surface illustration of hydrogen and the Ti seed layer.

## Conclusion

The lower Pt electrode of a Pt/PZT/Pt capacitor prepared by electrodeposition has been examined in detail.

1. The relative X-ray integrated intensity of electrodeposited Pt is the largest at an annealing condition of 823 K and 1 h. The Pt crystal orientation with the 5 nm Ti seed layer is much larger than that with the 15 nm Ti seed layer.

2. Lower Pt electrodes annealed at 823 K for 1 h with the 15 nm Ti seed layer had numerous several-μm-sized voids on their surface. Fewer voids exist and the surface is much smoother with the 5 nm Ti seed layer.

3. From the GDS result, the 15 nm Ti seed layer was found to contain a much higher concentration of hydrogen.

4. Pt/PZT/Pt capacitor with the 5 nm Ti seed layer achieved a well-saturated *D-V* hysteresis loop and suppressed leakage current up to ±200 KV/cm, due to better crystal orientations of the lower Pt electrode and PZT layer and smooth surface morphology.

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