REVERSE CONNECTION OF MTJ DEVICE IN STT-RAM CELL

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STT-RAM technology is an emerging memory technology which is a future replacement for conventional memory technologies. STT-RAM promises fast read-write-access speeds, low power consumption, high density, non-volatility and very long life time. As with any emerging technology, however, STT-RAM has its own set of characteristic disadvantages which must first be overcome before it can be considered a viable replacement for existing solutions, an example of such being its asymmetric behavior during write operations. Currently, reverse connection of the MTJ device in STT-RAM cells is being proposed as a novel solution for compensating for this asymmetric write operation. In this work, two different MTJ devices are examined to determine which one is better suited for use with conventional connection method and which is more convenient to use with the proposed reverse connection method. Thereafter, the results of the study are applied to determine what properties of an MTJ device most heavily influence whether it is best utilized with a reverse connection versus a conventional connection.

TABLE OF CONTENTS

LIST OF FIGURES

ACKNOWLEDGMENT

Before I finished my bachelor degree, I started to look for some opportunities to further my education in US. I wanted to have Electrical and Computer Engineering education US because I have a passion about hardware design, architecture and embedded systems. In the beginning of my education in US I was frightened because I realized how much I need to learn. My fear has gone after I became a part of the Pitt community and met helpful friends. I learn a lot from friends who helped me to improve my skills and develop a better knowledge about my study field.

While finishing two years of education I know that I have long way to be a good researcher. I am so happy and proud that I can walk through this long way as a PhD student with the help of experience and advices of Professor Chen.

I am very thankful to Professor Alex Jones, Professor Steven Levitan and Professor Helen Li for their kindly acceptance of being my committee members. Thanks to our research group who gave me motivation and knowledge which helped me to complete my work.

Thanks to my country (Turkey) which supports my education in US with a high trust and faith. Thanks to my parents who raised me and made me who I am today.

1.0 INTRODUCTION

Spin transfer torque magnetic memory (STT-RAM) is a newly developing technology which is showing strong promise as a future alternative for conventional memory technologies such as SRAM, DRAM and FLASH. These three existing types of memory each have their own unique advantages and disadvantages, lending them to be selectively utilized based on the desired application.

	SRAM	DRAM	FLASH (NAND)	STT-RAM
Non-Volatile	No	No	Yes	Yes
Cell Size (F^2)	50-120	6-10	5	6-20
Read Time (ns)	1-100	30	50	2-20
Write/Erase Time (ns)	1-100	15	1µs/0.1ms	2-20
Endurance	10^{16}	10^{16}	10^{5}	10^{15}
Write Power	Low	Low	Very High	Low
Other Power Consumption	Leakage	Refresh	None	None
High Voltage Required	No	3V	16-20V	<1.5V

Figure 1. Advantages and disadvantages of different memory technologies [1].

SRAM is described as static memory due to the fact that it requires only a very low amount power to retain data. SRAM is able to achieve very fast read-write speeds, but its large cell size

(with different designs, such as 4T, 6T, 8T, etc., each requiring different amount of transistors) limits the number of scenarios in which it can be effectively utilized. Because of this, SRAM is useful for performance or low power oriented applications such as caches or mobile devices. Despite its label, however, SRAM is in fact a volatile memory technology, and because of this will lose stored data if power is no longer supplied.

Because of its relatively small cell size, DRAM technology is most useful in applications which stand to benefit from high density memory, such as the main memory in most modern computing systems. A single DRAM cell consists of one transistor and one capacitor, with the charge of the capacitor being used as the data storage mechanism for the device. As the charge stored by the tiny capacitor leaks quickly, the DRAM cells must be refreshed frequently in order to maintain data integrity. The requirement of this memory to be actively powered and refreshed is the reason that it is referred to as 'dynamic,' and causes high power consumption even when values in memory are not being actively read or modified.

FLASH memory is quickly seeing adoption as the replacement for conventional mechanical hard disks when used as main storage in a system. Non-volatility, high density and low power consumption (no leakage or refreshing power consumption) make it particularly well suited for many mobile applications. Unfortunately, FLASH memory still has its disadvantages, such as very slow write speeds and, most importantly, very low durability. Most FLASH memory available today has only a 100,000 cycle wear-free lifetime. Beyond this point, memory wear begins to degrade performance and data integrity. The two main forms of FLASH memory are NAND or NOR, referred to as such because of the gates utilized in the memory's cell connection scheme.

Because of the unique characteristics of each type of memory, a system must selectively utilize some of each if it hopes to optimize performance, power consumption, and cost. One of the most exciting properties of STT-RAM is that it has all the advantages of SRAM, DRAM and FLASH combined [21]. This makes it a promising candidate to replace all of the conventional memory technologies, as the homogenization of memory architecture throughout the entire system would allow for both an increase in system performance and a reduction in power consumption and overall cost.

STT-RAM consists of two parts; a magnetic tunneling junction and an access transistor.

The magnetic tunneling junction (MTJ) has three basic layers, including two ferromagnetic layers and an insulation layer which is sandwiched between them. Electrons pass from one ferromagnetic layer to another by tunneling through the thin insulation layer. This phenomenon is called tunneling magneto resistance (TMR).

The conductance of MTJ depends on the magnetization direction of its ferromagnetic layers. One of the ferromagnetic layers is pinned, forcing it to maintain a constant magnetization direction, while the magnetization direction of the second ferromagnetic layer is adjustable. The parallel magnetization state is a low resistance state and denotes a logical ‘0’. The antiparallel state is a high resistance state and denotes a logical ‘1’. By utilizing the distinguishable properties of these two states, data is stored as different resistance states inside the MTJ.

During the 1990’s, the exploratory research into TMR in MTJ’s at room temperature sparked a large increase in interest in the area. In 1996, J. C. Slonczewski introduced the spin transfer torque effect in MTJ’s [2]. Before the usage of the STT effect, MRAM technology could not be reliably implemented with technology below the 90nm threshold due to its relatively high power requirements. After the application of Slonczewski’s discovery, STT-RAM can now be

successfully scaled to processes below 65nm [1]. STT-RAM technology offers features such as low access time (read-write), small cell size, high process compatibility and scalability, and the elimination of the need for standby power.

One of the largest drawbacks of STT-RAM is the asymmetric nature of the current required to change the logical value stored in the MTJ. Switching the ferromagnetic layers from parallel state (low resistance) to anti parallel state (high resistance) requires more current than switching from anti-parallel state (low resistance) to parallel state (high resistance). This in and of itself is not an issue – however, when it is considered that the size of the access transistor is determined by the maximum amount of current it will need to pass, it becomes easy to see that the transistor is oversized for anti-parallel state to parallel state switching. This means that the STT-RAM cell is less dense, more power hungry and slower than it can be. In order to reduce the transistor size to alleviate some of these inefficiencies, a solution of connecting the magnetic tunneling junction (MTJ) reversely (free layer to access transistor and pinned layer to bit line) has been proposed.

In this work, I delve into reverse connection usage in order to determine if there are any characteristic conditions in which the reverse connection method is superior to that of the conventional method. I examine the different source degeneration effects on access transistor for different MTJ connection schemes. I also observe the effects of the reverse connection on access transistor size and attempt to discover if reverse connections can in fact reduce the cell size.

1.1 THESIS OUTLINE

Part one (Introduction) discusses the motivation for STT-RAM and provides the reader with basic background knowledge. Part two (Background) contains three subsections, the first of

which reviews the fundamentals of spintronics, the technology's history, and how it works. The second subsection covers the MTJ device specifically, in addition to its operating characteristics. The final subsection of part two discusses the role of the access transistor in STT-RAM. Part three (STT-RAM Cell Structures and Operation) talks about different cell structures and how STT-RAM operates. Part four (Model Creation and Testing) is about model creation and testing for reverse-conventional connections of the magnetic tunneling junction (MTJ). Finally, part five (Conclusions and Future Work) presents relevant findings discovered during the course of this work, as well as the prototypical situations in which reverse connections can be particularly useful.

2.0 BACKGROUND

The background part concentrates on basics properties of MTJ devices and spintronics study field. Moreover, it states some historical achievements which led developments in this specific area.

2.1 BASICS OF SPINTRONICS

Spintronics which is a word derived from ‘spin’ and ‘electronics’ is seen as a strong replacement candidate for conventional charge based electronics [3]. Today’s commercialized electronic devices’ operations are based on controlling the flow of electric charge through silicon based semi-conductor devices. On the other hand, non-volatile storage devices such as hard disk drives depend on regulation of electrons’ spin polarization via ferromagnetic devices [3]. Spintronics focuses on integrating the methods used in storage devices and processing units with the usage of spin polarized current [3].

2.1.1 Development History

In 1930s the discovery of inconsistent resistance behavior in ferromagnetic materials created a starting point for spintronics [3]. In 1970s research continued in this field and the first spin

filters, creation of spin polarized current and the effects of spin polarized currents on ferromagnetic devices was observed. Early experiments were conducted at very low temperatures because at that time room temperature magneto resistive effects weren't discovered yet. With the exploration of room temperature magneto resistive effects in 1980s, radiation-hard (convenient to use in military applications such as satellites etc.) wire-plated resistive memories were replaced with anisotropic magneto resistive (AMR) memories [1]. In late 1980s another milestone was achieved by the discovery of giant magneto resistance (GMR) [4]. The newer GMR technology based devices replaced the AMR based technologies quickly. Electronic storage of information is based on spin polarization of electrons since the discovery of GMR.

The materials which can provide higher TMR ratios (at room temperature) in MTJ devices were discovered in early 1990s [1]. As a result devices with very high TMR ratios (%200) have been developed. Today many spintronics based devices are commercialized and spintronics based memories are gradually becoming a very big industry.

2.1.2 How It Works

The spin polarization of electrons is not fixed and can be altered. We can change the polarization direction for the electrons if we make the electrons pass through a magnetic field. There are two possible conditions for the relationship between electron's spin polarization and the magnetic field: parallel polarization to the magnetic field or anti parallel [1]. The spin polarizer works in regard to this phenomenon. We can use a ferromagnetic layer (Figure 2) which has the desired magnetization direction to create spin polarized current from un-spin polarized current [4]. Furthermore, polarized current only can pass through a ferromagnetic layer if it has parallel spin polarization to the magnetization direction of the ferromagnetic layer. Antiparallel polarized

current cannot pass through a ferromagnetic layer. Spin valves were developed based on this mechanism. A spin valve consists of a spin polarizer (Figure 2) which makes the current spin polarized in the desired direction and a spin filter (Figure 3-4) which lets the current pass if only it has the same polarization direction as its magnetization [3]. With the variable direction of the spin filter's magnetization we can control the current flow on the spin valve. MTJs are basically spin valves which have two states: high resistance which denotes logic '1' and low resistance which denotes logic '0' [1].

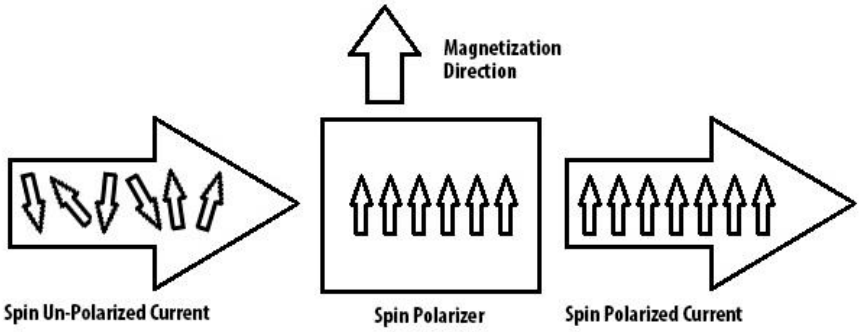

Figure 2. Spin polarizer operation.

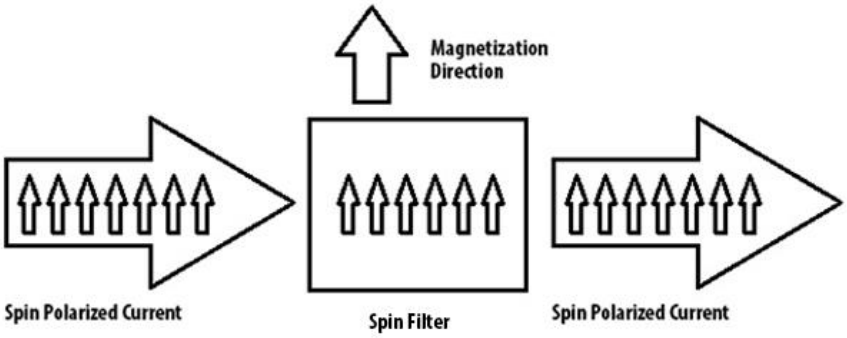

Figure 3. Spin filter operation.

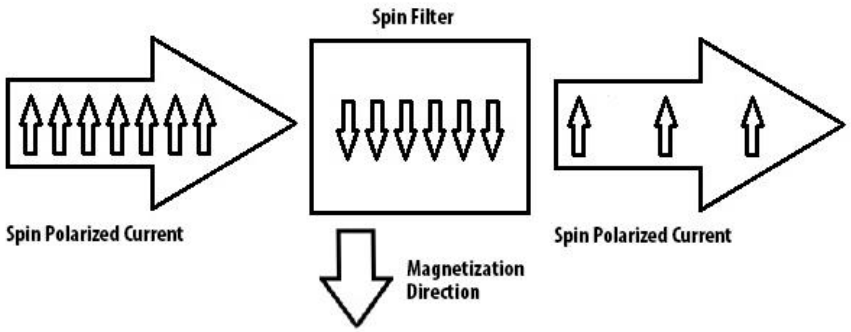

Figure 4. Spin filter operation.

2.2 MAGNETIC TUNNELING JUNCTION

Spin transfer torque random access memory cell (STT-RAM) consists of two parts; magnetic tunneling junction (MTJ) and access transistor. This part focuses on MTJ device, its principles and characteristics.

2.2.1 Hysteresis

Resistance hysteresis which MTJ devices have makes the MTJ device has two distinct resistance states. Controllability of switching between these two stages makes MTJ device a very convenient storage element. MTJ's resistance hysteresis is a result of spin valve structure [3]. As stated before MTJ device has three layers; an insulation barrier which is sandwiched between two ferromagnetic layers. One of the ferromagnetic layers has a constant magnetization direction while other has an alterable magnetization direction. Pinned layer is used as a spin polarizer and the free layer used as spin filter. This type of structure allows two states for the MTJ: parallel

state which both layers has same magnetization direction and anti-parallel state which two layers have opposite magnetization direction. For the parallel state when we apply a current through device spin polarizer creates a spin polarized current. Since the two layers have same magnetization direction current can pass through device without disturbance. For the anti-parallel state the spin polarized current which is created by spin polarizer has opposite polarization direction with the spin filter. As a result current cannot pass through the device freely. MTJ device's resistance has two stages based on whether FL's and PL's magnetization direction is parallel or anti-parallel as stated above. As illustrated in Figure 5 MTJ is in high resistance state when MDs are anti-parallel and low resistance state when MDs are parallel. Low resistance denotes logic '0' and high resistance denotes logic '1'.

Figure 5. Resistance states of MTJ.

The difference between the resistance states defined as Tunneling Magneto Resistance (TMR). TMR ratio shows the efficiency of spin valve structure of MTJ device. TMR formulated as:

$$TMR = \frac{R_{AP} - R_P}{R_P} \text{ [8]}$$

2.2.2 Critical Switching Current of MTJ

2.2.2.1 Asymmetry of Critical Switching Current

In order to switch the magnetization direction of free layer we need to apply a certain amount of current. We call this current the critical switching current. Critical switching current for anti-parallel state to parallel state switching is less than parallel state to anti-parallel state switching (I_C(P to AP) > I_C(AP to P)) [6]. Switching current asymmetry is related with TMR ratio and according to some papers increases linearly with it [7]. The MTJ switching current asymmetry of two directions, which are AP to P and P to AP, is a result of different spin-transfer efficiency η [7]. For instance, when MTJ works at thermally activated switching time region (>10ns), critical switching current density can be calculated as:

$$J_{C_0} = \left(\frac{2e}{\hbar}\right) - \left(\frac{a}{\eta}\right)(t_F M_s)(H_k \pm H_{ext} + 2\pi M_s) \text{ [7] (1)}$$

In equation 1, J_{C_0} is the minimal current density need for switching the stare of MTJ device when there is no external magnetic field at 0K. e is electron charge. a is damping constant. M_s is magnetization saturation. t_F is free layer thickness. ħ is reduced planck's constant. H_k is effective anisotropy. H_{ext} is external magnetic field. The spin transfer efficiency η depends on the magnetization directions of the FL and PL:

$$\eta = \left(\frac{P}{2}\right)(1 + P^2 cos\theta) \text{ [7] (2)}$$

In equation 2, P is the tunneling spin polarization and θ is the angle between free layer's and pinned layer's magnetization directions. When we combine equation 1 and equation 2 we get:

$$\frac{J_{C_0}^{0\to1}}{J_{C_0}^{1\to0}} = \frac{1+P^2}{1-P^2} \text{ [7] (3)}$$

As we can see in equation 3, switching from parallel to anti parallel state ($J_{C_0}^{0\to1}$) requires more current density than switching from anti parallel to parallel state ($J_{C_0}^{1\to0}$) [7].

2.2.2.2 MTJ switching Types

There are three different types of MTJ switching; precessional switching, dynamic switching and thermally activated switching [8]. Precessional switching occurs in very short time (less than 3ns). In order to accomplish precessional switching we need to apply a current density which

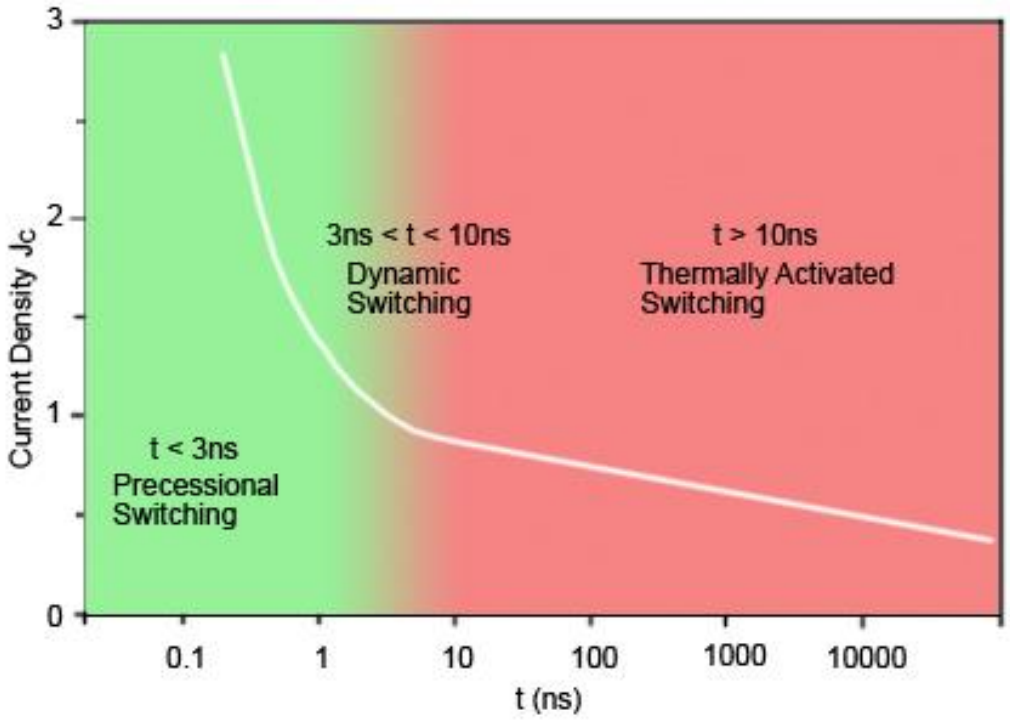

Figure 6. Different switching regimes [8].

should be many times larger than critical switching current density [8]. Dynamic switching occurs in 3ns to 10ns time interval. It needs medium level current density. Dynamic switching is like a mix of precessional and thermally activated switching. Because of its complicated process

it is hard to explain it with a mathematical formula. Dynamic switching corresponds to MTJ device's normal working condition. Final switching type is thermally activated switching. This switching occurs beyond 10ns time scale. The thermal activated switching depends on the current pulse width.

2.2.2.3 Thermally Varying Switching

Thermal disturbance makes the magnetization directions of ferromagnetic layers continuously changing [9]. The critical switching current becomes time-varying because of changing thermal effect [10]. It is possible to obtain a controlled switching current curve with using a probabilistic distribution [11].

2.2.3 Temperature Effect on MTJ

The Julliere conductance model describes the thermal effect on TMR at zero bias voltage [12]. According to the Julliere model MTJ conductance has two parts; G_T, as a result of tunneling, and G_{SI}, as a result of defects in insulation barrier. The total conductance (G) can be expressed as a function of Θ:

$$G(\Theta) = G_T\{1 + P_1P_2\cos(\Theta)\} + G_{SI} \text{ [21]}$$

P_1 and P_2 are tunneling spin polarization, Θ is angle between magnetization directions of ferromagnetic layers (Θ=0^o for parallel state, Θ=180^o for anti-parallel state). The temperature dependence of tunneling spin polarization is:

$$P(T) = P_0(1 - a_{sp}T^{\frac{3}{2}}) \text{ [21]}$$

Variations in G_T due to temperature effect are almost zero [21]. However, theoretical and experimental results show that G_{SI} is proportional to $T^{\frac{3}{2}}$ [13].

Basically speaking as the temperature gets high resistance of anti-parallel state degrades significantly. The resistance of parallel state is not affected from temperature change as much as anti-parallel state. The asymmetric changes of the resistances for different states cause the degradation of $TMR = \frac{R_{AP}-R_P}{R_P}$. Lower TMR means more difficult sensing. Moreover, high temperature reduces the critical switching current and magnetic stability energy. As a result variation of switching time increases and switching process of MTJ device becomes more unreliable.

2.2.4 Effect of Bias Voltage on TMR

The Julliere conductance model can only predict TMR ratio at zero bias voltage [14]. However, there is an anomaly in TMR ratio which is called zero bias anomaly [15]. What causes the bias voltage dependent anomaly in TMR ratio cannot be fully discovered [16]. Anyhow, elastic currents are considered as an effector at low voltages [17] and redistribution of density of states is considered as an effector at high voltages [16].

2.3 ACCESS TRANSISTOR

The access transistor is second part of a STT-RAM cell. The access transistors driving ability is important because it determines the current which the access transistor can provide to the MTJ device. This current used as switching current and switching time depends on it. If we need faster

switching time, we need to use larger transistor. Increasing the transistor width increases the transistors driving ability but it also increases the cell size. Thus transistor size needs to be selected in regard to balance between cell size and speed.

2.3.1 Source Degeneration

In a STT-RAM cell, access transistor can provide different amount of current for different switching schemes. This problem is a result of source degeneration effect on access transistor. If there is a resistor between access' transistor's source and the ground, the transistor has a reduced V_{GS}. This is called source degeneration and causes a lower transistor driving ability [23]. You can see the source degeneration effect in Figure 7.

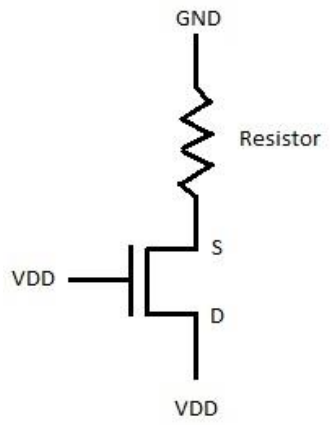

Figure7. Source degeneration. $\boldsymbol{V_{GS} = V_{DD} - I_R R_R}$

2.3.2 Temperature Effect on NMOS

Since the NMOS and MTJ device placed in the same cell the temperature change at MTJ cell also affects the NMOS. As temperature gets high the driving ability of the NMOS reduces. We can explain this via the formulas below.

$$\beta = \mu_0 T_r \left(\frac{T}{T_r}\right)^{-k_\mu} \frac{C_{ox}}{1 + U_0(V_{gs} - V_{th})} \frac{W}{L} \text{ [23]}$$

In the equation above T denotes the temperature. As we can see from the equation β reduces while T increases.

$$I = \beta \frac{V_{ds}(V_{gs} - V_{th}) - \frac{a}{2} {V_{ds}}^2}{1 + \frac{1}{V_{sat} L} V_{ds}} \text{ [23]}$$

In the equation above we can see that the current I increases with β. We can clearly see from both equations when the temperature gets higher the current transistor can provide gets lower.

3.0 STT-RAM CELL STRUCTURES AND OPERATION

3.1 CELL STRUCTURES

3.1.1 1T1J Cell Structure

1T1J structure is the basic cell structure of STT-RAM memories. It basically means one transistor and one MTJ device.

The transistor is used as an access transistor and it is the main component which determines the cell size. The access transistor has to provide certain amount of current to the MTJ device in order to make it switch between low and high resistance stages. The switching current determines the write speed of the memory cell. Therefore the transistor has to be properly sized in order to provide necessary current. Thus it is usually bigger than the MTJ device itself.

MTJ device has to have elongated cell shape in order to keep thermal stability. MTJ devices' and transistor's channel length is equal (in regard to used technology like 45nm etc.). But the width of the devices may differ. We usually use wider transistor to provide appropriate current to the MTJ.

There are two most common cell architectures for 1T1J type STT-RAM cells, the conventional connected MTJ and the reverse connected MTJ. In the conventional connection the free layer of the MTJ device is connected to bit line and the pinned layer is connected to source

line (Figure 8). In order to produce a good pinned layer, pinned layer has to have a smooth deposition surface. Because of the surface imperfections which are the result of deposition procedure, depositing the fixed layer on top of the free layer is less efficient. This is the reason why free layer is on top structure called conventional and commonly used [19].

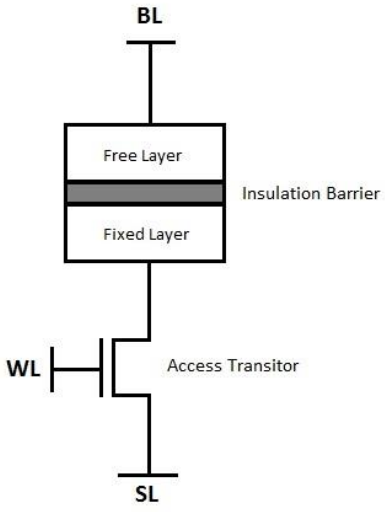

Figure 8. Conventionally connected 1T1J memory cell.

In the reverse connection fixed layer is on top of the free layer and connected to bit line (Figure 9). Free layer is connected source line via access transistor. Reverse connection is proposed for reducing the write operation asymmetry of STT-RAM cell [7].

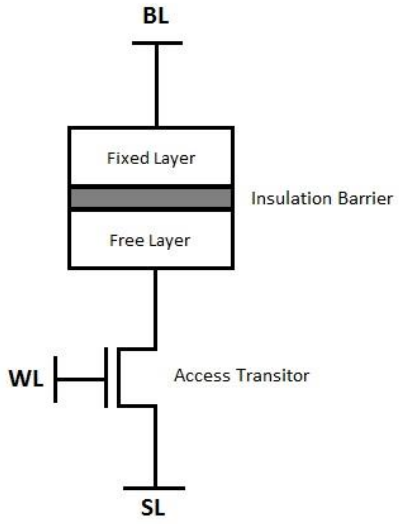

Figure 9. Reverse connected 1T1J memory cell.

Sub-arraying is applied in most memory architectures in order to maintain the balance between minimum area, high speed and power need. Single partition large memory cells require longer and complex access lines which mean additional buffering and slow access time. Therefore, memory cells can be divided into smaller sub-arrays and can be faster. Similarly, 1T1J cell memories divided in to sub arrays. Single bit line is usually used for up to 256 1T1J cells.

3.1.2 Shared Structure

In shared architecture access transistor is connected to more than one MTJ device [21]. Each MTJ device is connected to separate bit lines in order to provide single MTJ access. This architecture allows sizing up the access transistor to provide more current. Also even if we use

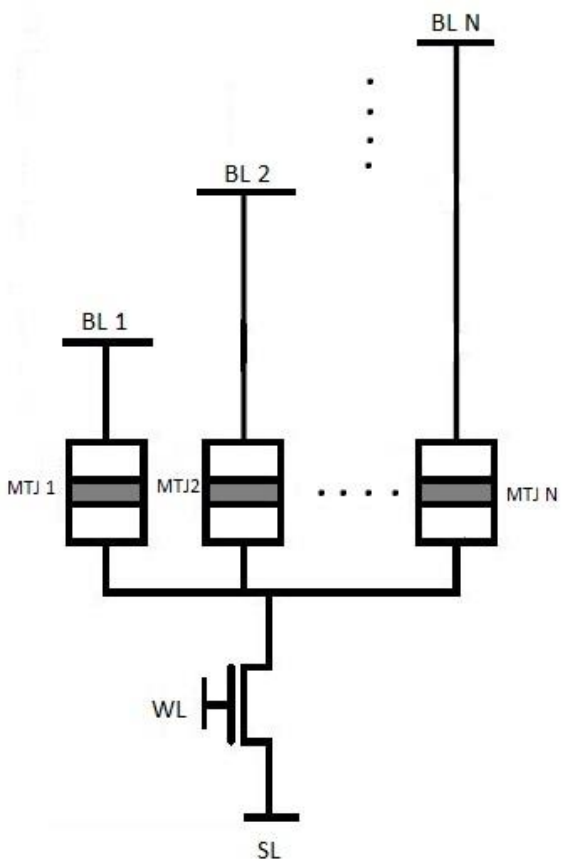

Figure 10. Shared architecture with n MTJs.

bigger transistor size because of we connect the transistor more than one MTJ device we can get the same or better density. The drawback of shared architecture is that when we try to write one of the n cells, current may go through different paths and causes unwanted switching or failure of other than desired cells.

3.1.3 Stacked Structure

Stacking is another cell structure for STT-RAM memories. In stacking architecture, multiple MTJ cells are connect to single access transistor as series [21]. This architecture is like multi cell Flash memory architecture. This architecture also can provide high density.

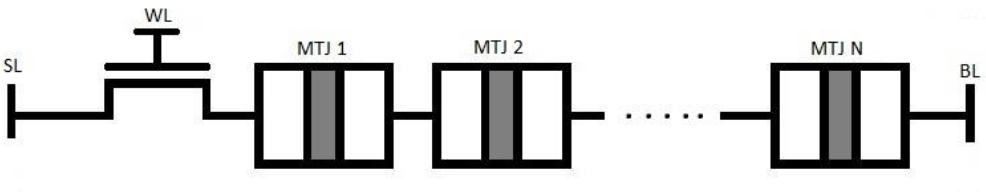

Figure 11. Stacked architecture with n MTJs.

When designing stacked memory, the resistances and critical switching current densities of each MTJ should be different and appropriately selected in order to create a properly functioning device. Reading from a certain MTJ device in the stack takes more than one cycle.

3.2 OPERATION

3.2.1 1T1J Cell

1T1J cell consists of a transistor and MTJ device. MTJ device also consists of two ferromagnetic layers and an insulation barrier, which is sandwiched between ferromagnetic layers. MTJ device is basically a spin valve. One of the ferromagnetic layers stands a spin polarizer while the other one stands a spin filter. One of the ferromagnetic layers has fixed magnetization direction and other one has an interchangeable magnetization direction. The magnetization direction of the free layer can be changed by applying a polarized current.

For the conventional connection as you can see from Figure 12 switching from low resistance state (logic‘0’) to high resistance state (logic‘1’) can be achieved by applying a current from source line (SL) to bit line (BL). In this case electrons pass through the free layer to fixed layer. Fixed layer does not let the electrons which are opposite polarized to its magnetization direction

pass. As a result the returning electrons scatter in the free layer and change its magnetization direction to opposite of fixed layer's magnetization direction. At the end of this process high resistance is achieved.

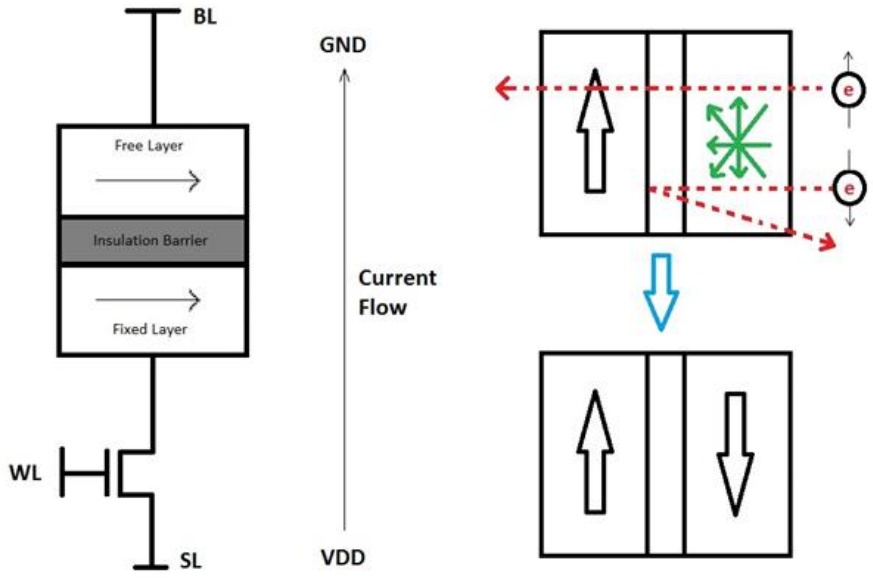

Figure 12. Parallel to anti-parallel switching.

For switching from high resistance state (logic'1') to low resistance state (logic'0'), we should apply a current from bit line (BL) to source line (SL). In this case electrons pass through the fixed layer first (Figure 13). Fixed layer again does not let the electrons which are opposite polarized to its magnetization direction pass. As a result the current passes through the free layer becomes spin polarized. The polarization direction is same as the fixed layer's magnetization direction. These electrons change the free layers magnetization direction parallel to fixed layer's magnetization direction. In the end both layers has the same magnetization direction which creates low resistance.

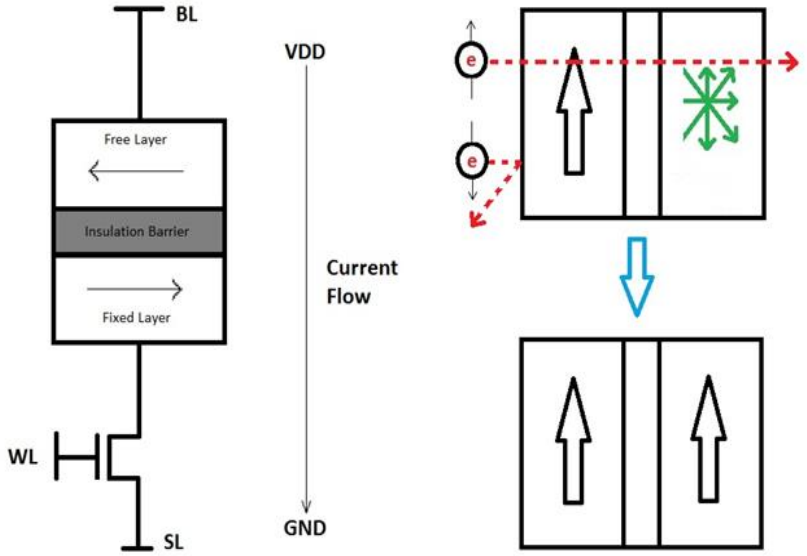

Figure 13. Anti-parallel to parallel switching.

3.3 STT-RAM WRITE OPERATION ASYMMETRY

Write operation in STT-RAM cell is not symmetrical. There are two main reasons for the asymmetric switching; MTJ device characteristics and driving ability change of access transistor due to source degradation.

As a result of MTJ device characteristics switching from parallel to anti-parallel state requires larger current than switching anti-parallel to parallel state (I_C(P to AP) > I_C(AP to P)) [6]. The critical switching current asymmetry is a result of the spin-transfer efficiency η change for different resistance states.

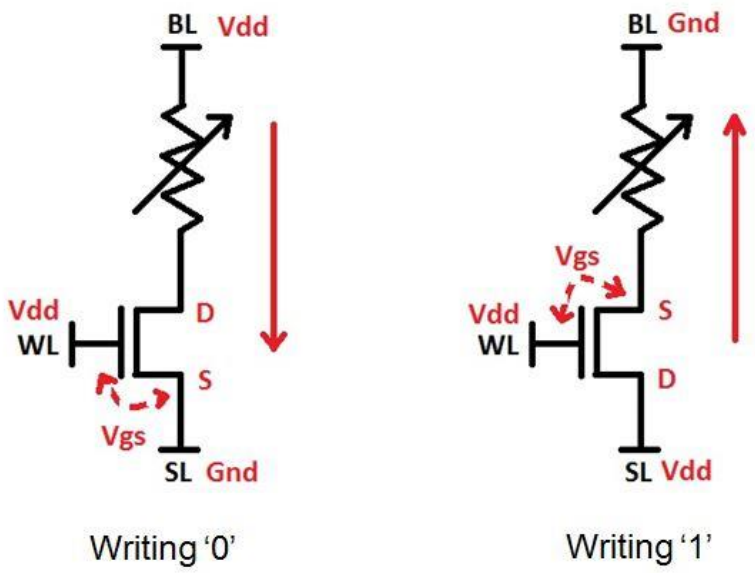

Figure 14. Write operation asymmetry.

The access transistor of STT-RAM cell has different driving ability for different switching types of MTJ. Source degeneration, which degrades the current applied to MTJ, is the reason of access transistor driving ability asymmetry. When switching '1' to '0' (parallel to anti-parallel state) word line (WL) and bit line (BL) is connected to V_{dd} and source line (SL) is connected to Gnd. In this case V_{gs} (gate voltage) is equal to V_{dd}. When switching '0' to '1' (anti-parallel to parallel state) word line (WL) and source line (SL) is connected to V_{dd} and bit line (BL) is connected to Gnd. In this case V_{gs} (gate voltage) is equal to $V_{dd} - I_{MTJ}R_{MTJ}$. In this case we have lower gate voltage which causes a reduced transistor driving ability.

4.0 MODEL CREATION AND TESTING

For this work I choose two MTJ devices from previous works and use their data (switching times for different switching currents). One of the MTJ devices is more convenient to use with conventional connection while the other one is more convenient to use with reverse connection. With comparing these devices I tried to find out which property of the MTJ device determines that the device is eligible to use with reverse connection. After finding this property I tried to examine equilibrium point for required access transistor size between conventional and reverse connection schemes.

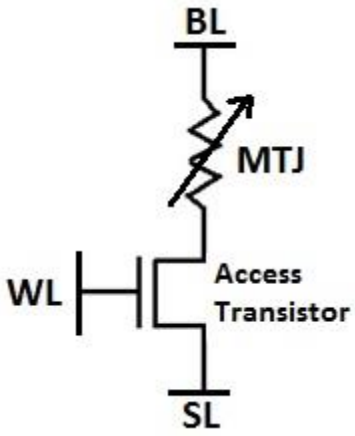

Figure 15. 1T1J memory cell model for simulation

As you can see in Figure 15 we can model a 1T1J memory cell with a resistance and a transistor. Resistor denotes the MTJ device and the transistor stands as access transistor. This is a basic model for simulation purposes. I created different models for different cases such as

reverse connection AP to P switching, reverse connection P to AP switching, conventional connection AP to P switching and conventional connection P to AP switching.

4.1 CONVENTIONAL CONNECTION COMPATIBLE DEVICE

4.1.1 Model Creation

First device I inspected is convenient to use with conventional connection. I started with creating models for different switching schemes. I used LTspice for my simulations. I used $V_{DD} = 1V$, 1kΩ for low resistance state and 2kΩ for high resistance state [22]. I used PTM 45nm library for the transistor because MTJ is 45nm.

First I created models for conventional connection. For the AP to P switching resistance is 2kΩ. V_{DD} is connected to bit line and ground connected to source line. Word line is connected to a pulse type voltage source. You can see the AP to P conventional connection switching model in Figure 16. For the P to AP switching resistance is 1kΩ. V_{DD} is connected to source line and ground connected to bit line. Word line is again connected to a pulse type voltage source. You can see the P to AP conventional connection switching model in Figure 17.

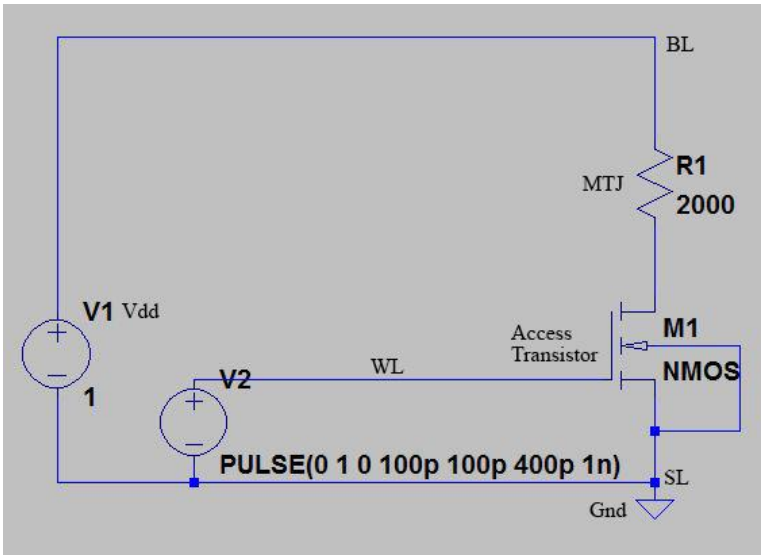

Figure 16. AP to P switching for conventional connection.

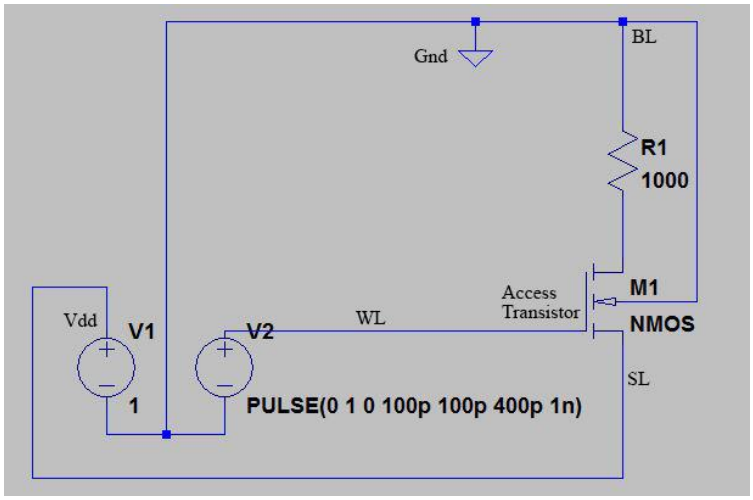

Figure 17. P to AP switching for conventional connection.

After I created models for conventional connection I created the models for reverse connection using same method. At this time V_{DD} is connected to source line and ground connected to bit line for AP to P switching. Word line is connected to a pulse type voltage source. AP to P switching resistance is 2kΩ. You can see the AP to P reverse connection switching model in Figure 18. For the P to AP switching V_{DD} is connected to bit line and ground connected to source line. Word line is again connected to a pulse type voltage source. P to AP

switching resistance is 1kΩ. You can see the P to AP conventional connection switching model in Figure 19.

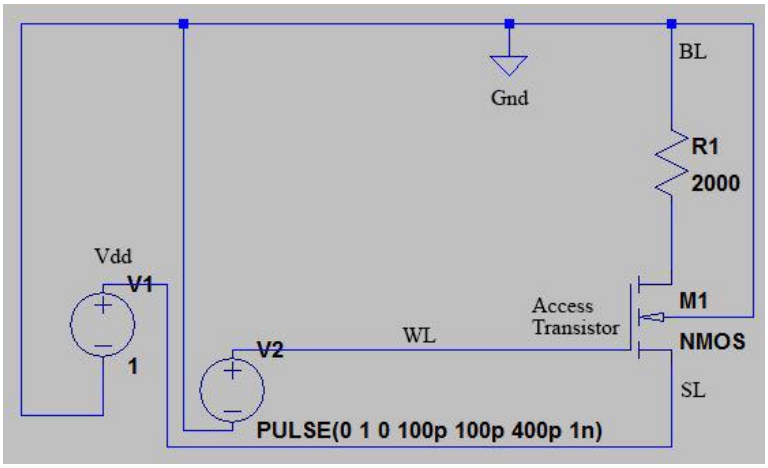

Figure 18. AP to P switching for reverse connection.

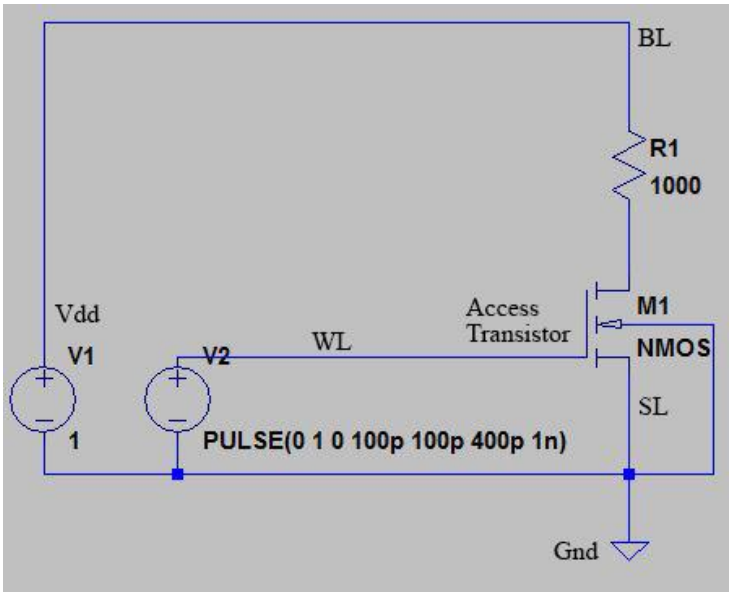

Figure 19. P to AP switching for reverse connection.

4.1.2 Simulation Results

For the simulations I gradually increased the transistor width and check the current on the resistor which stands as MTJ device. In this way I can see how much current access transistor can provide to MTJ.

First thing that I realized after simulations is that the reverse connection increases STT-RAM write operation. For the conventional connection source degeneration affects the P to AP switching. In this case MTJ is in low resistance state so the source degeneration is low. The purpose of using reverse connection is matching the source degeneration effect with AP to P switching which requires less current. As a result of having low resistance without source degeneration at P to AP switching, MTJ gets much higher current than conventional connection scheme. In the same way having high resistance with source degeneration at AP to P switching, causes having lower current than conventional connection scheme. You can clearly see the increased asymmetry in Figure 20.

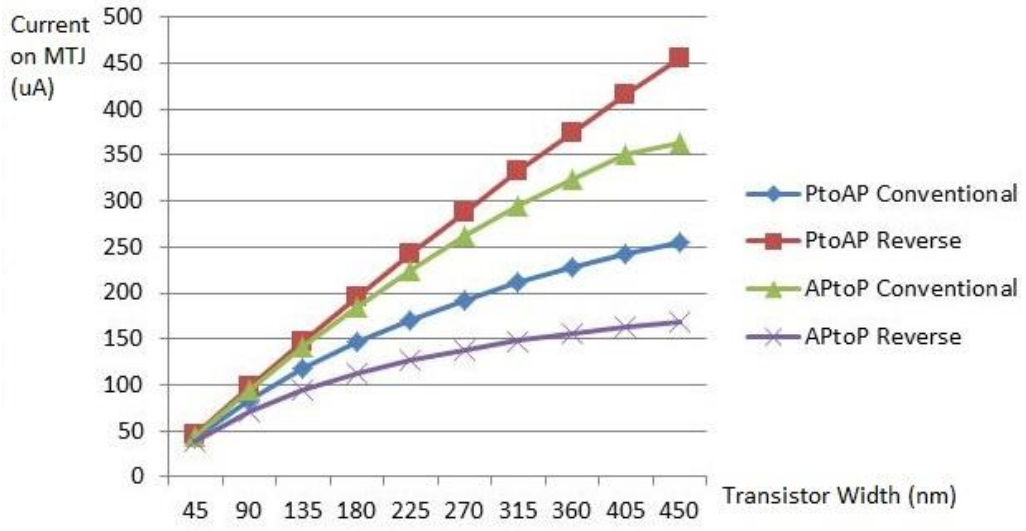

Figure 20. Switching current asymmetry change.

P to AP switching is bottle neck for the conventional connection because this switching scheme suffers from source degeneration. P to AP switching requires 201.8743uA current for 10ns switching time (Figure 21). We have to use 292nm transistor width in order to provide necessary current for 10ns switching time conventional connection.

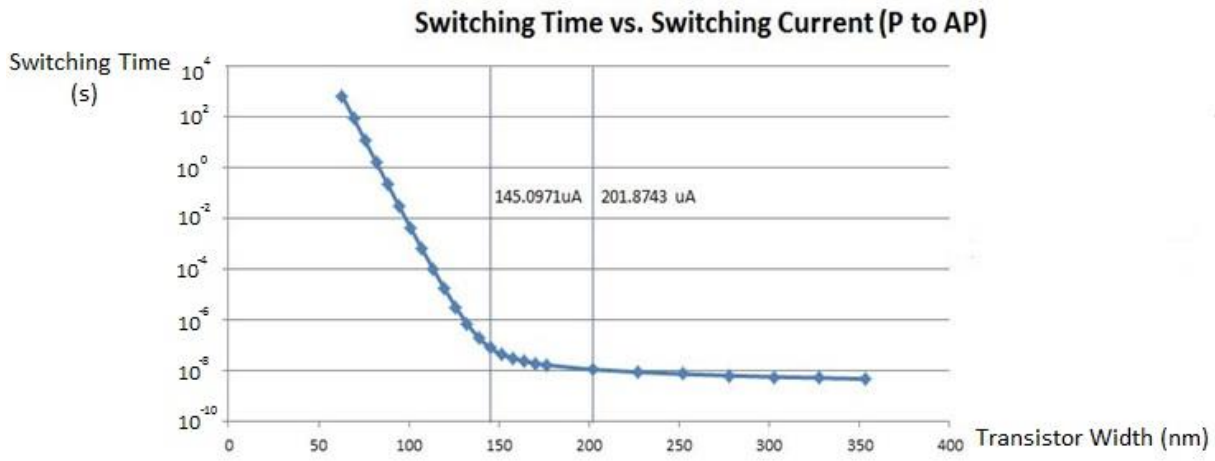

Figure 21. Switching time and switching current for P to AP switching.

For the reverse connection AP to P switching becomes the bottle neck since it matches with source degeneration. AP to P switching requires 108.8228uA for 100ns switching time (Figure 22). We have to use 335nm transistor width in order to provide necessary current for 10ns switching time.

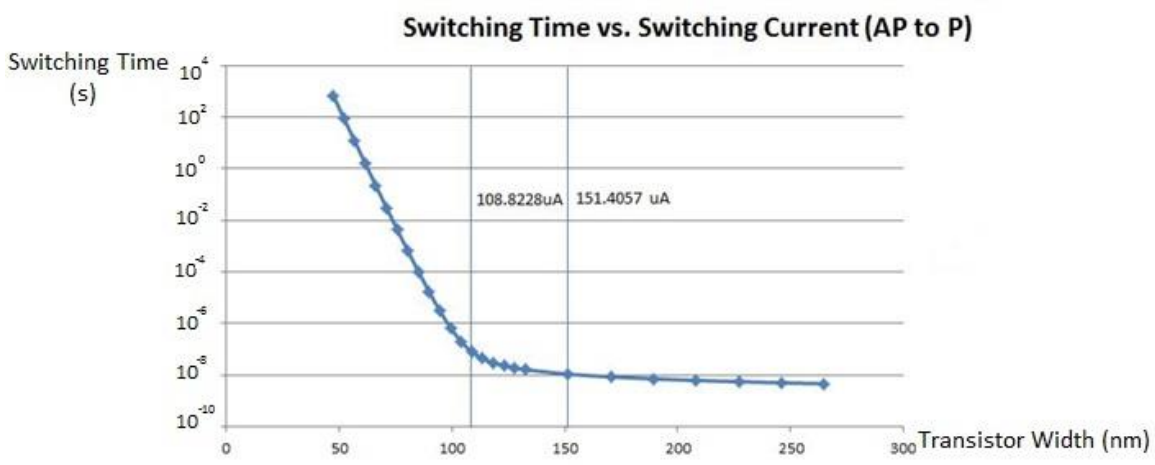

Figure 22. Switching time and switching current for AP to P switching.

When we compare the simulation results for reverse and conventional connection we can see that reverse connection requires larger transistor width. In this case the device has % 100 TMR and $\frac{P\ to\ AP}{AP\ to\ P} = 1.33$.

4.2 REVERSE CONNECTION COMPATIBLE DEVICE

4.2.1 Model Creation

The second device I inspected is convenient to use with reverse connection. For second devices simulation $V_{DD} = 1.1V$, low resistance is 2062.5Ω state and high resistance is 4331.25Ω [18]. Again I used PTM 45nm library for the transistor (channel length is 40nm) MTJ length is 40nm [18].

For the AP to P switching resistance is 4331.25Ω. At this time V_{DD} is connected to source line and ground connected to bit line. Word line is connected to a pulse type voltage source. You can see the AP to P reverse connection switching model in Figure 23. For the P to AP switching resistance is 2062.5Ω. V_{DD} is connected to bit line and ground connected to source line. Word line is again connected to a pulse type voltage source. You can see the P to AP reverse connection switching model in Figure 24.

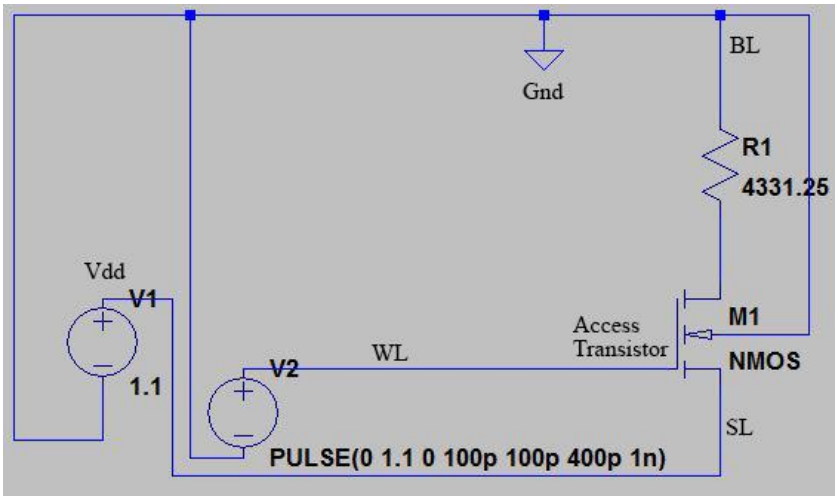

Figure 23. AP to P switching for reverse connection**.**

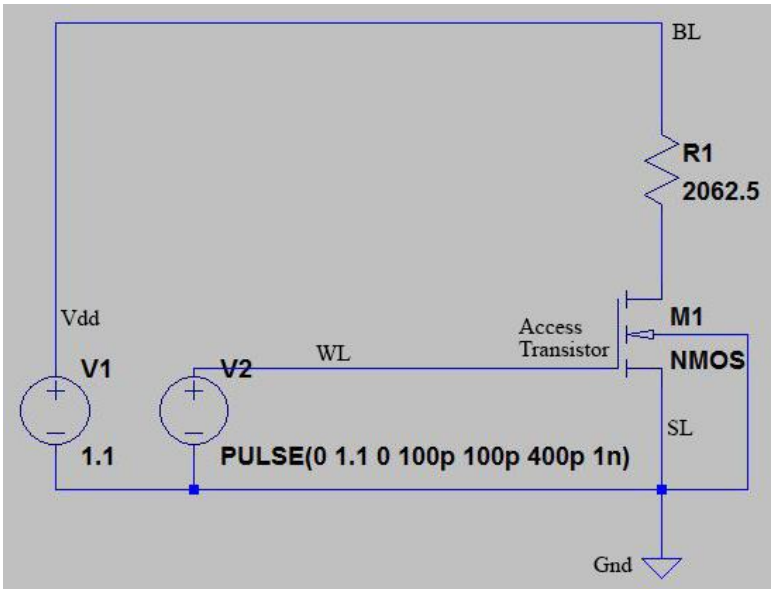

Figure 24. P to AP switching for reverse connection.

After creating models for reverse connection I created the models for conventional connection using same method. At this time V_{DD} is connected to source line and ground connected to bit line for AP to P switching. Word line is connected to a pulse type voltage source. AP to P switching resistance is 4331.25Ω. You can see the AP to P conventional connection switching model in Figure 25. For the P to AP switching V_{DD} is connected to bit line and ground connected to source line. Word line is again connected to a pulse type voltage source.

P to AP switching resistance is 2062.5Ω. You can see the P to AP conventional connection switching model in Figure 26.

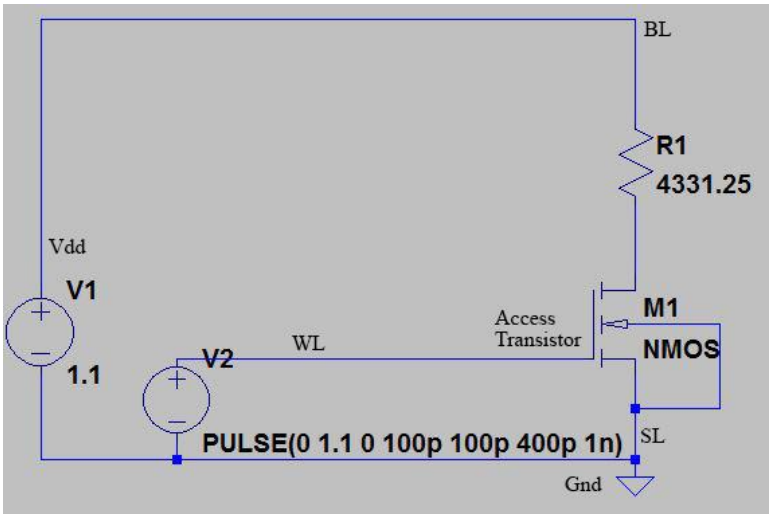

Figure 25. AP to P switching for conventional connection.

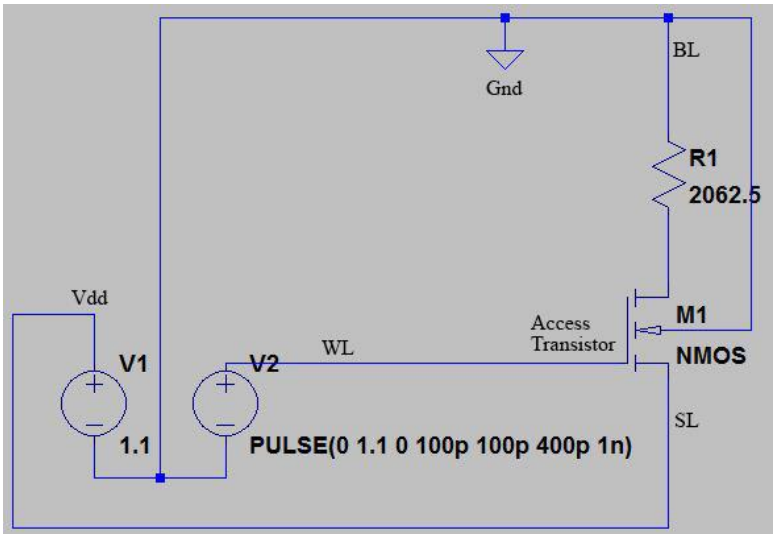

Figure 26. P to AP switching for conventional connection.

4.2.2 Simulation Results

I used the same method for the simulations as the first device. I changed the transistor width and check the current on the resistor in model circuit.

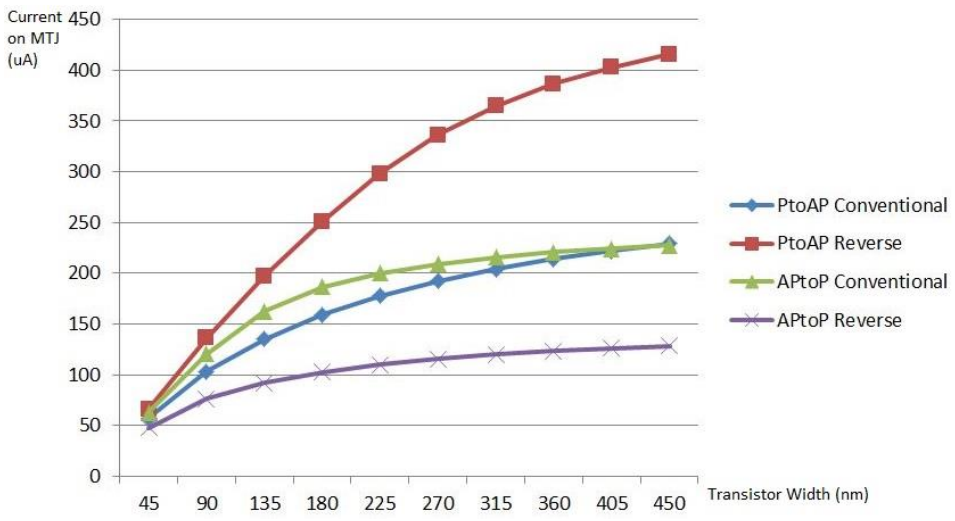

Figure 27. Switching current asymmetry change.

In Figure 27 we can see again that the reverse connection of the MTJ device increased the write operation asymmetry in STT-RAM cell.

P to AP switching is bottle neck for the conventional connection because this switching scheme suffers from source degeneration. P to AP switching requires 242.42uA current for 100ns switching time (Figure 28) [18]. When we use 270nm transistor MTJ device gets 192.065uA current. In this case 100ns switching time cannot be reached with conventional connection. 100ns switching time requires 555nm transistor width for conventional connection.

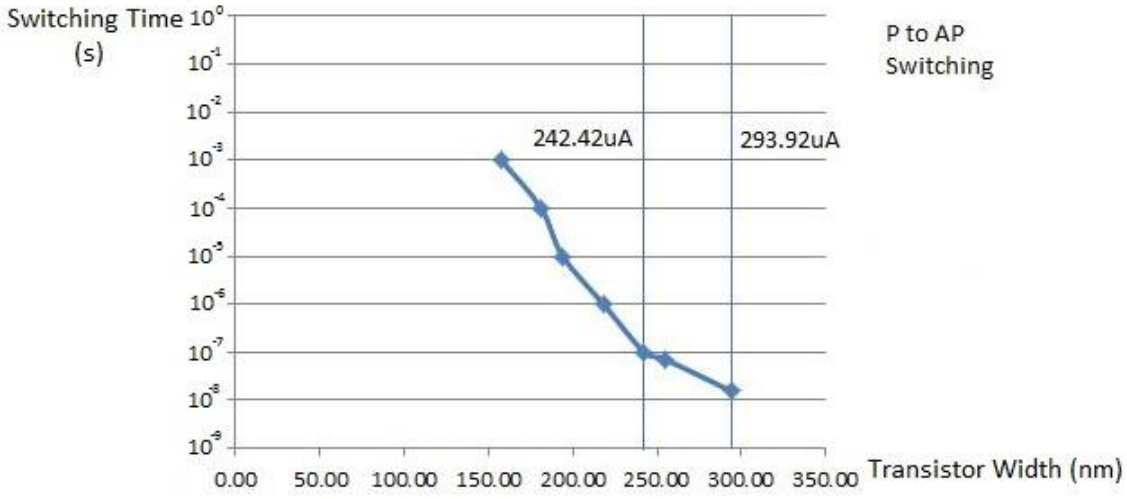

Figure 28. Switching time and switching current for P to AP switching

For the reverse connection AP to P switching becomes the bottle neck since it matches with source degeneration. AP to P switching requires 115.44uA for 100ns switching time (Figure 29). When we use 270nm transistor width MTJ device gets 155.688uA. As a result of supplied current 100ns switching time is possible in reverse connection.

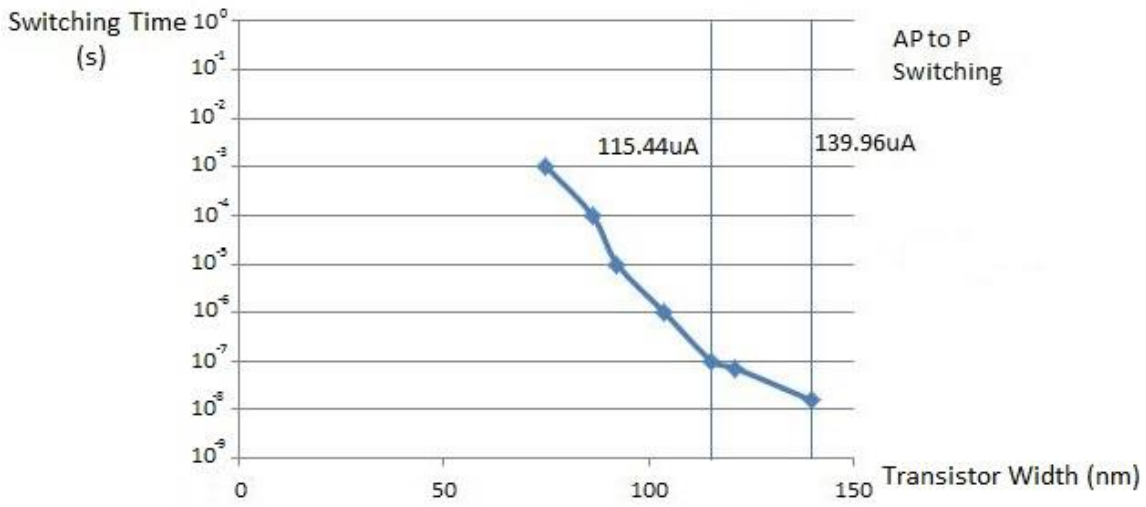

Figure 29. Switching time and switching current for AP to P switching.

In this case the device has %110 TMR and $\frac{P\ to\ AP}{AP\ to\ P} = 2.1$ [18]. For this device as we can understand from simulation results reverse connection scheme provides successful switching with smaller transistor width [18].

4.3 CONCLUSION

When I compared two devices I see that the main feature that determines which MTJ connection scheme is more convenient may be the ratio between P to AP and AP to P switching. I made simulations in order to find out what is the $\frac{P\ to\ AP}{AP\ to\ P}$ value when reverse and conventional connection schemes require same transistor width.

For the first MTJ device which is conventional connection compatible I reduced the AP to P critical switching current while keeping P to AP critical switching current constant. I calculated the $\frac{P\ to\ AP}{AP\ to\ P}$ value as 1.41 as you can see in the Figure 30.

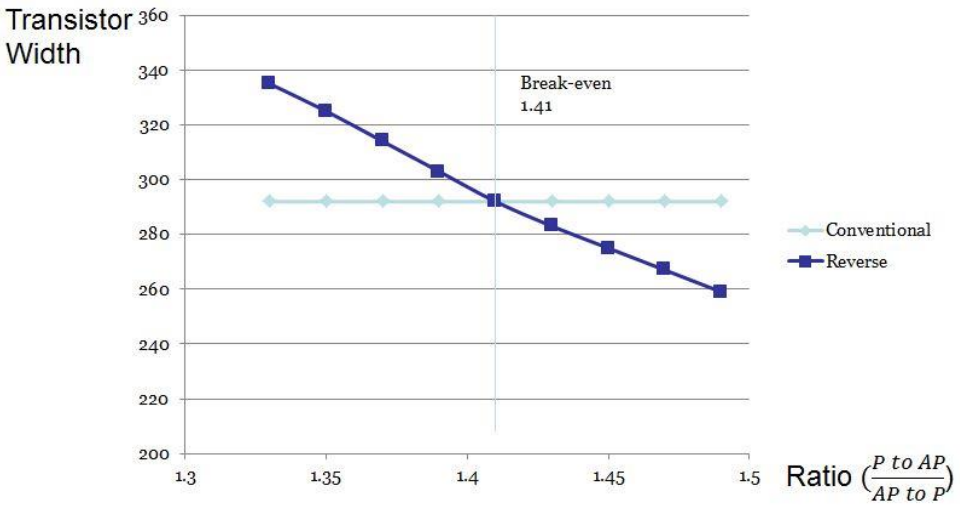

Figure 30. Transistor width vs. $\frac{P\ to\ AP}{AP\ to\ P}$

For the second MTJ device which is reverse connection compatible I reduced the P to AP critical switching current while keeping AP to P critical switching current constant. I calculated the $\frac{P\ to\ AP}{AP\ to\ P}$ value as 1.66 as you can see in the Figure 31.

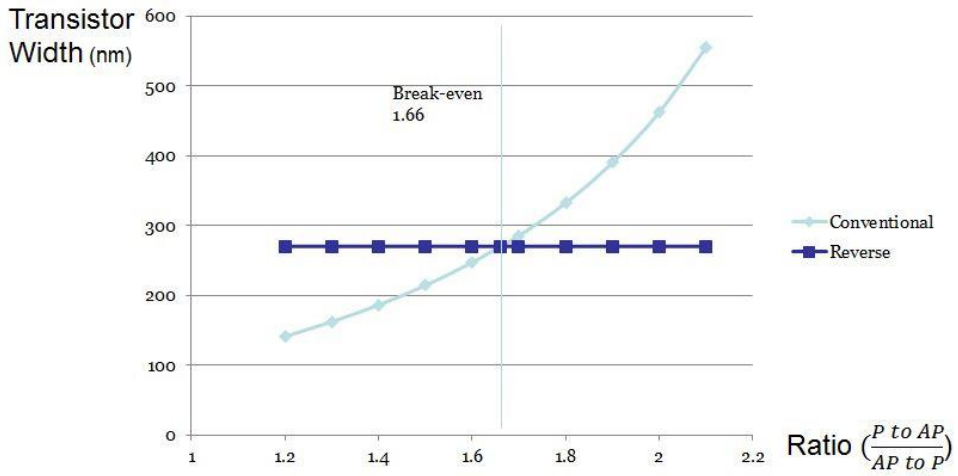

Figure 31. Transistor width vs. $\frac{P\ to\ AP}{AP\ to\ P}$.

5.0 CONCLUSION AND FUTURE WORK

In the beginning of this work the simulations were conducted to determine if transistor driving ability satisfied only P to AP switching (which requires higher current than AP to P switching). This approach was taken as many previous researchers had utilized the same method. As a result, when I checked the data regarding a reverse connection for the first MTJ device, I discovered that a transistor width of 900nm was required for proper switching. After this ridiculously large result, I realized I had to simulate both AP to P critical switching current and P to AP critical switching current. When the simulations were repeated again, this time considering AP to P critical switching current, I found that better and more reliable results could be achieved.

A reliable result of this research is that the reverse connected MTJ device increases the asymmetry of write operation of the STT-RAM cells as we can see in the Figure 20 and Figure 27.

For the first MTJ device, at least, as I understand from the simulation, results beyond a 1.41 $\frac{P\ to\ AP}{AP\ to\ P}$ ratio the reverse connection provides smaller transistor size. For the second MTJ device I calculate $\frac{P\ to\ AP}{AP\ to\ P}$ ratio as 1.66. Since I don't have the same ratio for both MTJ devices, I realize that there are some other properties also have effect. First I check the TMR. I reduce the TMR of the second device to 100%, which is the same TMR as first MTJ, causing the equilibrium point to reduce to 1.61. After that I check the resistance level. I reduce the resistances of the second MTJ device as the same level as those in the first MTJ device, causing the equilibrium point to

reduce to 1.22. As you can see from the ratios, both TMR and resistance level effect the transistor size for different MTJ connection schemes.

I have different but similar ratios for different scenarios. $\frac{P\ to\ AP}{AP\ to\ P}$ is 1.41 for the first MTJ and 1.66 for the second MTJ. Moreover, altering TMR and resistance changed the ratio, but the new ratios are not so dissimilar from the original ratios. Thus, I can say the break-even $\frac{P\ to\ AP}{AP\ to\ P}$ for the access transistor size of reverse and conventional connected MTJ is around 1.5.

5.1 FUTURE WORK

In my future work I will create a dynamic MTJ model and make more precise simulations with differing transistor technologies, MTJ dynamics, TMR, and resistances to determine a more reliable relationship between the reverse connection usage and $\frac{P\ to\ AP}{AP\ to\ P}$ ratios. In this way an optimization method can be found for MTJ devices to make them more convenient to use with either conventional or reverse connections. This would enable us to create devices like the sample design below (Figure 32), which can be useful in increasing the reliability of STT-RAM.

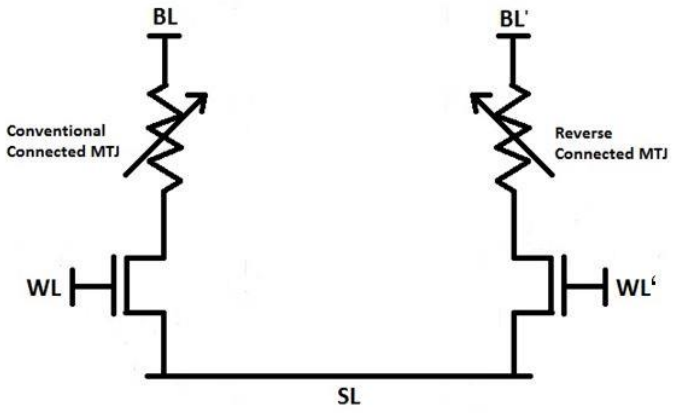

Figure 32. Sample STT-RAM cell design.

In this design I have two STT-RAM cells: one of them has a reverse connected MTJ device and the other has a conventionally connected MTJ device. Both cells share the same source line, but have different word and bit lines. As for first alternative usage, we can use this device for storing single bit. When we write ‘1’ to the conventionally connected MTJ, we can write ‘0’ to the reverse connected cell at the same time by setting the WL and WL’ lines to the same value. We can use the BL’ line for increasing the sensing ability. Moreover, when we apply read current from bit lines to the source line it is not possible to switch the MTJs value mistakenly if the conventionally connected cell’s value is ‘0’ and reverse connected cell’s value is ‘1’. Thus, we can reduce the read disturbance possibility in one direction. As for second alternative usage, we can program the MTJ cells separately to store two bits since we have two separate word lines. With this kind of usage we can reduce the read disturbance detection into one condition. As you can see in Figure 33 below we can read 4 possible combinations from BL and BL’. We may only have read disturbance when BL=0 and BL’=1.

Conventional	Reverse		BL	BL’
0	1	Disturbance is not possible for both MTJs →	0	1
1	0	Disturbance possible for both MTJs →	0	1
1	1	Disturbance possible for conventional MTJ →	0	1
0	0	Disturbance possible for reverse MTJ →	0	1

Figure 33. Read disturbance possibilities.

The observations above have not been verified by simulations yet. Thus, this work is stated as a future work.

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