Formation and Characterization of Columnar Porous SiC Fabricated by Photo-electrochemical Etching

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This thesis concentrates on the physical aspects of the columnar pore formation in the Si-face (0001), C-face $(000\bar{1})$, and a-face $(11\bar{2}0)$ n-type 4H and 6H SiC using photoelectrochemical etching. The electrochemical etching of p-type 4H and 6H crystals is also illustrated.

In Si-face n-type 4H and 6H SiC, the columnar pores are about one μm in diameter. The formed porous layer is of high porosity and thus fragile. The formation of a hybrid partial columnar porous structure to improve the mechanical strength for possible biomedical applications is discussed in detail.

Nano-columnar pores are successfully fabricated in C-face n-type 4H and 6H SiC. The self-organized columnar pores have diameters of about 20±5 nm. The average interpore spacing from center to center is between 40-60 nm. The porous layer can be as thick as 200 μm. Systematic studies on the experimental control parameters, such as voltage, temperature, surface roughness, HF concentration, and doping concentration, have been performed and explained in detail. The charge transfer mechanisms are discussed extensively. The mechanisms that determine the observed pore diameter, interpore spacing, and columnar pore shape have been explored. The pore pattern formation simulation using a diffusion limited aggregation model and an impedance analysis using an equivalent circuit are discussed.

The 20 nm diameter nano-columnar pore formation has also been observed on the a-face n-type 6H SiC. The experimental observations are recorded and the voltage effects on the formed

porous structure are discussed. The mechanism of the possible columnar pores formation in a-face SiC is discussed.

In the electrochemical etching of p-type 4H and 6H SiC, the electrochemical polishing, porosity dependence on the current density, porosity variation during the etching and doping effects on the porous formation are discussed. This work also contains useful information about how to electro-polish SiC and how to obtain low porosity p-type porous SiC.

The five appendices contain detailed information about: (1) my publication list, (2) the fabrication of porous SiC, (3) the fabrication of porous Al_2O_3, (4) operation/maintenance of the mechanical polishing of SiC, and (5) operation/maintenance of the Varian 936-60 Leak Detector and the E-beam Evaporator.

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PREFACE

Conventional electrochemistry is usually not considered related to physics. The later discovery and development of porous semiconductor formation (starting in the 50's) greatly changed this view. More and more physics methods are required in the research, so that semiconductor electrochemistry becomes a highly multidisciplinary field. Just as adding more water droplets to the sea, the work in this thesis is devoted to obtain improved physics understanding about a complicated process of the semiconductor electrochemistry: porous SiC formation.

I would like to express my deepest gratitude to my mentor, Professor W.J. Choyke, for his guidance which helped me becoming an experimental solid state physicist. I am obliged to Professor R.P. Devaty for the fruitful discussions and his enormous efforts to improve this dissertation. I sincerely appreciate Professor R.M. Feenstra, Professor Y.Y. Goldshmidt, and Professor J. Levy for serving on my committee.

I thank my friends and colleagues for help and companionship. Special thanks go to Y. Shishkin, S. Bai, and F. Yan. I really appreciate C. Weisdack's help from the physics stockroom and his friendship. I am indebted to the machinist fellows, B. Giles, K. Petrocelly, and K. Kotek, for their craftsmanship and friendship. I also thank G. Zuk from the electronics shop for his great help on repairing various important laboratory instruments.

Finally, I especially thank my family in China who have always trusted and supported me. I'm glad that I make you proud.

"There are two possible outcomes: If the result confirms the hypothesis, then you've made a measurement. If the result is contrary to the hypothesis, then you've made a discovery."

Enrico Fermi

1.0 INTRODUCTION

1.1 MOTIVATIONS

Silicon Carbide (SiC) is a wide bandgap semiconductor with many superior mechanical and electrical properties compared to silicon. The high thermal conductivity (5 $W/(cm \cdot K)$ at room temperature), high melting point (2830 ^{o}C), breakdown field of 3×10^{6} V/*cm*, and the range of possible wide bandgaps in SiC polytypes are desirable for switches in electric power distribution systems, high temperature turbine engines, high frequency power devices, high temperature ambient detectors as well as detectors for various harsh environments[1,2]. Despite the demands for SiC devices, the production technology for high quality SiC material, however, only became successful after 1990. At present, wafers of up to four inch diameter are commercially available[3] with micropipe (micron size vacancy defects formed in the SiC crystal growth) density of less than 5 cm^{-2}. The currently available high quality SiC material finally makes possible a variety of SiC for a broad range of research and device fabrication.

As a result of the availability of very good semiconductor grade SiC, in 2001, The "Defense University Research Initiative on Nanotechnology" (DURINT) program[4] was launched with the motivation to fabricate and study nano porous SiC (PSC) and GaN templates and explore their application for SiC and GaN epitaxy, catalysis, and biotechnology. The goals were:

(1) Reduce the density of screw dislocations in epitaxial SiC layers and point defects and line defects in GaN epitaxial layers by using PSC substrate. (2) Exploit the increased surface area provided by PSC and its application in nano-surface catalysis. (3) Exploit the PSC in semi-permeable membranes for implant microdialysis, biosensor, and tissue growth. (4) Exploit SiC porous templates and Mn doped GaN clusters for high-density robust storage applications[4].

This six year multimillion dollar program involved more than 15 researchers from different institutes. As part of the collaboration, our group was responsible for the fabrication of porous samples and related studies on the pore formation mechanism. Our porous templates and related research turned out to be the indispensable basis for the program and achieved fruitful research results.

The porous templates are fabricated in our laboratory using photo electrochemical etching (PECE). Nano structured SiC or nano SiC surface features might also be obtained by lithography[5] and other techniques[6,7,8]. We chose the PECE method because it is a parallel process (pores form simultaneously across the whole sample surface) and requires relatively simple instrumentation. We believe these advantages make PECE a promising technique for large area nano structures at a relatively low cost.

1.2 THE HISTORY OF POROUS SILICON CARBIDE RESEARCH

The field of semiconductor electrochemistry emerged in the fifties[9,10]. The charge transfer processes at the SiC electrodes was studied in the seventies[11]. Two decades later, in the nineties, studies of electrochemical etching of SiC were initiated[12,13]. Shor *et al.* demonstrated PSC

formation by anodizing single crystal n-type and p-type 6H SiC samples in hydrofluoric acid under UV illumination[14,15,16]. About the same time, the electrochemistry at the anodic SiC electrode was discussed by I. Lauermann *et al.*[17],[18] and Shor *et al.*[19]. Konstantinov et al. studied the electrical properties and the formation process of porous n-type SiC produced by photo assisted etching as well as in the dark-current mode, and proposed a model suggesting a self–regulation of the fiber size[20]. In 2000, Zangooie *et al* followed up with studies on different pore morphologies and possible formation mechanisms[21,22,23,24,25].

Since the DURINT program started, Y. Shishkin *et al.* have performed a more systematic study of the production of various porous morphologies in PSC. Many new porous morphologies were discovered[26]. Shishkin paid special attention to the mechanism of triangular morphology pore formation in n-type SiC[27] and filamentary pore morphology formation in p-type SiC[28] . In addition, low voltage etchings on the different crystalline surfaces were extensively studied.

However, many of the reproducible morphologies of PSC templates which were discovered by 2004 did not serve the needs of the DURINT program very well. Partially at the request of our collaborators, and partially stimulated by the work of electrochemical etching on other semiconductors (which will be discussed later), we started the work on nano-columnar PSC to obtain a practical columnar PSC with pore diameter between 10 nm to 1000 nm.

1.3 ELECTROCHEMISTRY BACKGROUND

1.3.1 An Oversimplified Overview of the PECE Process

Electrochemical reactions that take place in the PSC formation are of the form[17]:

$$\begin{aligned} SiC + 2H_2O + 4h^+ &= SiO + CO\uparrow + 4H^+ \\ SiC + 4H_2O + 8h^+ &= SiO_2 + CO_2\uparrow + 8H^+ \end{aligned} \qquad \textbf{1.1}$$

Holes are needed for the dissolution of the SiC lattice. The products SiO and SiO_2 will be dissolved in the solution by HF. The gas phase reaction products will be released as bubbles.

The electrochemical etching is performed in chemical cells shown in Figure 1.1. The SiC electrode is always anodically biased for both n-type and p-type SiC. UV illumination is applied if n-type SiC is etched. The three electrode configuration has an accurate control of voltage across the SiC/HF interface and therefore is very commonly used in regular electrochemical processes. The working voltage range for commercially available systems is ±10V. It is found, however, that all the nano columnar porous fabrication requires a voltage higher than 10 V. Therefore, a two electrode system is used in this work. As a matter of fact, when the applied voltage is high and the resistivity of electrolyte is low, the difference between the two and the three electrode configuration is negligible.

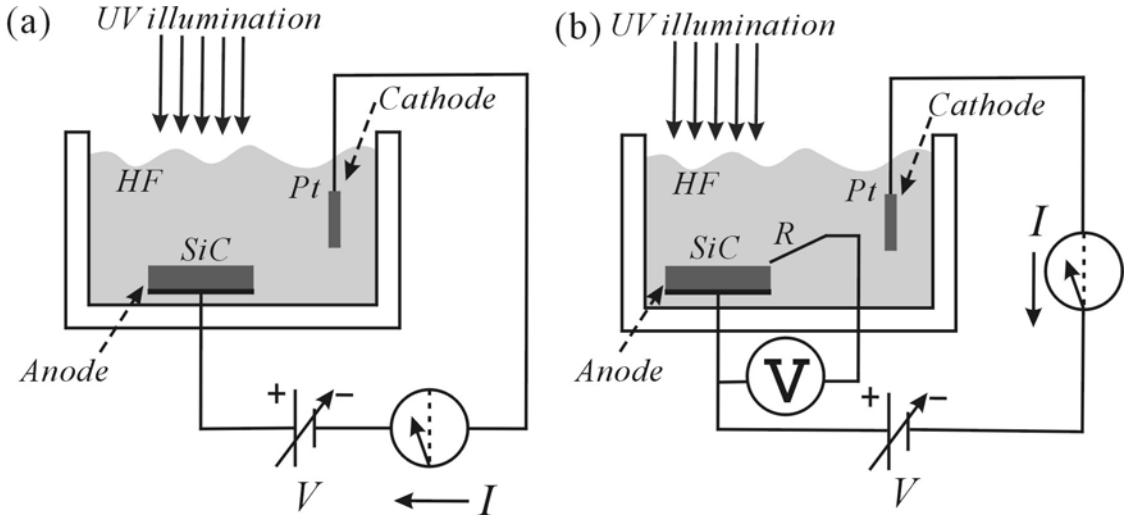

Figure 1.1 A simplified sketch of an electrochemical experiment setup. (a) A two electrode configuration. (b) A three electrode configuration, in which "R" stands for reference electrode. In both configurations, the SiC crystal is under anodic bias. A platinum plate serves as a cathode.

The details of the electrochemistry of semiconductors are actually very complex and at times a great puzzle for condensed matter physicists. The complexity is mainly what occurs in the solution and at the solution/semiconductor interface. Although books on the subject exist[29,30,31], a quantitative analysis is a great challenge, even for the simplest systems. The more detailed electrochemistry will be discussed in the section 3.8 where we try to explain some experimental observations and columnar pore formation mechanisms.

1.3.2 The Experimental Parameters

The greatest difficulty in the study of semiconductor electrochemistry is the complicated and sensitive control of the experiments. The experimental control parameters are all coupled in a

non-transparent fashion, which makes the systematic study of the pore formation mechanism very difficult.

In this work, based on the experience from a great many trial experiments, not included here, we were able to narrow down the important parameters. The effects of varying these experimental conditions are listed below and are the crux of this study.

The Solution: We only use an aqueous HF solution containing 5% ethanol* (weight percentage). The only variable which changes in the solution is the *concentration of the HF*.

The SiC Work Pieces: 4H or 6H SiC with different *doping*. For nano-columnar pore formation, we only use n-type material. The three studied *crystalline surfaces* (Si-face (0001), C-face $(000\bar{1})$, a-face $(11\bar{2}0)$) are shown in Figure 1.2. The effect of the *surface conditions* (scratches, smoothness, and flatness) will be discussed.

Electrochemical Reaction Control: The *voltage* is applied/measured on the cell and the drawn current is measured both by a Potentiostat/Galvanostat. *Temperature* is controlled by a thermo bath system and monitored using a Teflon coated Thermocouple. The UV illumination sources are a 1000 W or 350 W HgXe Arc Lamp using a 350-450 nm band pass filter. The *UV intensity* is adjusted to be either 0 or 600 mW/cm^2. These etching conditions are maintained for various certain *periods of time* to allow different thickness of pore formation.

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* The ethanol used here is to reduce the possible surface tension between the different material phases (solid/electrolyte, electrolyte/gas, and solid/gas). It helps the electrolyte to migrate inside the porous layer so that the porous structure can continuously form. Since there are CO and CO_2 as reaction products from the etching process, the ethanol will also ease the release of the gas bubbles to avoid trapping gas inside the pores.

1.3.3 Anisotropic Etching in Semiconductors

Self organized columnar porous structures have previously been fabricated electrochemically in Si[32,33,34,35,36], Al_2O_3[37,38], and InP[39, 40]. The typical minimum pore diameter is 300 nm in Si, 50 nm in Al_2O_3 and 200 nm in InP. During the etching of semiconductors, anisotropy electrochemical etching almost always occurs in these materials. For more examples, see Si[33,41], GaAs[42,43] and GaN[44]. Moreover, studies on more ionic polar semiconductors, such as ZnO[45] and InP[39,40], show that the etching rate is very different on the two surfaces perpendicular to the polar axis. This is also observed for SiC etching.

All these experimental findings suggest that choosing a specific crystal surface as the initial etching surface greatly influences the pore morphology, especially under high electric fields. In Figure 1.2, we show a picture of a hexagonal pyramid of 4H or 6H SiC, which are the only two polytypes in which we consider nano columnar pore formation. Four common surfaces are used for various studies: the Si-face, the C-face, the a-face, and the p-face (sometimes called the m-face). Our etching experiments on the Si-face, C-face, and a-face will be discussed in this dissertation.

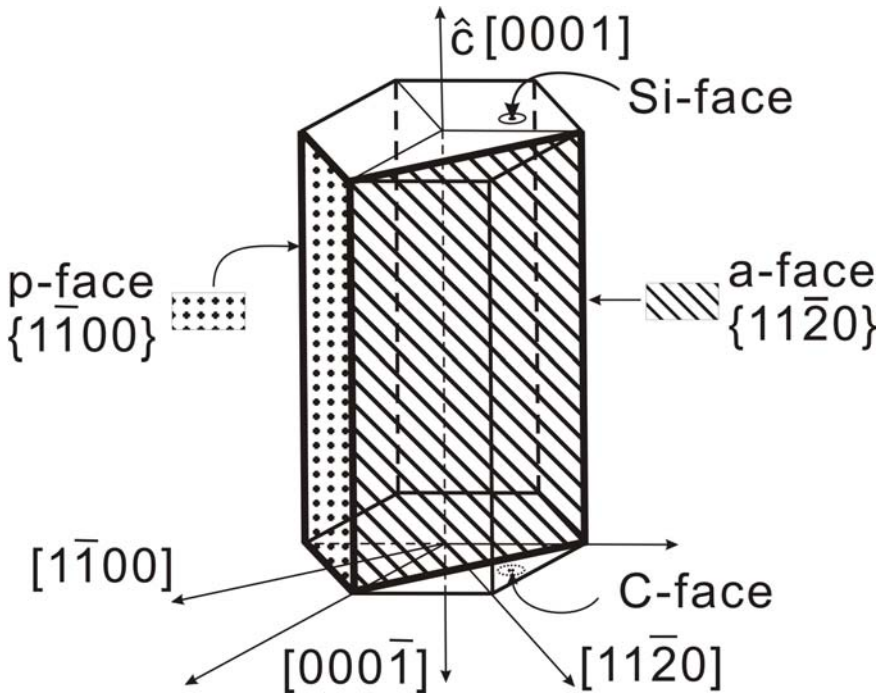

Figure 1.2 The hexagonal pyramid appropriate for the description of hexagonal polytypes of SiC. A p-face (m-face) belongs to the family of $\{1\bar{1}00\}$ planes whereas an a-face belongs to the family of $\{11\bar{2}0\}$ planes.

1.4 SYNOPSIS

Although the principle of the experiments seems to be straight forward, the actual control and choices of experiment control is very complicated. We estimated that there are total 15 possible choices of etching conditions. Combinations of these conditions can give one an ultimate freedom on doing the experiments and finding new porous morphologies. This indeed makes a systematic approach very difficult in these exploratory experiments. Table 1.1 shows the matrix of the experiment parameters we can choose from.

Experiment Parameters	Number of Freedom
Electrochemical cell configuration: 2 & 3 electrodes system	2
Electrolytic solution: ingredients & concentrations	2
SiC crystal properties: doping type, doping level, polytype, surface finish, & crystal surface exposed to etching environment	5
Etching voltage/current: DC & AC, amplitude	3
UV illumination: wavelength & intensity	2
Duration of etch	1
Temperature	1
Total number of experiment control parameters	***15***

Table 1.1 The complete matrix of experimental control parameters.

Our work showed that eight parameters will influence the columnar pore formation in different ways. They are listed in Table 1.2. Among these eight parameters, the crystal orientation is found to be the most important factor. The chapters are therefore arranged in the order in which the experiments on the Si-face (Chapter 2), C-face (Chapter 3), and a-face (Chapter 4) were done. The most extensive part is the discussion of the C-face columnar pore formation in Chapter 3. Chapter 5 is a supplementary part in which we record and explain many interesting experimental findings in the etching of p-type material.

Parameter	Discussed in this thesis
Crystal orientation	***Si-face, C-face, a-face***
Etching voltage	10-100V
HF concentration	1%-30%
SiC Doping	1×10^{17}-2.4×10^{18} cm^{-3}
SiC Polytype	4H and 6H
Surface roughness:	CMP and MP surfaces
Temperature	10-30 ^{o}C
UV illumination intensity	0-600 mW/cm^2

Table 1.2 Eight important experiment parameters in the columnar porous SiC study.

In Chapter 2, a special columnar porous structure, which we term the partial columnar structure, is discussed[46]. The columnar pore formation in Si-face SiC can produce one μm diameter pores resulting in a very high porosity (>0.9). The mechanical strength associated with this morphology is then very weak. The porous structure can be easily crushed by a Q-tip wipe. It is also found that the porous structure is not strong enough to hold as a self-supporting structure. Therefore, this kind of morphology is of no practical interest.

A hybrid porous morphology was later developed which allows for the coexistence of 200-500 nm diameter columnar pores and 20-30 nm dendritic pores. The lowered porosity (~0.3) gives a satisfactory mechanical strength for the applications such as biomedical protein dialysis. It is found that constant current condition should be applied for of the partial columnar porous structure formation. The surface pore diameter is proportional to the magnitude of the current density applied. The columnar pores show a diameter expansion during the growth. The ultimate pore diameter is stabilized at about 1-1.5 micron.

Chapter 3 is devoted to a discussion of nano columnar pore formation on C-face SiC. The most important result is the discovery of the self-ordered 20 nm diameter columnar PSC structures, which will be introduced in section 3.2. The columnar pore length can be as long as 200 μm[47]. This straight, parallel columnar mesoporous SiC is a promising material for many applications, such as biomedical membranes[48] and substrates for homo- and heteroepitaxial growth[49,50]. Defect reduction has been observed in GaN epitaxially grown on columnar PSC as a substrate. Other studies are also in progress to apply nanocolumnar PSC to be used for electroosmotic pumps, nanopattern templates, etc.

To investigate the pore formation mechanism and obtain columnar pores with different diameter, a serial of systematic studies on voltage, surface condition, UV illumination, temperature, HF concentration, and material doping effects in the etching of n-type 4H and 6H SiC have been performed. We will discuss the influence on the pore growth by varying these experiment control parameters one at a time in section 3.2-3.7. As a general result, we found that no matter how we vary the etching conditions, if the nano-columnar porous structure forms, the self-organized pores always have diameters of about 20 nm. The interpore spacing from center to center is 40-60 nm depending on the etching conditions. The detailed experiment results will be summarized in section 3.8.

Based on these experimental observations, the possible pore formation mechanisms are discussed. In section 3.9, we will first present the basic semiconductor electrochemistry (double layer model with a flat interface) as the footstone for the model. The impedance measurement results are then shown in section 3.10 to prove the validity of the basic double layer model in our SiC electrochemical system. The section 3.11 is then dedicated to explore the double layer system in the actual columnar pores and study the charge transfer process during the pore

formation. To explain the logic of the model better, we list the subsections as the flow chart in Figure 1.3. Last not least, the simulation work of pore pattern formation using a diffusion limited aggregation model will be presented in section 3.12. Finally, section 3.13 will conclude all the experiments and models.

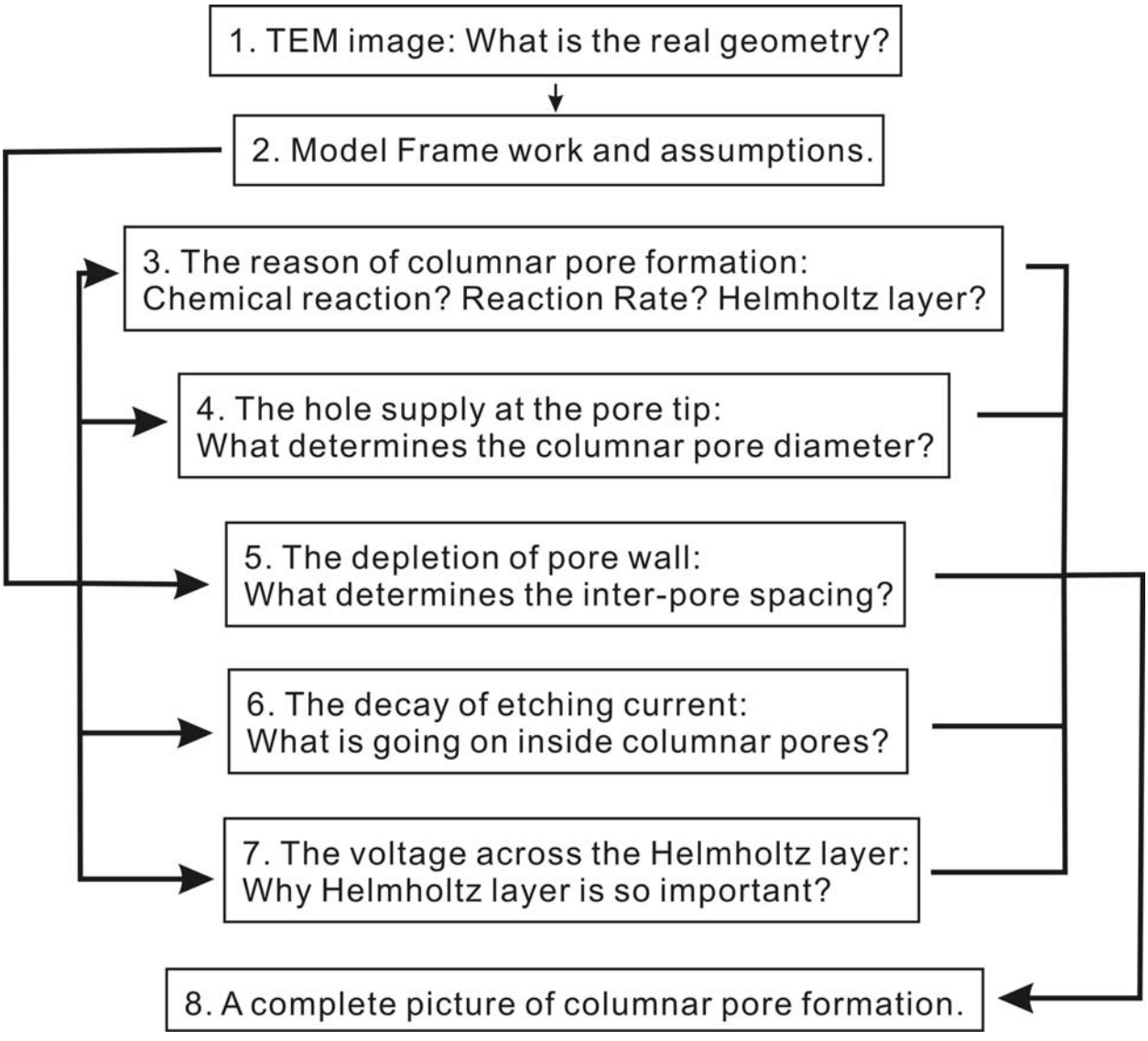

Figure 1.3 Flow chart of the charge transfer model discussion in section 3.11**.**

Chapter 4 discusses the columnar pore formation on the n-type a-face of 6H SiC samples. A 20 nm diameter columnar pore formation is again observed. The porous structure is not as uniform on the in C-face SiC. The work on the a-face SiC again proves that the columnar pore formation is depending on the oxidation rate of specific SiC lattice face.

Based on the studies of the three face etchings, we conclude that C-face is the best choice for obtaining columnar pore formation. The systematic study on C-face SiC shows that the nano-columnar pore formation is a very "stable" process, which means that the diameter of the pores and interspacing of the pore lattice can not be varied by applying a different etching condition. The model analysis shows that the pore diameter is determined by the electric breakdown process at the pore tip. About 3 V voltage is actually dropped across the space charge region at the pore tips. Large fraction of the total applied voltage is essentially across the Helmholtz layer at the interface. To maintain the necessary current, an appreciable voltage is distributed in the electrolyte inside columnar pores. The columnar pore formation is only possible due to the fast oxidation reaction rate and the favored spontaneous Helmholtz layer field of C-face SiC. These understandings greatly improved our knowledge of the porous SiC formation.

In Chapter 5, in addition to our earlier work on p-type SiC[51], additional experimental results are collected. In this chapter, electrochemical polishing is also discussed. A systematic current density study on highly doped p-type material reveals that one can obtain a much lower porosity porous p-type SiC with a reasonable etching rate. It is also observed that there is a porosity gradient inside the porous structure. The summarized experimental results qualitatively show the doping effects on the porous formation in p-type SiC.

1.5 TERMINOLOGY AND NOTATION

The Following terminology and notation will be used in this dissertation:

- *Pore* is the void or cavity inside the crystal. On the SEM images, the darker contrast represents the pore area.
- *Interpore spacing* is the distance between the centers of two columnar pores.
- *Porosity* is the volume fraction of the void to the whole porous structure.
- The directions along which the pores propagate are termed "*preferential directions*".
- *PSC*- Porous SiC.
- *HF*- Hydrofluoric acid.
- *PECE*- Photo Electrochemical Etching.
- *PEC*- Photo Electrochemical.
- *TEM*- Transmission Electron Microscopy.
- *HRTEM*- High Resolution Transmission Electron Microscopy.
- *SEM*- Scanning Electron Microscopy.
- *MP*- Mechanical Polishing/Polished.
- *CMP*- Chemical Mechanical Polishing/Polished.
- *FFT*- Fast Fourier Transform.
- *NHE*- Normal Hydrogen Electrode.

- *Error Bar issues*: The electrochemical process is very complicated and may even be unstable. An effort to give precise measurements is challenging. The chemical process is delicate. It depends on minor sample doping differences, defects from sample to sample, and minor differences in surface conditions. Instrumentation is not the only source here to cause an error in measurements. In some experiments, we have tried to give an estimate of errors by repeating the experiments numerous times. This statistical approach method is seriously limited by time required for each experiment and our sample resources. It is for these reasons that error bars had to be omitted in many of our experimental measuring results. Based on our broad experimental experience, we believe the experimental error is of the order of 5% (see Appendix B.7 for more information).

2.0 COLUMNAR PORE FORMATION IN SILICON-FACE N-TYPE 4H AND 6H SILICON CARBIDE

2.1 INTRODUCTION

Si-face polished and prepared SiC is the most commonly used in SiC research and industry (and therefore commercially available). To cut or polish other SiC faces involves enormous efforts and therefore is very costly due to the extraordinary hardness of SiC. For this reason, much effort was first devoted to either discovering or re-discovering many possible pore morphologies by following a systematic approach. Along with the discovery of these interesting pore morphologies, many potential applications were identified such as protein dialysis as well as SiC and GaN epitaxial growth on PSC. Since a simpler columnar pore geometry is easier to model and more attractive for practical applications, developing columnar porous SiC became the focus of our research.

We found that columnar porous structures can be fabricated in n-type Si-face 6H SiC under high electric field conditions. However, these Si-face columnar pore structures possess high porosity (>90%) and therefore are not physically strong enough to form self-supporting films. To find a solution to this problem, we developed a hybrid morphology PSC, which we term partial columnar PSC, by controlling the voltage or current in the electrochemical reaction. This hybrid morphology structure consists of dendritic PSC penetrated by large tubes (200-500

nm diameters). The reduced porosity obtained in this way allows us to fabricate a free-standing film having the advantage of columnar pores, such as the simple geometry and the uniformity. As a result of this research, we conclude that the constant current mode etching will give much straighter and more uniformly distributed columnar structure than the constant voltage mode. The columnar pore density is determined by both the doping of the SiC material and the current density. The maximum surface pore diameter of the columnar structure shows a linear dependence on the current density.

This chapter presents the results of our work presented at the 6th International Conference on Silicon Carbide and Related Materials in Pittsburgh, PA, USA, October 2005[46].

2.2 EXPERIMENTAL NOTES

The samples used to obtain columnar porous structure are 6H basal plane n-type SiC single crystal wafers with nitrogen doping of 5×10^{17} cm^{-3} to 3×10^{18} cm^{-3}. The PECE is performed on the (0001) Si-face in aqueous electrolytic solutions containing 5% HF and 5% ethanol (both measured by weight) with reverse bias voltage applied across the electrodes. A 1000 W Mercury Xenon lamp is used to produce UV light, which illuminates the front surface of the sample during the experiment. With optical filters, the wavelength interval at the sample surface is 350 to 450 nm. The UV power density is about 600 mW/cm^2, as measured by a thermopile power meter. A two-electrode photoelectrochemical cell is used, in which the SiC sample is connected as the anode and a platinum plate as the cathode. The voltage or current is controlled with a PAR 2273 potentiostat/galvanostat or a Xantrex 300-4 power supply. After the electrochemical

etching, the samples are carefully retrieved from the etching bath and cleaned in acetone and propanol. A Philips XL30 FEG electron microscope is then used to obtain plan and cross sectional SEM images for examination of the porous structure.

2.3 RESULTS AND DISCUSSION

2.3.1 The columnar porous structure

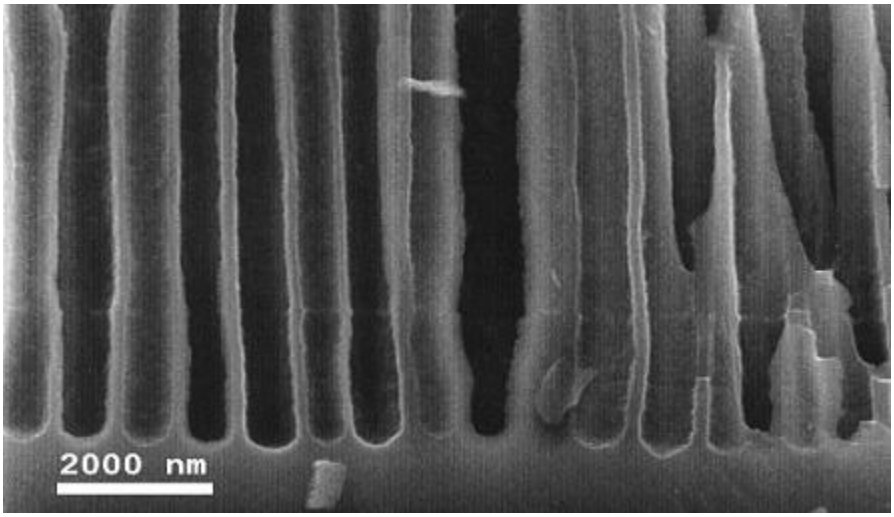

Figure 2.1 Columnar porous structure made in 5% HF and 5% ethanol aqueous electrolytic solution by applying 80 V to 6H SiC, doped n~5.7×10^{17} cm^{-3}.

Figure 2.1 shows a SEM image of a typical macro columnar structure. This structure can be obtained by applying 80 volts to a n-type Si-face 6H SiC sample (n~3×10^{18} cm^{-3}) during the UV photo-assisted electrochemical etching. The breakdown type etching condition yields a high current density normally greater than 1 A/cm^2. The electrochemical reaction, under these

conditions at the anode semiconductor surface, is therefore violent (lots of bubbling and agitation) and difficult to control. Such PSC samples have a structure characterized by micron diameter columnar shaped pores. Due to the difficulty of controlling the reaction, the diameter of the columnar pores is not under control and hard to reduce to the nano meter range which is more desirable for applications. In addition, this porous structure possesses a high porosity (about 0.9). The pore wall thickness is usually around 200 to 300 nm, which is the remaining SiC crystal left after the formation of the micron size pore. Such a porous structure is too fragile to be separated* from the substrate as a self-supporting free-standing film.

If we maintain the electrolytic solution and UV illumination condition constant, we find a qualitative relationship between the etching voltage and the resulting porous morphologies. To reviews, at a low voltage (< ~7V), a triangular (Figure 2.2a) porous structure forms, in the voltage range from ~7V to ~30V, chevron (Figure 2.2b) and dendritic (Figure 2.2c) pores dominate the porous structure, and by further increasing the voltage, some macro size (diameter ~ 1 μm) columnar pores appear together with the finer dendritic pores. The latter is called a partial columnar structure. The density of columnar pores rises with further increase of voltage until the columnar pores occupy all the available space, i.e., a complete columnar porous structure forms (Figure 2.1).

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* The separation procedure is performed by tuning up the etching voltage until a high current occurs (~1 A). The etching under this condition is very agitate and tends to remove most of the SiC material. At certain point, the porous structure formed at the bottom becomes so thin that the above porous structure layer will break off from the underneath bulk substrate.

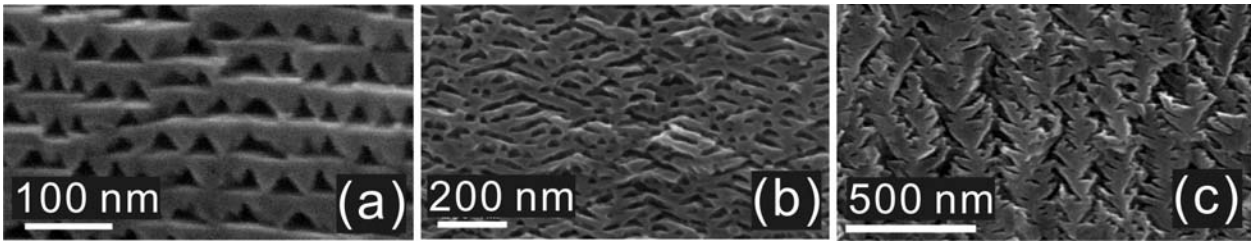

Figure 2.2 Cross sectional SEM images of the typical (a) triangular, (b) chevron, and (c) dendritic pores formed in highly doped n-type Si-face 4H and 6H SiC.

The complete (not partial) uniform columnar pore growth, with low porosity and nano meter diameter, hasn't been found yet on Si-face n-type 4H or 6H SiC. The challenge is to obtain a regular and mechanically strong columnar porous structure. In order to obtain a practical columnar structure, it is necessary to reduce the pore size together with the porosity. We have had investigated the experiment parameters as voltage, current density, surface patterning, HF concentration, SiC polytype, and SiC doping. So far, no such columnar porous structure has had been obtained.

2.3.2 A hybrid porous structure – partial columnar porous structure

Hybrid porous structures with both columnar and dendritic morphologies can be fabricated under certain conditions, for which the current density is in the transition region between dendritic and complete columnar pore formation. For the samples prepared in this study, the current densities in both etching modes are in the range from 20 to 300 mA/cm^2. The overall porosity of the partial columnar structures is about 20-40%, and this structure is sturdy enough to be separated as a free-standing film.

The partial columnar structure fabricated using constant voltage conditions is shown in Figure 2.3. In the constant voltage etching mode, the current density decreases during the etching process. The columnar pores tend to be bunched. The pore diameter is maintained at about one micron throughout the etching process. The diameters of the columnar pores do not depend strictly on the different voltages applied or the doping density of the starting SiC material. The experiments show that higher etching voltage or higher n-type doping density only changes the columnar pore density, but not the diameter. The fact that columnar pore diameter cannot be controlled using constant voltage conditions limits the possible applications of this partial columnar porous structure.

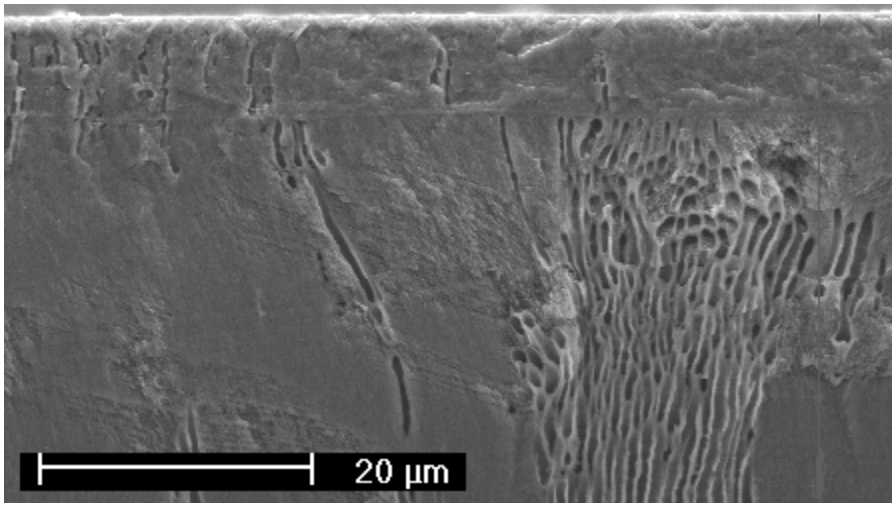

Figure 2.3 Cross sectional view of partial columnar structure fabricated with 50 V (constant voltage condition) applied to 6H SiC, doped n~5.7×10^{17} cm^{-3}.

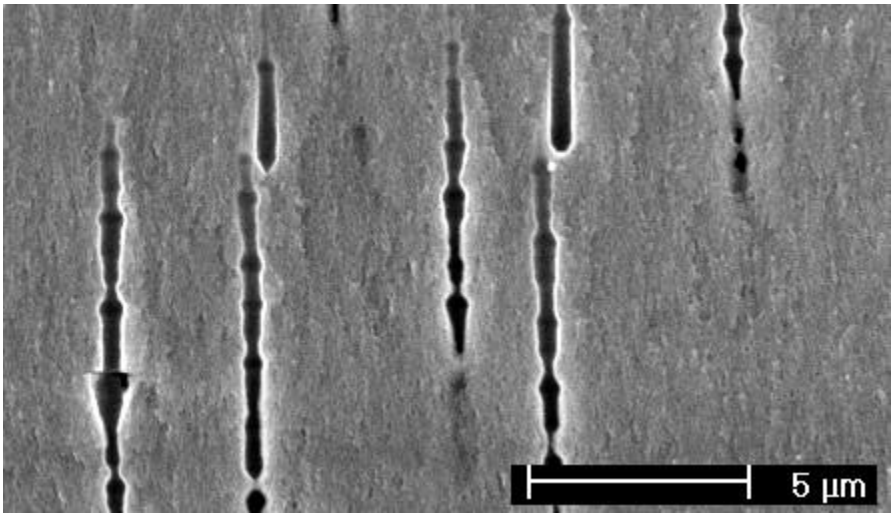

Figure 2.4 Cross sectional view of partial columnar structure fabricated in constant current mode using n-type 6H SiC doped at 5.7 $\times 10^{17}$ cm^{-3}. The desired current density is 45 mA/cm^2, but the power supply in this case was not capable of varying the voltage fast enough to maintain a steady current.

Constant current conditions have been investigated and found to be very effective in terms of controlling the partial columnar pore growth. It is believed that the constant current etching conditions regulate the rate at which holes are supplied to the anode. The columnar porous structure grown in this way (Figure 2.4) is much more spatially uniform, and the pores are straighter and better aligned compared to the porous structure fabricated by constant voltage conditions. The columnar pore density is also reduced. However, the anodic reaction produces gases, and the gas bubbles influence the HF flow into the pores. During the gas release, the etching chemical reaction could be partially interrupted. If the power supply used here is not capable of maintaining the current steadily when the disturbance happens, the resulting columnar pores will have a characteristic structure with an intermittently modulated diameter (Figure 2.4).

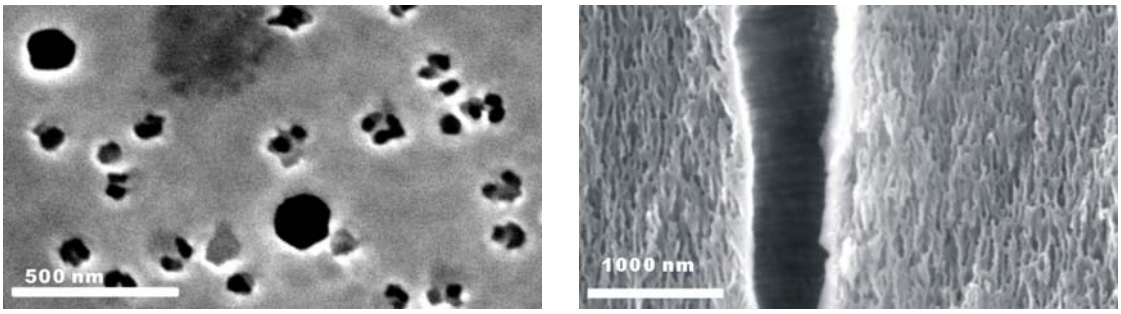

Figure 2.5 (a) Plan (as is after the etching) and (b) cross sectional views of a partial columnar PSC layer fabricated in 5% HF and 5% ethanol aqueous electrolytic solution with 45 mA/cm^2 (constant current condition) applied to 6H SiC, doped n~5.7×10^{17} cm^{-3} (Note the different scales).

To ameliorate this problem, a power supply unit with fast response and precise current control has been obtained. Figure 2.5 shows a partial columnar PSC made by controlling the current density steadily at 45 mA/cm^2 in n-type 6H SiC doped at 5.7×10^{17} cm^{-3} with UV photo-assistance. Figure 2.5a shows a plan view of the structure grown with this power supply. We believe that only the larger surface pores lead to the partial columnar pore formation while the smaller pits lead to the dendritic porous formation. The typical columnar surface pore diameter is ~200 nm, and the pore diameter gradually expands to ~500 nm (Figure 2.5b) approximately 20 μm beneath the surface. Although the surface pore diameters are not identical, the experiment shows a linear dependence (Figure 2.6) of the maximum surface pore diameters on the applied current densities. In addition, an increase in current density increases the columnar pore density, which results in higher porosity.

A possible explanation for the phenomenon of columnar pore diameter expansion in the constant current etching is based on a consideration of the HF diffusion in the pores and the consequent concentration gradient. As has been described previously, the electrochemical etching of SiC in HF electrolyte requires the participation of holes supplied from the

semiconductor. Under constant current etching conditions, the rate at which holes are supplied to the anode SiC is fixed. As the columnar pores grow into the bulk SiC perpendicular to the (0001) surface, the local HF concentration near pore tips decreases. Therefore, not all the holes generated by the injection of current from the power supply can combine by chemical reactions near the pore tips. The surplus holes can diffuse and drift to pore walls and participate in reactions that increase the pore diameter.

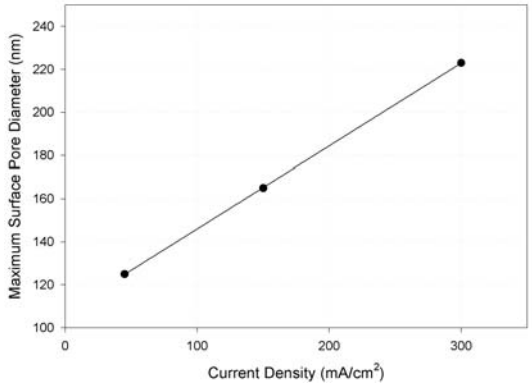

Figure 2.6 The maximum surface pore diameter vs. applied current density for Si-face n-type 6H SiC (n~5.7 $\times 10^{17}$ cm^{-3}) samples etched in 5% HF and 5% ethanol solution.

2.4 SUMMARY

We have fabricated a special porous structure, which we term the partial columnar structure, having variable surface pore sizes. This result opens a window to important applications such as

biomedical protein dialysis.[*] Two electrical etching modes are used to control the etching process: constant current and constant voltage mode. In general, the constant current mode etching will give much straighter and more uniformly distributed columnar structure than the constant voltage mode. The columnar pore density is determined by both the doping of the SiC material and the current density. The maximum surface pore diameter of the columnar structure shows a linear dependence on the current density. Due to the decreasing HF concentration as a function of depth into the porous sample during the etching process, a diameter expansion of the columnar pores is observed. We believe that balancing the effects of current density and the HF concentration distribution is important in obtaining uniform diameter columnar structures.

After the completion of the systematic electrochemical etching study on Si-face SiC samples, it became clear that other crystalline faces had to be considered. These experiments will be discussed in chapter 3 and chapter 4.

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[*] The columnar pores here are believed to be continuous and open at both sides of the porous film. This is simply because the nature of the photo-electrochemical etching process. During the etching, the electrolyte has to be filled inside the pores so that the etching can proceed. This ensures that the porous network is continuous, although may be very torturous and complicated.

3.0 COLUMNAR PORE GROWTH ON CARBON-FACE N-TYPE 4H AND 6H SILICON CARBIDE

3.1 INTRODUCTION AND EXPERIMENTAL NOTES

3.1.1 The work on obtaining the nano-columnar porous SiC

The photoelectrochemical etching (PECE) in SiC is known to be influenced by the different crystalline faces when the etching voltage is low, such as for the triangular porous structure formation.[27] In the etching, the Si-face appears to act as an etch stop. Therefore, one might conclude that trying to produce columnar porous growth on the Si-face is attempting to force etching in an unfavorable direction, namely <000-1>. Unless an avalanche breakdown PEC condition (even locally) is achieved, the columnar pore growth is not likely to take place (see Chapter 2)! It became clear that to achieve controllable columnar pore growth, PEC etching should be tried on "non-etch stop" faces, i.e., in etch preferred directions. From past experience we know that the C-face is oxidized much faster than the Si-face in wet oxidation of SiC. This suggests that in another kind of oxidation – the PEC process – the C-face is less likely to be an etch stop than the Si-face. Therefore we performed PECE in the <0001> direction (also parallel to the ĉ-axis as shown in Figure 3.1) and columnar pore formation has thus been achieved, as the most important result of this thesis. The fabrication of the self-ordered columnar PSC will be

discussed in detail in section 3.2. It will be shown that uniform columnar pores of about 20 nm in diameter have been successfully achieved. The columnar pore length can be as long as 200 μm[47]. The comparison experiments lead to the most important conclusion about the experiment control: to form nano-columnar porous structure in SiC, an optimized constant voltage etching condition should be applied to C-face SiC.

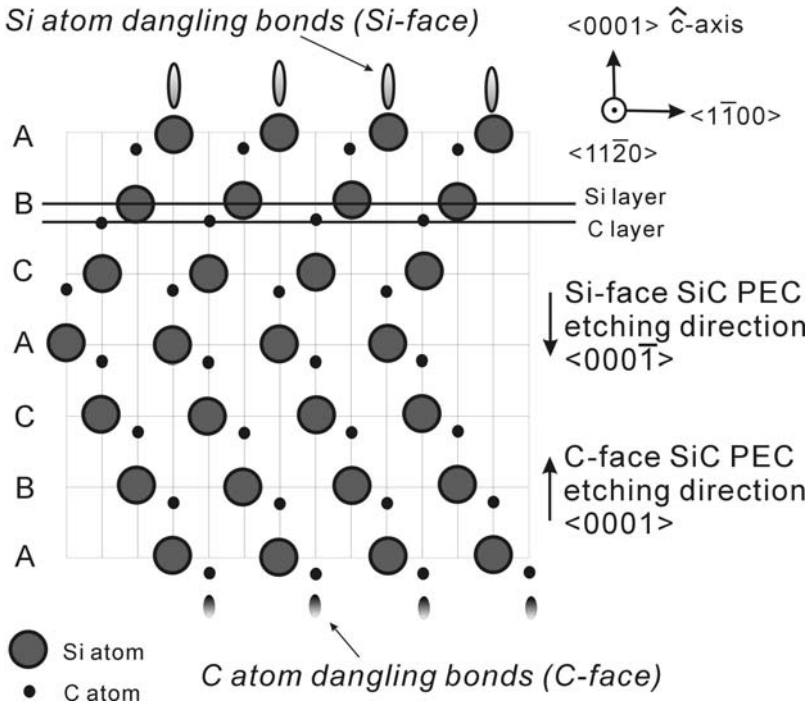

Figure 3.1 (11-20) plane of 6H SiC lattice structure with Si dangling bonds at the Si-face and C dangling bonds at the C-face. PEC etching directions on both faces are illustrated. Any atomic plane A, B, or C could be the surface layer.

3.1.2 Experimental systematic studies

After the observation of nano-columnar porous SiC, we intend to understand the columnar pore growth mechanism and explore the possibility to change the pore diameter and interpore spacing. From section 3.3 to section 3.7, we will present the systematic experiments on C-face SiC for the above purposes. The experiment parameters (see Table 1.1) that are important to the nano-columnar pore formation and will be discussed in the followed up sections are: etching voltage (section 3.3), surface conditions (section 3.4), temperature (section 3.5), HF concentration (section 3.6), and material doping (section 3.7). All the experiment observations will be concluded in section 3.8 to aid our later attempts to model the columnar pore growth.

In general, we found that the nano-columnar pore formation is a very "stable" process, which means that the diameter of the pores and interspacing of the pore lattice can not be changed by applying a different etching condition, such as etching voltage, surface conditions, temperature, HF concentration and SiC material doping. The resulting nano-columnar pore lattice remains almost the same (20±5 nm), if you ever obtain one. The formed columnar porous structures have almost identical pore diameter and center to center interpore spacing (40-60 nm). Our enormous effort to vary the pore diameters without destroying the columnar pore lattice remains fruitless so far.

3.1.3 Studies on the nano-columnar pore formation

Based on the experimental observations, the possible pore formation mechanisms are discussed with the intension to answer the following four questions:

(1) What determines the pores' cylindrical geometry?

(2) What determines the columnar pores' dimension?

(3) What is the potential distribution during the pore formation?

(4) What is the pattern formation mechanism?

In section 3.9, we will first present the basic semiconductor electrochemistry (double layer model with a flat interface) as the footstone for the model. The impedance measurement results are then shown in section 3.10 to prove the validity of the basic double layer model in our SiC electrochemical system. The impedance work in this section also provides the important information about the electron energy band edge positions at the interface. The knowledge will help some of our further discussions.

The section 3.11 is dedicated to explore the double layer system in the actual columnar pores and study the charge transfer process during the pore formation. We will try to answer the questions 1, 2 and 3 in this section. To explain the logic of the model better, we list the subsections in the flow chart Figure 3.2 (same as Figure 1.3). Last but not the least, the simulation work of pore pattern formation in a cubic lattice using a diffusion limited aggregation model will be presented in section 3.12. We will show that how difficult it is to apply the simulation in our columnar pore formation work to answer the question 4. Finally, section 3.13 will conclude all the experiment and modeling work.

The model analysis shows that the pore diameter is defined by the electric breakdown process at the pore tip. About 3 V voltage is actually dropped across the space charge region at the pore tips. Large fraction of the total applied voltage is essentially across the Helmholtz layer at the interface. To maintain the necessary current, an appreciable voltage is distributed in the electrolyte inside columnar pores. In addition, we also propose that the columnar pore formation

is only possible because of the fast oxidation reaction rate and the favored spontaneous Helmholtz layer field direction on C-face SiC.

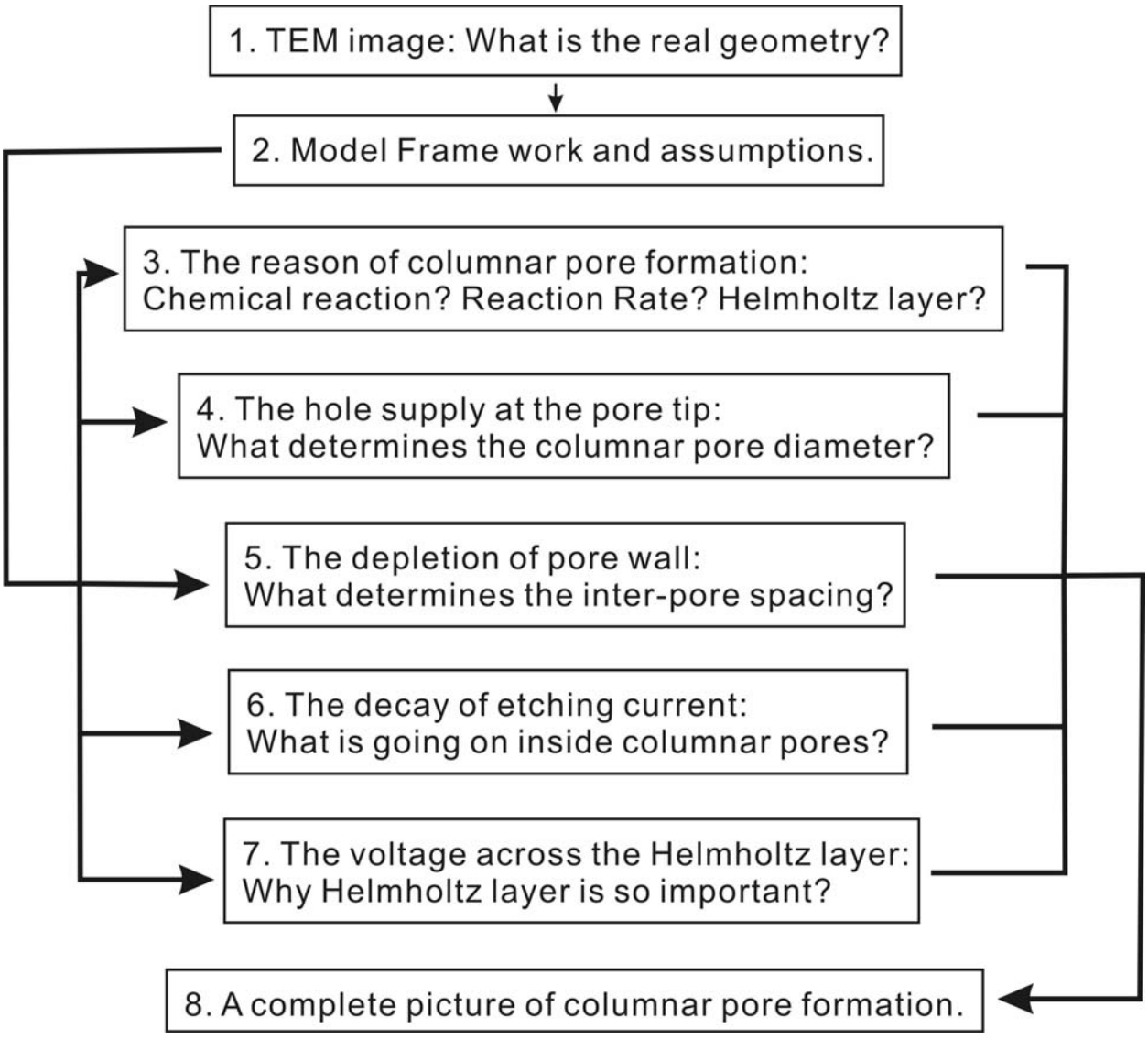

Figure 3.2 Flow chart that describes the logic of the charge transfer model in section 3.11.

3.1.4 Experiment note

The anodization is conducted in a two-electrode cell where a SiC crystal is used as the anode and a platinum plate as the cathode. Aqueous HF mixed with ethanol is used. A Nickel ohmic contact is made on the back side of the SiC sample and protected by Apiezon W wax. The front surface of the SiC sample is exposed to both the electrolytic solution and the UV illumination. A 1000W Oriel Hg Xe Arc Lamp combined with a dichroic mirror and water filter are used as the UV source to produce a flux of photons in the range from 380 nm to 420 nm. The intensity is about 600 mW/cm^2 as measured by a thermopile-type light power meter. Voltage is then applied across the two electrodes using a PAR 2273 Potentiostat/Galvanostat.

After anodization, samples are cleaned in acetone to remove the black wax mask. A Sartorius MC21S micro balance is used to measure the mass loss of the sample due to the photo-electrochemical (PEC) etching. The sample is then broken to expose cross sections in either $[1\bar{1}00]$ or $[11\bar{2}0]$ direction. Planar and cross-sectional SEM imaging is performed using a Philips XL30 FEG microscope at an operating voltage of 15 kV. The thickness of the porous structure is determined by the cross-sectional SEM measurement. In some cases, to reveal the structure at some depth from the top surface, we use a Plasma-Therm 790 Reactive Ion Etching (RIE) system to remove a known thickness of the porous structure. In the RIE etching process[52,53,54], SF_6 gas is used with 250 W power applied.

3.2 RESULTS ON NANO-COLUMNAR PORE FABRICATION

Our first attempts at columnar growth were with wafers of on axis n-type ($1\times10^{18}cm^{-3}$) C-face 6H SiC. Aqueous 10% HF mixed with 5% ethanol (measured by weight) electrolyte was used. For comparison of porous structures, we set the etching times at one hour in all experiments, unless specifically stated otherwise. The rest of this section describes the procedures used to obtain the columnar pore structure. This has been published in part in Electrochemical and Solid-State Letters 10 (7), p. K24 (2007)[47] and partly in Materials Science Forum Vols. 556-557, p. 741 (2007)[55].

3.2.1 Nano-columnar Porous Structure

The columnar morphology formed using C-face SiC wafers and applying 20 V anodic voltage is similar to that seen in porous Si (mean pore diameter D > 300 nm)[35,36], porous Al_2O_3 (D > 50 nm) [37,38] and porous InP (D > 200 nm)[39,40]. From our cross-sectional SEM images, we estimate that the pore diameter is about 20 nm and the pore wall thickness is about 40 nm (Figure 3.3(d)). With our SEM resolution (~2 nm), no detailed structure is seen on the pore walls (TEM work will be discussed in section 3.11.1). The 200 μm long nano-columnar pores are generally straight and arranged in a quasi hexagonal array.

The planar SEM image (Figure 3.3(a)) shows that the columnar pores do not form right at the surface. Surface pore nucleation tends to follow the damage left behind by the mechanical polishing and shows no particular order[56]. The areal density of the surface pores (~10 μm^{-2}) is far less than that of the columnar pores formed later in the bulk (~300 μm^{-2}). The cross-sectional

SEM image on the air/porous interface (Figure 3.3(b)) indicates a ~10 nm thick initial skin layer. The subsequent porous growth originates from the initial surface pores. The pores are neither regular nor straight and keep branching with increasing depth. This phenomenon occurs mostly within the first micron from the surface. Then, in the next few microns of porous structure, the pores take on the "columnar" shape but are still not well ordered. This roughly ten microns thick first porous structure below the skin layer is called the "cap layer". Following this layer, a regular columnar porous structure forms, as shown in the cross-section image (Figure 3.3(d)).

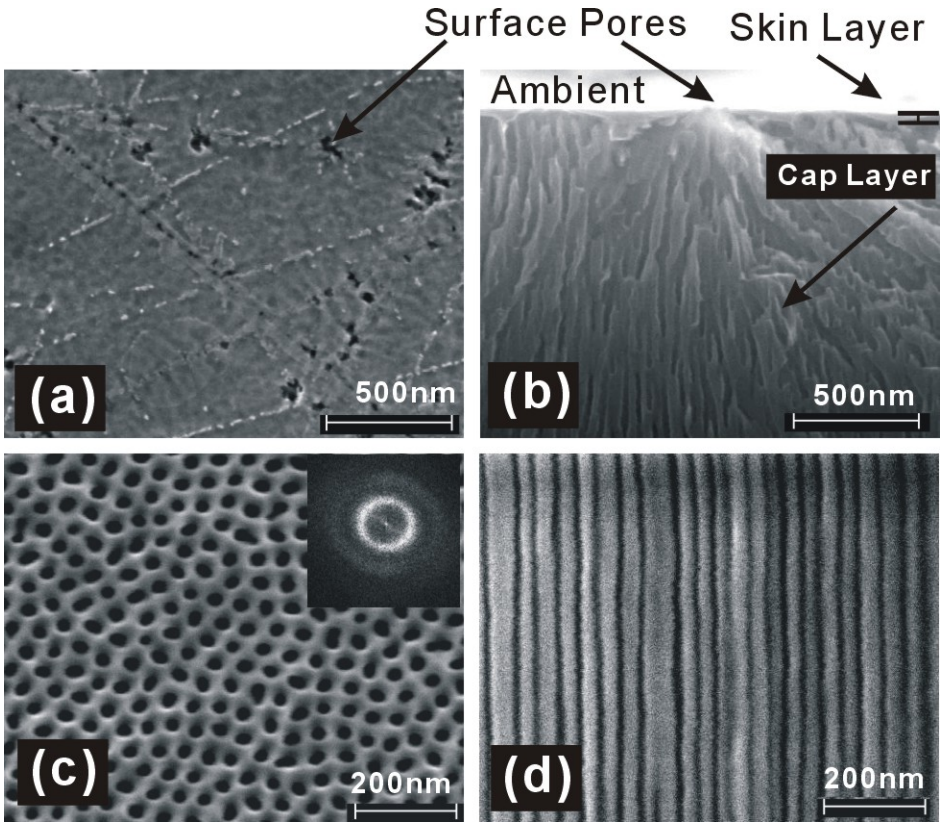

Figure 3.3 SEM images of (a) porous surface at the beginning of PEC etching, (b) early stage columnar pore formation in cross-section (beginning of the cap layer), (c) porous surface structure 20 μm below the original surface after 90 minutes of RIE to remove sufficient material to lay this layer bare (The inset shows the Fourier transform of a larger area of this picture), and (d) the self-ordered columnar porous structure below the cap layer in cross-section. All samples are etched on the C-face of 6H SiC.

To reveal the columnar porous structure and check the regularity of the porous pattern below the cap layer, we apply RIE to the sample for 90 minutes and remove roughly 20 μm of material from the top. A planar-view SEM image of the freshly exposed surface shows a semi-self-organized porous pattern, shown in Figure 3.3(c). The diameter of the pores is now about 30 nm instead of 20 nm as seen on the cross sections (Figure 3.3(d)). We believe this happens because the RIE etching not only removes basal plane SiC material but also removes material at the rims of the pores. The inter-pore distance between two adjacent pores' geometric centers is about 60 nm, which is not affected by the diameter enlargement of RIE.

The estimated porosity based on measuring the weight loss due to the PEC process is about 10%. To verify this measurement, the porosity can be estimated with the geometrical structural measurements using SEM images. Here we assume that the columnar porous structure is a uniform hexagonal packed lattice of circular cylindrical pores (Figure 3.4).

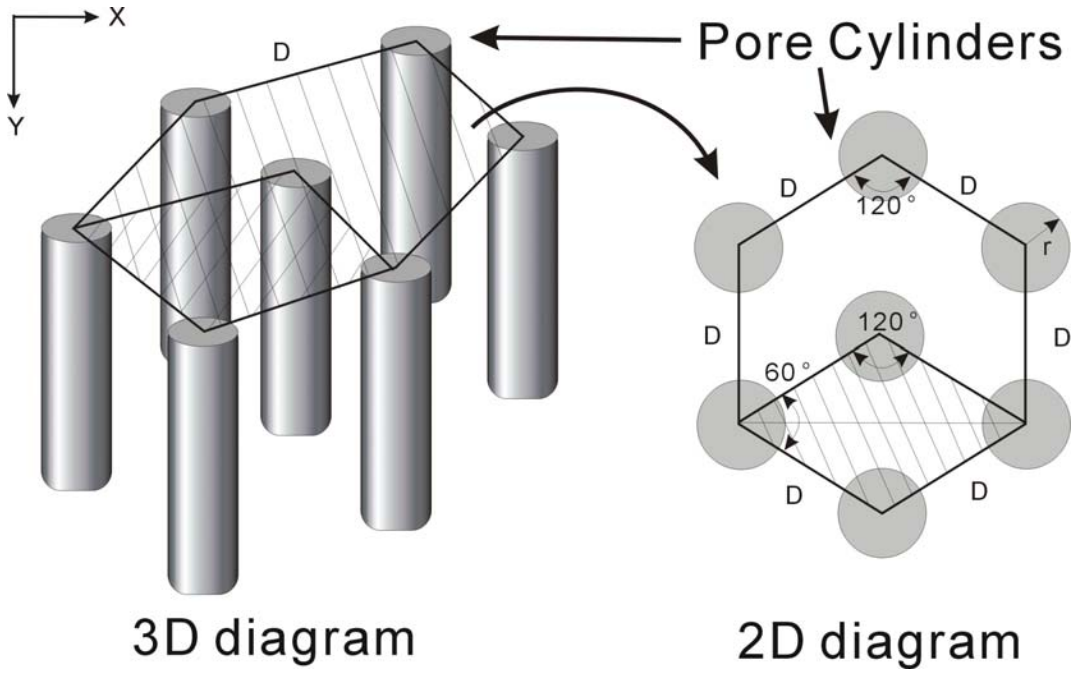

Figure 3.4 Idealized perfect surface pore pattern of the columnar porous structure. The hatched area in the two dimensional diagram is the 2 dimensional unit cell.

The porosity of the whole structure is the same as the porosity of the 2 dimensional (2D) unit cell, as shown in Figure 3.4. Each 2D unit cell contains one columnar pore. The expressions for each 2D unit cell are:

$$A_{pore} = \pi \cdot r^2 \,;\, A_{2D\ \text{Unit Cell}} = \frac{\sqrt{3}}{2} D^2 \,;\, P_{2D} = \frac{A_{pore}}{A_{2D\ \text{Unit Cell}}} . \qquad \textbf{3.1}$$

In the above expressions, r is the radius of the columnar pore, D is the distance between the adjacent pore centers, A_{pore} is the area of a pore inside the unit cell, $A_{2D\ Unit\ Cell}$ is the area of the 2D unit cell, and P_{2D} is the two dimensional surface porosity. P_{3D} is the porosity we want to calculate. For a perfect columnar porous lattice as shown in Figure 3.4, because the porosity P_{2D} remains constant for any arbitrary 2D intersection plane, $P_{3D}=P_{2D}$. We have

$$P_{3D} = P_{2D} = \frac{2\pi}{\sqrt{3}} \left(\frac{r}{D} \right)^2 . \qquad \textbf{3.2}$$

For the measured values r=10 nm and D=60 nm, the porosity P_{3D} is calculated to be 0.1. The mechanical strength* associated with this low porosity makes this nano-columnar PSC a practical nano-material for many applications. This estimate of the porosity agrees with the gravimetric porosity determined by using the microbalance and the SEM thickness measurement. As a matter of curiosity, this value also happens to be the same as the porosity of self-organized porous alumina. The reason for this particular porosity is discussed for the porous alumina[38] but remains unclear for PSC because of the different growth mechanisms.

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* The mechanical strength is not a measured or modeled quantity here. We say so because the nano-columnar porous structure can survive the mechanical polishing and form a self supporting structure. It is also observed that any surface scratching with Q-tip cannot damage the porous structure.

3.2.2 Discussion of Comparison Experiments

To investigate the most important control for the nano-columnar pore formation, three comparison PECE experiments have been performed:

EXP. 1: On axis **C**-face 6H SiC etched under constant voltage conditions of 20 V.

EXP. 2: On axis **Si**-face 6H SiC etched under constant voltage conditions of 20 V.

EXP. 3: On axis **C**-face 6H SiC etched under constant current conditions of 30 mA/cm^2. The reason of using the current density in the EXP. 3 will be explained later in the text.

All the experimental data of the three experiments are concluded in Table 3.1 for the following discussion.

Experiment	Crystal Surface & Etching Mode	Porous Layer Thickness (μm)	Pore Diameter (nm)	Gravimetric Porosity (%)	Average Unit Area Mass Loss (mg/(cm^2 hour))	Average Unit Area Charge Flow (C/(cm^2 hour))	Average Number of holes for Etching One SiC Pair
EXP.1	C-face 6H SiC & Constant Voltage	201	20	10	6.3	111	7.3
EXP.2	Si-face 6H SiC & Constant Voltage	81	~30	18	4.6	77	6.9
EXP.3	C-face 6H SiC & Constant Current	152	~20	13	6.3	108	7.1

Table 3.1 PECE experimental data.

We will discuss the possible electrochemical reaction happened during the pore formation. Number of holes "γ" needed in order to etch away a single SiC pair[27] is a very important parameter to evaluate the actual electro-chemical reactions in these PEC processes. The agreement among different experiments will suggest a specific electro-chemical process. We calculate γ for this PEC process using the following expression:

$$\gamma = N_{holes} / N_{SiC} = \frac{Q}{e} \Big/ \frac{V_p}{V_o} = \frac{Q}{e} \Big/ \frac{\Delta m}{\rho \cdot V_o} = \frac{Q \cdot \rho \cdot V_o}{e \cdot \Delta m} \quad \textbf{3.3}$$

Here, Q is the total electric charge flowing through the sample. e is the unit electric charge (1.6×10^{-19} C). N_{holes}=Q/e is the total number of holes that flowed. Δm is the mass loss in grams and ρ is the SiC mass density (3.21 g/cm^3). V_p, the pore volume, which is the total volume of SiC pairs removed by the PEC process, is then just Δm/ρ. V_o is the volume of a SiC pair, as determined below. N_{SiC}= V_p/V_0 is the number of SiC pairs chemically removed. Therefore, $N_{SiC} = \frac{\Delta m}{\rho \cdot V_o}$.

For a 6H SiC single crystal, V_0 can be calculated by the following method. The 6H SiC unit cell volume is $\frac{\sqrt{3}}{2}a^2c$ where a and c are the lattice constants. The measured values[57] are a = 3.08 Å, c = 15.12 Å. Since the unit cell contains six SiC pairs, each pair occupies an effective average volume: $V_0 = \frac{\sqrt{3}}{12}a^2c = 20.7\times10^{-24} cm^3$.

For each of the PECE processes, the total amount of charge is estimated by integrating the current-time curve, such as the ones shown in Figure 3.6a and b. The number of holes required to etch a SiC pair is then calculated.

It is believed that there are two steps in the PEC reactions of PSC formation. The SiC interface is first oxidized under anodic conditions with H_2O and then the oxidation layer is removed by the HF electrolyte. Two kinds of electrochemical reactions are proposed by I. Lauermann *et al.* [17,18] and Y. Shishkin[27] *et al.*, which will be discussed in detail in section 3.8.2. In all of our three experiments, about seven holes (7.3 in EXP. 1; 6.9 in EXP. 2; 7.1 in EXP. 3) on average are needed for a single SiC pair to be removed. These results are also consistent with

the number of holes calculated for triangular PSC formation[27] and the PECE reported by J. Shor *et al.*[15]. This implies that all the PECE electrochemical reactions are similar, at least in the number of holes needed to remove each SiC pair. Figure 3.5 and Figure 3.6 show SEM images and PECE curves, respectively, from the three experiments. The different porous morphologies obtained in the different electrochemical processes (Figure 3.5) are therefore unlikely to be related to different PECE reactions.

The SEM images (Figure 3.5) of EXP. 1 vs. EXP. 2 and EXP. 1 vs. EXP. 3 show that the columnar structure does not form in the Si-face sample (EXP. 2). For C-face samples, the constant current condition will not lead to a uniform columnar porous structure (EXP. 3). Only in EXP.1 when a constant voltage condition is applied to a C-face SiC sample, we obtain the uniform nano-columnar porous structure. Therefore, we conclude that two PECE conditions are necessary for the columnar structure formation: the C-face of 6H SiC rather than the Si-face must be used, and an appropriate constant voltage condition must be maintained during PECE.

In EXP. 1 (Figure 3.5a-d), we observe the formation process of a self-ordered columnar porous structure as described earlier. In EXP. 2 (Figure 3.5e-h), even though the same identical condition is applied to the Si-face sample, no columnar pore growth is observed! The "dendritic" pores grow approximately parallel to the ĉ-axis with pore diameters of about 20-50 nm. The etching current-time (I-t) curves of Figure 3.6a and Figure 3.6b both display a rapid non-exponential (cannot be fit to $e^{-At} + B$ where A and B are constants) current density drop. After an initial interval, the current density scales as a power law with time:

$$J = A \cdot (t / t_0)^{-\beta} \ , \qquad \textbf{3.4}$$

where t_0 is the unit of time (second), J is the current density (mA/cm^2 will be used in this thesis), t is the etching time in seconds, A is a parameter with units the same as J, and β is a dimensionless number.

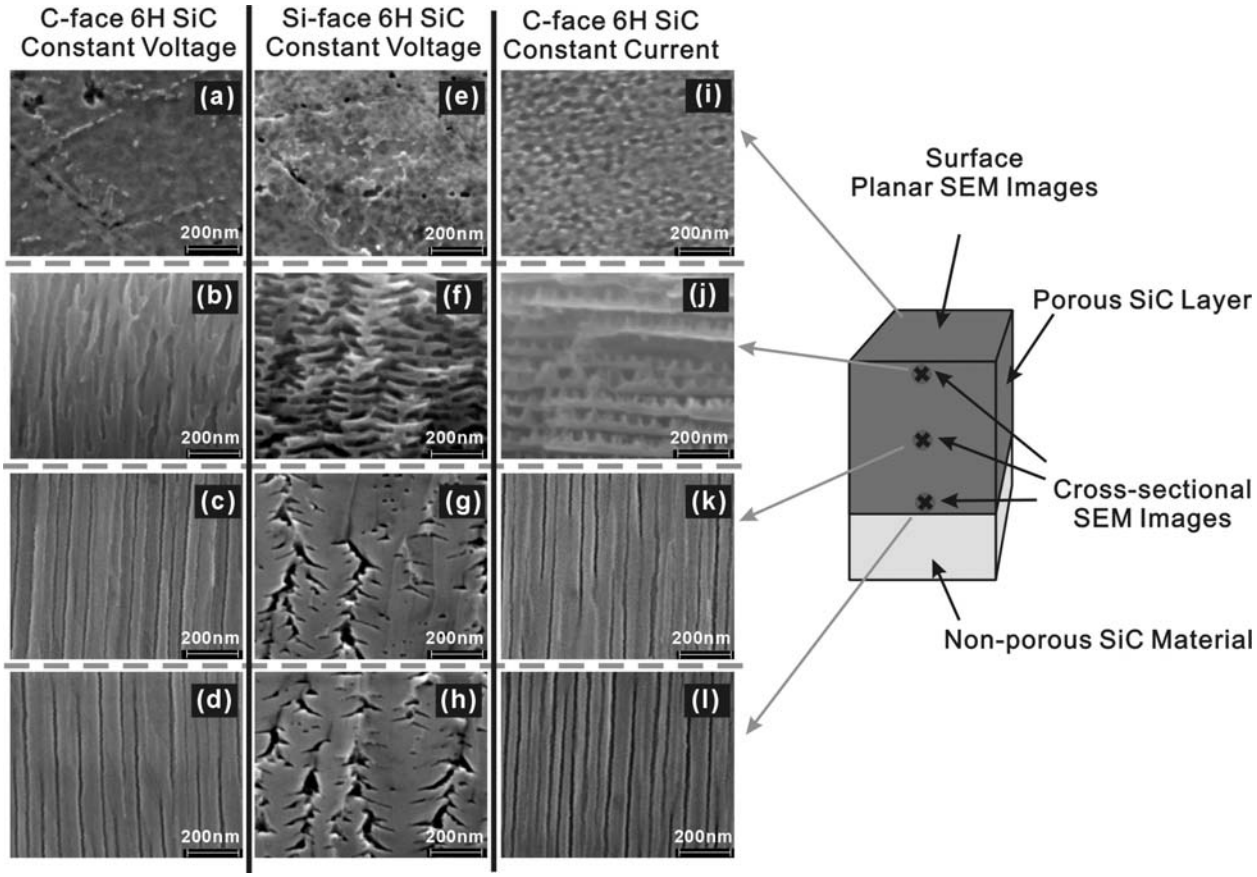

Figure 3.5 Planar and cross sectional SEM images of (a)-(d) C-face 6H SiC porous structure of EXP.1. (e)-(h) Si-face 6H SiC porous structure of EXP.2. (i)-(l) C-face 6H SiC porous structure of EXP.3.

For the C-face sample in EXP. 1, we have $A \approx 510$ and $\beta \approx 0.40$, while for the Si-face sample in EXP. 2, $A \approx 415$ and $\beta \approx 0.43$. The current density decay associated with the PEC process might be correlated with the time evolution of the optical absorption (As the pore front moves deeper into the sample, due to the optical absorption, the

intensity of the UV illumination will decay exponentially. This detailed intensity decay will be more complicated for PSC because of the strong scattering) and the migration of ions within the pores.

The influence of the UV light absorption on the current decay can be evaluated by comparing EXP. 1 to an experiment on C-face SiC in which no UV light was applied but all the other etching conditions are unchanged. As an experiment result, nano-columnar porous structure forms (more discussion in section 3.11.4). We also obtained a current-time curve with very similar decay behavior to the curve obtained under UV light illumination. The two fitting constants are $A \approx 90$, $\beta \approx 0.40$. This means the light only shifts the current density-time decay curve in the double log plot. The time evolution of the optical absorption doesn't change the characteristic decay of the current curve in the double log plot (in EXP. 1, the fitting constants are $A \approx 510$, $\beta \approx 0.40$). Therefore, the observed decay of the current density here is probably related to the ion migration in the pores, which will be discussed later (section 3.8.7).

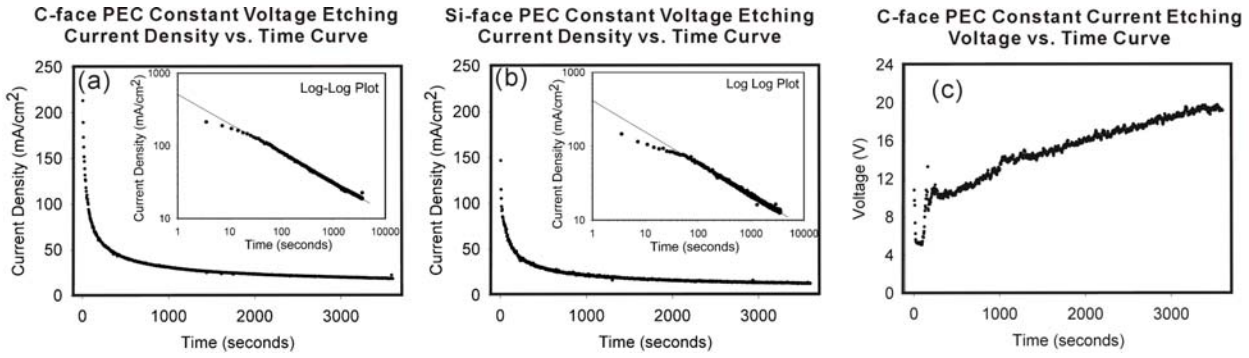

Figure 3.6 I-t curve during (a) EXP.1 and (b) EXP.2; (c) V-t curve in EXP.3**.**

A high current density reflects a large electrochemical reaction rate. The large electrochemical etching rate will lead to a high rate of pore volume expansion. Consider the C-

face columnar pore growth, which is uniform and has simple pore geometry. The two dimensional areal porosity of a columnar porous layer is almost constant below the first few microns of etching. The effective etching area is therefore roughly a constant throughout. Consequently, the high electrochemical reaction rate results in a higher growth rate of the porous layer thickness at the beginning of the etching process compared to the rate at the end. This behavior is confirmed by etching a C-face sample at constant voltage for one minute. The resulting 23 μm thick columnar porous layer shows that the average rate of increase of the porous layer thickness for the one minute etching is about seven times the rate for one hour PECE.

If we compare the current densities at the same etching time in the two experiments, it is found that the current density on the C-face is in general higher than that on the Si-face. This observation shows that the electrochemical reaction rate is higher for the C-face under the same etching conditions. Current voltage (I-V) measurements were performed on both the C-face and the Si-face of 6H SiC to see if there are, indeed, differences in the electrolyte-semiconductor junction properties due to the two different crystal faces (Figure 3.7). For both the C-face and Si-face, UV illumination in general enhances the current density, although "abnormal" behavior (for a small region, current density without UV illumination is larger than the one with UV illumination between ~7 V and ~15 V for the C-face SiC scan) is not understood. There are two distinct steps (the shift of the steps could indicate the onset of certain electrochemical reactions) in the curves with UV illumination at which the current increases abruptly. These steps are separated by a plateau (Δ_{Si} for the Si-face scan and Δ_C for the C-face on Figure 3.7). The voltage range and the corresponding current densities of Δ_{Si} and Δ_C are not very different. Beyond this plateau, the I-V curve for the C-face SiC shows a larger and more rapidly increasing current

density than that for the Si-face. The current density for C-face SiC under UV illumination can be as large as 400 mA/cm^2 at 50 V reverse bias, compared to 100 mA/cm^2 for the Si-face. This clear difference between the Si-face and C-face I-V curves indicates dissimilar interface junction properties of the two crystalline faces in a PECE process. The larger current density on the C-face also suggests a faster electrochemical etching rate or oxidation rate in PECE than the rate on the Si-face. The ratio of the mass loss in EXP. 1 to that in EXP. 2 is 1.4 and confirms this suggestion. This result is also in agreement with the result from wet oxidation experiments, where C-face wet oxidation has a much higher rate than the Si-face one[58]. Moreover, the ratio of the porous layer thickness in EXP. 1 to that in EXP. 2 measured along the ĉ-axis is 2.5. This means the PECE proceeds more rapidly in the <0001> direction for the C-face than in the <000-1> direction for the Si-face. More discussion to understand this different etching rate will be presented in section 3.11.3. Therefore, to achieve controllable columnar pore growth, PECE should be performed on the C-face SiC.

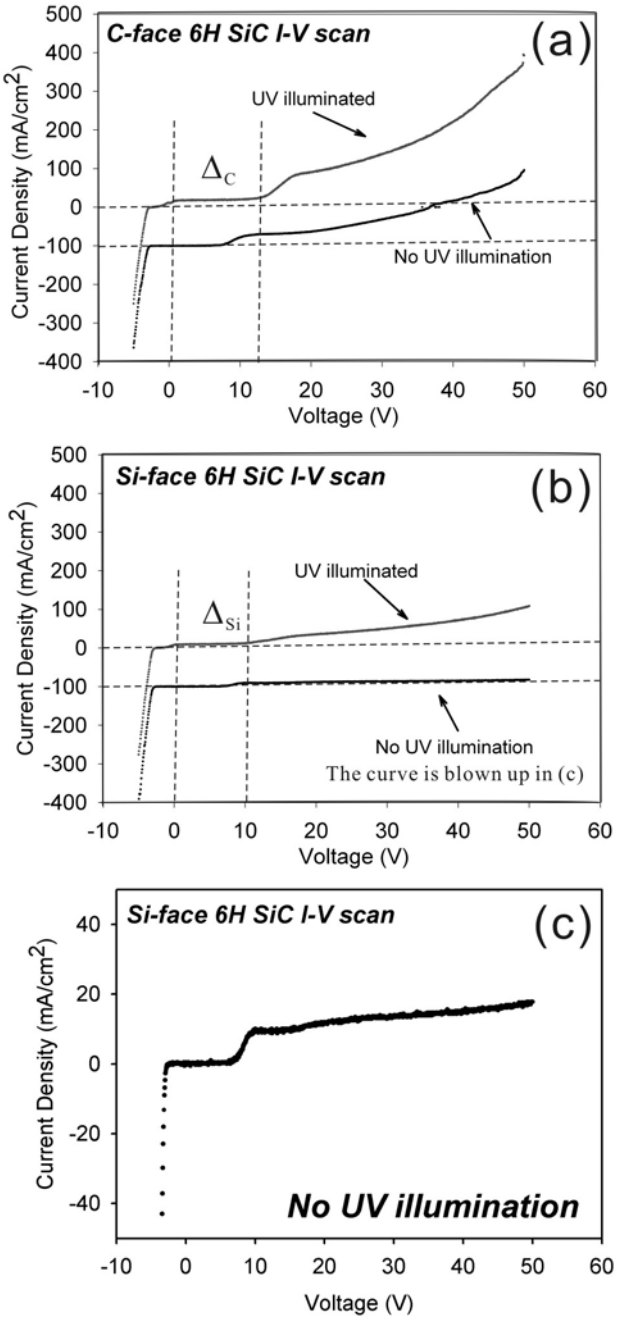

Figure 3.7 I-V scan (a) on a C-face and (b) on a Si-face of 6H SiC in 10% HF, 5% ethanol electrolyte at 1 V/s scan rate. (c) The expanded plot of the same I-V scan curve on Si-face 6H SiC without UV illumination. Note that in order to better distinguish the curves recorded with and without UV illumination, the I-V curve without UV illumination is arbitrarily lowered by 100 mA/cm^2.

In EXP. 1, after the rapid current decrease at the beginning of the process as shown on the linear plot in Figure 3.6a, the current density is about 30 mA/cm^2 during most of the etching interval. Despite the obvious decay observed on the double log plot, the value of the current density does not change significantly. We therefore think we have a quasi-constant current in the most of the etching interval. In order to determine whether it is this quasi-constant current flow is critical for forming the columnar PSC, we conducted a constant current density experiment at 30 mA/cm^2 with all other PECE conditions unchanged in EXP. 3. The constant current density maintained during the whole etching does not lead to a uniform porous morphology. The resulting porous structure (Figure 3.5i-l) is changing with the applied voltage (Figure 3.6c). The voltage increases from 5 V to about 20 V towards the end of the etching. Correspondingly, we observe that at the start of the constant current etching, we obtain a triangular morphology. Following the triangular layer, we have primarily irregular columnar PSC structure. It is only towards the latter stage of etching (after 50 minutes), where the voltage approaches 20 V, we observe a relatively ordered and straight columnar porous structure. This terminal structure resembles what we obtain under constant voltage etching. This result indicates a constant voltage condition is crucial in forming the ordered nano-columnar porous structure. It also suggests that a certain electric field at the electrolyte/solid interface is required to obtain columnar pore formation. As will be discussed in the section 3.3 to 3.7, we saw that, in columnar PSC fabrication, the columnar porous morphology, pore diameter and inter-pore spacing are all correlated with the etching conditions such as voltage, doping, HF concentration etc. No evidence has been found thus far that a change of any of the above experimental conditions will vary the pore diameter and interpore spacing without radically changing the columnar pore morphology. Further experiments are discussed below in which we tried to find the necessary

etching conditions that may change the pore diameter and spacing, as well as to determine the pore formation mechanism.

3.3 THE OPTIMUM VOLTAGE FOR THE COLUMNAR PORE FORMATION

During the experiments for fabricating the nano columnar porous structure, it was determined that the applied voltage has a crucial effect on the resulting pore morphology. A constant voltage etching condition appears to be crucial in order to produce a regular and uniform pore lattice.

In the earlier described photo-electrochemical etching in section 3.2 on the n-type C-face of 6H SiC doped at 1×10^{18} cm^{-3}, it seemed that columnar pore growth was optimized when the applied voltage was around 20 V. A series of SEM images are shown in Figure 3.8 to compare the pore formation when the voltage is lower or higher than 20 V. Figure 3.8e-h shows the SEM images of a columnar porous structure using 20V as discussed in section 3.2. If 10 V is applied (Figure 3.8a-d), the porous structure close to the surface has a layered morphology filled with triangular shaped pores[27]. The relation between the surface pores and the subsequent pore growth has not been determined as yet. Below this layer, in the major portion of the porous layer, we find a very irregular columnar pore structure. The pore morphology can hardly be recognized as columnar. The sinuous pores go in and out of the exposed SiC cross sectional plane and do not show a connected porous network in the SEM cross-section image. After one hour of etching, the final porous structure thickness is about 210 μm and the average porosity is 0.1. Comparison with the 20 V etching, the 10 V voltage porous layer thickness and the overall porosity are both similar.

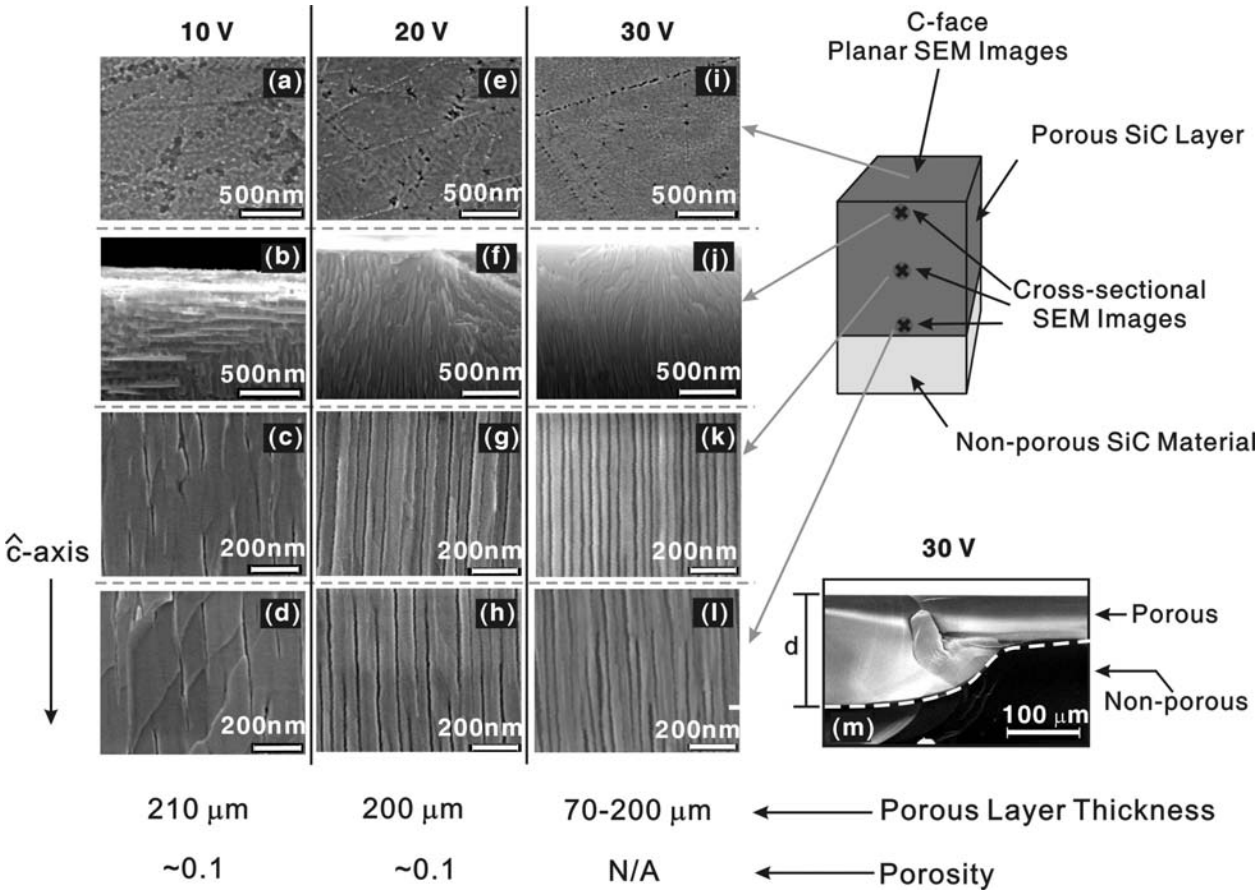

Figure 3.8 Planar and cross sectional SEM images of (a)-(d) 10 V, (e)-(h) 20 V and (i)-(l) 30 V constant voltage etching on C-face 6H SiC. (m) At the right of the main figure, is a cross sectional image and shows the inhomogeneous porous thickness of a columnar porous structure fabricated by applying 30 V voltage.

30 V etching changes the columnar porous structure formation in another way. In Figure 3.8i-l, we can see that the porous structure close to the air/porous interface is quite similar to the 20 V etched porous structure. In the middle of the porous layer, the columnar pores are straight and ordered. The pores are 20 nm in diameter, but the pore density is higher than that in 20V etched sample. However, towards the porous/bulk interface, the porous structure becomes irregular. This means the columnar porous etching becomes very unstable with 30 V etching.

Most importantly, the vertical thickness of the porous structure is inhomogeneous (Figure 3.8m). The thinnest part of the structure is about 70 μm thick while the thickest part is about 200 μm. It is interesting to see that the maximum thickness remains close to those obtained for 10 V and 20 V etching. However, some part of the porous growth is slower or even stopped at some point. The reason for this large variance in the thickness is not clear yet. Because of this thickness variation, the porosity of the porous structure can not be evaluated gravimetrically.

The recorded current density-time curves for three different voltages are shown in Figure 3.9. In all three curves we can observe a linear decay section on the log-log plot. If we fit the curve to the relation 3.4, we have $A \approx 545$ and $\beta \approx 0.43$ for 10 V etching, and $A \approx 510$ and $\beta \approx 0.40$ for 20 V etching. For 30 V etching, there are two linear sections. For the first 500 seconds, $A \approx 893$ and $\beta \approx 0.43$, while for the rest (time > 500 s) of the curve, $A \approx 388$ and $\beta \approx 0.37$. The decay constants β here are not very different from what we obtained (~0.4) in section 3.2. The reason of this current decay will be discussed in a much greater detail in section 3.11.6. It is interesting to see that the current density curves (a) and (b) eventually overlap after an initial interval of 100 seconds. The curve fitting results for these curves are also very close. However, the very different pore morphology suggests that the initial high current flow is important for the columnar pore growth. Curve c with 30 V etching shows a larger current density at the outset. The curve has a similar decay constant to the other two curves in the first 500 seconds but the decay rate becomes slower in the later etching process (see log-log plot).

The experiments here prove that there exists an optimum voltage that should be found for the most uniform nano-columnar porous structure formation.

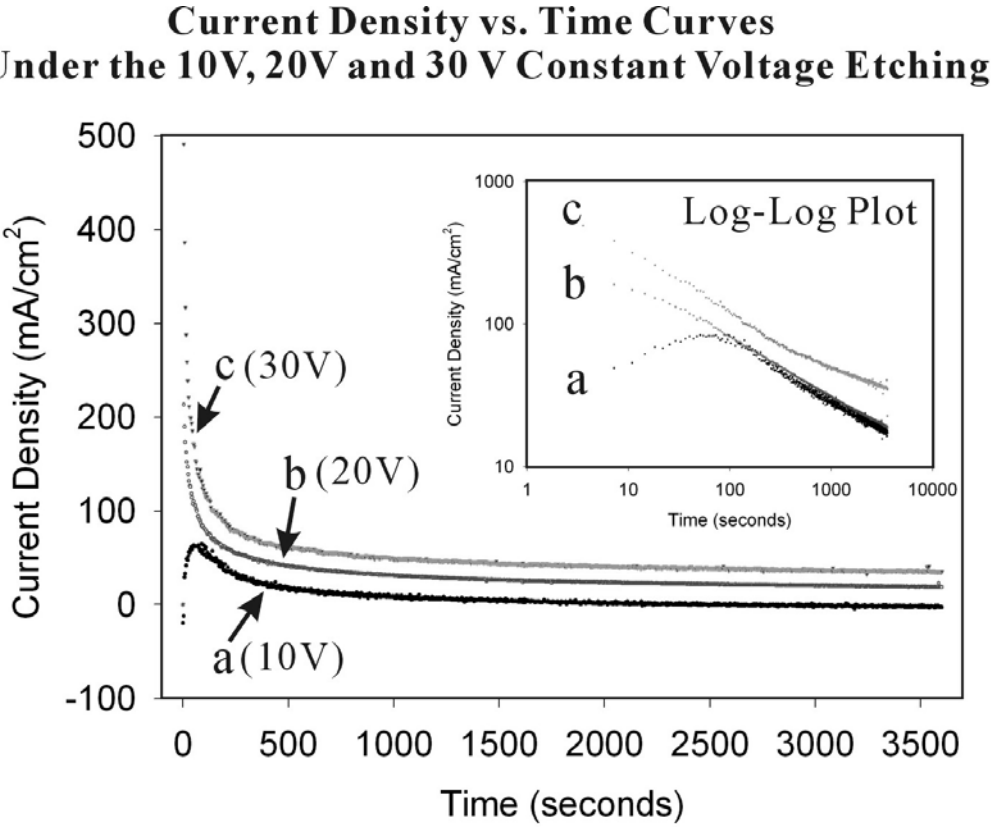

Figure 3.9 The current density vs. time curves recorded for constant voltage etching of SiC at (a) 10V, (b) 20V and (c) 30V. Note that to better distinguish the curves a and b on this linear plot, curve a has been shifted down by 20 mA/cm^2. The inset shows the log-log plot of the same curves.

3.4 THE EFFECTS OF SURFACE CONDITIONS ON COLUMNAR PORE FORMATION

In the formation processes of other columnar porous materials, such as porous Si [59, 60] and alumina[37], it is known that the surface patterning or tailoring can change the pore initiation and thus alter the pore dimension and distribution. To investigate the columnar pore formation in SiC, it is then necessary to understand the effects of the surface condition on pore initiation.

Before any experiment on C-face SiC, we did a comparison etching on Si-face 6H SiC, doped around 1×10^{18} cm^{-3}, in 5% HF and 5% ethanol (weight percentages) electrolyte.[56] Two samples were used. One has a chemical mechanical polished (CMP) Si-face while the other sample was mechanical polished (MP) finishing with ¼ μm diamond. The planar and cross sectional view of each porous sample are shown in Figure 3.10. Both samples were etched with 20 V bias but without UV illumination. For the MP Si surface, most surface pores initiate along surface scratches from the mechanical polishing (Figure 3.10a). The cross sectional view (Figure 3.10b) reveals that the dendritic shaped pores grow uniformly into the bulk material roughly perpendicular to the initial surface. For the CMP Si-face sample, fewer surface pores are nucleated and their spatial distribution is random without any preferential nucleation sites. A hemispherical growth profile* (Figure 3.10c and d) and dendritic type porous structure are observed (SEM images are not shown here) below every surface pore, which indicates isotropic pore growth starting from the initial surface nucleation site. These experiments on Si-face SiC show that the surface pore nucleation can be changed by the surface condition.

UV illumination, however, changes the pore nucleation greatly. The experiments on MP and CMP Si-face samples do not show the distinctive pore nucleation difference. In order to focus on our discussion and because the interest is now to see if surface features can change the pore nucleation on the C-face for the possible different columnar pores, the experiments on Si-

* The SEM image shows a much smaller fraction of a sphere than half here. This happens to be so in this case because two surface pores are close to each other so that the underlying pore growth interferes with each other. If there is a surface pore far away from others, we do observe what appears to be a hemispherical profile.

face will not shown here. Instead, we will present the comparison experiments on C-face with UV illumination.

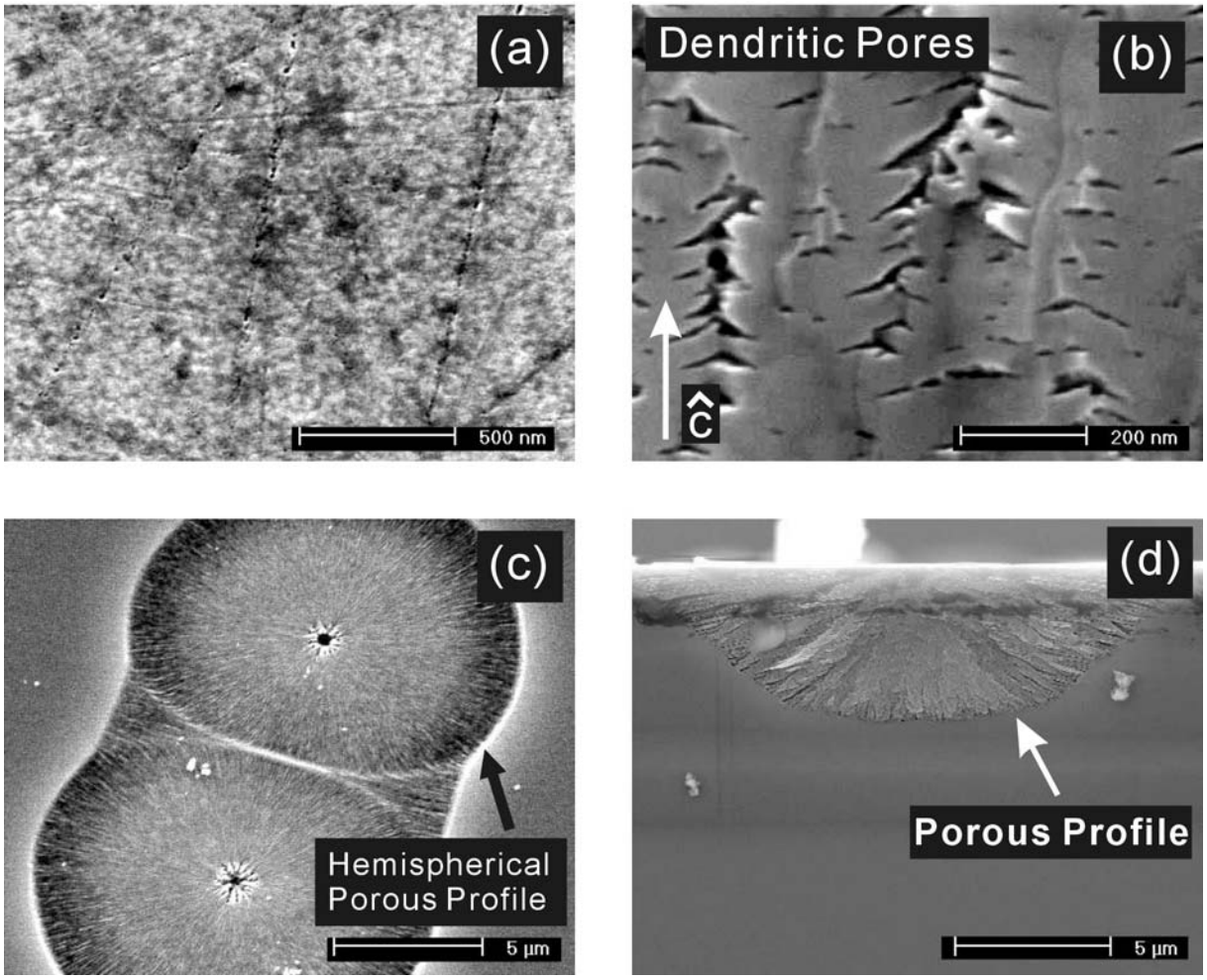

Figure 3.10 (a) Plan and (b) cross sectional views of porous structure in MP Si-face (Note the different scales); (c) Plan and (d) cross sectional views of PSC prepared using CMP Si-face SiC (see Ref. 56).

The experiments on C-face SiC were then performed on CMP and MP on-axis 6H SiC samples doped at 2.4×10^{18} cm^{-3} in 10% HF and 5% ethanol (weight percentage) aqueous electrolytic solution. To study influence of the surface condition influence on the columnar pore formation, the optimum voltage 15 V is used to ensure the nano columnar pore formation. 600

mW/cm^2 UV illumination was also used to facilitate the electrochemical process. The etching time was set to 15 min in each experiment. The electrolyte temperature was controlled at 20 $^oC \pm 0.2\ ^oC$. A total of four samples were studied:

(1) *CMP sample*: NOVASiC polished CMP C-face 6H SiC.

(2) *¼ μm MP sample*: NOVASiC CMP C-face 6H SiC roughened up by ¼ μm diamond lapping compound mechanically.

(3) *1 μm MP sample*: NOVASiC CMP C-face 6H SiC roughened up by 1 μm diamond lapping compound mechanically.

(4) *6 μm MP sample*: NOVASiC CMP C-face 6H SiC roughened up by 6 μm diamond lapping compound mechanically.

Figure 3.11 shows the AFM images of the samples. All the images are taken after we ultrasonically cleaned the samples in acetone and then ethanol for 10 minutes. The RMS surface roughness values for the CMP, ¼ μm MP, 1 μm MP and 6 μm MP sample surfaces are 0.8, 0.9, 2.1, 6.8 nm, respectively. There are some surface features on the CMP surface. The reason for the white spots on the CMP surface is not clear to us and shallow scratches were observed. For the MP samples, in general, the scratch depth and width increase with the increase of the diamond size in the lapping compound.

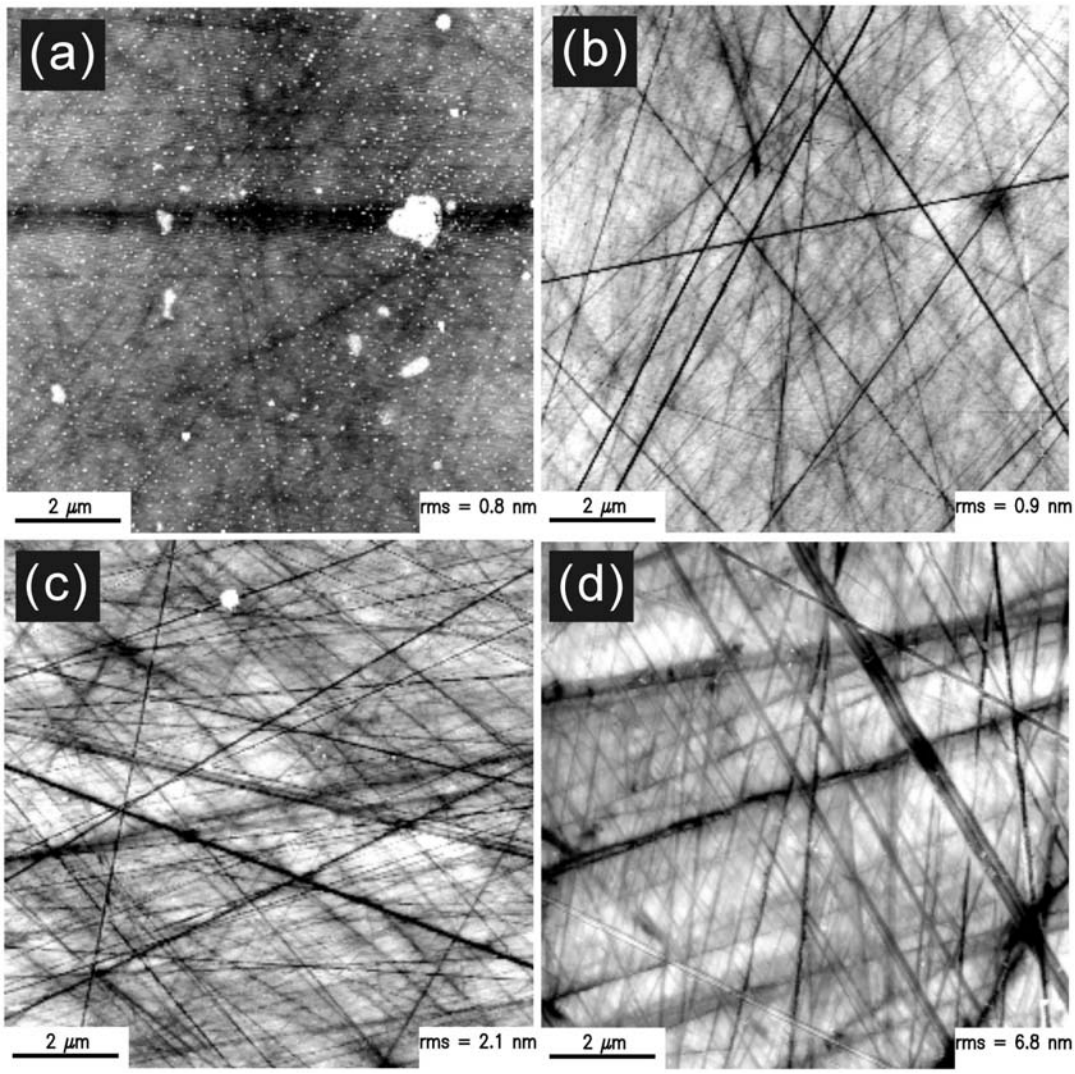

Figure 3.11 AFM images of the (a) CMP sample, (b) ¼ μm MP sample, (c) 1 μm MP sample and (d) 6 μm MP sample surfaces before the PECE. The cause of white spots in (a) is not clear to us. Special thanks to S. Nie and R.M. Feenstra for their kindly help on the AFM work.

Surface	Area (cm^2)	Mass Loss (mg)	Porous Layer Thickness (μm)	Porosity	Transferred Charge (C)	γ
CMP	0.16	1.025	132	0.15	18.24	7.4
¼ μm MP	0.23	1.466	132	0.15	25.64	7.3
1 μm MP	0.24	1.527	133	0.15	26.62	7.2
6 μm MP	0.24	1.715	133	0.17	30.28	7.3

Table 3.2 Experimental results from the etching of the four C-face n-type 6H SiC samples with different surface roughness.

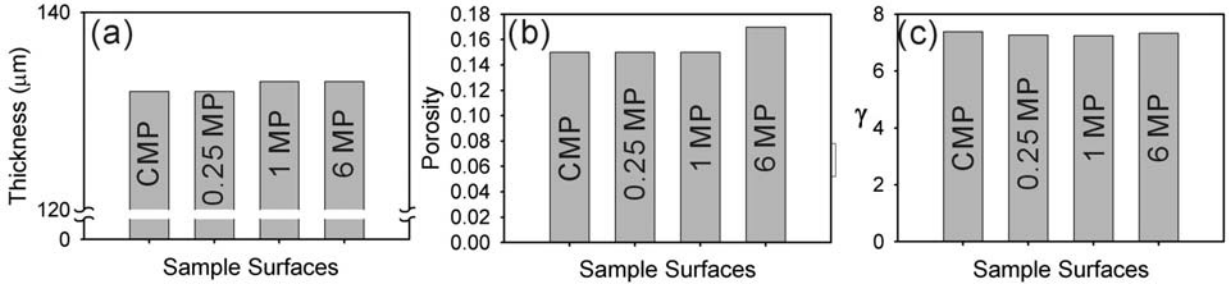

Figure 3.12 Plot of the (a) porous layer thickness, (b) porosity and (c) γ from the photo-electrochemical etching.

Table 3.2 lists the experiment data from these experiments. These results are also plotted in Figure 3.12. The porous layer thickness, porosity and γ are almost identical within the experimental error.

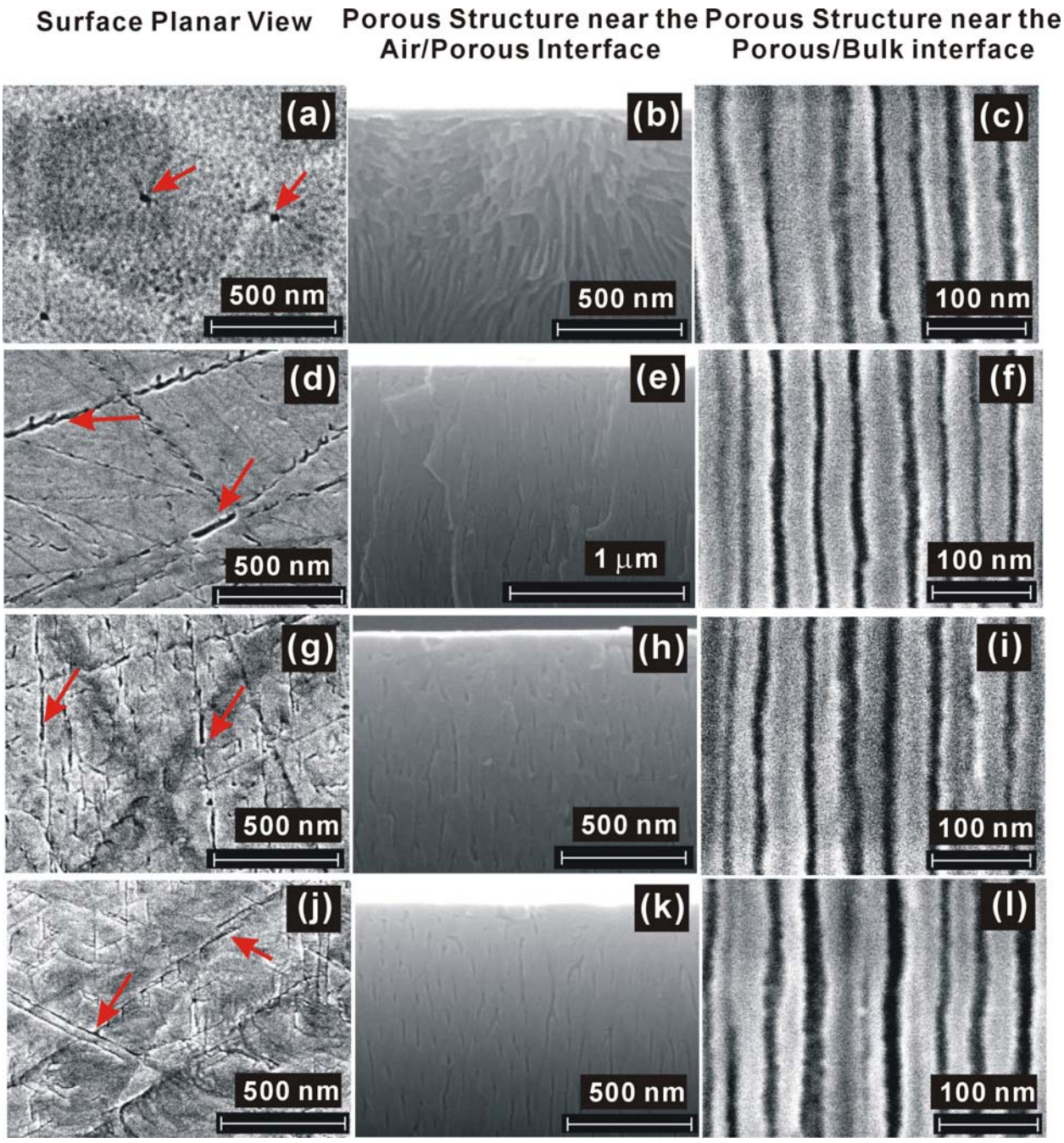

Figure 3.13 SEM images of the (a-c) CMP, (b-e) ¼ μm MP, (g-i) 1 μm MP and (j-l) 6 μm MP samples after the photo-electrochemical process. From left to right, each row shows the planar surface, a cross section close to the air/porous interface and a cross section close to the porous/non porous interface. The arrows on the planar surface SEM images are pointing to the possible surface pores.

The SEM images in Figure 3.13 show that the formed nanocolumnar structures are almost identical near the porous layer/bulk interface, although there is a difference in the pore nucleation. For the CMP sample, there are much fewer nucleation sites compared to the MP ones. The surface pores are distributed almost evenly across the surface and the pores inside the bulk initiate from these pores. As for the MP samples, the surface pores are mostly located at the scratches caused by the mechanical polishing. Because there are far more surface pores on these surfaces, the strong branching phenomena as observed in the CMP sample (Figure 3.13b) near the air/porous interface in the initial stage of the pore formation is not apparent for the MP samples.

As shown in the Figure 3.14, the four current density vs. time curves are almost identical. When plotted on a double log scale, all four become straight lines as the etching proceeds. We fit the linear section of each curve to the power law relation 3.4. The fit results for the parameters A and β are shown in Figure 3.14 b and c separately. Parameter A fluctuates around 800 and β fluctuates around 0.4. No obvious change in β is observed for the four experiments.

Finally, we need to point out that during the etching process we observe a periodic current oscillation (Figure 3.15). This means the actual current density curve is actually an AC signal with a significant DC part. If we subtract the predicted fit values from the original current density to eliminate the DC part of the current density signal, we can plot the current density residual (AC part of the current density signal) vs. the time, as shown in Figure 3.15. It is observed that, despite the fact that the behavior of the DC current density decay is similar in all four cases, the oscillation of the current density during the etching is not the same. The magnitude of the oscillation is about 2 mA/cm^2, around 4% of the total current density at 1500 s. These results show that the periodicity of the current density oscillation is less apparent as the

initial crystal surface is made rougher. This is in agreement with the Fast Fourier Transform (FFT) analysis of the original oscillating curves. The FFT power spectrum shows a strong peak for the CMP sample with the characteristic frequency about 0.08 Hz. The power spectrum for the ¼ μm MP sample shows that the frequency is lowered to be 0.06 Hz. The peak is also broadened, which means periodicity is decreasing. As for the 1 μm and 6 μm MP samples, there is no longer apparent periodic oscillation frequency peak in the FFT power spectrum. The oscillation of the current density becomes more like a non-periodic fluctuation.

From these data we can conclude that the roughness of the surface does not influence the columnar pore formation in any obvious way. However, the surface condition will strongly influence the current oscillation during the nano-columnar pore formation. The most periodic oscillation current curve is obtained from the CMP SiC sample. This explains that for the inconsistence of the oscillation behavior during the nano-columnar pore formation in various samples.

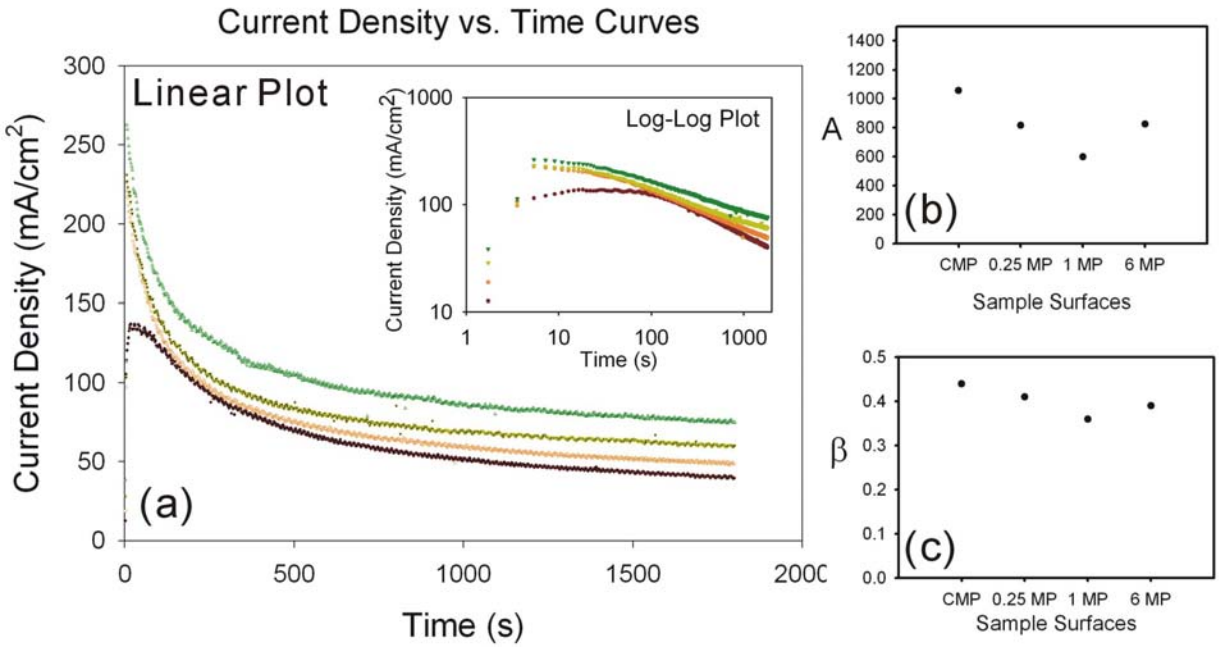

Figure 3.14 (a) Current density vs. time curves recorded during the etching of the four samples plot on linear and double log scales. From the bottom to the top, the curves are corresponded to CMP, ¼ μm MP, 1 μm MP and 6 μm MP sample etching curves. Note that, in the above order, each curve is offset up in both scales by 10 mA/cm^2 with respect to the previous one to better distinguish the different curves. Without the offset, the four curves nearly overlap. (b) Fitting results for the parameter A in Equation 3.4 for the four curves. (c) Fitting results for the decay parameter β in Equation 3.4 for the four curves. The fitting errors are all within 1%. The error due to the electrochemical process could be 5%.

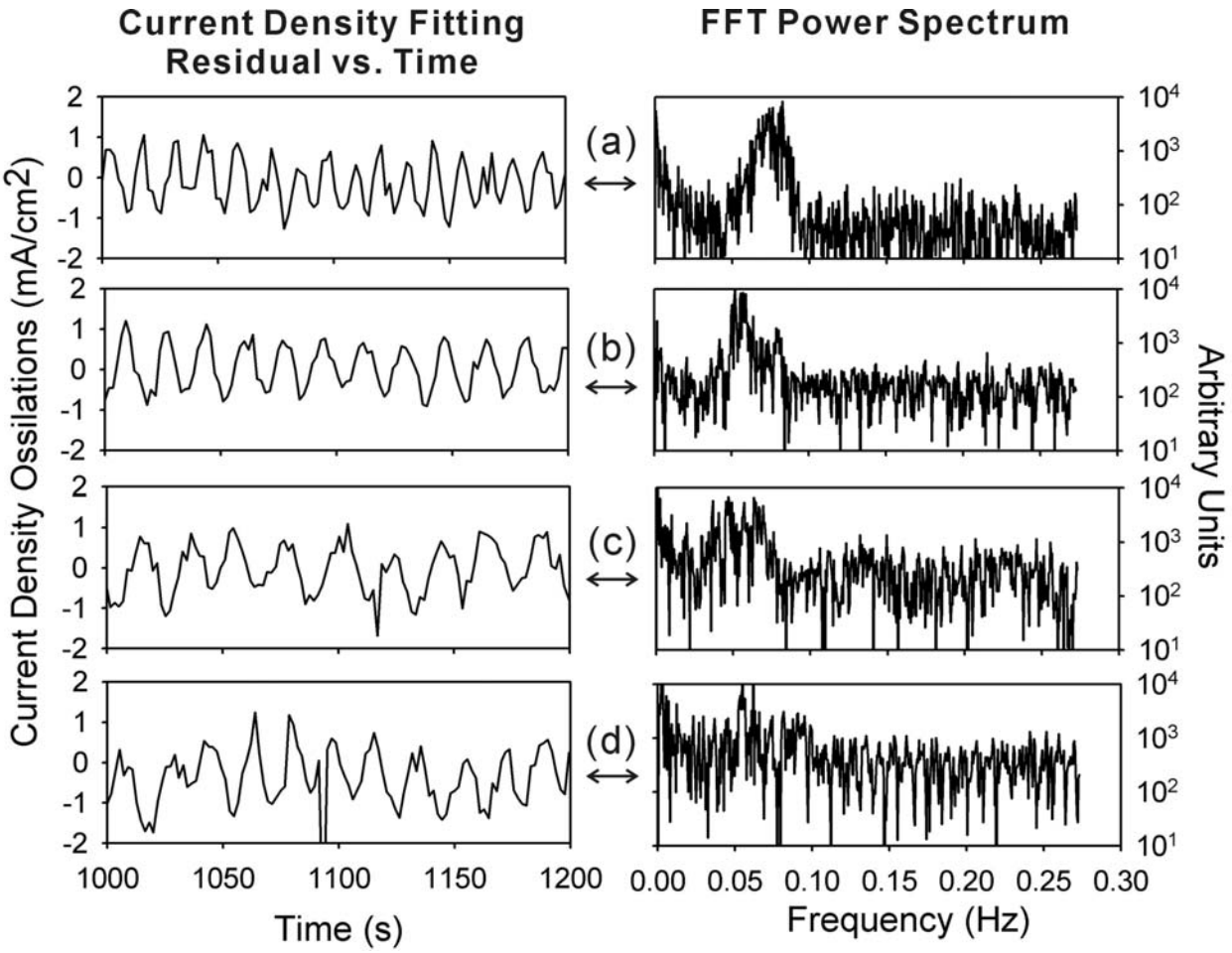

Figure 3.15 Current density oscillation during the etching of (a) CMP, (b) ¼ μm MP, (c)1 μm MP and (d) 6 μm MP samples. The panels in the left column show the current density residuals during 1000 s to 1200s in order to highlight the oscillatory behavior. The right column panels are the power spectra obtained by performing a FFT on the current density residual curves.

3.5 TEMPERATURE CONTROLLED EXPERIMENTS TO OPTIMIZE THE PORE GROWTH

Because of the UV illumination and the possible large current flow through the system, the heat introduced during the reaction cannot be neglected. Therefore, during the etching process, the temperature of the electrolytic solution is increasing without any cooling. It is common to see a 3 to 5 ^{o}C temperature increase during a one hour long experiment. It is well known that the temperature affects the rate of the chemical reaction and the diffusion and drifting processes. For many electrochemical processes of porous fabrication such as porous Si and porous Alumina[37], the electrolyte temperature is strictly controlled for various reasons. In our case, to ensure that the experiment result is more consistent and reproducible in a truly systematic study, we use a thermo bath unit and maintain the temperature throughout the etching. In addition, we also want to find out whether the long range order of the formed columnar pore lattice can be improved by controlling the reaction temperature. The temperature dependence of the photo-electrochemical etching process is studied as well.

3.5.1 The voltage effect at controlled etching temperature

The comparison experiments were carried out on C-face n-type 4H SiC doped about $1x10^{18}$ cm^{-3}. The idea was to see if temperature affects the columnar pore formation in any unexpected way. The corresponding optimum voltage for the nano-columnar pore formation in the 4H SiC material is about 45 V. The optimum voltage difference between 4H and 6H SiC at the same doping is not understood so far.

The experiments with increasing voltage in 5 V steps were performed. The goals are to determine and understand the effect of voltage on the columnar pore formation under different temperatures. Other experimental conditions fixed. The electrolyte used in this study is 10% HF and 5% ethanol (weight percentage). UV illumination intensity is about 600 mW/cm^2. The etching time is set at 30 minutes in all cases. Five experiments have been carried out:

1. 45 V without the temperature control. The temperature rises from 21 ^oC to 24 ^oC.
2. 45 V while the temperature is controlled at 10 ^oC with ±0.1 ^oC tolerance.
3. 50 V while the temperature is controlled at 10 ^oC with ±0.1 ^oC tolerance.
4. 55 V while the temperature is controlled at 10 ^oC with ±0.1 ^oC tolerance.
5. 60 V while the temperature is controlled at 10 ^oC with ±0.1 ^oC tolerance.

The Current density vs. time curves and SEM images are shown in Figure 3.16. The planar view SEM images are taken after MP the porous structure so that ~50 μm of the porous layer is removed from the original sample surface. The pore lattice below the cap layer is thus exposed and reflects the planar view of a self-organized columnar porous structure. From these experimental results we can conclude as the following:

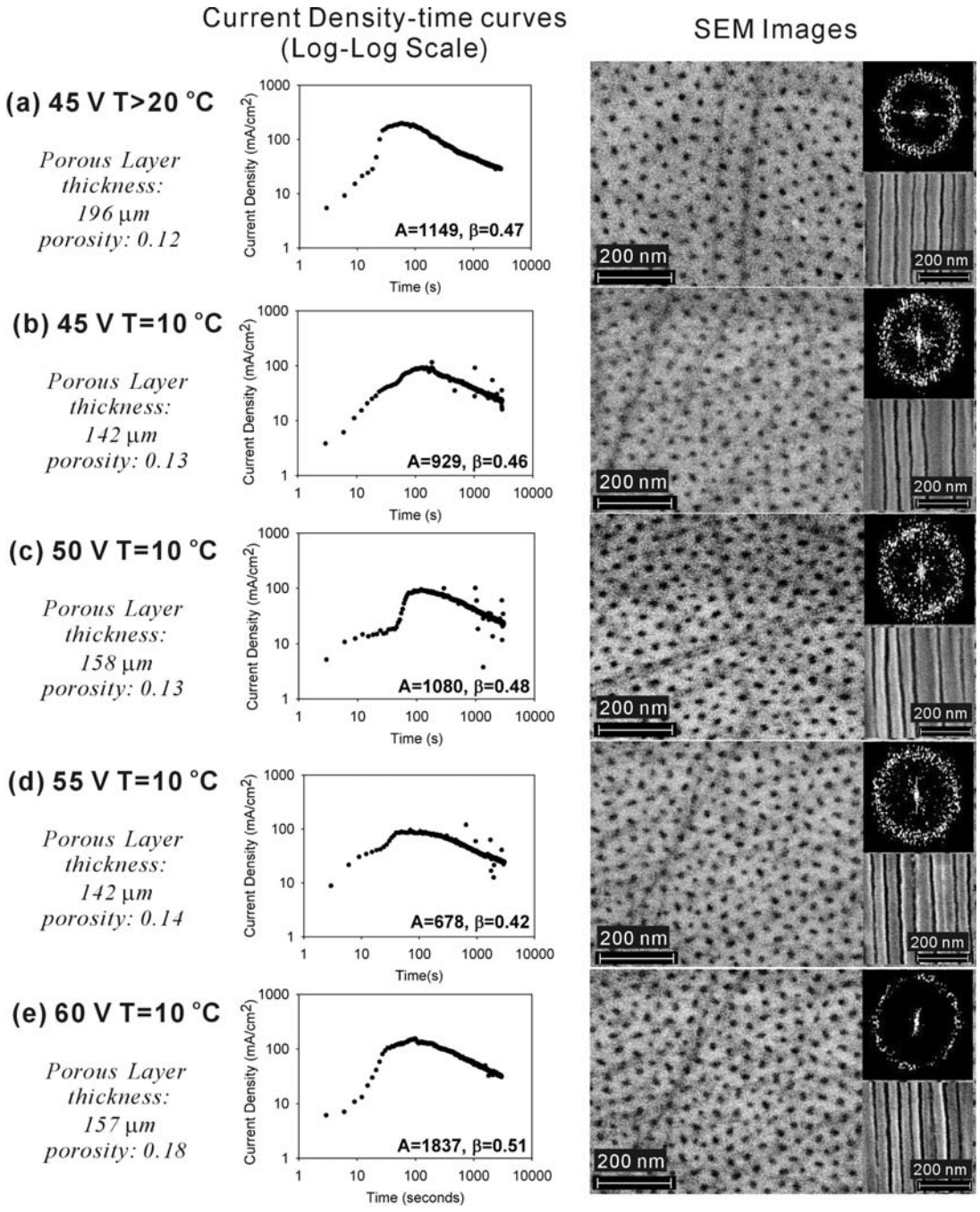

Figure 3.16 Current density-time curves (left column) and corresponding planar view SEM images (right column) of columnar PSC etched under (a) 45 V without temperature control, (b) 45 V at 10 ^{o}C, (c) 50 V at 10 ^{o}C, (d) 55 V at 10 ^{o}C, and (e) 60 V at 10 ^{o}C. Porous layer thickness and porosity are indicated. The fitting parameter A and β from Eq. 3.4 are shown in the current density-time plots. In each SEM picture, the upper inset shows the FFT image of a larger area of the surface and the lower right inset is the cross sectional SEM image.

Experiments 1 and 2 show that reducing the temperature slows down the pore formation rate. There is no noticeable change in the pore morphology according to our SEM images. There is no change in the dimensions of pore lattice and the long range order is not improved by controlling the temperature. The porosity remains the same within experimental error (5%).

The four experiments (Exp. 2 to 5) performed at 10 ^{o}C with increasing etching voltage show that the increasing electric field (between 45 to 60 V) does not improve or change the pore lattice order. The mean pore diameter remains about the same (~20 nm). However, the pore density increases with the increasing etching voltage. Therefore the columnar pores are closer to one another and the pore wall thickness is reduced. The porosity of the porous layer is increased, as shown in Figure 3.16. It is also observed that increasing the voltage does not increase the porous layer thickness for the 30 min etching process. The current density vs. time curves are also similar. These curves possess similar maximum current densities and decay constants β. These experiments show that, over a limited voltage range with precise control of temperature, one can change the pore lattice without destroying the columnar pore morphology. The pore wall distance can be reduced from 40 nm to 20 nm by increasing the voltage. The pore diameter and the etching rate remain about the same.

3.5.2 The temperature effect in the nano-columnar pore formation

A systematic study was performed to investigate the co-effects of both the reaction temperature and the applied voltage in the columnar pore formation. Here we still use 10% HF and 5% ethanol (weight percentage) aqueous solution. The UV illumination is 600 mW/cm^2. The etching time is 30 minutes. We chose three different test temperatures: 10 ^{o}C, 20 ^{o}C and 30 ^{o}C.

The SiC material we used here is C-face on axis 6H SiC doped around $n \sim 2.4 \times 10^{18}$ cm^{-3}. The optimum voltage for the nano-columnar pore formation in this material is about 15 V. We vary the voltage to have a full picture of the temperature effect in the nano-columnar porous formation. The voltages chosen are 5V, 10V, 15V, 18V, 20V and 25V. A total of 18 experiments have been performed and the cross sectional SEM images of the formed structures are shown in Figure 3.17.

The SEM images show that changing the temperature in a 20 ^{o}C interval doesn't change the columnar pore morphology under a fixed etching voltage. The voltage effect is similar to we found before on the 4H SiC doped at $1 \times 10^{18} cm^{-3}$. The lowest voltage tested here is 5V. The formed porous structure is hardly recognizable as a self-organized columnar pore array. The 10-20 nm diameter columnar pores are of low pore density. Some triangular pores can also be observed together with the columnar pores. When the voltage is increased to 10V, more columnar pores appear. The pore diameter remains about 10-20 nm. Branching of the pores happens even in the late stage of the pore growth. At higher etching voltage, such as 15 and 18 V, the porous structure is relatively well organized. The pore morphology is uniform and stable after the initial pore nucleation stage. If a higher voltage (20 V and 25 V) is used, the pore wall thickness decreases and the pore density increases. However, the pore formation becomes less uniform and there is a pore size variation (20-40 nm) throughout the complete porous structure.

The measured porous layer thickness, porosity and the parameter γ are plotted in the Figure 3.18. The recorded current density-time curves are shown in Figure 3.19. These curves all have a linear section on the log-log plot. We can fit this section of the curve to the power law decay Equation 3.4. The fit parameters A and β are also plotted in Figure 3.19. During the etching process, we also discovered an oscillatory behavior in the drawn current. The fitting

process gives the “DC” (slowly varying) part of the current signal. After this part is subtracted from the original current data, the AC part can be readily observed. To better tell if we have a periodic oscillation in the etching, we then FFT the AC part of the current density. The resulted power spectra are plotted in Figure 3.20. Finally, a cyclic voltammetry scan is performed on non-porous SiC for each temperature. The results are shown in Figure 3.21.

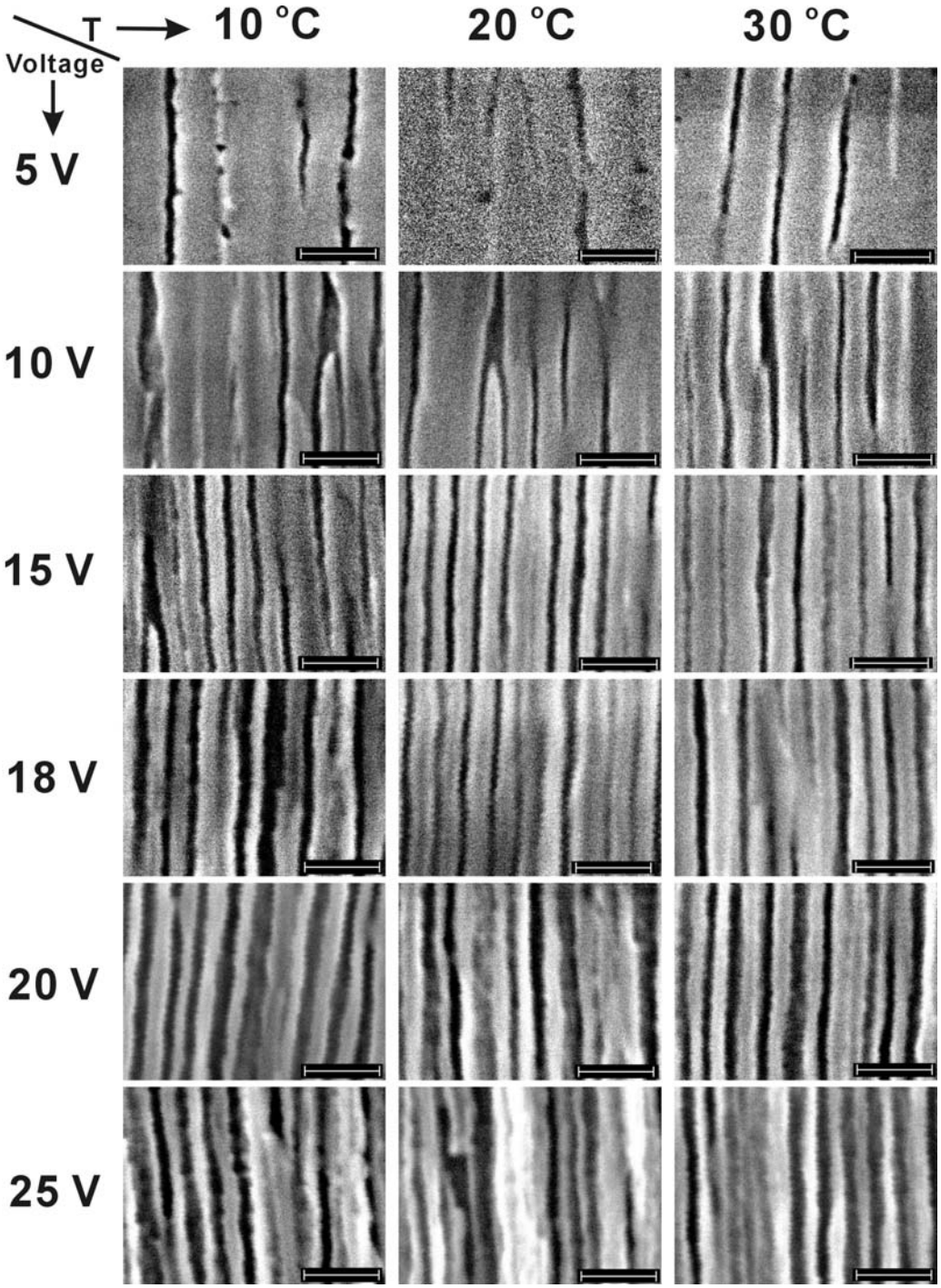

Figure 3.17 Cross sectional SEM images of formed columnar porous structure. The scale bar indicates 100nm on all SEM images. Each column show the structures formed at the specified temperature. Each row shows the porous structures fabricated under the indicated voltage fixed.

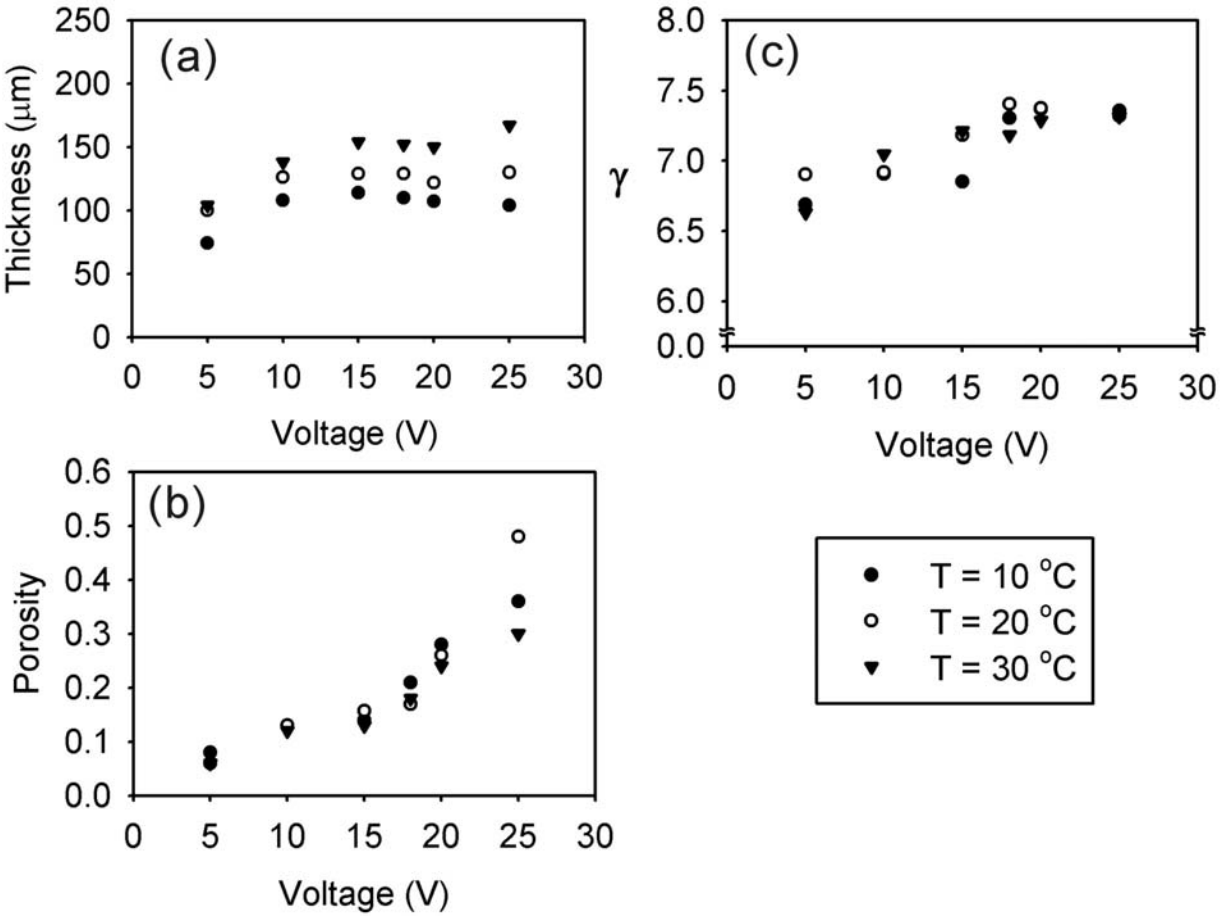

Figure 3.18 (a) Porous layer thickness, (b) porosity and (c) γ for the porous structure etched under different voltages and temperatures. The material used here is C-face on-axis n-type 6H SiC doped at 2.4×10^{18} cm^{-3}. The electrolyte used is aqueous 10% HF and 5% ethanol electrolyte (weight percentage). The UV illumination is set at 600 mW/cm^2. The etching time is fixed at 30 minutes.

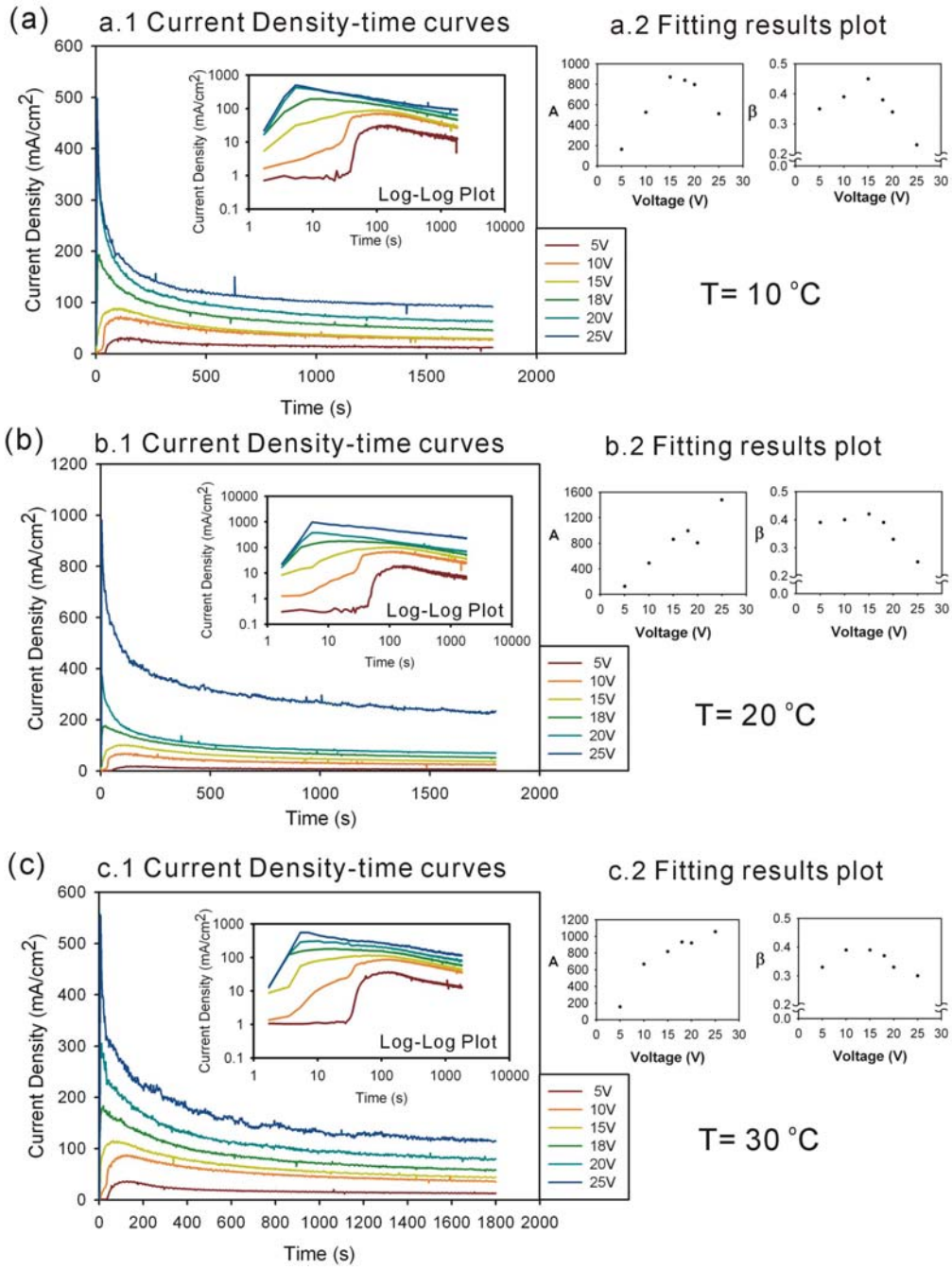

Figure 3.19 (1) Current density vs. time curves recorded and (2) the plots of fit parameters A and β are shown for the temperatures (a.1) 10 ^{o}C, (b.1) 20 ^{o}C and (c.1) 30 ^{o}C. The double log plots are shown as insets in the linear plots of the current density curves. From bottom to top in each current density plot, the corresponded etching voltage is 5, 10, 15, 18, 20 and 25 V.

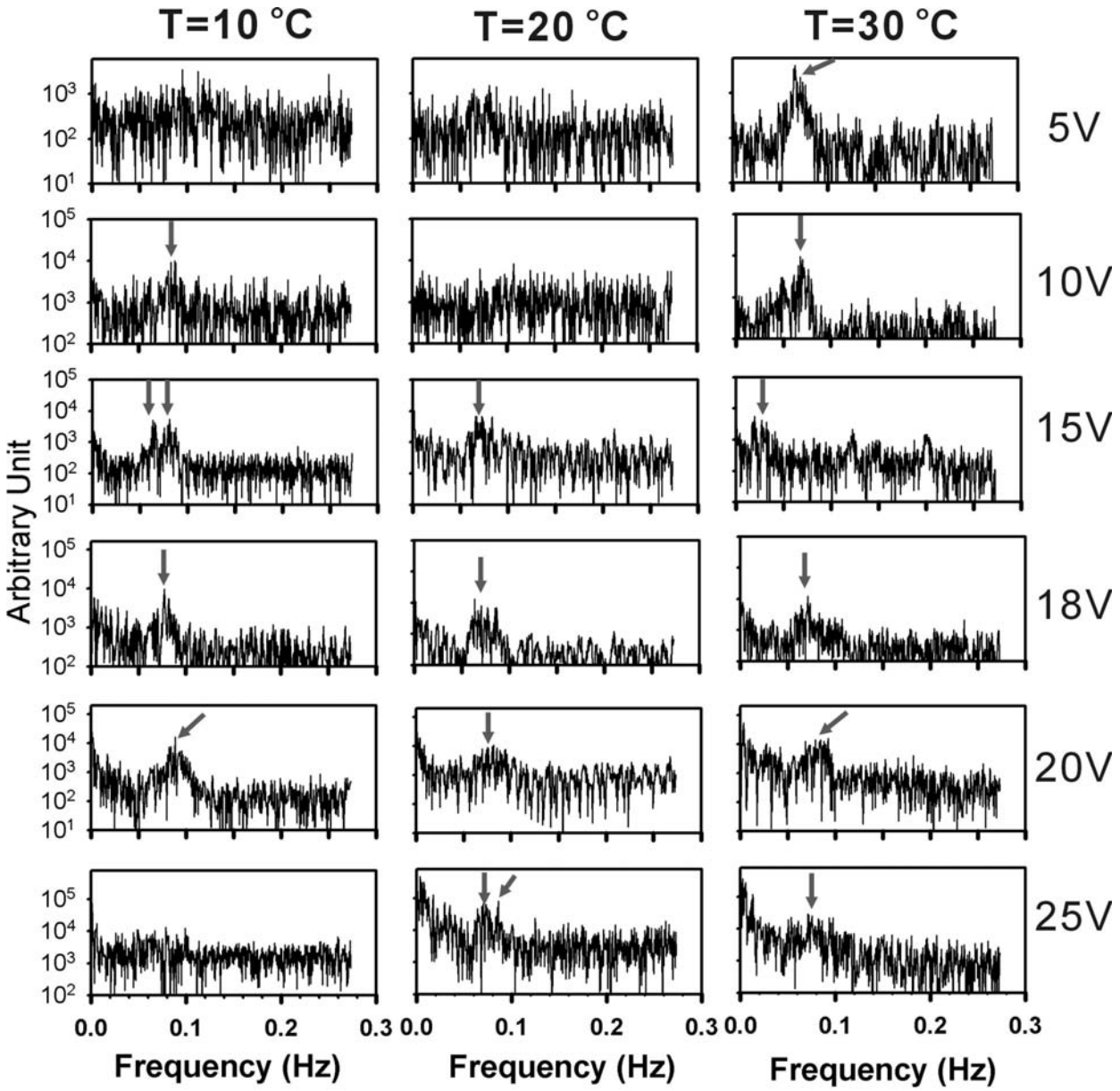

Figure 3.20 Power spectrum plots of the FFT to the current density oscillations recorded in each experiment. The experiments performed at the same temperature are listed in the same column. Those etched with the same voltage are placed in the same row. The y-axis of each power spectrum plot is on log scale and the peak is indicated with an arrow.

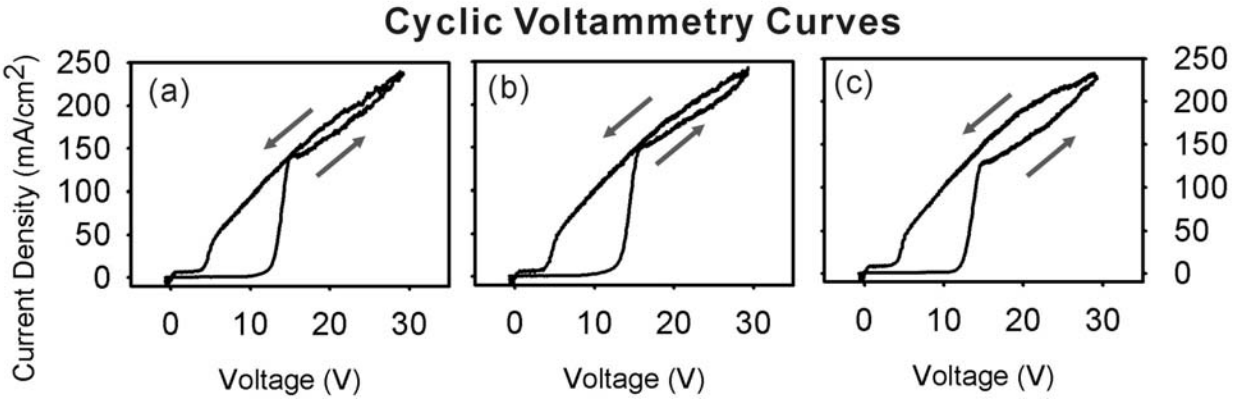

Figure 3.21 Cyclic voltammetry experiments performed at the temperature of (a) 10 ^{o}C, (b) 20 ^{o}C and (c) 30 ^{o}C with 600 mW/cm^2 UV illumination in aqueous electrolyte containing 10% HF and 5% ethanol. The scan starts at about 0 V. The voltage scan direction is indicated by the arrows in each plot. The scan rate is 0.5 V/s. We believe the hysteresis is due to the actual pore formation during the rising part of the scan.

The experimental results in Figure 3.18 show that, although the electrolytic solution temperature does not influence the columnar pore morphology under fixed applied etching voltage, the temperature does affect the etching rate. A higher reaction temperature results in a larger porous layer thickness for a fixed etching time. The temperature does not significantly affect the porosity of the structure, nor the number of holes needed for etching away a SiC pair. It seems that the porosity and γ are mainly determined by the voltage applied. γ varies between 6.5 and 7.5.

The current density-time curves (Figure 3.19) all show a section of power law decay after the initial etching period (first 100 seconds). The fit results for parameters A and β (Eq. 3.4) show different behavior at different temperatures. When T =10 ^{o}C, both A and β peak at about 15 V, and the resulting columnar porous structure is the best. If the temperature is raised up to 20 or 30 ^{o}C, parameter A increases with the applied voltage. The parameter β, however, peaks at 15V,

at which voltage the best columnar pore morphology is obtained. It seems that the most uniform columnar pore morphology has the fastest decay with the decay constant at about 0.4. The decay rate is associated with the applied voltage. The columnar pore formation is related to the fastest kinetic process while the current decay is the largest. This 0.4 decay will be discussed in Section 3.8.7.

Current oscillations are observed and varying with temperature. At 10 ^{o}C, the periodic oscillations occur from 10 V to 20 V, but not above or below. For 20 ^{o}C etching, the periodic current oscillations appear from at 15 V up to the highest voltage used (25V). If the etching temperature is 30 ^{o}C, it appears that all the current curves contain a periodic oscillation behavior. After the FFT, all the power spectra (Figure 3.20) are very noisy. On a log-log plot, the peak is not very obvious, and some spectra show multiple peaks. For most of the oscillations, the period is about same and the characteristic frequency is about 0.6-0.7 Hz. The corresponding period is about 15 seconds.

The current-voltage scans at different temperatures show a hysteresis effect. The rising part of the current density shows several turning points. An abrupt onset appears at 12 V. There is a change in slope at about 15 V. The different current-voltage behavior very often suggests that the different change exchange mechanism. The voltage at which the kink appears is the voltage corresponding to the best nano columnar porous structure. The decreasing part of the current voltage curve shows an approximately linear decay with a larger current density than the scan with increasing voltage. The mechanism underlying this cyclic voltammetry behavior is not understood.

Finally, to check the reproducibility of the above experiments, three experiments have been repeated at 15V for 20 ^{o}C etching. The results are listed below. It shows that the experiments are reasonably repeatable.

Average porous thickness (μm)	Thickness deviation	Average porosity	Porosity deviation	Average γ	Deviation of γ
129±3	±2.3%	0.16±0.006	±3.6%	7.18±0.16	±2.2%

Table 3.3 The average experiment results and the error of the three experiments repeated at 15V, 20 ^{o}C.

These experiments show that the temperature variation here does not influence the nano-columnar pore formation in any obvious manner. The increasing of the temperature will cause a faster pore formation. The pore diameter variation and porosity increase is observed but not clear. The experiments found that the nano-columnar pore formation is very reproducible if the temperature is controlled. We believe that the current oscillation does not depend on the voltage. This will invalidate the current burst model proposed for the porous Si formation to explain the case of porous SiC.

3.6 THE HF CONCENTRATION EFFECT ON NANOCOLUMNAR PORE FORMATION IN 4H SILICON CARBIDE

Having studied the effects of voltage and temperature on the nano columnar pore formation, in the preceding section, we now turn to understand the HF concentration effect on the columnar pore formation. The goal is to find the experimental conditions that can produce a columnar pore

structure with long range order. It is also hoped that the pore diameter could be varied without destroying the uniformity of the columnar pore lattice.

The experiment is designed so that the temperature is set at 20 ^{o}C. The SiC material used in this systematic research is C-face on axis 4H SiC doped n-type at 1×10^{18} cm^{-3}. The electrolyte is aqueous HF solution containing 5% ethanol (weight percentage). The HF concentrations tested are 1%, 2%, 5%, 10% and 30% (weight percentage). The selected voltages are 20, 40, 60 and 80 V. UV illumination is fixed at 600 mW/cm^2. To check the reproducibility of the experiments, the experiments with 10% HF solution were repeated three times. A total of 28 experiments have been performed in this systematic study. The experimental results for porous layer thickness, porosity and γ are summarized in Figure 3.22. The current vs. time curves recorded in the experiments are plotted in Figure 3.23. SEM images are shown in Figure 3.24 to Figure 3.28.

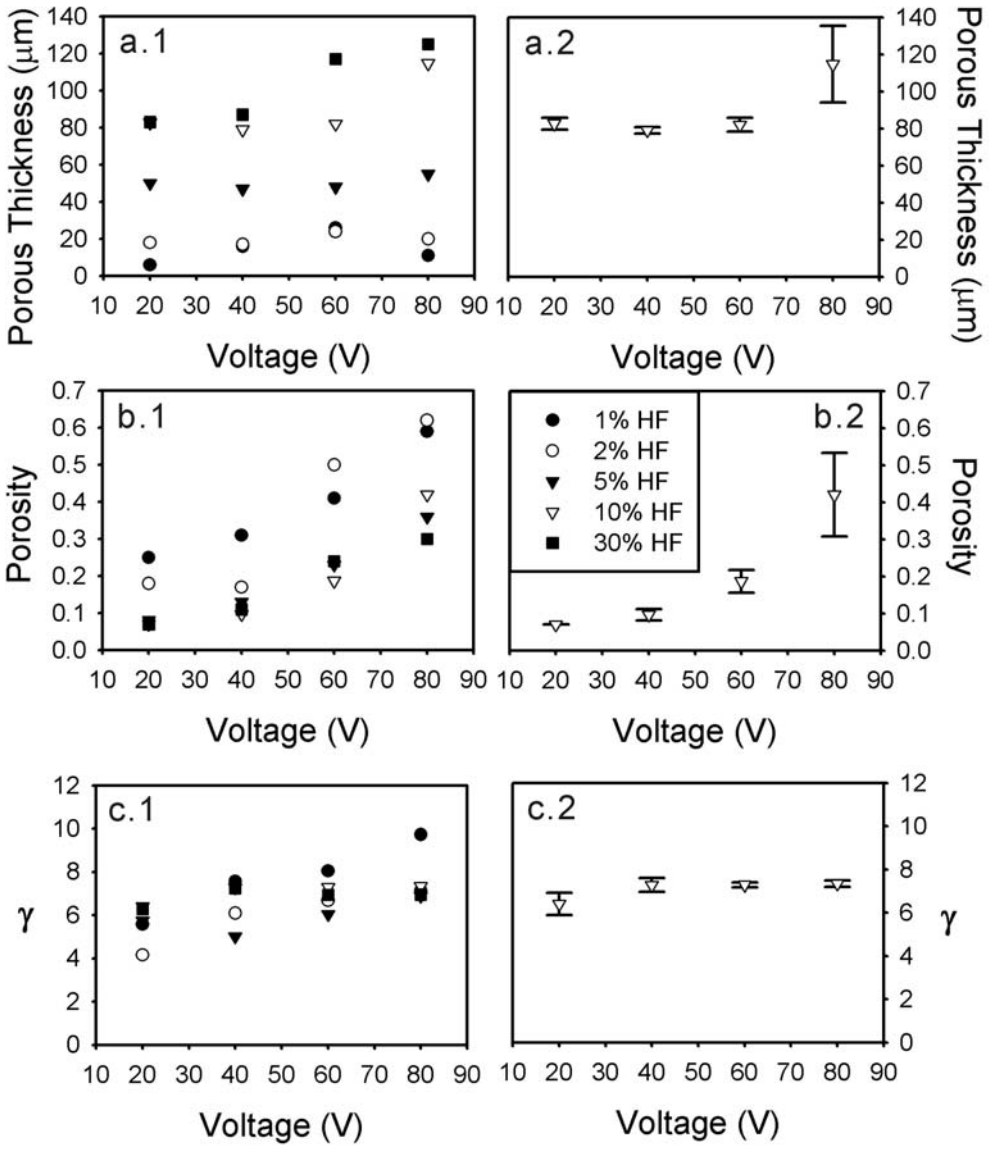

Figure 3.22 The (a) porous layer thickness, (b) porosity and (c) γ of formed PSC structure. The left column contains the plots for all the HF concentrations. Note that the 10% HF data are the average values from the three runs. In the right column are the plots for the 10% HF electrolyte. The error bars indicate the reproducibility of the experimental results. The inset in b.2 serves as the legend for all six panels.

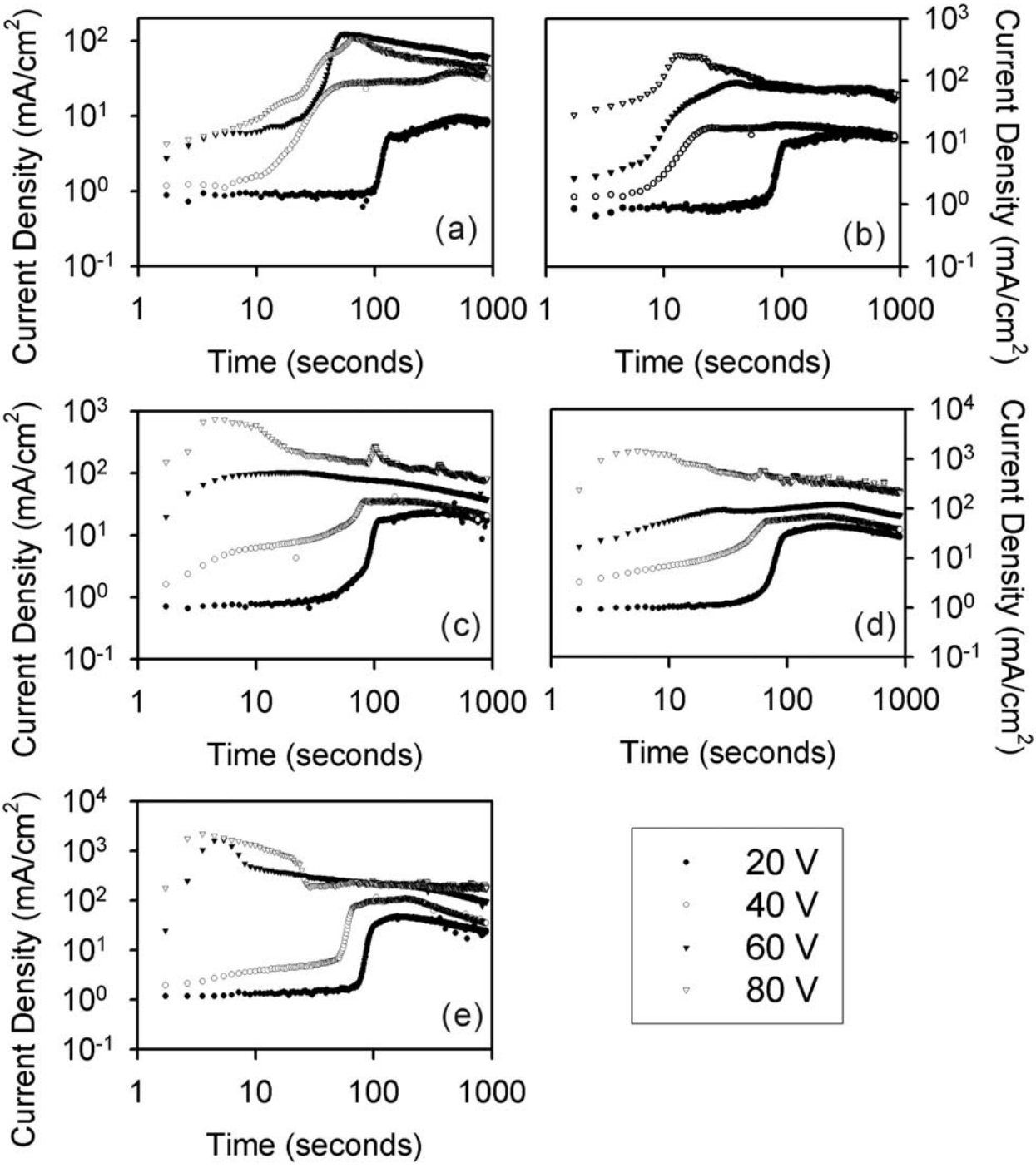

Figure 3.23 The current density vs. time curves recorded during the etching in (a) 1%, (b) 2%, (c) 5%, (d) 10% and (e) 30% HF aqueous electrolytic solution mixed with 5% ethanol (weight percentage). All the experiments are performed at 20 ^{o}C with ± 0.2 ^{o}C tolerance.

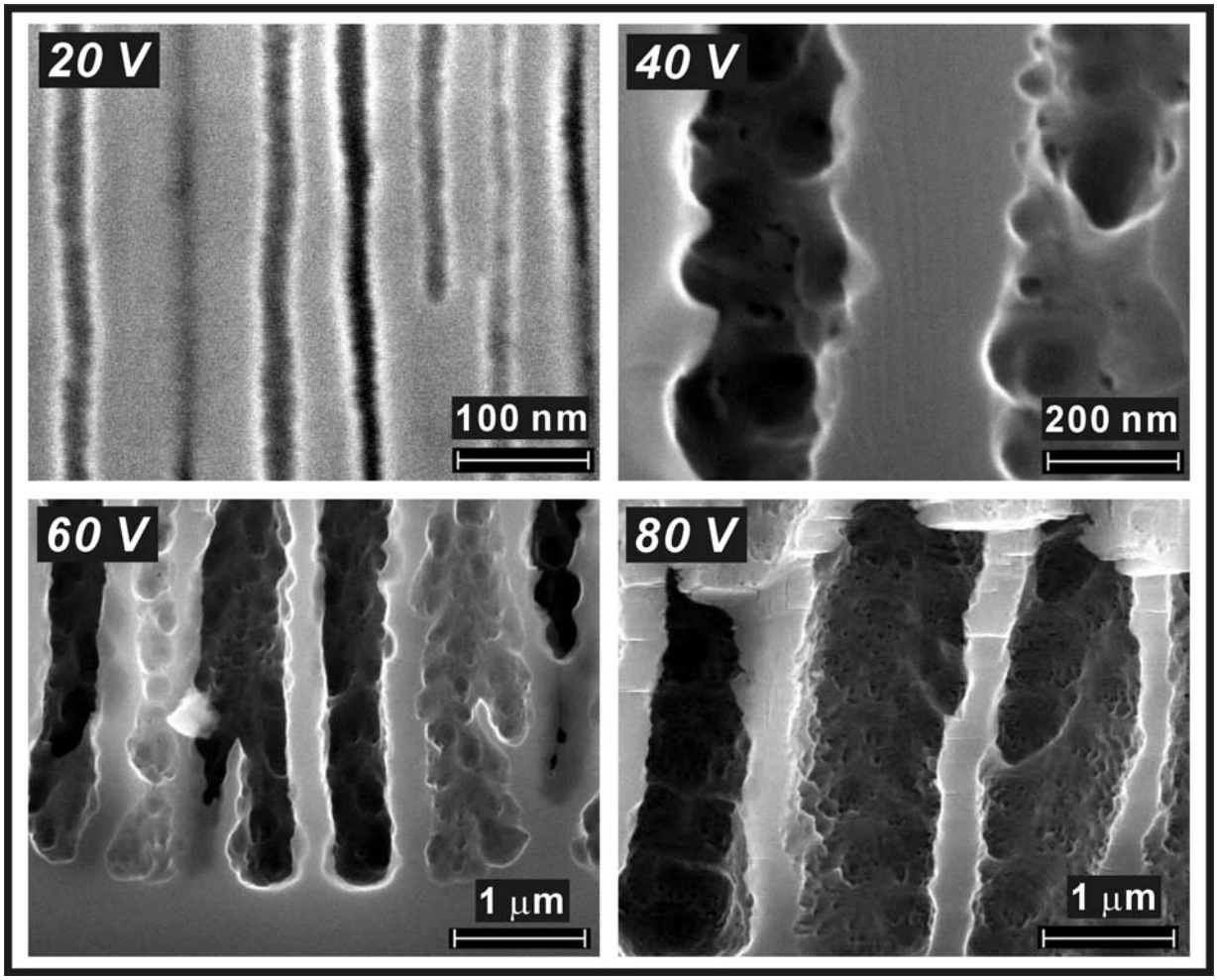

Figure 3.24 Formed pore structure under four different voltages in 1% HF and 5% ethanol electrolytic solution. (Please note the different scales in the cross sectional SEM images)

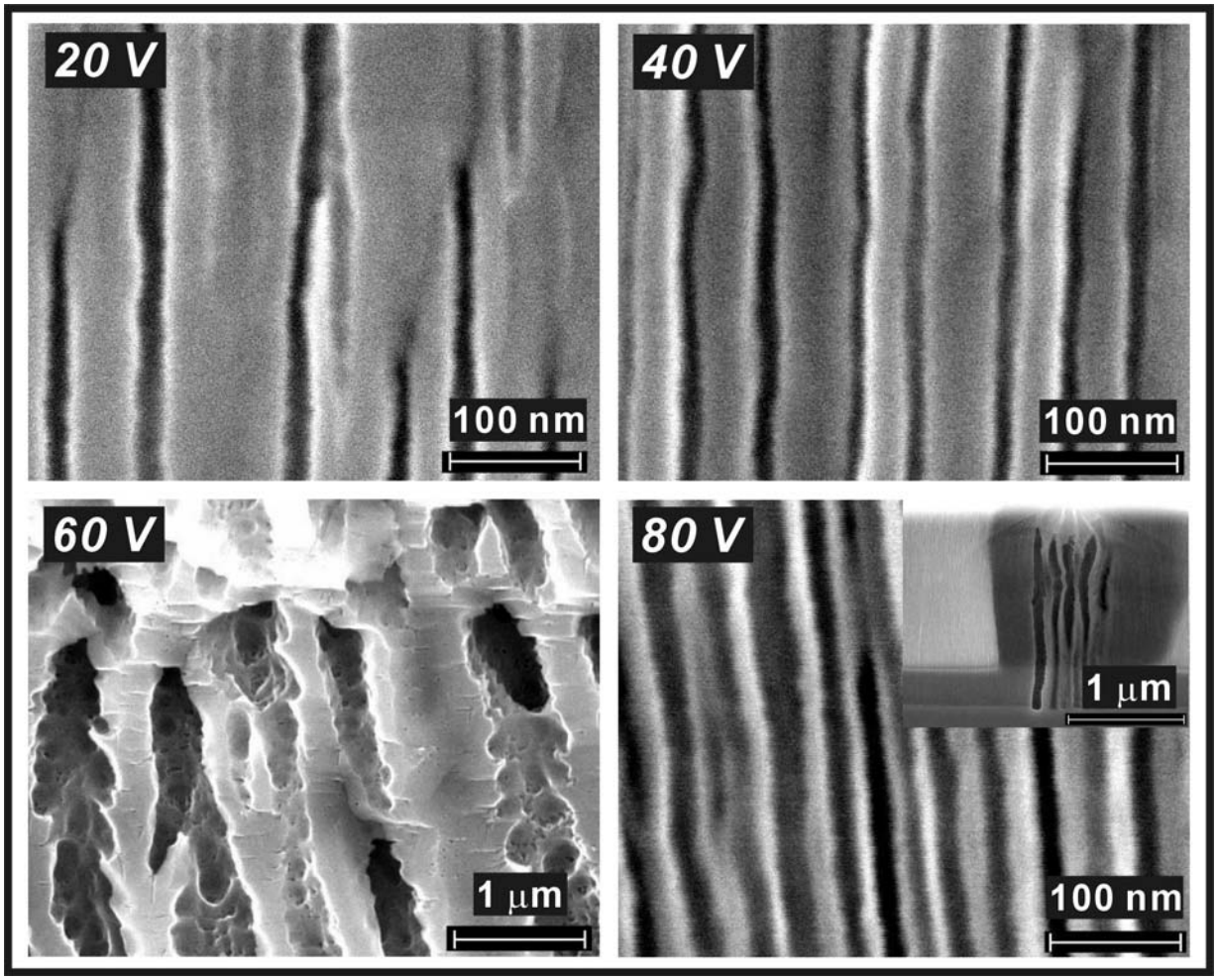

Figure 3.25 Formed pore structure under four different voltages in 2% HF and 5% ethanol electrolytic solution. (Please note the different scales in the cross sectional SEM images) The inset in the 80 V image shows the simultaneous micron diameter columnar pore growth in the cross section.

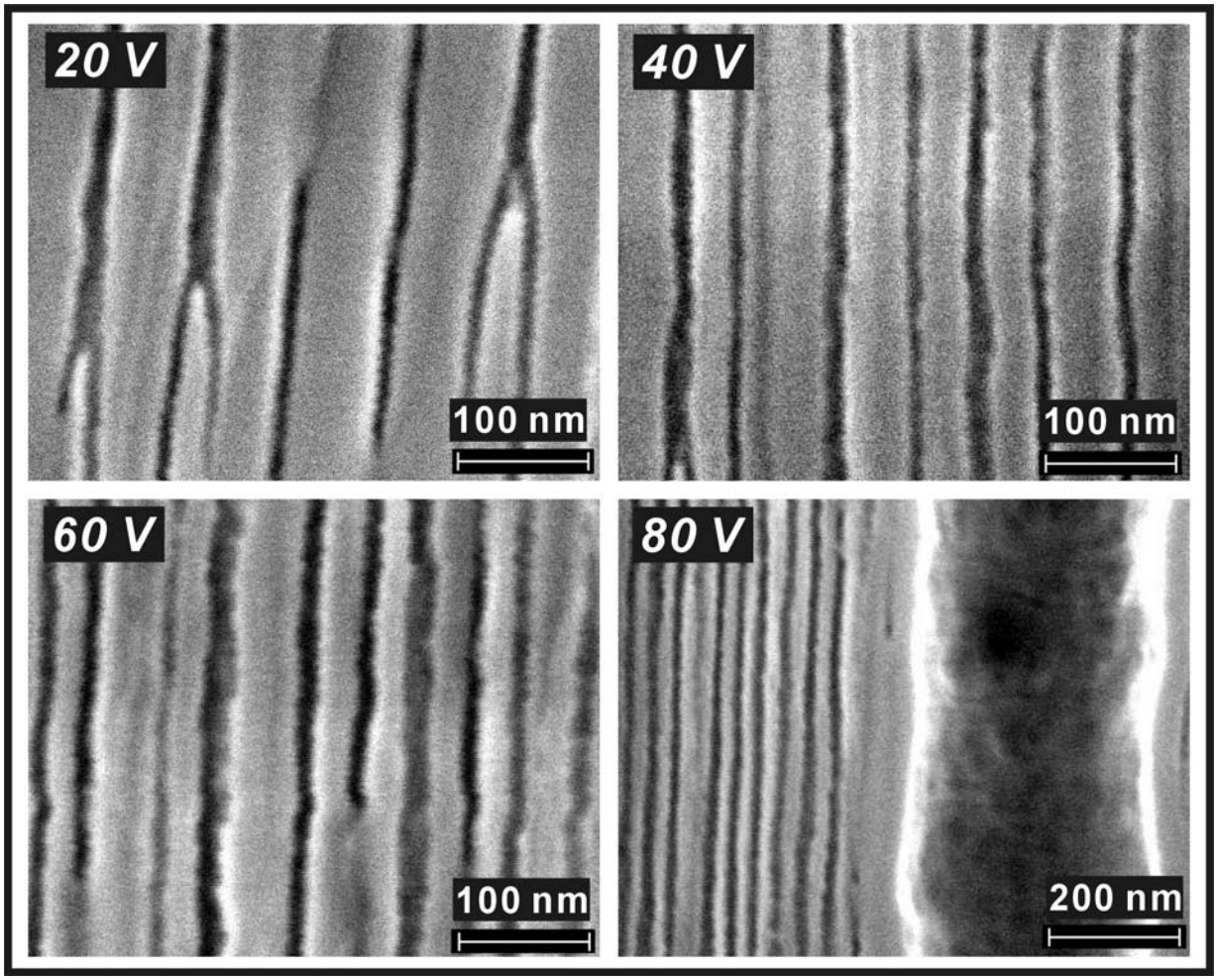

Figure 3.26 Formed pore structure under four different voltages in 5% HF and 5% ethanol electrolytic solution. (Please note the different scales in the cross sectional SEM images)

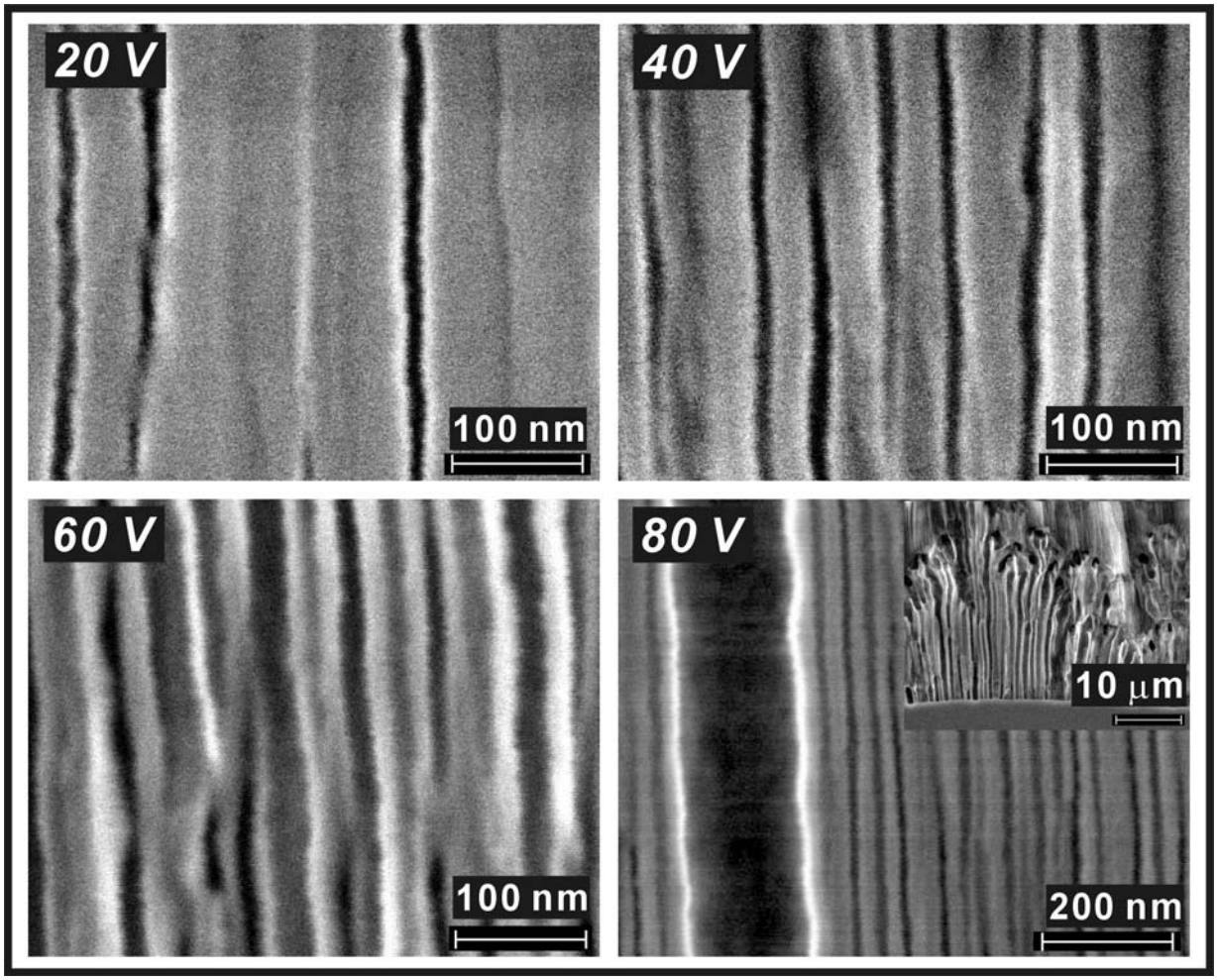

Figure 3.27 Formed pore structure under four different voltages in 10% HF and 5% ethanol electrolytic solution. (Please note the different scales in the cross sectional SEM images) The inset in 80 V images is the cross sectional SEM image of a much larger area, which suggests a very unstable, chaotic pore growth.

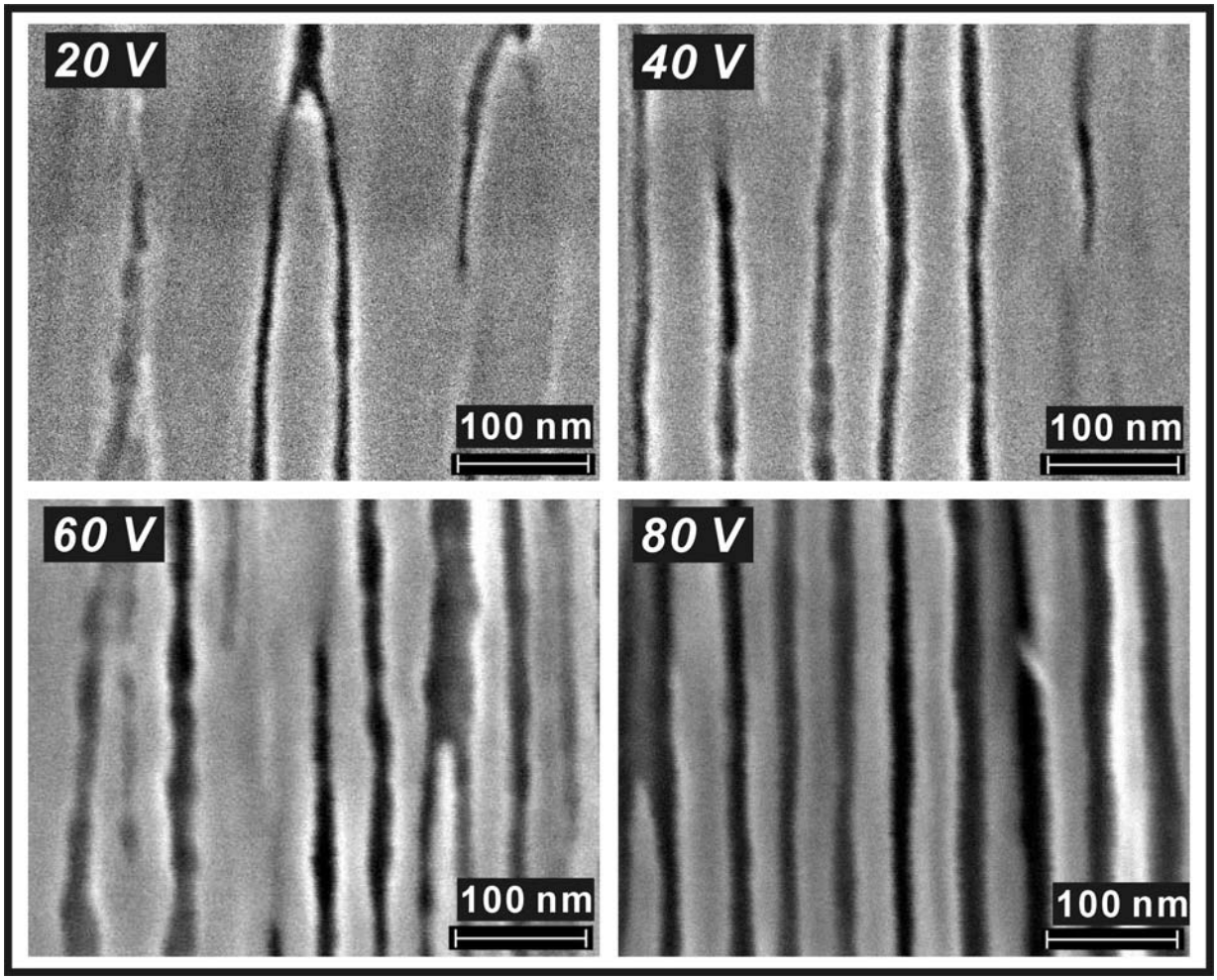

Figure 3.28 Formed pore structure under four different voltages in 30% HF and 5% ethanol electrolytic solution. (Please note the different scales in the cross sectional SEM images)

These results show that the HF concentration has a substantial effect on the columnar pore formation in all respects, including (1) porous layer thickness, (2) porosity, (3) value of γ, (4) magnitude and shape of the current-time curve and (5) pore morphology.

(1) Porous layer thickness:

A lower concentration of HF will slow down the porous layer thickness growth rate. For 1% and 2% HF, the growth rates are similar. For HF concentrations higher than 10%, the growth rate of the porous layer is much higher. For 15 minute etching, the formed porous structure is roughly 4-5 times thicker than the structure fabricated in 1% or 2% HF under the same etching votlage. This growth rate appears to saturate at about 10% HF concentration. There is no obvious difference in pore morphology observed for the etching in 10% and 30% HF. The etching rate in 5% HF is an intermediate case. There appears to be a rapid transition region around 5% HF concentration where the growth rate changes rapidly with HF concentration. When the concentration is relatively low (< 2%) or high (> 10% for what's observed in this set of experiments), the growth rate is roughly independent of the HF concentration.

(2) Porosity:

The porosity dependence on the applied etching voltage is shown in Figure 3.22b. This dependence is in agreement with our previous experiments. The porosity, however, is also influenced by the HF concentration that is used in the etching. Generally speaking, lower concentration HF will produce a higher porosity porous structure, while a higher concentration of HF can reduce the porosity substantially. For HF concentrations larger than 5%, the porosity dependence on HF concentration is not large. The HF concentration effect on the porosity is mainly in the low concentration region.

(3) Value of γ:

For all the experiments, the value of γ clearly rises with the applied voltage. It is observed that most of γ are around 7 and some of them deviate from 7 but locate between 4 and 10. For the electrochemical reactions suggested (see section 3.8.2), these numbers are reasonable. It is also seen that for lower HF concentration, the variation of γ larger. The experiments in higher HF concentration electrolyte show less dependence of γ on the etching voltage. This suggest that chemically, higher concentration HF ensures a more consistent and stable chemical process, while lower concentration of HF will cause unstable chemical process simple because kinetically, the dissolution of SiO_2 by HF in solution can no longer keep up with the electrochemical reaction.

(4) Current density – time curves:

It is observed that lower concentration HF solution will result in a lower current density during the reaction under the same etching voltage. The resistivity of the aqueous HF electrolytic solution in various HF concentrations at 25 ^{o}C is listed below.

[HF]	1%	3%	5%	10%	20%	30%
Resistivity (Ohm-cm)	85.5	28.8	16.1	8.5	4.3	2.6

Table 3.4 Aqueous HF solution resistivity for different HF concentration in weight percentage.[61]

An estimation of the resistance of the cell during the reaction can be done dividing the applied voltage by the drawn current. In a typical reaction (see section 3.2.2), the current is about 20-30 mA/cm^2 at 20 V The estimated resistance of the cell is therefore around 1 kΩ at 20V. Therefore, for the low voltage etching processes, the change in the resistance of the solution is

comparatively small compared to the total system resistance. The magnitude of the current density therefore should have very little dependence on the HF concentration.

For higher voltage, such as 80 V in this study, the resistance of the cell system decreases to about 800 Ω (Figure 3.23, $R = \frac{V}{I}$) during the later stage (t > 500 s). This value is about the same for all HF concentrations tested. It seems that the HF concentration has little effect on the late stage current density drawn in the electrochemical cell. The maximum current density at the beginning of the etching, however, depends on the concentration of HF. For more concentrated HF solution, the maximum current density value is larger. This is probably due to both the resistivity decrease of the HF solution and the increase of the reaction rate when the HF is more concentrated and becomes more available (The discussion may be oversimplified due to the fact that HF is a complicated acid. See the reference) [62, 63].

It is also observed that the long-time current density decay depends mainly on the etching voltage used. The decay behavior has very little relationships to the HF solution used. For different formed pore morphologies, the current decay rate during the etching process is also different. A smooth power low decay is in general commonly seen for the uniform columnar pore growth.

(5) Pore morphology:

Cross sectional SEM images from Figure 3.24 to Figure 3.28 show the pore morphologies formed in different HF concentrations under various etching voltages. The results prove that the voltage is the decisive etching conditions to fabricate columnar porous structure. For lower applied voltage, it seems that in the HF concentration range from 2% to at least 10%,

the formed pore morphologies are similar. Different pore morphologies appear when the HF concentration is at 1% (lowest) and 30% (highest).

In 1% HF electrolyte, the average pore diameter is much larger than for the pores formed using higher concentration HF. For 40 V etching, the formed columnar pores have a diameter of about 200 nm. Rough pore walls can be observed. Higher voltage increases the diameter of the pores. At the voltage of 80 V, the formed columnar pores are about 1 μm in diameter. in contrast to 1% HF, 30% HF solution (Figure 3.28) however eliminates the occurrence of any large size (>50 nm) pore growth for the above voltage range, although in 80V pore growth, the pore diameter and density do increase. No micron size columnar pores, however, have been observed in the structure, in contrast to what happens for the lower concentration HF etching.

It should also be pointed out that the experiments with 10% HF for each set voltage have been repeated three times. The results show that for the voltage lower than 60 volts, the deviation of measured parameters such as the porous layer thickness and porosity is well within 5%. Considering the experimental error we have in the experiments, the results are considered reproducible. When high voltage is applied, such as 80 V in this set of experiments, the results start to diverge. The deviation could be as big as 25%. This is caused by the instability of the electrochemical process due to any minor change in the material doping, defects, etc.

The above experiments show that HF concentration can alter the pore diameter and etching rate. These results point out that the columnar pore growth is a kinetic process. The reaction rate depends on the HF concentration, and the magnitude of the etching voltage. The voltage would likely determine charge exchange rate at the interface and how fast the ions drift in the solution. The HF concentration decides how fast the reaction product will be removed. The

two variables compete with each other and therefore change the pore diameter and porosity of the formed porous structure.

3.7 DOPING DEPENDENCE OF NANO-COLUMNAR PORE GROWTH IN N-TYPE 4H AND 6H SILICON CARBIDE

After the systematic experiments on the voltage, surface nucleation, temperature and HF concentration effects, the effect of n-type SiC doping on the columnar pore formation is studied. This work is challenging due to the difficulty and the cost of obtaining n-type SiC wafers covering a wide range of dopings. The following data are essentially a summary of the columnar pore formation covering the doping range of the SiC crystals we have used.

It is always true that for a certain doping, there is an optimum voltage for the uniform columnar pore growth in 5% or 10% HF concentration electrolyte, independent of the temperature and surface condition. However, there is no simple relation that has been found between this voltage and the doping. For n-type SiC, there is a correlation between the material doping and material resistivity. The equations that relate the doping to the resistivity obtained by fitting the CREE data tables are as follows:

For 6H SiC:

$$\log(N_D - N_A) = 16.08 - 1.83 \cdot \log \rho \quad \textbf{3.5}$$

For 4H SiC:

$$\log(N_D - N_A) = 16.07 - 1.63 \cdot \log \rho \quad \textbf{3.6}$$

In the above equations, N_D-N_A is the doping of the material in cm^{-3}. ρ is the resistivity of the material in Ω·cm.

We thus plot the optimum voltage against the resistivity of the material on a log scale for 6H SiC in Figure 3.29.

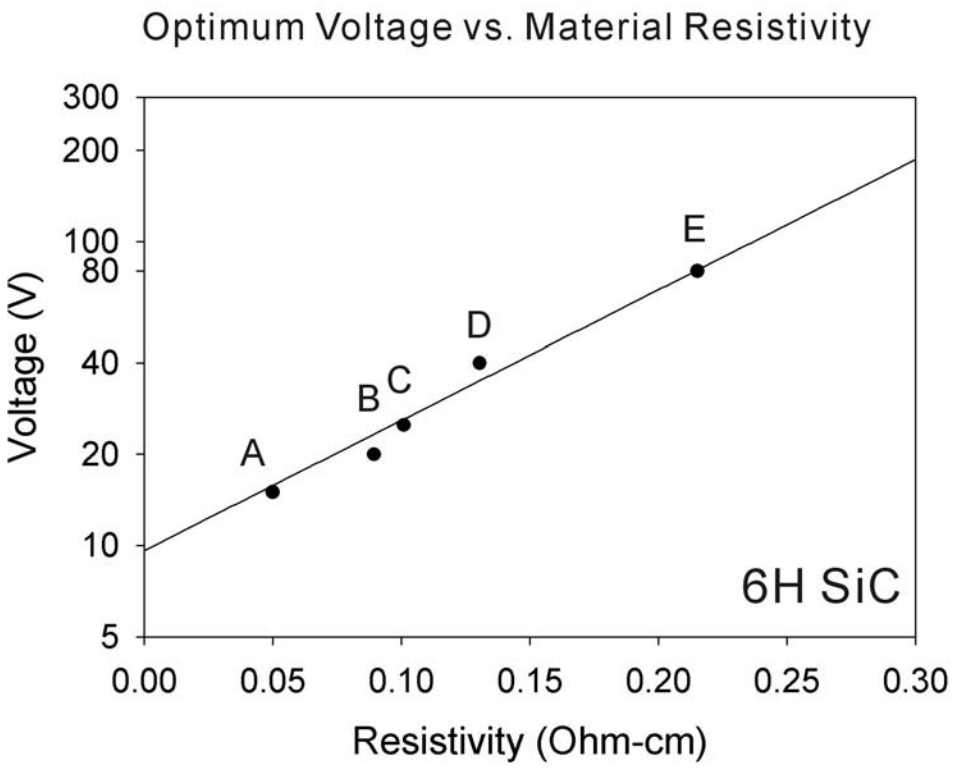

Figure 3.29 The relation of optimum voltage for nanocolumnar pore growth and the 6H SiC resistivity. The plot is on a single log scale. The corresponding doping for each data point is: (A) 2.4×10^{18} cm^{-3}, (B) 1×10^{18} cm^{-3}, (C) 8×10^{17} cm^{-3}, (D) 5×10^{17} cm^{-3}, (E) 2×10^{17} cm^{-3}. The line in the plot is the result from a fitting, which is describe in the text.

It is found that on a single log scale the voltage points roughly follow a straight line. This suggests that the data points could be fit to a simple relation,

$$V = ae^{b\rho}, \quad \textbf{3.7}$$

where V is the optimum voltage (V), ρ stands for the resistivity (Ω·cm), and a and b are the fitting parameters. The fitting results are listed in Table 3.5:

Parameter	Value	Standard Error	Percentage Error
a (V)	9.64	1.35	13.99%
b ($\Omega^{-1}\cdot cm^{-1}$)	9.88	0.73	7.44%

Table 3.5 Fitting results for the optimum voltages in n-type 6H SiC nano-columnar porous etching.

This fitting result in Table 3.5 shows that for different doped 6H SiC, the optimum voltage which will lead to a uniform nano columnar pore growth could be estimated. The theoretical minimum voltage (parameter a) is about 10 V. For highly doped material ($n > 1\times10^{18}$ cm^{-3}), the voltage window (the voltage deviation that is allowed from the optimum predicted by the fitting) that will allow a good nanocolumnar porous etching is much narrower for low doped material. Of course, any extrapolated prediction, which is beyond the range of the experimental data points, is not reliable and needs to be confirmed by further experiments.

For n-type 4H SiC, there are only two different material dopings we have tried 1×10^{18} cm^{-3} and 5×10^{17} cm^{-3}. There are simply not enough data points to do any data fitting as above for 6H SiC. However, it is observed that for the same doping at 1×10^{18} cm^{-3}, the voltage that is required for nano columnar pore growth is about 45V, and is much higher than the voltage needed for 6H SiC etching, which is about 20 V. For the same doping, the 4H material has a lower resistivity and is more conductive. The reason for this voltage difference is not clear. If we speculate that the optimum voltage vs. different doping is similar in 4H SiC and 6H SiC, we can

do a fitting using the same expression Eq.4.7. The results are $a = 12.9\ V; b = 13.99\ (\Omega \cdot cm)^{-1}$. These results are of course very qualitative because we only have two data points for the fitting.

Figure 3.30 presents the SEM images of the actual nano-columnar porous structures formed at the optimum voltages in various doped C-face 6H SiC. The experiments show that despite the dramatically increased optimum voltage needed to form nano-columnar porous structure, the nano-columnar pores that are formed are of similar pore diameter. The fact that doping of the SiC cannot alter the pore diameter will be very important for our model discussion.

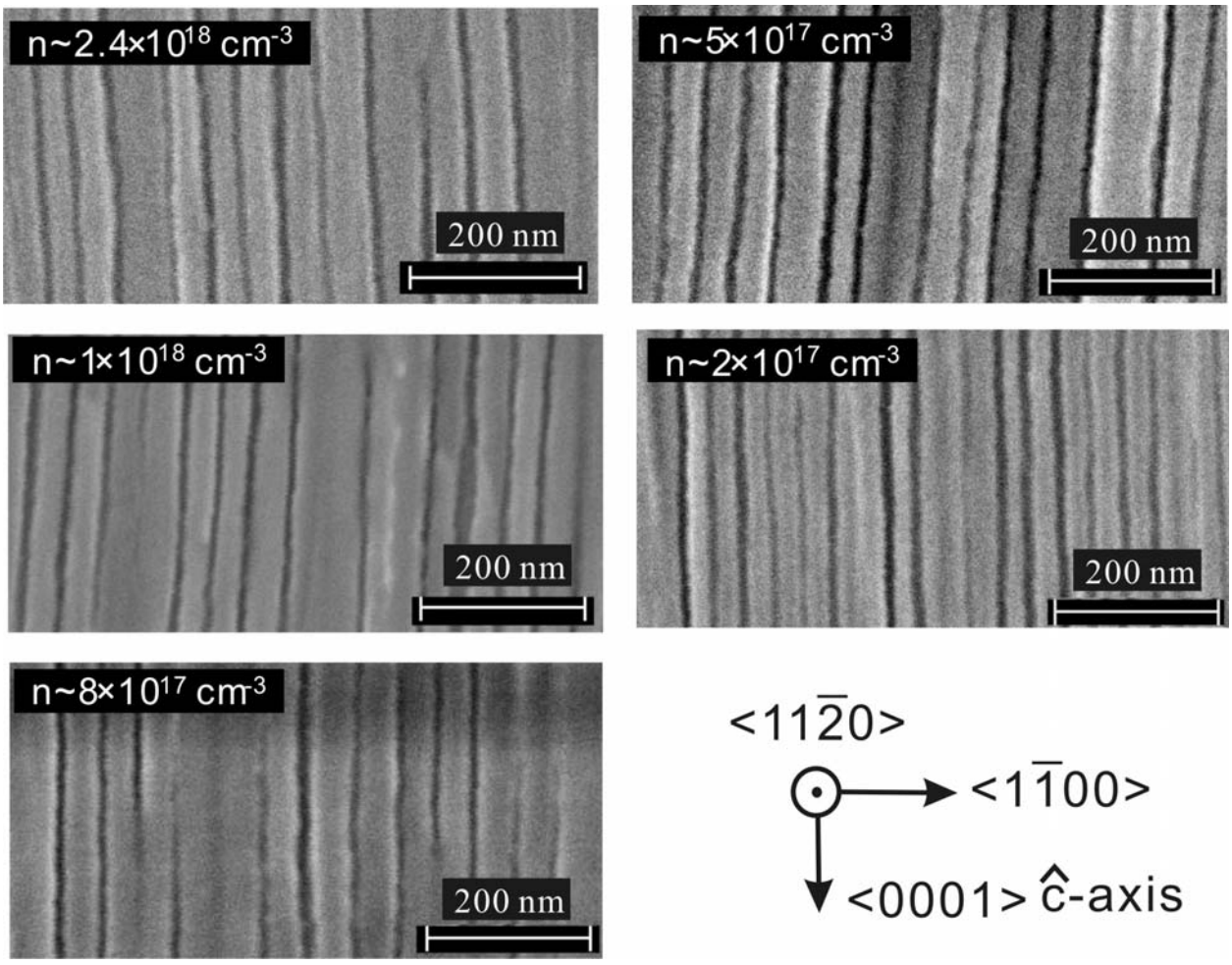

Figure 3.30 The cross sectional SEM images of the nano-columnar porous structure formed in different doped C-face n-type 6H SiC.

3.8 SUMMARY OF EXPERIMENT OBSERVATIONS

We list the important experiment results as follows:

(1) To form a nano-columnar porous structure in C-face SiC, an optimum voltage needs to be applied. (Section 3.2 and 3.3)

(2) The optimum voltage increases with the resistivity of the SiC material. The formed nano-columnar pore morphologies, however, are independent of the doping. The columnar pores are always around 20±5 nm diameter. The interpore spacing is about 40-60 nm. (Section 3.7)

(3) Surface conditions do not influence the columnar pore formation, which suggests that the surface patterning will neither improve nor change the nano-columnar formation process. (Section 3.4)

(4) Temperature will not influence the nano-columnar pore diameter in any obvious way. The higher temperature only increases the pore growth rate. The rate change is related to the faster reaction rate at higher temperature. (Section 3.5)

(5) The oscillation of the current during the pore formation is associated with the surface roughness and shows a unique frequency at about 0.6 Hz (Section 3.4). It is also found that the current oscillation at controlled temperature does not change with different voltages. This invalidates the application of current burst model to explain the porous SiC formation. (Section 3.5)

(6) HF concentration will change the columnar pore diameter and growth rate. This is related to the complicated HF chemistry which will change the oxide

removal rate during the columnar pore formation. We believe at low concentration of HF, the pore growth is determined by the oxide removal rate by HF. In the cases of using high concentration of HF, the pore growth is determined by the charge transfer across the interface. The later one is the case we obtain the nano-columnar porous structure. In another word, to obtain nano-columnar porous structure, we ought to use an appropriately concentrated (2%-10%) HF electrolytic solution. (Section 3.6)

(7) It is observed that the current decay occurs during every porous formation process. When the nano-columnar pore forms, the exponent of the power lay decay relation is about 0.4. This is not a sufficient condition, which means that during some of the porous SiC formations, we observe ~0.4 exponent power law current decays but the final pore morphology is not nano-columnar. (Section 3.2-3.6)

(8) It is also shown that values of γ (average number of holes needed to remove a SiC atom pair) can change greatly. However, in the highly concentrated HF, the values are about 7, especially during the nano-columnar pore formation. We will use this information to discuss the possible chemical reaction that happens during the nano-columnar pore formation. (Section 3.2-3.6)

(9) The nano-columnar pore formation is a reproducible process (Section 3.5-3.6). At larger voltages, the etching process becomes unstable and gives a large variation of experiment results. (Section 3.6)

The experimental observations reveal an interesting fact that in aqueous HF solution no matter how we change the experimental conditions, such as doping of the sample, etching voltages, polytype of the material, surface conditions, reaction temperature, and HF concentration, the resulting nano-columnar pore lattice remains the same (20±5 nm), if you ever obtain one. The formed columnar porous structures have almost identical pore diameter and center to center interpore spacing (40-60 nm). Our enormous effort to vary the pore diameters without destroying the columnar pore lattice remains fruitless so far.

In the following subsections, we will discuss charge transfer mechanism during the nano-columnar pore formation, which is mainly based on the above experimental observations. Some supplemental experiments will also be discussed as needed.

3.9 A SIMPLIFIED INTRODUCTION TO THE SEMICONDUCTOR ELECTROCHEMISTRY

The study of an electrochemical system inevitably involves the understanding of the properties of the solid (metal, insulator, and semiconductor) electrode, solution and their interface. This section tries to explain the necessary basic electrochemistry that is useful to our discussion. We will focus on introducing the important concepts briefly without extensive explanations. The material follows that given in a book written by S. Morrison[29] in much greater detail, although similar material can also be found in other semiconductor electrochemistry books.[30,31]

For any electrochemical process, current flow between a solid that conducts by electrons and an electrolyte that conducts by ions always implies a chemical reaction at the interface. To

etch any SiC electrochemically, an anodic reaction is desired. In order that anodic current can flow, electrons have to be injected, or holes captured, by a reducing agent in solution. The reducing agent is oxidized in these anodic processes. To understand this process, we first need to know the electron energy distribution in the solid (semiconductor in our case) and the electrolyte separately. Figure 3.31 shows the electron energy band diagram in the metal, solution and semiconductor, which will be explained below.

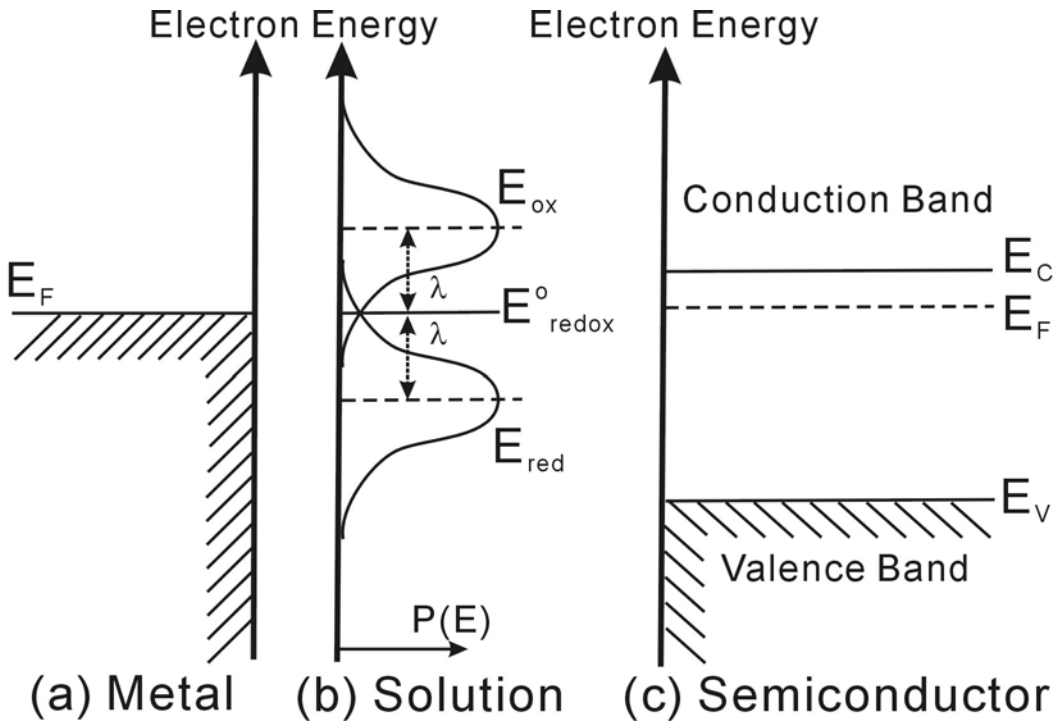

Figure 3.31 Electron energy band diagram for (a) metal, (b) solution, and (c) n-type semiconductor. E_F is the Fermi energy level. E_C and E_V are the energy band edges of the conduction and valence band. The ordinate shows the approximate positions of E_{ox} and E_{red} at equilibrium for equal concentrations of oxidizing and reducing agents. E^o_{redox} is the average energy value of the two when the concentrations are equal. P(E) is the probability that the state E_{ox} or the state E_{red} has fluctuated to the energy E. λ is the constant describing the Franck-Condon splitting of E_{ox} and E_{red} ,as explained in the text.[29]

Energy levels in metal:

For a metal electrode, the Fermi energy is located within the conduction band with a large density of states. At 0 *K*, the energy levels below the Fermi energy are filled with electrons and the levels above the Fermi level are unoccupied. The electron transfer within the metal electrode is thus simple.

Energy levels in semiconductor:

On the other hand, the Fermi level is located in the band gap for any non-degenerate semiconductor. If the material is doped with donors, the material is an n-type and E_F is shifted towards the conduction band. For a non-degenerate n-type semiconductor (E_c-E_F > *2kT*), the densities of conducting carriers can be calculated using the formulas:

$$\begin{aligned} n &= N_C \exp[-(E_C - E_F)/kT] \\ p &= N_V \exp[-(E_F - E_V)/kT] \\ np &= N_C N_V \exp[-E_g/kT] \end{aligned} \qquad \textbf{3.8}$$

Here *n* is the density of electrons in the conduction band, *p* the density of holes in the valence band. N_c is the conduction band effective density of states (usually around 10^{19} cm^{-3}) at an energy E_c. N_v is the effective density of valence band states. E_g is the energy band gap (>3 eV for 4H, 6H SiC).

From a chemical point of view, the Fermi energy E_F is the electrochemical potential of electrons in the solid. Statistically, electrons transfer from the metal or semiconductor electrode to ions in solution originate with a free energy of E_F. At equilibrium all electronically conducting materials in contact have the same electrochemical potential for electrons, so the same Fermi energy. A voltage measurement gives the Fermi energy difference between two electrodes in

solution when the system is not in equilibrium, where there is a continuous electronically conducting path between each of the electrodes and the voltmeter.

Energy levels in solution:

There are no free electrons in the solution. The electron transfer is realized via the ions/molecules. The electron energy levels in solution reflect the tendency of that species to give up or to accept an electron when the species approach the electrode. Here, we will use an energy level description rather than a chemical potential description only because we want to conveniently connect the properties of semiconductor electrodes with the properties of the solution.

For the simplest consideration, the energy level of the ion (unoccupied or occupied by an electron) will locate at E_{redox}. The subscript "redox" stands for reduced and oxidized. E_{redox} is thus the effective energy level describing the tendency of an ion to lose an electron from its reduced form (energy level E_{red}) or gain an electron to its oxidized form (energy level E_{ox}), i.e. the "Fermi energy" E_F in the solution for the specific ions.

It is found that in solution, the energy levels E_{red} and E_{ox} corresponding to the reduced and oxidized state ion energy level do not equal each other and do not overlap at E_{redox}. E_{red} is always lower than E_{ox} with E_{redox} positioned within the energy gap. This split of E_{red} and E_{ox}, which is called Franck-Condon Splitting, is due to the energy level fluctuation of ions that is caused by the thermal fluctuation of surrounding dipoles (say water molecules) in the solution. Below, we first calculate this Franck-Condon splitting and then we calculate energy level E_{redox} accordingly.

Consider the energy ΔE_{reorg} necessary to cause fluctuations from the equilibrium polarization of the dielectric around an ion without changing the actual charge qZ (Z is the actual charge on the ion) of the ion. A parameter σ is introduced such that the polarization of the dielectric corresponds to the central charge qZ differing by $\pm q\sigma$ from the central charge actually present. In other words, in its lowest energy configuration, the dielectric medium is polarized an amount corresponding to the charge qZ on the ion. When the central charge remains qZ but the polarization fluctuates from its equilibrium configuration to a new configuration which would normally correspond to the lower energy configuration with charge $(Z\pm\sigma)q$ on the ion, the energy change due to the polarization thermal fluctuation is calculated [64,65,66] to be:

$$\begin{aligned} &\Delta E_{reorg} = \sigma^2 \lambda = (E - E_{equ})^2 / 4\lambda \\ &\lambda = (q^2 / 8\pi\varepsilon_0 a)(\kappa_{op}^{-1} - \kappa_s^{-1}) \\ &\sigma = (E_{equ} - E) / 2\lambda \\ &P(E) = (4\pi\lambda kT)^{-1/2} \exp[-\Delta E_{reorg}{}^2 / kT] \end{aligned} \qquad \textbf{3.9}$$

λ is also called the "reorganization energy". κ_{op} is the optical and κ_s is the static dielectric constant of the medium. q is the charge of electron. ε_0 is the permittivity of free space. E_{equ} is equilibrium energy of E_{ox} or E_{red}. $P(E)$ is the probability function of E_{ox} or E_{red} as illustrated in Figure 3.31b.

The Franck-Condon splitting is essentially caused by the same reorganization effect of the surrounding medium but due to the electron exchange caused charge change of the central ion. For a one electron transfer process, $\sigma = 1$. The reorganization energy ΔE_{reorg} is therefore just λ for one electron exchange. ΔE_{reorg} is always positive and therefore the additional energy needed in both reduction and oxidation reactions. If one electron is injected into the electrode from the solution at equilibrium, the total energy change is $\Delta E_1 = E_{red} - E_F + \Delta E_{reorg} = E_{red} - E_F + \lambda$.

When one electron transfers from the electrode to the solution at equilibrium, the energy change will be $\Delta E_2 = E_F - E_{ox} + \Delta E_{reorg} = E_F - E_{ox} + \lambda$. Since the summation of the total energy change in this complete reaction loop in equilibrium should be zero, we have the Franck-Condon splitting $E_{ox} - E_{red} = 2\lambda$.

E_{redox} is defined as the average electron energy in solution to describe the tendency of the electron exchange of ions, i.e., the effective Fermi level of the redox couple in solution. We here try to find out the relation between the E_{redox} and E_{ox}, E_{red}. At equilibrium, if we assume there is only one dominant redox couple, the Fermi level in the electrode equals the effect Fermi level of the redox couple in solution, and thus we have $E_F = E_{redox}$. At equilibrium, the electron transfer between the electrode and solution causes no energy change. And therefore

$$E_{red} - E_F + \Delta E_{reorg}^{red} = E_F - E_{ox} + \Delta E_{reorg}^{ox} = 0, \quad \textbf{3.10}$$

where ΔE_{reorg}^{red} and ΔE_{reorg}^{ox} are the reorganization energies during the total reduction and oxidation reactions respectively. The relation between the E_{redox} and E_{ox}, E_{red} is therefore:

$$E_{redox} = \tfrac{1}{2}(E_{ox} + E_{red}) + \tfrac{1}{2}(\Delta E_{reorg}^{ox} - \Delta E_{reorg}^{red}). \quad \textbf{3.11}$$

Combined Eq. 3.12 with Eq. 3.9, we have:

$$E_{redox} = E_{redox}^{o} - kT \ln \frac{[oxidized\ ion\ concentration]}{[reduced\ ions\ concentration]}, \quad \textbf{3.12}$$

where E^{o}_{redox} is therefore defined as the redox level E_{redox} when the oxidized ion concentration is equal to the reduced ion concentration.

If we assume that the concentrations (activity) of the redox couple ions are the same in the solution at equilibrium and the number of the ion changes is the same in both reduction and

oxidation reactions, since for one electron transfer $\Delta E_{reorg}^{red} = \Delta E_{reorg}^{ox} = \Delta E_{reorg} = \lambda$, we eliminate the second right term in equation 3.11. So we have

$$E_{redox}^{o} = \tfrac{1}{2}(E_{ox} + E_{red}), \qquad \textbf{3.13}$$

E^{o}_{redox} is therefore always located in the middle of the energy gap. The energy levels of E^{o}_{redox}, E_{ox}, and E_{red} are shown in Figure 3.31b.

It is necessary to point out that in solution the energy levels we used here are thermodynamic effective energies relative to the electrode. There is no direct electron exchange between different energy levels in the solution. The electron transfer has to occur through a solid electrode in contact with the specific redox couple system. Above discussion shows that the energy level in the electrolyte depends on the actual concentration of the redox agents. This directly tells us that the electrolyte concentration is very important in the electrochemical reaction.

Semiconductor/electrolytic solution system:

After knowing how to define the redox energy (effective Fermi energy) in the solution to describe the occurrence of electron transfer, we will try to explain the model that describe the electron energies when solid and electrolyte are in contact. For our research interest, we focus our discussion on the semiconductor/electrolyte system.

When the semiconductor is placed in contact with an electrolytic solution, the charge distribution has to be rearranged in order to achieve an equilibrium status. It is well accepted that there are three major charge double layers formed: space charge layer, Helmholtz layer, and Gouy layer.

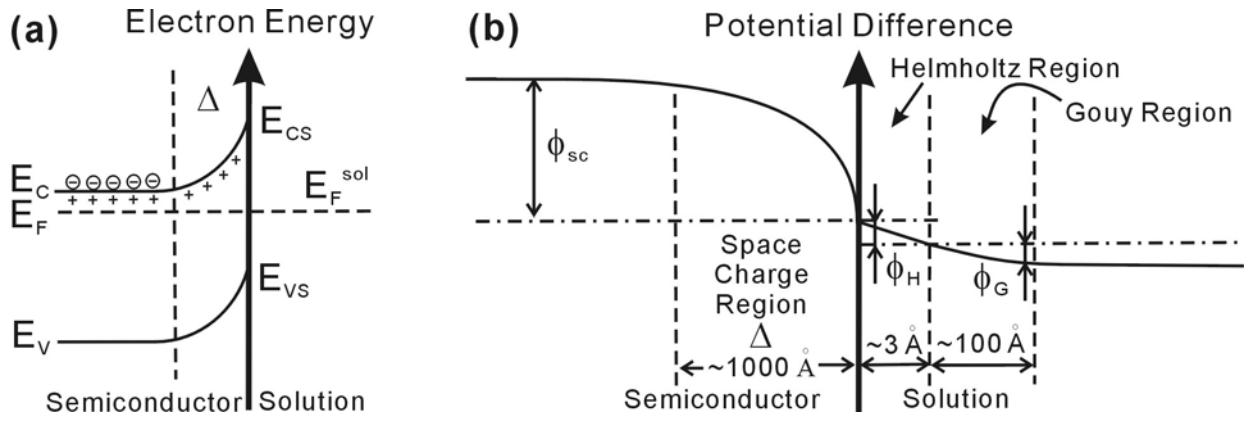

Figure 3.32 (a) Energy band diagram at the n-type semiconductor surface in contact with solution. E_c, E_F, E_v are the conduction band edge energy, valence band edge energy, and Fermi energy in the semiconductor respectively. E_{cs} and E_{vs} are the conduction and valence band edge energies at the surface, respectively. E_F^{sol} is the effective Fermi energy in the solution. (b) Electron potential distribution across the semiconductor and solution when an external reverse bias to semiconductor is applied. The semiconductor is at higher potential than the solution. Three double layer regions of electronic charges (space charge, Helmholtz, and Gouy region) are formed.

As shown in Figure 3.32a, for an n-type doped semiconductor in contact with an electrolytic solution, the charge will appear in the form of uncompensated impurities or trapped holes or electrons, or possibly in the form of mobile holes or electrons very near the surface. The analysis of how this layer of bulk charges, together with the counter-charge located at the surface, leads to a space charge double layer within the semiconductor.

Besides this space charge layer, in the electrolyte, we have charged planes on the two sides of the Helmholtz region that form the Helmholtz double layer. One plane is at the semiconductor surface and the charge is in surface states or at the location of adsorbed ions. The

other plane is called the "outer Helmholtz plane", the position of closest approach of mobile ions.

Finally, there is an extended region of excess space charge in the Gouy-Chapman region of the solution, associated with mobile ions, a region where the field near the surface separates the positive from the negative ions. This charged region, together with the countercharge in the Helmholtz region and in the solid, form the Gouy double layer.

The symbols ϕ_{sc}, ϕ_H, and ϕ_G represent the total voltage drop across the semiconductor space charge region, Helmholtz layer, and Gouy layer, respectively. To understand the electron exchange process in this system, we need to study the potential distribution across these three regions, as shown in Figure 3.32b.

The potential distribution $\phi(x)$ in the Gouy region can be expressed:[29]

$$(d\phi(x)/dx)^2 = (2ckT/\kappa\varepsilon_0)\{[\exp(q\phi_G/kT)-1]+[\exp(-q\phi_G/kT)-1]\}, \qquad \textbf{3.14}$$

where c is the redox specie concentration, k is the Boltzmann constant, T is the absolute temperature, κ is the electrolyte dielectric constant, ε_0 is the vacuum permittivity, q is the charge of an electron, ϕ_G is the change of potential from that in the bulk solution. We here estimate the field in the Gouy region. If c is 10^{20} cm^{-3} (just higher than 0.1 M), κ is 80 (for H_2O), and ϕ_G is 0.25 V, the field at the outer Helmholtz plane is about ± 2×10^7 V/cm. Therefore, most of the excess potential ϕ_G will be lost in about an angstrom. If c is higher than 0.1 M, the Gouy layer will be almost indistinguishable from the Helmholtz layer, except for a very small residual voltage, of the order of 0.1 V at most. It is for this reason that the Gouy layer will be neglected in our discussion.

The Helmholtz layer is considered to be formed between two planar sheets of charge. On the solution side, the charge originates by the accumulation of ions at the outer Helmholtz plane. One the solid side, the charge can arise in three forms: an accumulation of free charge, free charge trapped from the solid onto surface states, and adsorbed ions. This layer can be described as a simple capacitor, described by:

$$C = Q/V = A\kappa\varepsilon_0 / d \;;\; E = \phi_H / d = Q/\kappa\varepsilon_0 , \qquad \textbf{3.15}$$

where C is the capacitance, Q is the charge, κ is the dielectric constant for the electrolyte in the Helmholtz layer, d is the thickness of the Helmholtz layer, ε_0 is the vacuum permittivity, E is the electric field and ϕ_H is the voltage change across the Helmholtz layer. For a metal electrode, the Helmholtz capacitance is measured to be on the order of 10^{-5} F/cm^2.[29] κ is proposed to be around 5 and thus d is on the order of few angstroms (~ 3 Å).

For a nondegenerate semiconductor, under low reverse bias, the surface excess charges are caused by the adsorption/desorption since the electron transfer is relatively small due to the low concentration of free carriers in the semiconductor. It is estimated that one sign of charge density adsorbed on the solid surface is no larger than 10^{12} to 10^{13} cm^{-2}. If the Helmholtz layer thickness resembles that for metal electrode, the capacitance remains at about 10^{-5} F/cm^2. Therefore, the Helmholtz voltage ϕ_H for the semiconductor normally will be about $\phi_H = V = Q/C = 1.6\times10^{-19}\times10^{12}/10^{-5} = 0.016\ V$. It has to be pointed out that if the semiconductor is strongly inverted at the surface, the surface of the semiconductor will have free carriers on the surface. Thus, the surface of the semiconductor becomes metal like. Then, the surface excess charges could be changed by the electron transfer and lead to a much larger value of ϕ_H . Once again, for the nano columnar pore formation process, a large voltage bias is applied

so that the above approximation may not be appropriate. Later discussion (in section 3.11) will point out that the voltage drop across the Helmholtz should not be neglected in our case and in fact the Helmholtz layer voltage drop may be large to enable a fast electrochemical process.

In this work, it is therefore suggested that under conditions when the reverse bias voltage is applied during the porous SiC formation in concentrated HF solution, the potential drop across the Gouy layer is negligible for a semiconductor/electrolyte interface. The main potential drop will occur in the semiconductor and the Helmholtz layer. There are three possible surface electron energy band bending in the "space charge" region: depletion, inversion, or deep inversion (breakdown), depending on the magnitude of the applied voltage. Most of applied voltage will therefore appear across the semiconductor and its interface:

$$\phi_{applied} = \phi_{sc} + \phi_H + \phi_G \approx \phi_{sc} + \phi_H , \qquad \textbf{3.16}$$

where ϕ_{sc} stands for the potential drop across the space charge layer in the semiconductor and ϕ_H stands for the potential drop across the Helmholtz layer at the interface. During the porous formation, it is found that the current density decays (Figure 3.6) during the pore formation. The decay is caused by the increasing length of the columnar pore. This suggests that the resistance increase of the whole electrochemical cell is due to the electrolyte inside the growing columnar pores. There should be an appreciable voltage dropped in the electrolyte.

Therefore, we propose that the total voltage in the nano-columnar pore formation is across three parts: space charge region, Helmholtz layer and electrolytic solution in the pores. We rewrite the Eq. 3.16 as following:

$$\phi_{applied} = \phi_{sc} + \phi_H + \phi_G \approx \phi_{sc} + \phi_H + \phi_{Pores} , \qquad \textbf{3.17}$$

where ϕ_{Pores} stands for the potential drop in the electrolyte inside the columnar pores.

We will calculate the likely potential distribution in a SiC electrode to discuss the charge transfer in our electrochemical experiments later in section 3.11.

3.10 IMPEDANCE SPECTROSCOPY TO UNDERSTAND THE POTENTIAL DISTRIBUTION IN THE ELECTROCHEMICAL SYSTEM AT EQUILIBRIUM

Impedance (including capacitance) measurements[67,68,69] are very useful to investigate the charge distribution in the electrochemical system. To better support our model discussion in section 3.11, we here try to use the impedance measurements to verify the double layer model described in section 3.9 and understand the energy band positions in our system. There are two kinds of impedance measurements one can perform: 1) Measure the capacitance as a function of electrode potential. 2) Measure the impedance as a function of electrode potential frequency.

The measurements of capacitance as a function of potential have been performed on a SiC electrode with non reacting electrolyte[11,18,30]. The measured results can be plotted on a Mott-Schottky plot ($\frac{1}{C^2}$ *v.s.* V plot, where C is the capacitance measured and V is the applied scan voltage). As explained in the section 3.9, if there is no accumulation or inversion happens at the semiconductor interface (i.e. only low voltage is applied on the non-degenerate semiconductor), only the space charge region varies with the applied voltage. The result of the measurements can be fit into a Mott-Schottky equation:

$$\frac{1}{C_{sc}^2} = \frac{2}{\kappa\varepsilon_0 q N_{sc} A^2}(V - \phi_{sc} - KT/q), \qquad \textbf{3.18}$$

here A is the area of the sample, V is the applied bias voltage in the scan, Csc is the capacitance measured, N_{sc} is the space charge density in the space charge region, ϕ_{sc} is the total voltage drop on the semiconductor space charge region, K is the Boltzmann constant, T is the absolute temperature, q is the absolute electron charge, κ is the dielectric constant and ε_0 is the vacuum permittivity. The importance of this plot is that one can readily extract the value ϕ_{sc} and use it to determine the surface band edge position E_{cs} (Figure 3.32).

Published results, however, are not in agreement[11,70,71] and apparently depend on the pH value of the electrolyte. We here use the values of E_{cs} and E_{vs} determined by M. Gleria and R. Memming[11]. A diagram describing the SiC/electrolyte interface is shown in Figure 3.33. It should be pointed out that the values for E_{cs} and E_{vs} are only valid when there is no accumulation or inversion at the surface of the semiconductor.

This energy band diagram suggests that the center of the band gap of SiC is approximately located at 0 V vs. Normal Hydrogen Electrode (NHE). The redox potential for H_2O/O_2 is just above E_{vs}. E_{cs} is 1.4 V lower and E_{vs} is 1.6 V higher than the NHE potential. It is observed experimentally that under cathodic conditions, no decomposition of SiC occurs. This suggests that E_n^{decomp} is above E_{cs}.[30] Under anodic conditions, the decomposition of SiC does happen, therefore E_p^{decomp} must be located within the band gap. Since no O_2 formation is observed at the anodic biased SiC electrode, E_p^{decomp} should be more negative then H_2O/O_2 redox energy on the NHE scale. In the dry oxidation, the activation energy of the reaction $SiC + 2O_2 \rightarrow CO\uparrow + SiO_2$ is around 1.3 eV for Si-face and C-face SiC[78]. The free energy change for the reaction $SiC + 2O_2 \rightarrow CO_2\uparrow + SiO_2$ is about -1180 kJ/mol, which is equivalent to -12.3 eV. Considering that the potential of NHE (H_2/H^+) is about - 4.5 ~ - 4.7 V in vacuum

scale[72], in the NHE scale, the activation dry oxidation energy is 6 eV and the free energy change is about 17 eV. We concluded these results and show them in the Figure 3.33 to have a more complete picture of the SiC/electrolyte interface energy band diagram. These results point out that the instability of SiC toward electrochemical oxidation has reasons other than the thermo dynamical stability explanation. I. Lauermann *et al*[18] suggested that the well-known chemical stability of SiC therefore has only kinetic reasons. M. Gleria, and R. Memming[11] believed that surface states are involved during the anodic reaction and thus greatly lowered the activation energy in electrochemical oxidation, as shown in Figure 3.33.

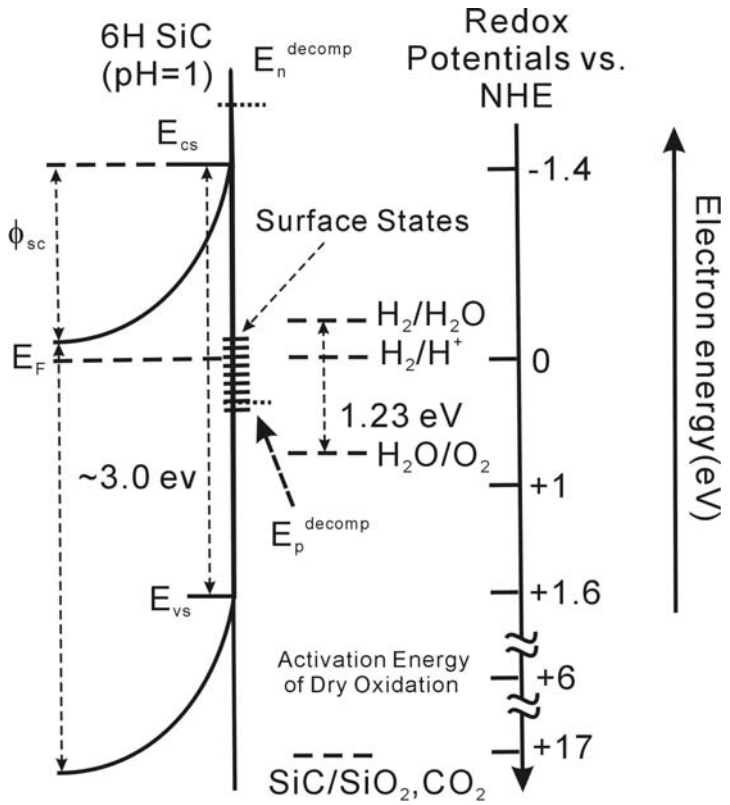

Figure 3.33 Relative position of energy bands at the surface of 6H SiC electrodes. All the potential values are vs. NHE. E_n^{decomp} is the energy for cathodic decomposition of the crystal. E_p^{decomp} is the energy for anodic decomposition.

On the other hand, the frequency dependent impedance measurements will help us to determine the potential drop profile. This is done by fitting the data to an equivalent circuit containing resistors, capacitors, and inductors. The choice of circuit model is not unique. One needs to use a physically meaningful model to understand the electrochemical system. The data on an n-type 4H SiC sample doped at about $1\times10^{18}cm^{-3}$, taken without UV light illumination, are shown in Figure 3.34a. The experiments are carried out in aqueous HF solution (10% HF and 5% ethanol in weight percentage). Fore this reason, we don't apply any bias voltage in order to avoid the anodic reaction. In Figure 3.34a, the dots are the recorded data and the solid line is the fit, which will be explained later.

Figure 3.34b shows an often used model which can replicate the impedance of a semiconductor/electrolyte system. Such a model includes all the important elements that can influence the electrical properties. However, it contains too many elements and many of them cannot be separated from one other. Therefore, we simplify the model so that only the most important elements are left. For our SiC/HF electrolyte system, the SiC is highly doped so that its resistance can be neglected. The Helmholtz layer will have a large capacitance so that the voltage drop across it is small. We therefore neglect the Helmholtz layer resistance and. Since it is very difficult to separate the surface states effect from that of the space charge region, we neglect it. After all this simplification, we have the equivalent circuit shown in Figure 3.34c.

The calculated impedance Z of the equivalent circuit in Figure 3.34c contains a real and imaginary part Z_{re} and Z_{img}:

$$
\begin{aligned}
Z_{re} &= R_{sol} + \frac{R_{sc}}{1+(\varpi R_{sc} C_{sc})^2} \\
-Z_{img} &= \frac{\varpi {R_{sc}}^2 C_{sc}}{1+(\varpi R_{sc} C_{sc})^2} \quad . \\
\varpi &= 2\pi f
\end{aligned}
\tag{3.19}
$$

ω is the angular frequency and f is the frequency of applied voltage. The fitting results using this equivalent circuit are: $R_{sol} \approx 6\ \Omega$, $R_{sc} \approx 1.5\times10^8\ \Omega$, $C_{sc} \approx 0.033\ \mu F$.

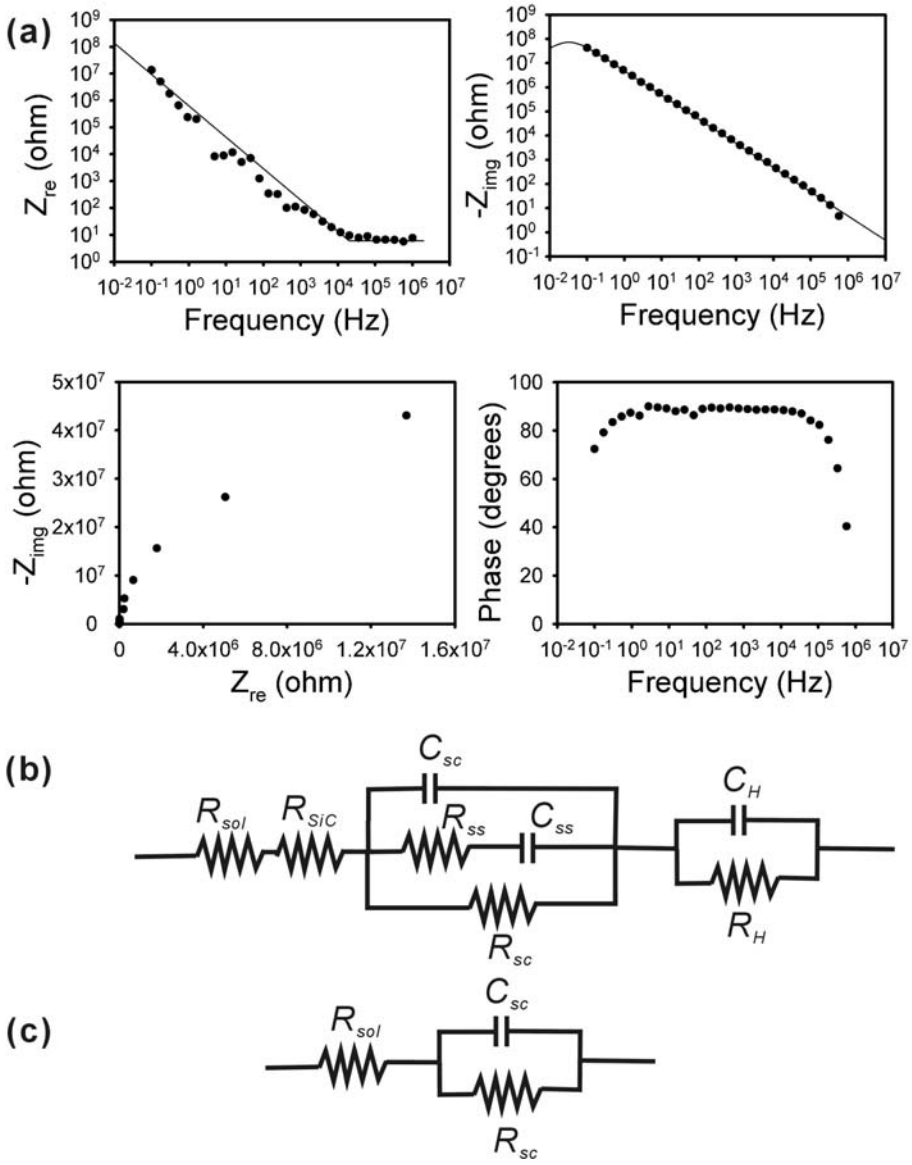

Figure 3.34 (a) Impedance data recorded on a C-face n-type (1×10^{18}cm^{-3}) 4H SiC sample in 10%HF,5%ethanol electrolyte without UV illumination. The amplitude of the AC signal is 20 mV. The current response ranges from μA to pA. No bias is applied to the electrochemical cell. (b) A well accepted equivalent model describing the electrochemical cell. In order, R_{sol}, R, R_{ss}, R_{sc}, R_H are electrolyte, SiC, surface states, space charge region, and Helmholtz layer resistances. C_{sc}, C_{ss}, C_H are space charge region, surface states, and Helmholtz layer capacitances. (c) A simplified circuit model.

The fit results can be examined as following:

1) As $\varpi \to 0$: $Z_{re} \to R_{sol} + R_{sc} \to 1.5 \times 10^8\ \Omega$; $-Z_{img} \to 0$

2) As $\varpi \to \infty$: $Z_{re} \to R_{sol} \to 6\ \Omega$; $-Z_{img} \to 0$

3) By solving $\frac{dZ_{img}}{d(\varpi R_{sc} C_{sc})} = 0$, we get when $\varpi R_{sc} C_{sc} = 1$, Z_{img} has the maximum value.

   Substitute the fit values, we obtain $f = 0.032\ Hz$.

All these results agree with the experimental data shown in Figure 3.34a.

The results show that the double layer model could be used to describe the electric property of SiC/HF electrolyte interface. The major resistance is from the space charge region. It supports the argument that most of the DC voltage drop is occurred in the space charge region. This picture of the double layers in the electrochemical system therefore can be used to examine the SiC/HF electrolyte system at equilibrium using the above simplified model. However, when the semiconductor is strongly reverse biased, the space charge region will be inverted and minority carriers will accumulate at the interface by breakdown or tunneling even without UV illumination. The electrochemical etching can take place under these conditions. The equilibrium condition does thus not exist any more. The questions such as how these double layers change under the high field near the interface required for the nano columnar pore formation can not be tested by this method.

It is, however, found that we can use this method as an *in situ*, nondestructive method to characterize the SiC/HF or PSC/HF interfaces. Without too much quantitative explanation we here show the results from one experiment in Figure 3.35. The idea was to see if UV illumination

and the formed columnar pores lead to any change in the frequency dependence of the complex impedance.

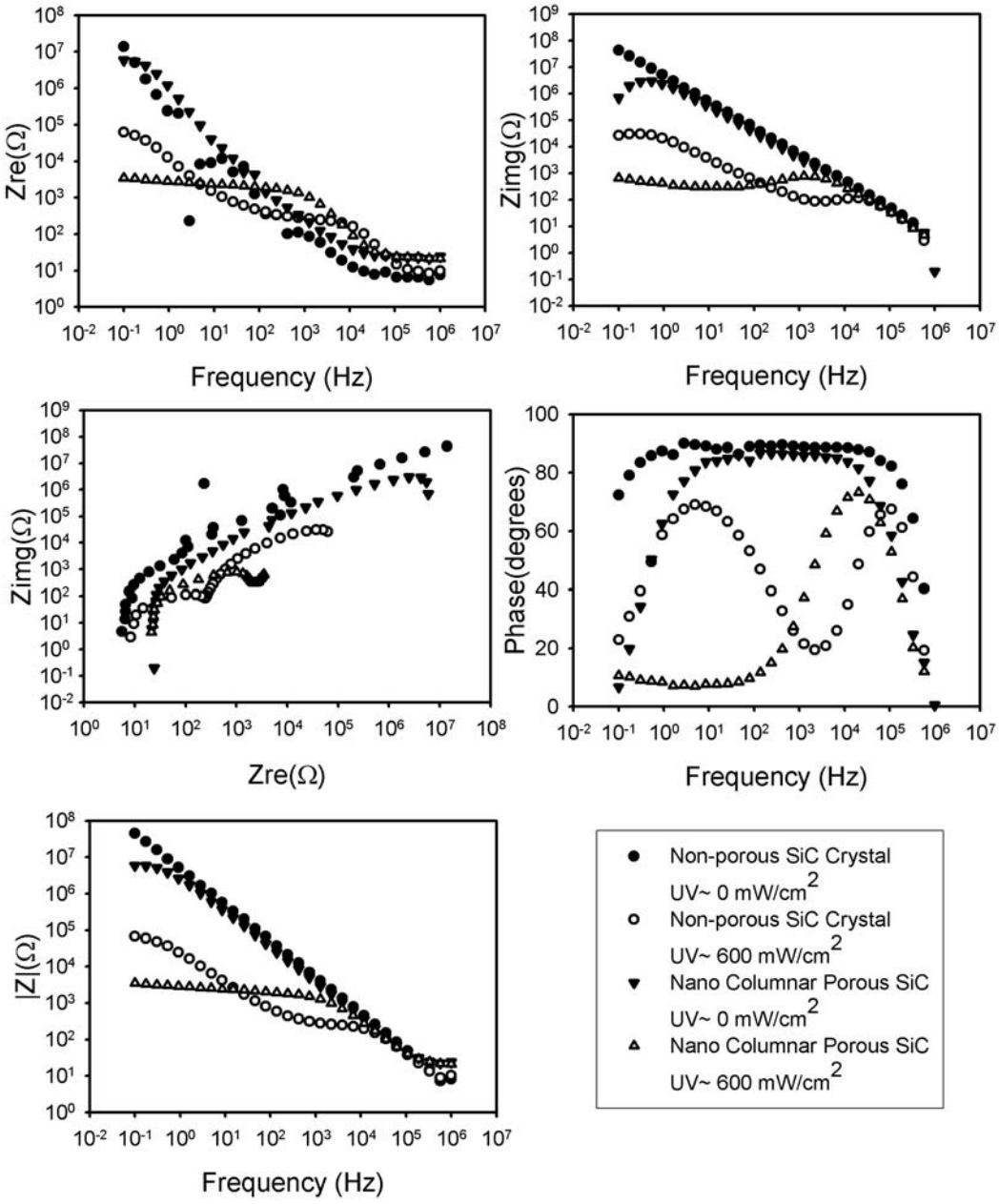

Figure 3.35 Impedance measurements on 4H SiC (n~ 1×10^{18} cm^{-3}) in 10%HF, 5% ethanol electrolyte. The AC voltage amplitude is 20 mV and the DC voltage applied is zero. Four measurements are carried out before etching with/without UV and after etching (nano columnar porous structure) with/without UV illumination.

The results show that UV illumination will decrease the impedance in the low (<1 kHz) frequency region. This almost three order of magnitude decrease of the impedance suggests that a large number of holes are created and there are much more free electron/hole carriers at semiconductor surface. The high frequency impedance is not changed by the UV illumination. This suggests that the hole transfer across the interface is slower than ~0.1 ms. The charge transfer will not respond to higher frequency oscillating voltage.

After the etching, which leads to nano-columnar PSC, the impedance data do not change much from the initial bulk SiC (There are some differences at low frequency). As will be explained in section 3.11.5, the depletion width at the SiC pore wall can be evaluated using a cylindrical Poisson's equation. The band bending at equilibrium is around 1.4 V and the calculation shows that the depletion width is 30 nm. The average pore wall thickness here is observed to be about 40 nm, therefore we believe that the pore wall is depleted of free carriers and becomes an insulator. If we assume the electrolyte remains at a relative high concentration inside the pores (a good conductor), the solution will then short the depleted pore walls in the circuit. The SiC/HF interface that responds to the impedance measurement is then just the interface between the solution and pore tip. The result is therefore similar to the impedance data measured with the original SiC crystal.

3.11 THE CHARGE TRANSFER IN THE NANO-COLUMNAR PORE FORMATION

3.11.1 The actual pore geometry of nano-columnar pores

Above discussion of SiC/HF electrolyte interface using the double layer model deals with a flat interface. It is well known that the geometry of the interface changes the distribution of the electric field in very effective way. Therefore, we need to understand the exact pore shape of both the pore wall and the pore tip.

The resolution of our SEM system cannot serve for this purpose. No matter how hard we try, the detailed pore structure cannot be distinguished by the SEM with 2-3 nm resolution. This work is therefore achieved using Titan® High Resolution Transmission Electron Microscopy (HRTEM) by Prof. Ute Kaiser at University of Ulm, Germany. Cross sectional images of pore wall and pore tip structures are shown in Figure 3.36 and Figure 3.37 below, respectively.

Figure 3.36 clearly show that the pore wall is still made of single crystalline SiC lattice. The diameters of the columnar pores are about 15-20 nm. Besides, it is also observed that there is an amorphous surface layer of unknown composition exists after the etching. The likely candidates are SiO_2 and chemical product deposited from the electrochemical etching. The layer can be as thick as 6 nm and usually around 1 nm. The amorphous layer could decrease the real columnar pore diameter down to about 3-8 nm. At this point, we don't know whether this surface layer is formed by the electrochemical etching, by the ambient oxidation after the electrochemical process, or by the sample preparation process for TEM. If this layer is formed during the etching, it could be the passivation layer that stops the etching from further dissolving the pore wall material.

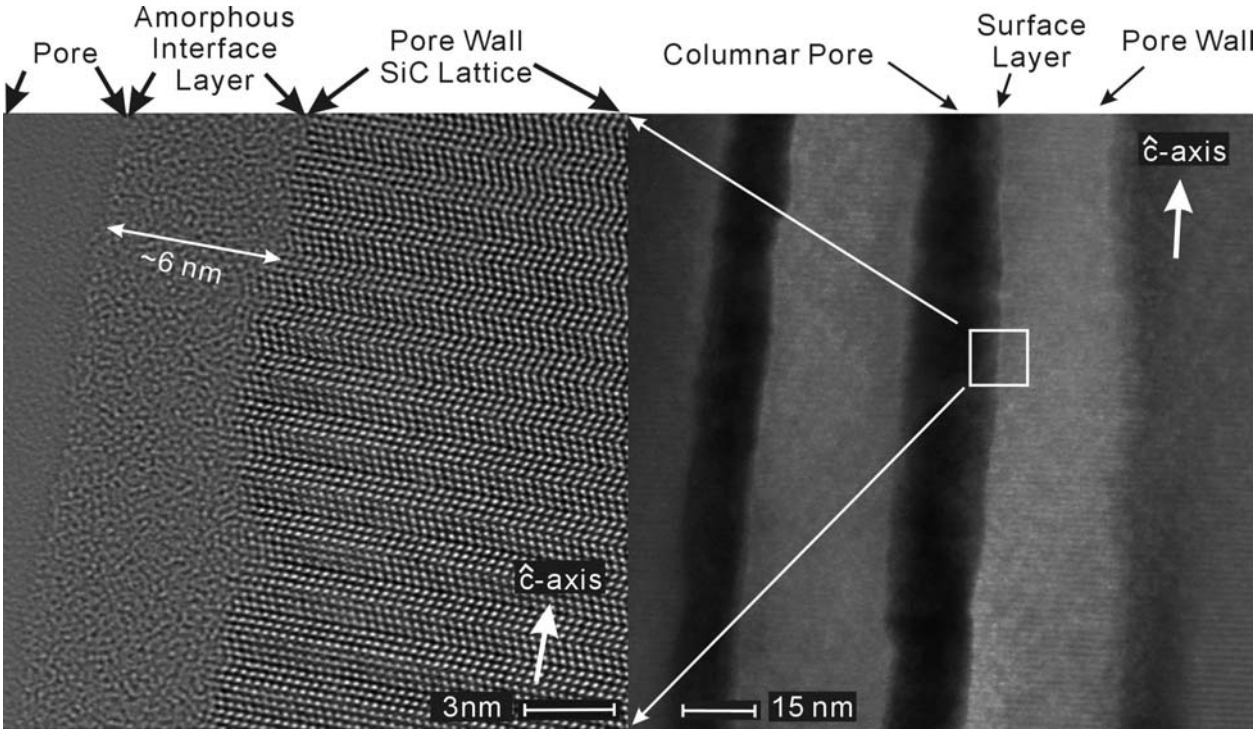

Figure 3.36 Cross sectional HRTEM images of detailed columnar pore and pore wall structure after the photoelectrochemical anodization of n-type 6H SiC.

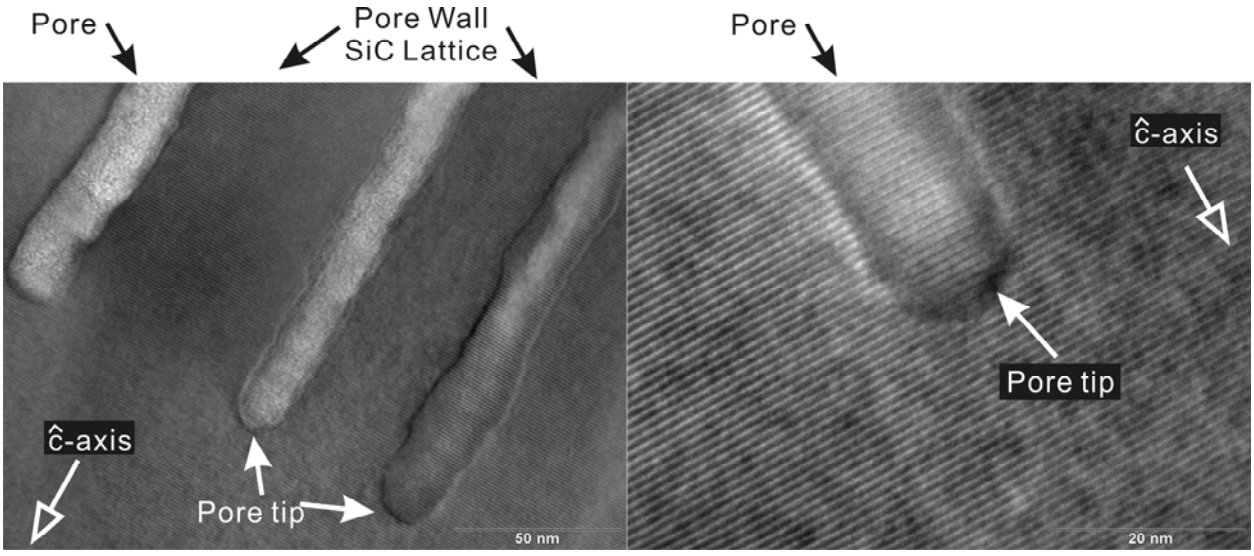

Figure 3.37 Cross sectional HRTEM images of detailed columnar pore and pore tip structure after the photoelectrochemical anodization of n-type 6H SiC.

The HRTEM images at pore tip in Figure 3.37 show that the columnar pore tip has a hemispherical geometry shape. The pore diameter is also about 15-20 nm at the pore tips. The pore wall has a cylindrical geometry. We here use this information to construct the double layer model in the columnar pores.

3.11.2 The double layer model inside the columnar pore and related model assumptions

The SiC/HF electrolyte interface is described using the diagram in Figure 3.38.

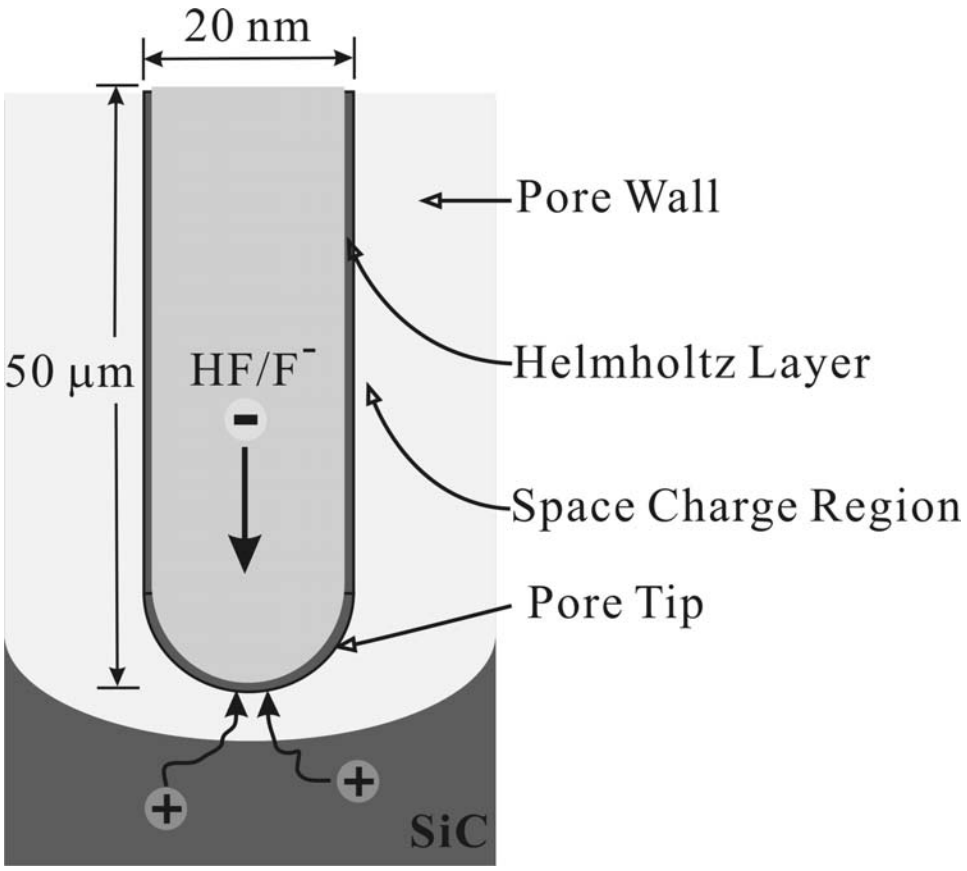

Figure 3.38 The double layers inside a nano-columnar pore during the columnar pore formation. The details will be explained in the text.

The double layers inside a columnar pore can be divided into two different parts: cylindrical pore wall and hemispherical pore tip. Each part contains the three double layers: space charge region in the SiC, Helmholtz layer at the interface, and the HF electrolytic solution. Because the columnar pores have a uniform diameter, we believe that the electrochemical etching only happens at the pore tip. To understand the columnar pore formation is to understand the charge transfer mechanism at the pore tip and the passivation mechanism at the pore wall.

In this section, we focus on the five aspects of the columnar pore formation and base on these discussions, we will have a clearer picture of the physics process.

First, we intend to explore the reason why chemical reaction is so anisotropic in terms of the crystal orientations. By studying this, we will find the necessary condition to enable columnar pore growth. (Section 3.11.3)

Second, we will try to understand the pore tip charge transfer process. This study will help us understand what is controlling the pore diameter. (Section 3.11.4) Third, we then try to investigate the pore wall passivation and understand what is determining the pore wall thickness. (Section 3.11.5)

Finally, we will explore the current decay observations during the nano-columnar pore formation. This work will help us understand the time variation of voltage distribution in the columnar pores. (Section 3.11.6) The knowledge of the voltage distribution across the Helmholtz layer will then guide us in the future researches. (Section 3.11.7) Before jumping in, we will need some assumptions so that the quantitative analysis is possible.

First, during the nano-columnar pore formation, we assume that a steady state charge transfer happen at the pore, which means at the SiC surface, the holes from UV excitation and electric breakdown are steadily consumed at the interface by electrochemical reactions.

Second, it was estimated in section 3.10 that the hole transfer across the SiC/HF electrolyte interface takes about 0.1 ms. As a very rough estimation, for a 30 minutes etching, the nano-columnar porous layer can be as thick as 100 μm. This gives an average columnar pore length growth roughly 5.6×10^{-2} Å per 0.1 ms. Therefore, it is reasonable to assume that during a single hole transfer, the interface does not change.

Third, the *I-V* scans show that the current increases rapidly in the voltage region for the nano-columnar pore formation. It suggests that the hole supply is the rate limiting factor here. Most of the holes that reach the interface are then transferred either as the stored charge in the Helmholtz layer to maintain the necessary voltage drop or as the consumed charge of the electrochemical reactions. To simplify the discussion, we here assume that there is no free hole accumulation at the SiC surface at the steady state. For this reason, the supposedly deep inversion region near the SiC surface becomes a space charge region with E_F far below E_{VS}.[29]

3.11.3 The crystal surface influence on the electrochemical etching of SiC

Nano columnar pore formation happens on C-face 4H and 6H SiC but not on the Si-face. We believe that this is due to the faster oxidation rate on the C-face compared to the Si-face, which has been discovered in the wet oxidation process.[58] However, the detailed mechanism hasn't been discussed. In this section, we will first discuss the electrochemical reactions that we believe occur during the etching of SiC. After this, we suggest a possible explanation of how the polarity property of basal plane 6H SiC (4H SiC is similar to the 6H SiC in this study) lattice influences the rate of the electrochemical process in addition to the different oxidation rate.

3.11.3.1 The similar electrochemical oxidation reactions

The etching process is realized by anodizing SiC, which suggests that holes are needed during the etching processes. CO/CO_2 have been found as the reaction products, but there is no O_2 formation detected. [17,18,73] The following electrochemical reactions are therefore suggested:

$$\begin{aligned} SiC + 2H_2O + 4h^+ &= SiO + CO\uparrow + 4H^+ \\ SiC + 4H_2O + 8h^+ &= SiO_2 + CO_2\uparrow + 8H^+ \end{aligned} \quad . \qquad \textbf{3.20}$$

If one regards only SiO_2 as stable and thus the product of the electrochemical process, we could then suggest another set of equations[27]:

$$\begin{aligned} SiC + 3H_2O + 6h^+ &= SiO_2 + CO\uparrow + 6H^+ \\ SiC + 4H_2O + 8h^+ &= SiO_2 + CO_2\uparrow + 8H^+ \end{aligned} \quad . \qquad \textbf{3.21}$$

Experiments[18] have shown that the ratio of CO and CO_2 is close to 1:1. Other experiments studying the PSC formation suggest an average of seven holes per reaction during the etching[15,27,47]. These experiments suggest that the likely reactions that actually happen are those given by equation 3.21 with the two reactions taking place at the same rate. If the electrolyte contains HF, the formed SiO_2 is then steadily removed from the surface of SiC. The reaction is therefore able to continue and a pore network can form.

However, it is worth mentioning that even without the presence of HF, the anodic process can continue, but at a very slow rate[18]. This process is probably similar to a wet oxidation process of SiC that has been studied elsewhere.[58] However, unlike the electrochemical etching of Si in water without HF, where a thin layer of SiO_2 will form and then stop the oxidation process, a thick layer of SiO_2 will form on SiC, because the oxide layer is so porous that the electrolyte can be kept in contact with the SiC surface. This is in agreement with our experimental observations of the voltammetry scan (Figure 3.7 and Figure 3.21). In these scans, we do not

observe a large cathodic critical voltage when a noticeable cathodic current is flowing. If there is an impermeable insulating layer formed, we should observe a rectification in the current-voltage curves.

Moreover, in the published work of porous Si[74,75,76,77], current oscillation is observed during the pore formation. The current oscillation frequency is found to be proportional to the applied voltage. The impermeable oxide layer formed at the interface was suggested to cause this phenomenon. The current burst model has then been proposed[74,75,76,77] to explain the porous Si formation at high fields and the current oscillations during the Si dissolution process. The current oscillations we observed during the etching of SiC, however, seem to have a unique frequency and the frequency does not change with applied voltage. This again suggests that the oxide formed on the SiC surface is porous. Therefore, the current burst model that has been proposed to explain the and the current oscillation cannot be applied to SiC. Excluding the possible surface oxide influence on the PSC formation will greatly simplify and help our discussion below.

It is also important to point out here that, the calculated γ valves (average number holes to remove one SiC pair) in the nano-columnar pore formation are all about 7 in all the experiments. When γ is about 7, the two oxidation reactions in Eq. 3.21 happen at the same rate. These results are consistent with the γ value reported for triangular porous SiC formation[27] and the photo-electrochemical etching of SiC reported by J. Shor *et al*[15]. The same value of γ argues for the similar photo-electrochemical reaction process in all the porous SiC formation, at least in the number of holes needed to etch one SiC pair. The different porous morphologies and different current density observed here are unlikely to be related to any different electrochemical reaction processes.

3.11.3.2 Anisotropic electrochemical oxidation reaction rate

It is an experimental fact that the C-face etches faster than the Si-face. It is true not only in electrochemical etching (oxidation) process but also in the wet[58] and dry oxidation of SiC.[78,79,80,81,82] At the moment, the detailed oxidation reaction route is not clear. The question whether the Si-face (C-face) remains as Si-face (C-face) during the oxidation process is not answered. In our electrochemical oxidation process, the details of the surface reconstruction and surface properties during the etching are not clear either.

Contrary to the dry/wet oxidation, in which case SiO_2 forms across the whole SiC surface, SiO_2 is formed only partially in the SiC crystal in the electrochemical etching. The formed oxide is then dissolved by HF and become what we call pores. The different morphologies of the pores contain the information about how the oxidation reaction is occurring. Because the fact that Si-face and C-face etching lead to uniform but different pore morphologies under the identical etching conditions, we tend to believe that the oxidation process is a double layer by double layer process. This means the Si-face (C-face) remains as the Si-face (C-face) during the etching. If the etching is a single layer by single layer process, the significant pore morphology difference should not be observed at all. This basic conclusion/assumption we have here is the basis for the following discussion.

In the most studied dry oxidation process, it is found[78,82] that there are roughly three steps in the oxidation: 1) O_2 diffusion through the oxide film. 2) Reaction at the interface. 3) Out-diffusion of product gases (e.g. CO) through the oxide film. Atom clusters and defects can form at the oxide/SiC interface.

In the dry oxidation work reported by Song *et al*[78], authors show that the differences in the oxide layer thickness growth are mainly due to the different oxidation reaction rate on

various crystal surfaces. It is concluded that on the C-face, there is a large driving force for C atoms in the first layer to easily break Si-C bond and from C-O, a very stable molecule. Following the first layer removal, the Si atoms in the second layer can react with O since there is only one Si-C bond connected to the third layer (C layer). However, on the Si-face, it is more difficult to break Si-C bonds and form Si-O since there are three Si-C bonds connected to the second C layer. It is proposed that only one Si-C will be broken and form a Si-O-C specie. The CO is then released and leaves a Si-Si bond with the second bilayer Si. Because of this, they propose that the oxidation reaction rate is mainly proportional to the carbon areal density of the first interface layer.

Because the electrochemical etching process is an oxidation process, we are proposing that the same explanation in the dry/wet oxidation to the different etching rate on C-face and Si-face can be applied to our case. The final reaction products CO and CO_2 suggest a similar oxidation process as that in the dry/wet oxidation. We can use the same argument in the dry/wet oxidation above to explain the different electrochemical reaction rate on C-face and Si-face qualitatively. Figure 3.39a and b show the schematics of the preferred etching direction at the pore tip in C-face and Si-face etching, respectively. Figure 3.39c and d show the actual pore morphologies formed at identical etching conditions accordingly.

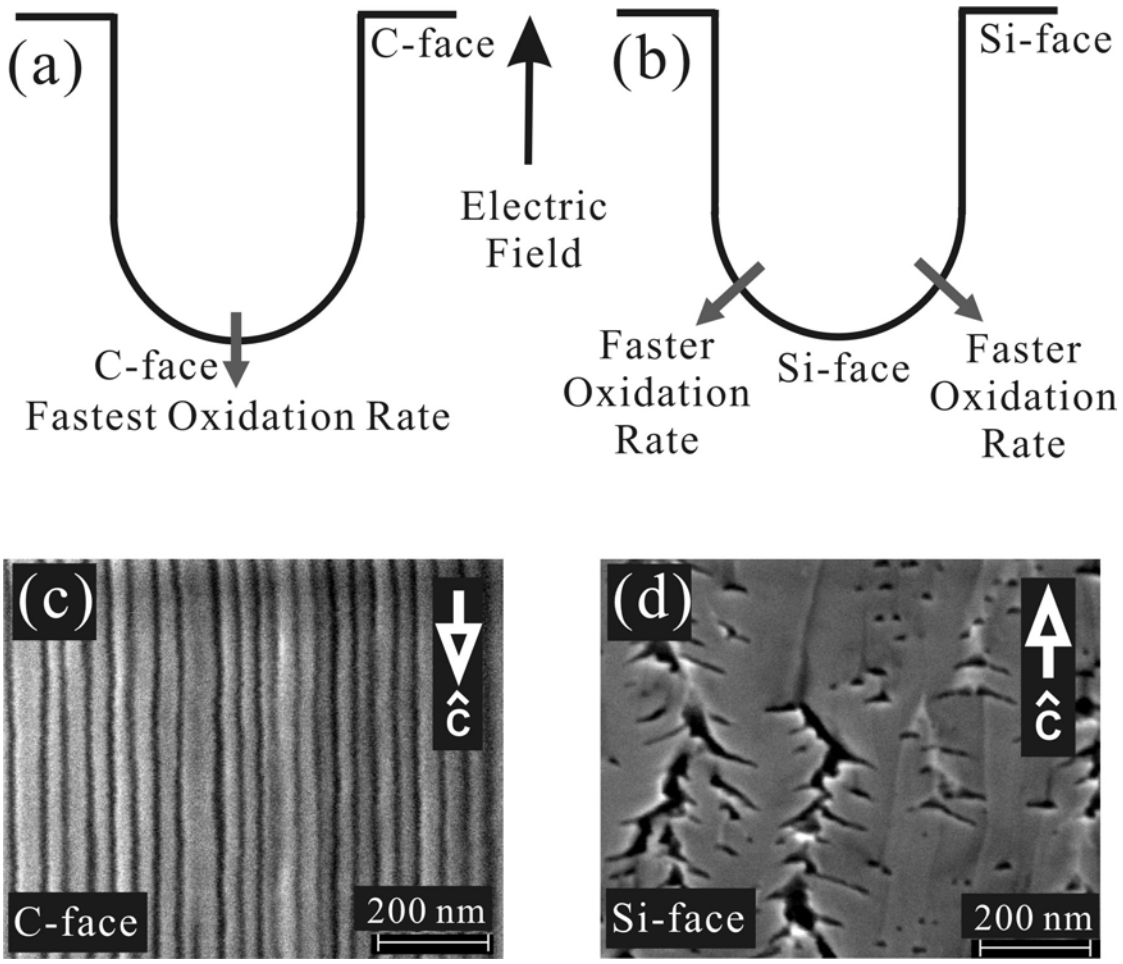

Figure 3.39 Schematic of preferred etching direction in the photoelectrochemical etching on (a) C-face and (b) Si-face SiC. The actual cross sectional SEM images of (c) C-face and (d) Si-face pore morphologies at the same etching conditions are shown, respectively**.**

In the porous formation processes, the pores generally grow towards the direction of the electric field applied. In the case of C-face etching, the fastest reaction direction is parallel to the field direction and therefore straight down pores formation is strongly preferred. When Si-face SiC is etched, the faster oxidation reaction directions are not in the direction of the electric field and therefore the pores will branch while growing along the direction of the elec-tric field, i.e.,

dendritic pores will form. A columnar pore formation is therefore not preferred at all in the Si-face SiC etching.

It also needs to be pointed out that the detailed oxidation process may be different in the electrochemical oxidation than that in the dry/wet oxidation. First, we do not have O_2 molecule in the aqueous solution. The oxidation agent is H_2O (or OH^-) rather than O_2. The oxidation process may be different. Second, in the electrochemical etching of SiC, no only CO but also CO_2 is formed in the ration of 1:1, which is not observed in the dry/wet oxidation. This could suggest more complicated oxidation reactions. Third, the SiO_2 formed during the reaction is porous and steadily removed by HF. Even if the removal rate of SiO_2 by HF is smaller than the SiO_2 formation rate in the steady state etching, the remaining thickness of the oxide should be limited. The possible in-diffusion of the OH^- and the out-diffusion of the CO and CO_2 should therefore be very different than that in the dry/wet oxidation. Because all these differences, the true reaction path may not be the same as that in the case of wet/dry oxidation.

3.11.3.3 The spontaneous field in the Helmholtz layer

It is notable that the different anodic etching rates on the two polar surfaces of semiconductors are also observed other than SiC, such as ZnO[45], InP[39,40]. This suggests that, besides the different oxidation reaction rate on the C-face and Si-face of SiC, there is another possible mechanism that favors the C-face etching and slows down the Si-face reaction. In the case of ZnO, a surface compensation charge argument was used to explain the different surface etching behavior of ZnO[45]. Pettingger *et al*[45] suggested that holes that reach the Zn-surface will be more likely (compared to the O-surface) to react with adsorbed OH^- ions (Eq. 3.19.2) and H_2O molecules (Eq. 3.19.3). Reactions are proposed to be:

$$2ZnO + 4h^+ \rightarrow 2Zn^{2+} + O_2 \uparrow \quad (1)$$
$$4OH^- + 4h^+ \rightarrow H_2O + O_2 \uparrow \quad (2) \qquad \textbf{3.22}$$
$$2H_2O + 4h^+ \rightarrow 4H^+ + O_2 \uparrow \quad (3)$$

Some of current is thus "wasted" by this instead of oxide the ZnO lattice atoms. Due to this, the electrochemical oxidation is slower on the Zn-surface than on the O-surface. We here try to apply the same theory with some alteration to explain our experiment observations.

6H SiC has an hexagonal structure and consists of atomic double layers. Each double layer can be assumed to carry on the Si side an excess surface charge density $+\sigma$ and on the C side $-\sigma$. Calculations[83] show that a crystal structure that is based on stacking of double layers has to have compensating charges at the surfaces to stabilize the crystal. Such compensating charges can reside in electronic surface states, or be generated by the removal/addition of some of the atoms of the surface plane which leads to different surface configurations [superstructures] at the polar surfaces. If the crystal is in contact with an aqueous electrolyte, a polar lattice like SiC can get the compensating surface charge from ions of the electrolyte (H^+, OH^-, …) bonded at the surface atoms. This layer of charge is also recognized as inner Helmholtz layer. The surfaces that exist during the etching of both Si-face and C-face 6H SiC are therefore proposed and shown in Figure 3.40.

The (0001) surface (Si-face) therefore attracts OH^- ions and the $(000\bar{1})$ surface (C-face) attracts H^+ or its complexes. The bindings in each case occur at preferred sites on the surface. In ZnO cases, the argument is some current is wasted in the etching of Zn-face ZnO by oxidizing OH^- into O_2 rather than decomposing the ZnO lattice. If this is also true in SiC, there will be O_2 formation (Eq. 3.17 and Eq. 3.18) and the average number of holes γ required to remove a SiC

pair should be different for Si-face and C-face etching. Both of these consequences are contrary to our experimental observation.

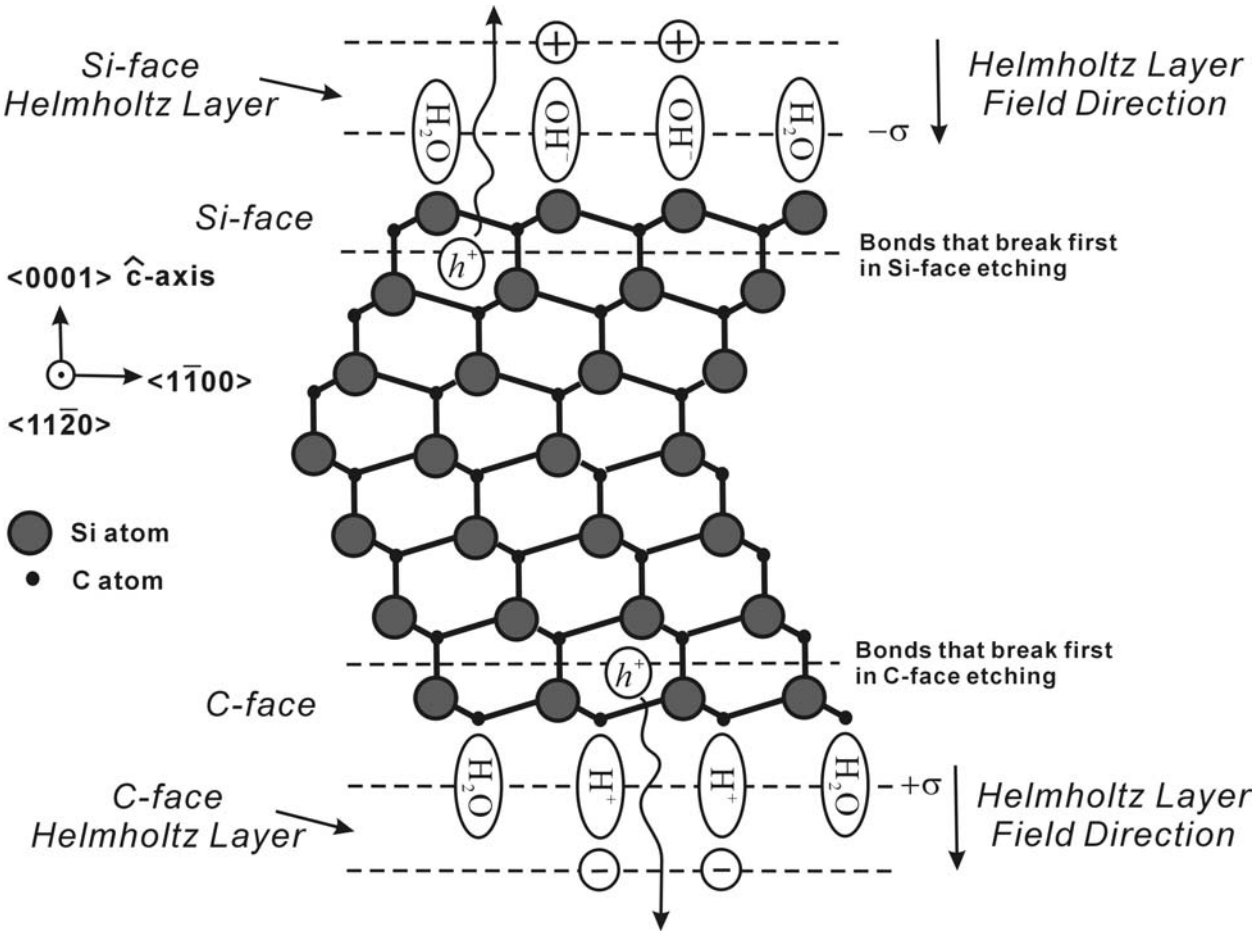

Figure 3.40 Schematic diagram of polar SiC surfaces in contact with aqueous electrolyte. The compensation charges ±σ are representations of adsorbed ions.

Here, we suggest that the reason for the different pore morphology formation on the two different surfaces lies in the different surface Helmholtz layer. In the case of SiC etching, for the Si-face, the adsorbed ion for the inner Helmholtz layer is negative. The outer Helmholtz layer is thus positive. Therefore, the internal electric field in the Helmholtz layer is oriented toward the

crystal surface (Figure 3.40). Although the thickness of the Helmholtz layer is thin and the voltage change across this layer is small, the field is respectable and is on the order of 10^5 V/cm. The direction of this field on Si-face is against the electronic transfer direction we need for the anodic etching. This field therefore hinders electron transfer into the SiC, or hole transfer into the solution.

On the other hand, for the C-face, the field direction in the Helmholtz layer is just the opposite of the case on the Si-face. The field will then aid the electrochemical charge transfer in the anodic etching. The energetically much easier charge transfer across the Helmholtz layer on the C-face leads to a much larger current density and much faster reaction rate than on the Si-face.

As a conclusion, we believe that the nano-columnar pore formation is only possible because of the anisotropic oxidation reaction rate and the anisotropic spontaneous Helmholtz layer field on different SiC faces. The oxidation reactions that take place in the nano-columnar pore formation are very similar as those in the electrochemical etchings lead to other pore morphology formation.

3.11.4 The charge transfer across the SiC/electrolyte interface during the columnar pore formation

From previous sections of this chapter, we learned that the electrochemical reaction requires holes. The electrochemical process could be pictured as hole transfer from the solid to the solution. The understanding of this minority carrier transfer across the interface, even

qualitatively, helps us to understand the pore formation mechanism. Based on the double layer model discussion sections 3.10 and 3.11, we investigate the hole transfer process during the pore formation.

Because SiC is a large band gap ($E_G = 3\ eV$) semiconductor, the valence band minority carrier density is very small (a few per cm^3) in highly doped n-type material according to equation 3.8. Therefore, for an n-type doped SiC, there are generally two ways to create the necessary holes for the electrochemical reaction. One is by above band gap UV illumination; the other is by breakdown (tunneling or avalanche). The attenuation of UV light due to the absorption is neglected in this discussion. Not only because the penetration depth[84] of above bandgap UV light is large (about two mm at 4000 Å wavelength) for 4H and 6H SiC, but also the penetration depth inside the PSC is complicated by significant scattering. Besides, since earlier experiments on 6H SiC doped at 1×10^{18} cm^{-3} show that the current decay is the same with or without UV illumination, we here neglect the UV light attenuation to simplify our discussion.

In most of our experiments, we use highly doped n-type 4H and 6H SiC material (10^{17}-5×10^{18} cm^{-3}). The breakdown study with highly doped material is not usual. Based on the article we found on 4H SiC[85], we here choose a 4H SiC sample doped at 1×10^{18} cm^{-3} as an example. The experiment shows that the voltage needed for columnar pore formation is about 45 V in 10% HF and 5% ethanol solution (weight percentage). Since the SiC sample is reverse biased, we first illustrate the three possible band bending schemes and the measured current-voltage scan in Figure 3.41.

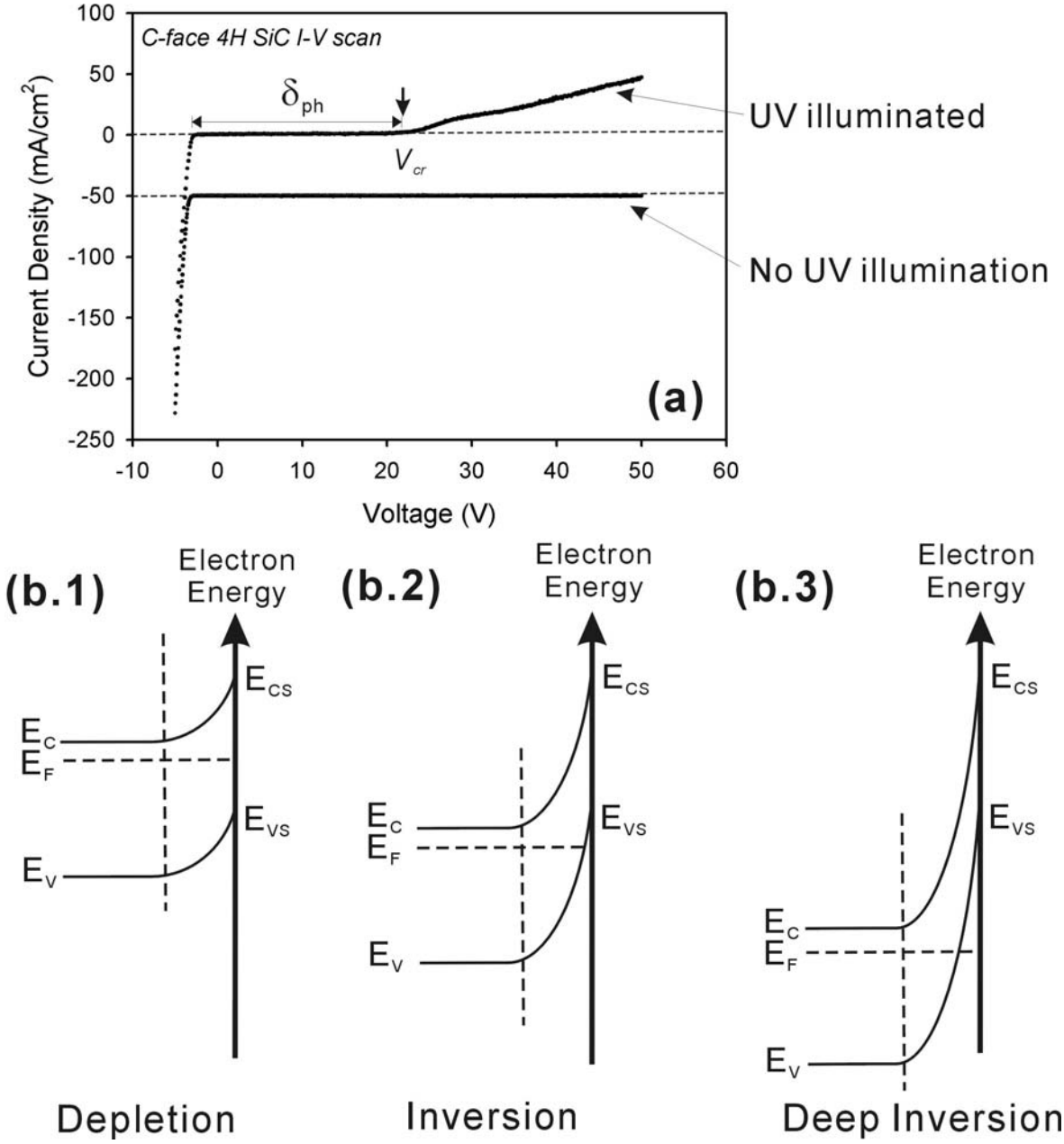

Figure 3.41 (a) Current-voltage scan on C-face 4H SiC doped at 1×10^{18} cm^{-3} in 10% HF, 5% ethanol electrolyte. The scan rate is 0.1 V/s. The curve recorded without UV illumination is lowered by 50 mA/cm^2 to distinguish the curves better. (b) The possible reverse biased electron energy band diagrams: (b.1) depletion, (b.2) inversion, and (b.3) deep inversion. There are minority carriers accumulated in the inverted valence band area.

3.11.4.1 Initial stage during the columnar pore formation

The etching process begins with a flat surface. In the absence of significant anodic current flow (< 1 mA/cm^2), there should be little pore formation (less than 100 nm thick porous layer formation caused by the scan). Therefore, the semiconductor/electrolyte interface is not changed significantly due to the pore formation. The electron band near the semiconductor surface during the initial stage of porous structure formation can be described by using a one dimensional Poisson's equation, assuming that the SiC sample has no compensation, uniform doping and complete ionization, in the space charge region[29]:

$$\frac{d^2V_{sc}}{dx^2} = qN_D / \kappa\varepsilon_0 . \qquad \textbf{3.23}$$

The solution for the electric field at the semiconductor surface (x=0) is therefore:

$$E_{x=0} = \sqrt{\frac{2qN_D}{\kappa\varepsilon_0}\phi_{sc}} , \qquad \textbf{3.24}$$

where q is the charge of a hole, N_D is the doping of the SiC, κ is the dielectric constant of SiC, ε_0 is the vacuum permittivity, ϕ_{sc} is the total potential drop across the space charge region, V_{sc} is the potential in the space charge region, x is the one dimensional coordinate axis perpendicular to the interface with 0 defined at the interface, and $E_{x=0}$ is the maximum electric field, which occurs at the interface. The breakdown field for 1×10^{18} cm^{-3} 4H SiC is about 4.98×10^8 V/m[85]. Therefore the breakdown voltage is about 70 V. If there is no UV illumination and the breakdown voltage is not reached, the free hole density is so low that, even if the total voltage drop is across the space charge region and E_F is far lower than E_p^{decomp}, we will not observe significant anodic current. This is confirmed by our observation in the I-V scan without UV illumination from

-5→50V in Figure 3.41a. It needs to be pointed out that, if the actual SiC surface is either not ideally flat enough (any scratches and surface dents) or the surface defects density is high enough, the breakdown voltage can be much lower than the ideal value. Therefore, the surface scratches or an initial pattern will assist the pore initiation in the absence of UV illumination.

If UV illumination is applied, we use Poisson's equations to describe a steady state but not an equilibrium state potential profile near the semiconductor surface. When UV light is applied onto the sample surface, we do not see an obvious anodic current flow until 20 V bias voltage is reached. We can estimate using Eq. 3.8 that for highly doped material, the hole density in the n-type (1×10^{18} cm^{-3}) 4H or 6H SiC at equilibrium is about 1 cm^{-3}. From the impedance measurements (Figure 3.35), we know that the UV illumination will decrease the resistance at low frequency by 3 orders of magnitude. We therefore deduce that there should be approximately 10^3 free holes per cm^3 induced by UV light at the semiconductor surface available for the electrochemical reaction. However, the *I-V* scans below 20 V in Figure 3.41a show only approximately a factor of five current density increase due to the UV illumination. Moreover, the current density under the UV illumination does not increase with the voltage either.

Assume that the system is in steady state when the voltage applied is lower than 20 V but larger than 3 V. The relative large reverse bias shifts E_F below E_{vs}. Considering the free minority carriers induced by the UV illumination, we believe that an inversion layer or deep inversion layer near the semiconductor surface is present, as shown in Figure 3.41b.2 or Figure 3.41b.3. The photon induced holes will be swept to the semiconductor surface by the electric field. Since the current density doesn't increase as much as the hole density does, we believe most of the holes are then transferred and stored on the inner Helmholtz layer plane (adsorbed ion layer) as explained in section 3.10.

If we assume that the capacitance of the Helmholtz layer does not change, the voltage drop across the Helmholtz layer will then increase. We therefore suggest that a significant current flow is only possible when a large voltage drop is occurring on the Helmholtz layer to enable any significant charge transfer across the Helmholtz layer, as in the case of breaking down an ideal capacitor. In this experiment, a critical voltage V_{cr} is present in order for a significant current to be observed (Figure 3.41a), which supports our assumption. The region δ_{ph} (Figure 3.41a) covers the voltage range from 0- V_{cr} in the *I-V* scan. δ_{ph} roughly corresponds to the voltage range that will lead to triangular pore formation, although in the real triangular pore formation, the voltage has to be larger than 1 V to obtain a reasonable etching rate. We suggest that when $V<V_{cr}$, the charge exchange rate across the Helmholtz layer is low and limits the current that can flow in the system.

Critical voltage V_{cr} is observed in all I-V scans on different doped n-type 4H and 6H SiC materials (Figure 3.42). For both polytypes, we did not find any doping dependence of V_{cr}. However, for 6H SiC doped from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}, V_{cr} is varying between 5-15 V. For 4H SiC doped from 5×10^{17} cm^{-3} to 1×10^{18} cm^{-3}, V_{cr} is between 15-25 V. We therefore conclude that for highly doped 6H SiC, $V_{cr} = 10 \pm 5\ V$. And for highly doped 4H SiC, $V_{cr} = 20 \pm 5\ V$. The reason for the 10 V V_{cr} shift between 4H and 6H SiC remains unclear at the moment. The current drawn with the voltage below V_{cr} does not increase with the voltage significantly. Again, we suggest that for different doped 4H and 6H SiC materials, the Helmholtz layer limits and decides the charge transfer rate.

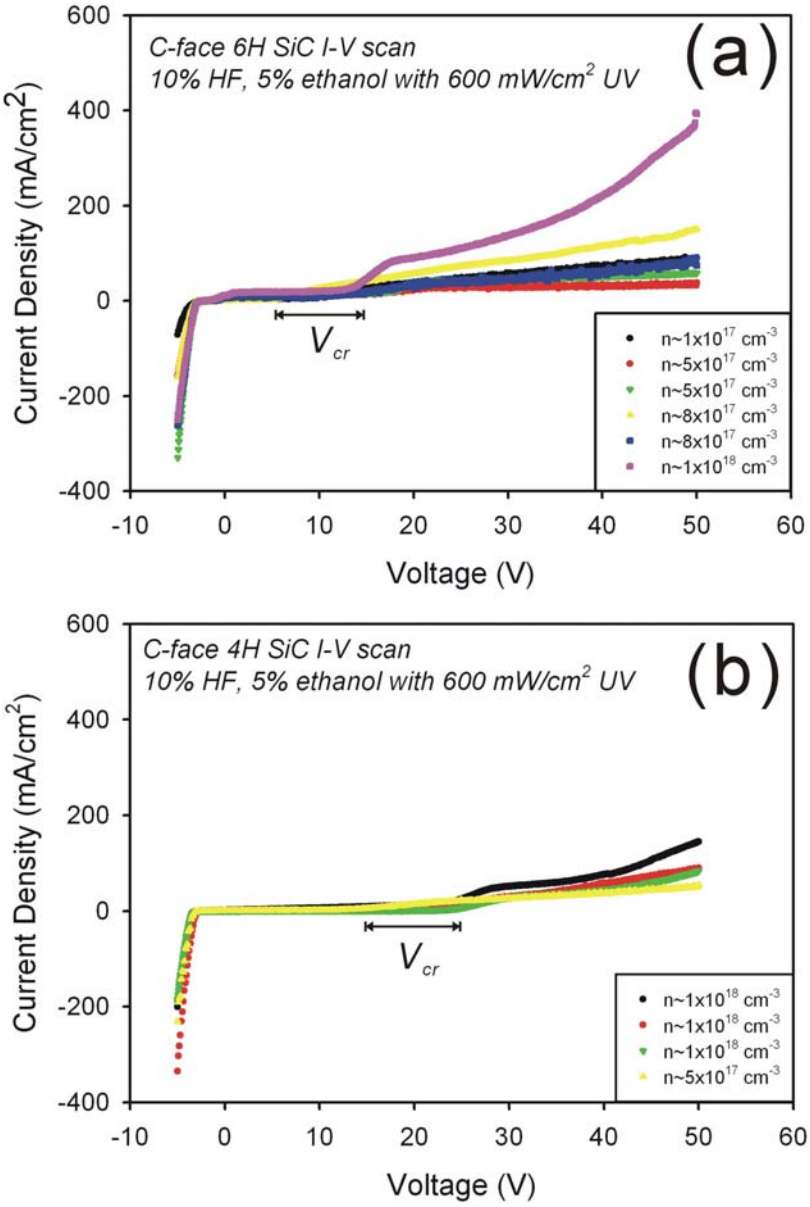

Figure 3.42 (a) I-V scans on C-face 6H SiC doped from 1×10^{17} to 1×10^{18} cm^{-3}. (b)) I-V scans on C-face 4H SiC doped from 5×10^{17} to 1×10^{18} cm^{-3}. In both sets of experiments, the electrolyte is 10%HF and 5% ethanol. UV illumination is at 600 mW/cm^2. Each scan is performed on unique wafer material even when the doping is claimed to be the same. Different scan rates ranged from 0.1 V/s to 1V/s have been applied. V_{cr} specifies the voltage at which a significant current increase is observed. The ranges of V_{cr} are indicated for different doped 4H and 6H SiC materials on the plots by doubly arrowed lines.

3.11.4.2 Steady state of the nano-columnar pore formation

Once the columnar pores form, the pore/electrolyte interface will change the interface geometry from a plane sheet to a cylinder (pore wall) or a hemisphere (pore tip). The curvature involved in the two geometric morphologies will then influence the potential distribution in the space charge region of the semiconductor. The potential and field can be calculated using cylindrical and spherical Poisson's equations. We first investigate the charge transfer (chemical reaction) only happens at the pore tip.

For pore tip, the charge distribution doesn't have angle dependence. The potential distribution calculations in the spherical pores tip reduce to single variable radial Poisson's equations written as below.

$$\textbf{Spherical: } \frac{2}{r}\frac{dV}{dr}+\frac{d^2V}{dr^2}=-\frac{qN_D}{\kappa\varepsilon_0} \qquad \textbf{3.25}$$

The parameters have their usual definitions. Omitting all the calculational details, we first use the spherical Poisson's equation to discuss the potential distribution near the pore tip. For the proper calculations, we need to know more about the boundary conditions to determine the voltage drop across the space charge region.

We therefore performed an experiment without UV illumination to see whether electronic breakdown (tunneling or breakdown) field is reached in the SiC crystals. The experimental results are shown in Figure 3.43. The experiments were performed using n-type C-face 6H SiC doped at 1×10^{18} cm^{-3}. The electrolytic solution used in 10% HF mixed with 5% ethanol (weight percentage). In both case, 20 V was applied for one hour. The only different etching condition is the UV illumination. In one experiment, we carried out the experiment in the dark (Figure 3.43c and d). The other experiment was performed with 600 mW/cm^2 UV light (Figure 3.43a and b).

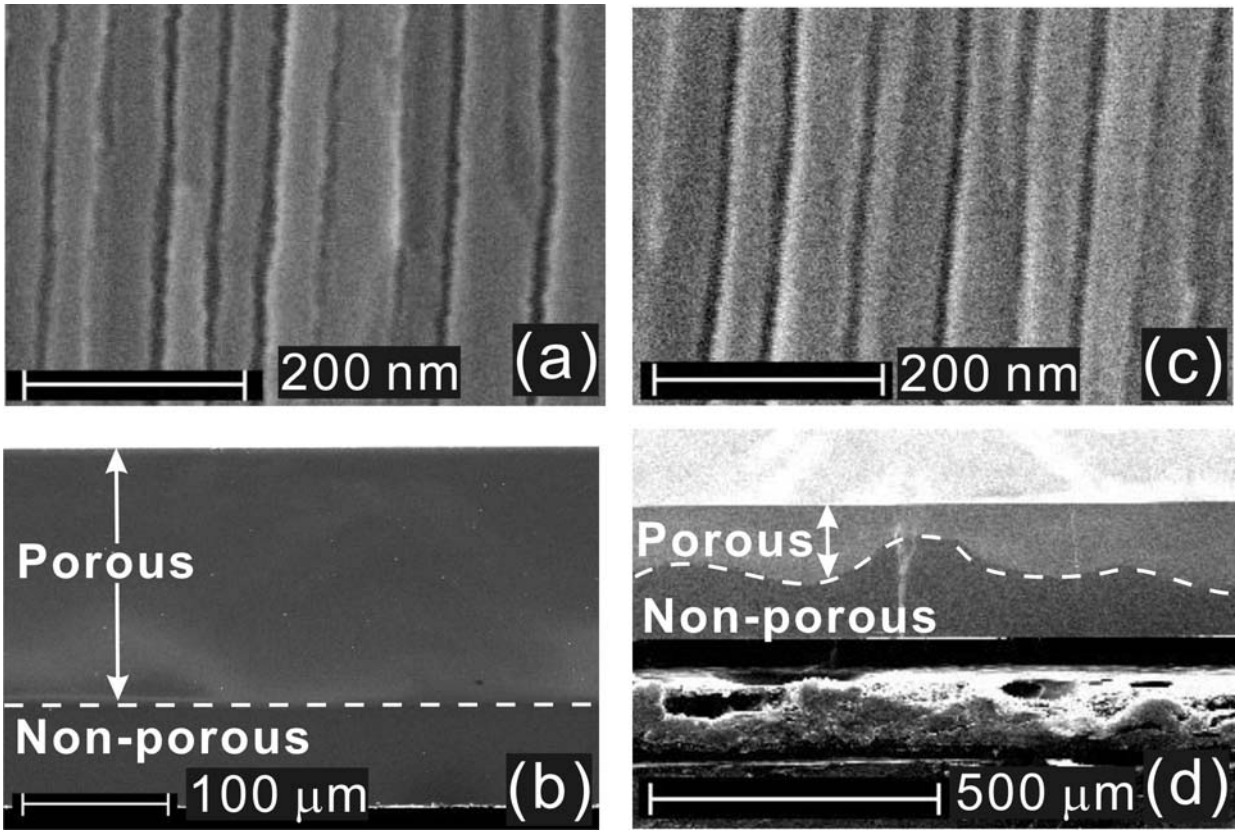

Figure 3.43 Cross sectional SEM images of the porous sample etched with UV illumination: (a) nano-columnar pores and (b) complete view of the porous layer. Cross sectional SEM images of the porous sample etched without UV illumination: (a) nano-columnar pores and (b) complete view of the porous layer.

These experiments show that the nano-columnar pores form without the UV illumination. The difference is the homogeneity of the porous layer thickness across the sample. if the experiment is carried in the dark, the porous layer thickness fluctuate between 70 and 200 μm, while the porous layer obtained with UV assist has a uniform porous layer thickness at about 200 μm. The experiment proves that electric breakdown does occur in the semiconductor at the pore tip. The UV illumination will improve the homogeneity of the nano-columnar porous structure.

For our calculation, knowing that some kind of electric breakdown is occurring at the pore tip, we would like to search in the literatures to find out the breakdown field for n-type SiC. A. Konstantinov[85] did research on the avalanche breakdown effect of n-type 4H SiC. Therefore,

we here use their 4H SiC breakdown field in our calculation and discussion as the boundary condition at the SiC pore surface (we believe that the situation for 6H SiC is also similar in the principle).

For 4H SiC doped at 1×10^{18} cm^{-3}, the critical electric field to obtain electric breakdown is about 4.98×10^{6} V/cm.[85] Using this value as the field boundary condition at the surface (r=10 nm, which is radius of the pore tip observed in experiments) of the spherical Poisson's equation (Eq. 3.25), we calculated that the corresponding breakdown voltage needed across the space charge region is about 3 V.

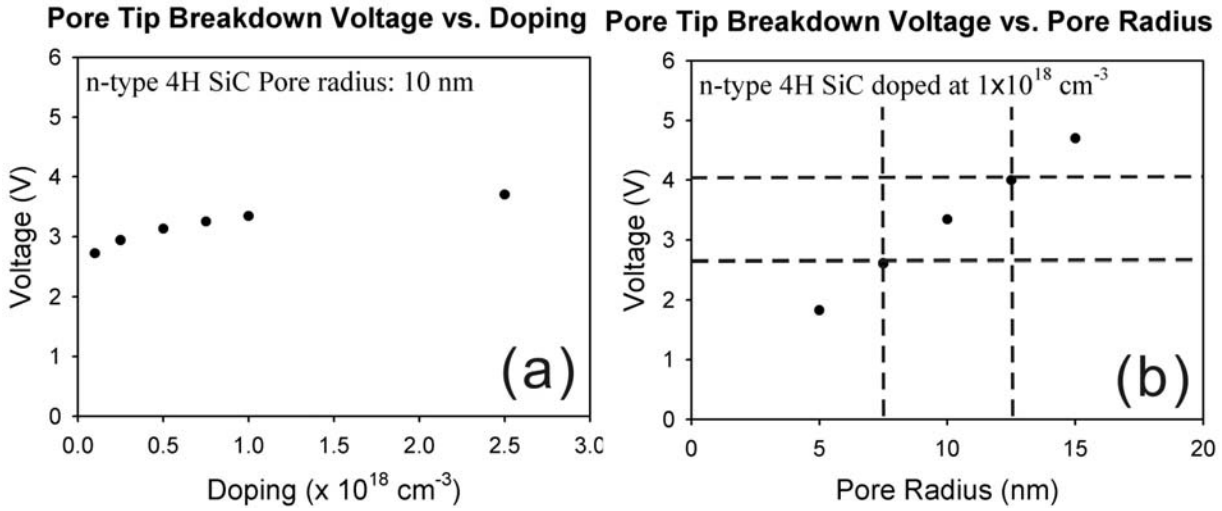

Figure 3.44 (a) Calculated critical voltage dependence of doping at the 10 nm columnar pore tip in n-type 4H SiC. (b) Calculated critical voltage dependence of pore radius in 1×10^{18} cm^{-3} doped n-type 4H SiC. The four dashed lines show that a small variance of radius (7.5 nm- 12.5 nm) can cover the critical voltage range (2.7 V-3.7 V) that is found for different doped material.

We then use the same calculation and critical field values from A. Konstantinov's article[85] to calculate the required voltage to achieve breakdown at the pore tip in differently

doped 4H SiC samples. And we can also calculate the critical voltage dependence of the pore radius in n~1×10^{18} cm^{-3} n-type 4H SiC. The results are shown in Figure 3.44. The results indeed show that the critical voltage does not change much with the doping. In the range of the doping discussed in this work, the critical voltage is in the range between 2.7-3.7 V. Later calculations show that if a small variation of pore radius from 7.5 nm to 12.5 (diameter 20±5 nm) will cause the critical voltage to change from 2.7-4 V. The later voltage range covers the voltage variation needed due to the different doping of SiC. This explains the experiment observations where the columnar diameter does not change with the SiC doping. The columnar pore diameter is therefore fixed at 20±5 nm.

Since 4H and 6H SiC band gap are about 3 V, 3 V is also the minimum band bending voltage to obtain inversion at equilibrium. In a steady state with the assumption proposed earlier that all the holes are removed quickly from the semiconductor bend banding region, it seems that E_F also needs to be pinned below E_{vs} so that holes could be first temporarily accumulated at the surface valence band edge and then steadily transferred into the Helmholtz layer or the chemical reactions. We deduce that only when E_F is pinned below E_{vs} and meanwhile breakdown field is reached at the pore tip interface, a large hole concentration could be possibly accumulated on inner Helmholtz layer plane, which leads to a high voltage drop across the layer to obtain a significant steady charge transfer. This agrees with our earlier discussion in section 3.11.4.1, where we were dealing with a flat interface without any existence of pores.

Based on above discussions, we believe that for any nano-columnar pore formation, the voltage across the pore tip space charge region is always about 3 V so that E_F is pinned just below E_{vs}. Breakdown condition at the surface is satisfied by the pore tip radius of curvature being about 10 nm.

3.11.5 The depletion of nano-columnar pore wall

For a cylindrical pore wall, the charge is uniform in the axial direction and also does not have angle dependence. The potential distribution calculations in the cylindrical pores wall reduce to single variable radial Poisson's equations written as below.

Cylindrical: $$\frac{1}{r}\frac{dV}{dr}+\frac{d^2V}{dr^2}=-\frac{qN_D}{\kappa\varepsilon_0} \qquad \textbf{3.26}$$

(Solution: $V=-\frac{qN_D}{4\kappa\varepsilon_0}r^2+C_1\ln r+C_2$ **),**

where the variables have their usual definitions. C_1 and C_2 in the solution are the constants defined by the boundary conditions in specific problems.

Using the cylindrical Poisson's equation 3.26, and assuming that the voltage across the pore wall is the same as the voltage drop at the pore tip (3 V), we can calculate the field at the interface to be about 7.2×10^5 V/cm. The corresponding depletion width is about 43 nm. This suggests that if the pore wall is under the same bias voltage as that at the pore tip, electric breakdown at the pore wall does not occur.

During the reaction, we believe the pore wall is depleted because there should be no holes available in the pore wall for the electrochemical reaction. Since we apply UV illumination during the etching, we propose that at pore wall surface, E_F is above E_{vs} so that inversion will not occur. The above argument is supported by the experimental observation: the electrochemical reactions only happen at the pore tip because the pores diameters are not changing during the process. This is only possible during the etching because no applied voltage is across the pore wall interface. The direction of the applied field is the same as the direction of the columnar pore growth. The surface direction of pore wall interface is therefore perpendicular to the direction of

the applied field direction. Therefore, no applied voltage drop is occurred at the pore wall interface. The voltage drop at the pore wall surface is only due to the Fermi level pinning in the SiC lattice.

Therefore, the depletion of the pore wall is caused by the spontaneous equilibrium band bending at the interface, as shown in Figure 3.33. The fact that the formed porous structure is stable in HF electrolyte also supports this assumption. As shown in Figure 3.45, the minimum depletion width to deplete the entire pore wall SiC crystal (nano-columnar porous structure has a 20 nm pore diameter and 60 nm interpore spacing) is about 25 nm. According to equation 3.26, the corresponded voltage drop across the space charge region is about 0.9 V.

If we use the band bending model proposed by M. Gleria and R. Memming[11], the conduction band edge at the surface at equilibrium is about -1.4 V vs. NHE. The open circuit potential between the PSC and Platinum (Pt) counter electrode is observed to be about -0.5 V in the dark. If we believe that at equilibrium the electrochemical potential of Pt in the solution is very close to that of a NHE, the Fermi level of semiconductor in Figure 3.33 is 0.5 V above 0 in the electron energy scale (-0.5 V vs. NHE). The band bending at the interface is therefore about 0.9 V, which happens to be the same as the voltage needed for the 25 nm depletion width in the pore wall. This could explain why the largest average interpore spacing one can obtain so far is about 60 nm.

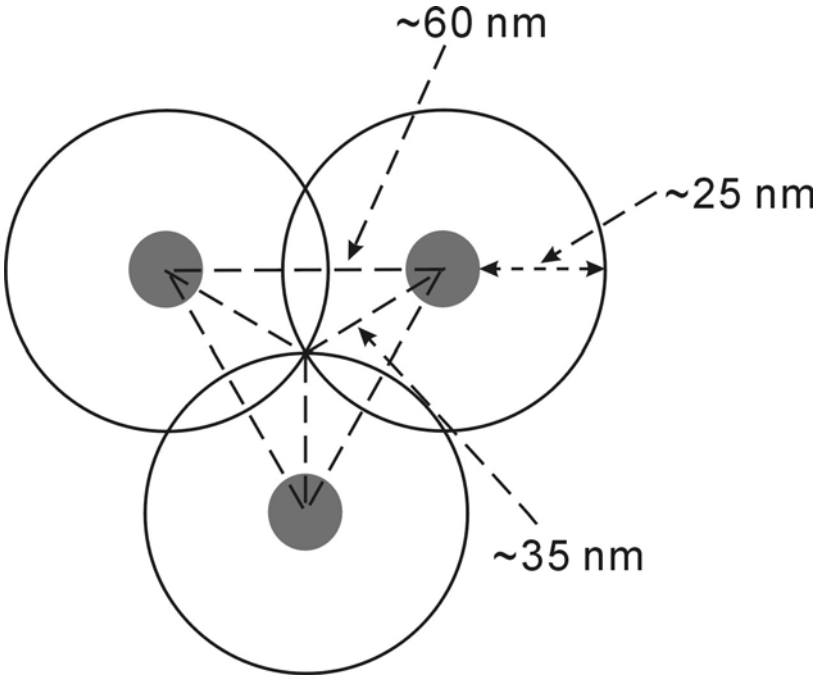

Figure 3.45 The diagram of the planar top view of the ideal nano-columnar pore lattice. The dark circles are the pores with 10 nm radius. The corresponded depletion region edge is represented by a concentric circle. The interpore distance is measured to be 60 nm (section 3.2). If the entire pore wall is depleted, the minimum radius of the depletion region circle is then about 35 nm. The thickness of the depletion layer is then about 25 nm.

It is, however, possible to obtain a closer packed nano-columnar porous structure with smaller interpore spacing. According to the experimental observations, such as the result shown in Figure 3.8, the interpore spacing can be changed by the applied etching voltage in such a way that, the larger applied voltage, the closer pores will be (thinner pore walls). Of course, if the applied voltage is too large, the formed porous structure becomes unstable in terms of the porous layer thickness and also one micron diameter pores will appear. A possible qualitative suggestion is: the density of the pores is decided by the charge transfer rate during the etching. The higher reaction rate under larger applied voltage (larger current) means more 20 nm diameter pores can form. These pores will, somehow, distribute in a uniform manner and thus reduce the pore wall

thickness. It seems that if the pore wall thickness is smaller than 40 nm, the nano-columnar pore growth will be unstable. On the other hand, the spontaneous band bending at the pore wall surface decides the maximum depletion width in the pore wall lattice and therefore decides the largest interpore spacing, which is 60 nm. If pore wall thickness is beyond this value, it will lead to un-depleted pore wall structure. The pores can then form at these locations between the original pores. And as a result, the pore wall thickness will be then reduced.

3.11.6 The current decay during the columnar pore formation

As the columnar pores are formed, there is a characteristic current decay after an initial time interval. The current decays as a power law (Eq. 3.4) with exponent 0.4. More experiments (Figure 3.16 for example) show that the decay exponent can be in a range from 0.4 to 0.5. To understand the mechanism of the current decay, here we use the current density curve recorded during the etching of a 6H SiC sample doped at about 1×10^{18} cm^{-3} as an example. 600 mW/cm^2 UV illumination is used during the etching process. The electrolytic solution is 10% HF and 5% ethanol. The experimental results and the model we propose to attempt to explain this phenomenon are shown in Figure 3.46.

Before we discuss a possible model to describe the current decay, it is worth mentioning that a diffusion process leads to a 0.5 power decay[30] in concentration profile at the steady state. However, we believe that it is inappropriate to apply it here. There are two reasons: First, in our experiments, the constant etching of SiC causes a moving boundary (pore tip), which is described in the diffusion model. Second, during the etching, the large current also indicates a possible ion migration process, which cannot be explained by the ion diffusion.

The experiment data we use here is recorded during the columnar pore formation in 1×10^{18} cm^{-3} n-type doped 6H SiC. The total voltage applied is about 20V. The electrolytic solution is aqueous 10% HF and 5% ethanol (weight percentage). The current density –time and voltammetry scan curves are shown in Figure 3.46a and b respectively.

The model we attempt to use is based on an equivalent circuit model shown schematically in Figure 3.46d that represents the electrochemical system. As the first step to construct a possible model, we neglect the concentration variation and assume that the electrolyte concentration is the same everywhere even inside the pores. If the solution resistivity is larger than the bulk SiC material, as the columnar pore length ℓ increases with time, the resistance of the system should increase. This change will therefore change the voltage distribution across the different elements including the voltage drop across the interface (space charge region and Helmholtz layer).

First we write down the loop equation:

$$V - IR_{Pores} - IR_{SiC} - V_{Interface} = 0. \qquad \textbf{3.27}$$

I is the measured current (mA), V is the applied voltage (V), $V_{Interface}$ is the voltage drop across the SiC space charge region and Helmholtz layer (V), R_{Pores} is the resistance of the electrolyte inside the pores (Ω), and R_{SiC} is the bulk SiC material resistance (Ω). From equation 3.27 we have

$$V - J\rho_{Pores}\ell - J\rho_{SiC}(L-\ell) = V_{Interface}. \qquad (\ell<L) \qquad \textbf{3.28}$$

J is the current density (mA/cm^2), ρ_{Pores} and ρ_{SiC} are the resistivity of the electrolyte inside the pores and the bulk SiC material respectively (Ω-cm).

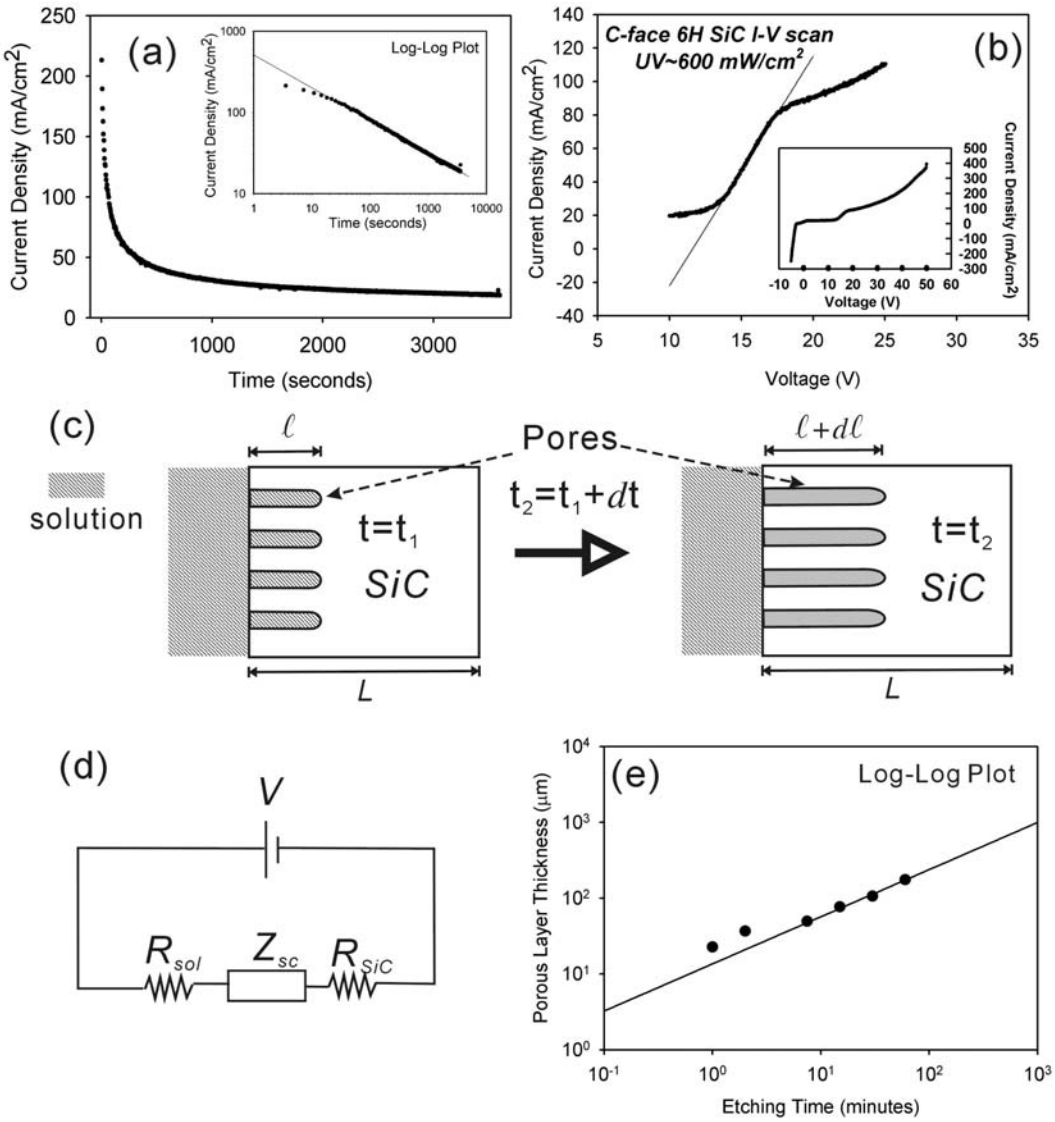

Figure 3.46 (a) The current density decay during the columnar pore formation. The inset shows the same curve on a double log scale. The solid line is the fit of the linear part of the curve in the double log scale. (b) A section of the current-voltage scan performed under UV illumination. The solid line shows the linear fit between 13 V and 18 V. The inset shows the complete scan. (c) Schematic drawing of the columnar pore growth. ℓ is the thickness of the porous layer. L is the thickness of original SiC sample. (d) The equivalent circuit we propose to describe the electrochemical cell. Z_{sc} describes the space charge impedance. (e) The columnar porous layer thickness as a function of etching time on a log-log plot. The solid line is the fit of the four data points at later etching time, as will be explained in the text.

To find out the relationship between V_{sc} and J, we here use a J-V scan data as shown in Figure 3.46b. In an ideal fast J-V scan, ℓ is small and thus means no porous formation. Because ρ_{SiC} is small for highly doped material, based on Eq. 3.27, we have $V \approx V_{Interface}$. The J-V scan therefore can represent the J-$V_{Interface}$ relation. Because during the nano columnar pore formation, in the time intervals between 100 to 3600 s, J decays from 100 to 20 mA/cm^2. This range of J corresponds to a linear part in the J-V scan curve (Figure 3.46b) between the voltage about 13 V and 18 V. If we here use linear function as the first approximation, the result is then:

$$V_{Interface} = 11.6 + 0.073J\,, \qquad \textbf{3.29}$$

as shown in Figure 3.46b. Since the pore etching is a Faradic process and the instant current density determines the etching rate of the SiC material, if we have perfect cylindrical pores with known pore diameter and uniform porosity, we can then express the relation between I and ℓ as:

$$J = D\frac{d\ell}{dt} \qquad \textbf{3.30}$$

The equation 3.30 is conceptually validated by the porous layer growth rate experiment as shown in Figure 3.46e. The thickness increases with time as a power law with exponent 0.6, when the etching time is longer than 2 min. Eq. 3.30 then predicts J~t$^{-0.4}$, which is in agreement with the measured current decay (Figure 3.46a).

γ has been defined earlier (section 3.2) as the number of holes needed for etching one SiC pair, therefore we have the relation:

$$\frac{dn_h}{\gamma} = \frac{dV_p}{V_0}. \qquad \textbf{3.31}$$

n_h is the number of holes that have been consumed during the etching of SiC, V_p is the volume of pores and V_0 is the volume of single SiC pair. For a simple columnar morphology, the volume of pores is "the area of the pores (A_{pore})"× "the length of the pores (ℓ)". The area of the pores is 10% of the total area of the sample (A) because of the 10% porosity. We then have the relation:

$$\frac{dn_h}{\gamma}=\frac{0.1Ad\ell}{V_0}\Rightarrow\frac{dn_h}{A}=\frac{0.1\gamma d\ell}{V_0}\Rightarrow\frac{dQ}{eA}=\frac{0.1\gamma d\ell}{V_0}\Rightarrow Jdt=\frac{0.1\gamma e}{V_0}d\ell\Rightarrow J=\frac{0.1\gamma e}{V_0}(\frac{d\ell}{dt}) \quad \textbf{3.32}$$

Q is the charge (mC), t is the etching time, and e is the charge of hole. Compare Eq. 3.27 and Eq. 3.25, we have $D=\frac{0.1\gamma e}{V_0}$. As mentioned in section 3.2, V_0 is 20.7×10^{-24} cm^3. γ=7. e=1.6×10^{-16} mC. D is therefore calculated to be 5.4×10^6 mC/cm^3.

Insert Eq. 3.29 and 3.32 into Eq. 3.28, we have:

$$V-D\frac{d\ell}{dt}\rho_{sol}\ell-D\frac{d\ell}{dt}\rho_{SiC}(L-\ell)=11.6+0.073D\frac{d\ell}{dt} \quad \textbf{3.33}$$

V=20 V is the applied voltage. D =5.4×10^6 mC/cm^3. ρ_{SiC} is about 0.09 Ω-cm according to Eq. 3.5. For 10% HF, ρ_{Pores} is about 85 Ω-cm (because the porosity is 0.1, the area of the electrolyte is just 0.1 cm^2 if a sample of 1 cm^2 area is etched), based on the data in Table 3.4. Assume that the total thickness of the bulk SiC sample L is 300 μm. Insert all the numbers except ρ_{sol} and rearrange Eq. 3.33 to obtain:

$$1.6\times10^6-(\rho_{Pores}-0.09)\ell\frac{d\ell}{dt}-0.076\frac{d\ell}{dt}=0. \quad \textbf{3.34}$$

Eq. 3.34 has the only analytical solution for ℓ>0:

$$\ell = \frac{\rho_{Pores} - 0.09}{0.076}\left[\sqrt{1 + \frac{4.2\times10^{7}}{(\rho_{Pores} - 0.09)^{2}}t} - 1\right] \quad \textbf{3.35}$$

Substitute Eq. 3.35 into Eq. 3.30, we then have:

$$J = \frac{8.6\times10^{12}}{\rho_{Pores} - 0.09}\left[1 + \frac{4.2\times10^{7}}{(\rho_{Pores} - 0.09)^{2}}t\right]^{-\frac{1}{2}} \quad \textbf{3.36}$$

Eq. 3.36 shows that for this model, when $t \gg \frac{(\rho_{Pores} - 0.09)^2}{4.2\times10^{7}}$, $j \propto t^{-0.5}$. Figure 3.47a shows the plot of Eq. 3.36 when $\rho_{Pores} = 85\ \Omega\cdot cm$. The result appears to be a straight line in the double log plot with the exponent of 0.5 (β=0.5 in Eq. 3.4) in a power law decay, which is different from our experimental observations as shown in Figure 3.47a.

If we define ρ_{Pores} as an effective unit areal electrolyte resistivity in the pores, we can speculate that ρ_{Pores} could be much larger due to the microfludic diffusion and migration property inside the nano scale pores. When ρ_{Pores} is set to be 85×10^{4} Ω-cm, the curve shape of Eq. 3.36 changes in the range from 1 to 2000 s (Figure 3.47a). There seems to be a linear part in the double log scale between 200-2000 s. If we fit this part of the curve with the power law decay equation Eq. 3.4, the exponent we get is 0.43 (β=0.43), which is close to the experimental value 0.4.

It seems that by varying the value of ρ_{Pores}, we can obtain different β values in the range from 0 to 0.5. However, although it seems that using this model we can obtain any wanted decay constant β by adjusting ρ_{Pores}, we realized that when the decay constant is satisfactory (Figure 3.47a), the calculated current density values are much larger than the actual ones in the experimental data (Figure 3.47a). Also, if we plot the calculated porous layer thickness growth

curve using Eq. 3.35 in Figure 3.47b, it is observed that both curves for $\rho_{Pores} = 85\ \Omega \cdot cm$ and $\rho_{Pores} = 85 \times 10^4\ \Omega \cdot cm$ show a much larger porous layer thickness than L. This overrides the basic assumption of the model: $\ell < L$. Obviously, the calculated results do not agree with the experimental data. The model we developed here cannot explain the current decay we observe.

We believe the work of finding out more accurate and reliable J-$V_{Interface}$ relation is crucial to improve this model in the future:

(1) The current-voltage scan curve is dependent on the scan rate. Besides, when a voltammetry experiment is carried out in HF solution and UV illumination, pore formation is inevitable. The scan takes about 1 min to finish, during which an about 10 μm thick porous layer will form. More systematic J-V experiments should be performed with different scan rates (faster rates to reduce the pore formation, slower rates to reduce the charge accumulation at the interface) in order to improve the input to our model.

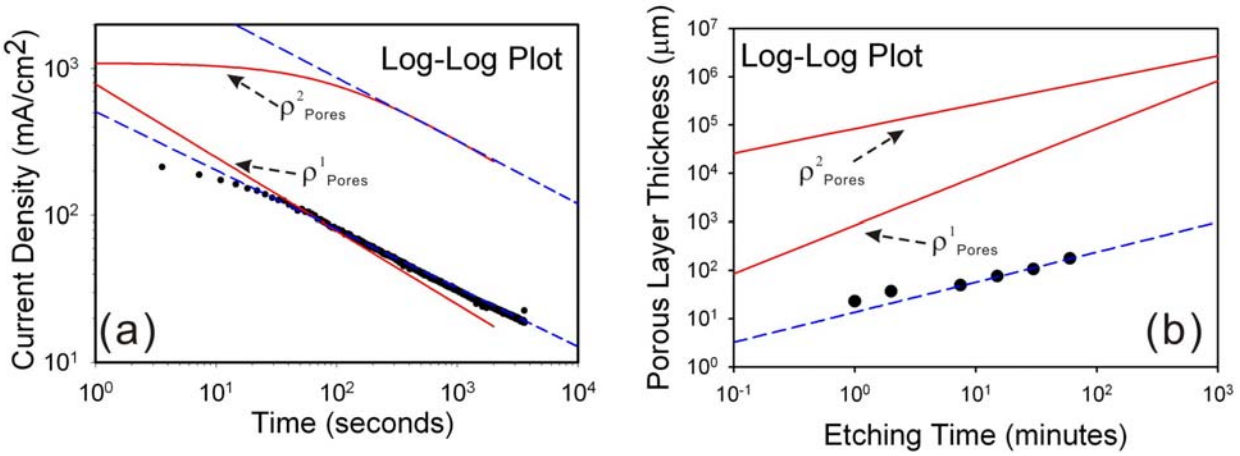

Figure 3.47 (a) Current density-time curves in the double log plot. The solid dots are the experimental data recorded during the columnar pore formation. The red solid lines are the calculated results based on Eq. 3.36 when

$\rho_{Pores} = \rho^1_{Pores} = 85\ \Omega \cdot cm$ and $\rho_{Pores} = \rho^2_{Pores} = 85 \times 10^4\ \Omega \cdot cm$ as indicated on the plot. The blue dashed lines are the fits using Eq. 3.4 ($J = A(t/t_0)^{-\beta}$). (b) The porous layer thickness (ℓ) vs. time plot (t) in the double log scale. The solid dots are the experimental data recorded. The red solid lines are the calculated results based on Eq. 3.35 when $\rho_{Pores} = \rho^1_{Pores} = 85\ \Omega \cdot cm$ and $\rho_{Pores} = \rho^2_{Pores} = 85 \times 10^4\ \Omega \cdot cm$ as indicated on the plot. The blue dashed line is the fit using an exponential rise equation: $\ell = \alpha(t/t_0)^{\eta}$. The exponent η here is found to be 0.6.

(2) In the fitting of J-$V_{Interface}$ curve, a nonlinear expression containing terms such as $J^{1/2}$, $J^{1/4}$, J^2, etc. will change the calculation result of Eq. 3.28. The nonlinear differential equation may give numerical solutions that agree with the experimental data.

(3) A much better model to describe the ρ_{Pores} inside the pores. ρ_{Pores} may not be a constant but vary with the depth ℓ caused by the ionic concentration decrease due to the diffusion effect inside the pores.

3.11.7 The voltage across the Helmholtz layer during nano-columnar pore formation

As discussed in section 3.11.6, without considering the details, the current decay during the etching suggests the voltage across the SiC/solution interface decreases during the nano columnar pores formation. During the etching, the current density finally drops to about 20 mA/cm^2. According to the I-V scan shown Figure 3.41a, the voltage drop across the interface during the etching is suggested to be between 45 V (total applied voltage) and 25 V.

The three voltages obeys the equation 3.17, which basically says that the summation of the three voltages (voltage across the pore tip space charge region, voltage across the Helmholtz layer at the interface, and voltage drop in the electrolyte inside the columnar pores) is the total voltage applied during the etching process. Assume that at some moment during the etching, the voltage drop in the electrolyte inside the columnar pores are about 5 V, the voltage drop across the semiconductor/solution interface, including the pore tip space charge region and Helmholtz layer, is 40 V. As we have shown in section 3.11.4, only 3 V drops across the Helmholtz layer. Therefore, 37 V of the 40 V voltage drop should occur across the Helmholtz layer at pore tips.

If the excessive voltage over 3V across the SiC/HF electrolyte interface is believed to drop across the Helmholtz layer, the voltage across the Helmholtz layer is decreasing as the etching proceeds because of the current decay (According to *J-V* scan, if current decreases, the voltage across the interface decreases). This explains why the nano-columnar pore growth rate will be slowing down as the etching proceeds. Although the quantitative model in section 3.11.6 to explain the current decay is failed, we still believe increase of the electrolyte resistance in the growing nano scale pores should be responsible to the current decrease. We believe that by applying a constant optimum voltage across the electrodes, an appropriate voltage across the Helmholtz layer is achieved during the whole etching process to satisfy the balanced delicate kinetics of the charge transfer across the interface. This kinetics could be influenced by the temperature, complicated chemical reactions, the ion transport in the electrolyte in the pores, reactant concentration change due to the diffusion of chemicals inside the pores, etc. This assumption is therefore supported by our experimental observations, such as the one shown in Figure 3.8.

The large voltage drop (42→22 V in this case) across the Helmholtz layer enables a high charge exchange rate. The additional voltage (0→20 V) in the electrolyte inside the columnar pores enables a fast ion migration, which is represented by the current density observed during the process (200→20 mA/cm^2). The optimum total voltages required for nano-columnar pore formation realize a balanced kinetic of the charge transfer rate across the three double layers. We suggest that the 3 V voltage drop across the pore tip space charge layer does not change by changing the applied total voltage. The external voltage applied larger than the optimum value will only increase the voltage drop across the Helmholtz layer and in the electrolytic solution. This will then only increase the change transfer rate, i.e., the current, and destroy the balanced kinetics of the charge transfer process. This explains why the resulting columnar pore diameter is always about 20±5nm, no matter how the applied voltage is changed. But the columnar pores may become torturous and columnar porous layer may have inhomogeneous thickness in the nano-columnar pore formation. For example, as shown in section 3.3, the experiments were carried out by applying 10 V, 20 V and 30 V to the n~1×10^{18} cm^{-3} doped 6H SiC (Figure 3.8). 20 V is found to be the optimum voltage. If the voltage is lower than the optimum value (i.e. 10 V), the 10 nm radius columnar pore is tortuous. If the voltage is larger than the optimum value (i.e. 30 V), the columnar pore growth becomes unstable. The optimum voltage is needed to satisfy what is probably a very complicated balance of charge transfer kinetics in the system during the whole etching process.

3.11.8 A complete picture of the charge transfer during the columnar pore formation

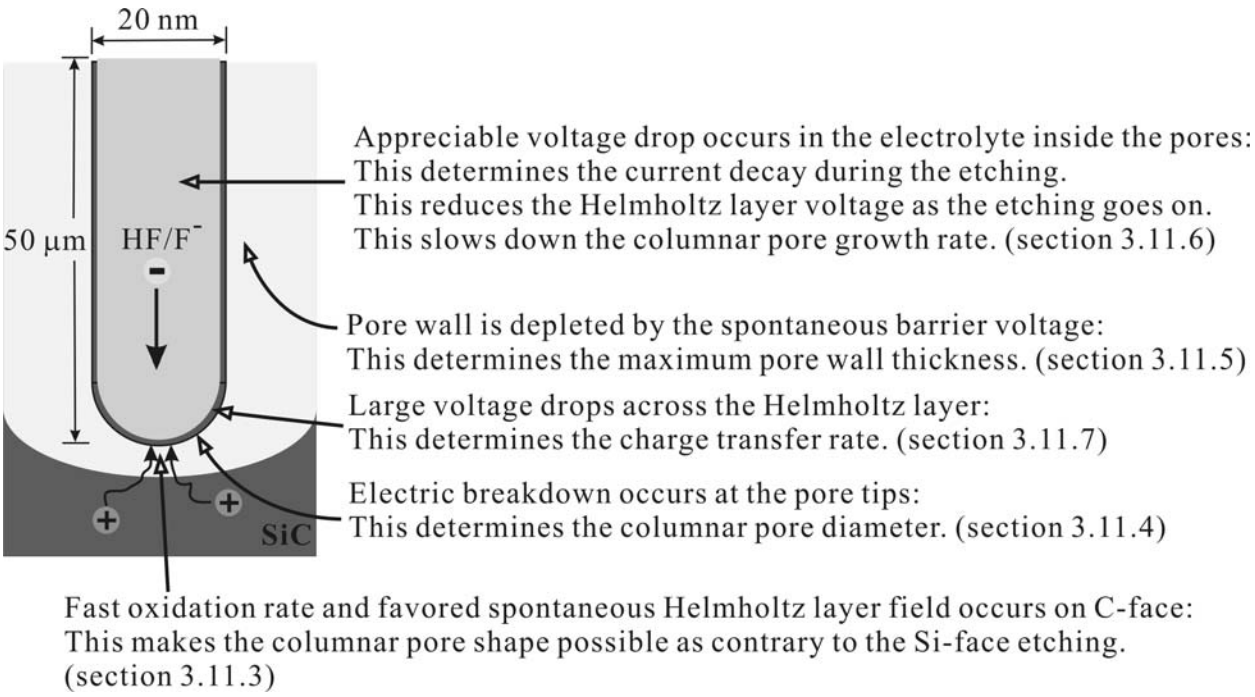

Figure 3.48 The complete picture to describe the physics process during the nano-columnar pore formation.

A picture is worth of thousand words. We conclude our discussion (section 3.11) in Figure 3.48. The details could be found in the corresponding subsections explained in the figure.

3.12 PORE NETWORK FORMATION (DIFFUSION LIMITED AGGREGATION SIMULATION)

The study of columnar pore formation naturally involves the study of pattern formation. Although some non-linear analysis can be found[86] that attempts to describe the initial pore formation, we found it is hard to apply the same method here simply because the columnar pore

formation does not resemble the initial process. The columnar pores are formed after a transition layer by self-organization (section 3.2).

In porous Si pore network formation study, a biased diffusion limited aggregation model was used to simulate the pattern formation[87]. We here use the same model and try to reproduce their work. The result is then compared to the porous cubic SiC fabricated[88] in our laboratory (Figure 3.50b). Based on this work, further work on the columnar pore formation in hexagonal SiC is in progress.

The simulation presented here models the dissolution on a two-dimensional grid representing a section of cubic Si. An ensemble of mobile electronic holes moves according to their spatial relationship to the Si/HF electrolyte interface. If the holes are not in the space charge region, far away from the SiC/HF electrolyte interface, their movement is controlled by a small electric field (highly doped material) and the motion is considered to be random. A multiparticle diffusion limited aggregation model[89,90,91] can be used. If the holes are within the space charge region, they will naturally be swept toward the pore tips, and their trajectories will be determined by the local electric field.

As the first step, we use a simplified model by neglecting the curvature effects of the space charge region to describe the hole movement within the high field region. Two parameters are defined and varied to control the simulation. (1) A fixed space charge layer thickness L. (defined by number of pixels). (2) We also define a simplified two dimensional minority charge density ρ (defined by the percentage of the total grids). More details can be found in the work by J. Erlebacher *et al*.[87]

In the beginning, an ensemble of holes is randomly dispersed on a 300×200 pixel rectangle grid at the given concentration. The top row of the grids is considered to be the initial

SiC/HF electrolyte interface. During a Monte Carlo iteration, each hole is moved according to rules determined by its position in the field, either in the space charge region or diffusional region. When a hole moves onto the interface, the SiC pair that resides at that lattice site is annihilated, and the pore extends onto that lattice site, locally moving the SiC/HF interface. Periodic boundary conditions are imposed on the sides of the growth field so that if a hole moves off either side of the lattice it is reinjected on the opposite side. The concentration of holes was maintained constant at the base of the lattice. A simulation was stopped as soon as the edge of the space charge region envelope reached the base of the grid. All hole motions were constrained to the four directions of the square lattice and holes were not allowed to overlap. The motion of particles in the high field region was biased so that their trajectories pointed to the nearest pore tip. On the square lattice, this corresponded to modifying the probability of motion in the four directions using the following construction, illustrated in Figure 3.49,

With no bias, the probability of motion in each direction is the same. If the hole movement is biased with the high electric field, the hole would tend to move towards the region of largest electric field, i.e., the pore tip. This will give a relative probability of movement as shown in Figure 3.49b. We use this in our program to carry out a biased random walk.

One of the simulation results with L=50 and ρ=0.5 is shown in Figure 3.50a. The result shows that the morphology resembles the actual porous structure formed in cubic SiC as shown in Figure 3.50b.

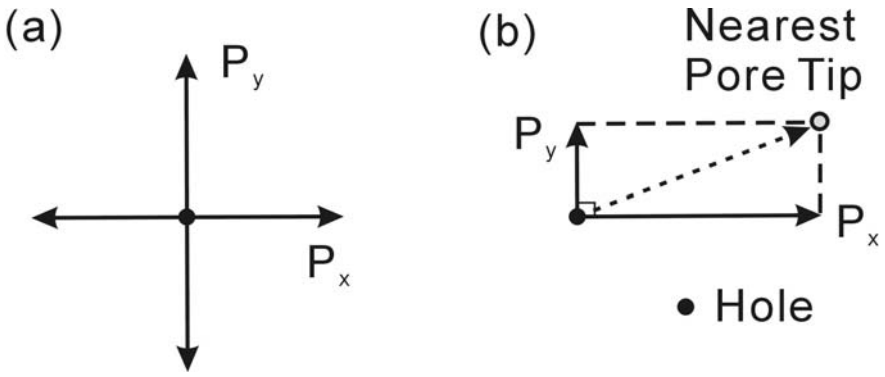

Figure 3.49 The probability for biasing random walkers on a square lattice. With no bias (a), the hole moves with equal probability in each of the four directions. If the motion of a hole is to be biased in a particular direction (b), the relative probability is defined by a decomposition of the probability vector. P_x and P_y are the probability of moving in x and y direction respectively. The total probability of P_x+P_y is unity.

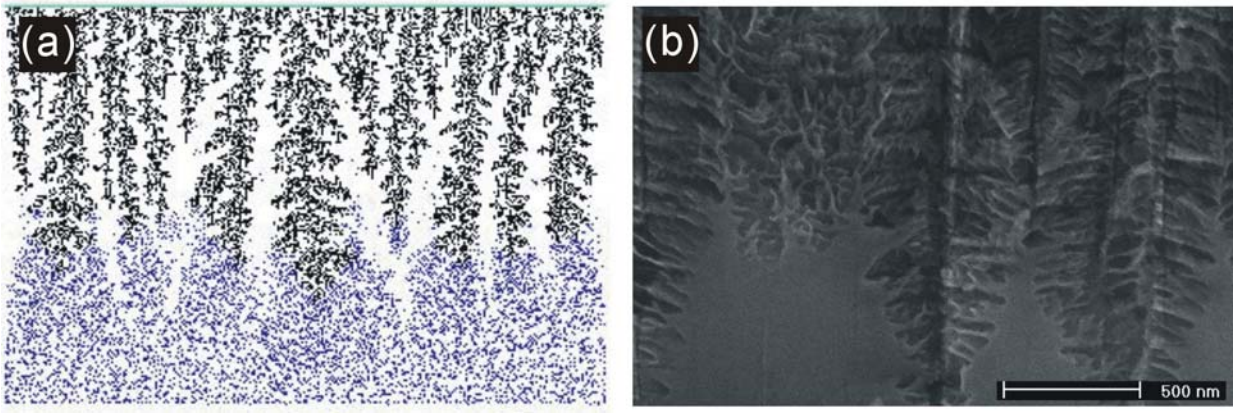

Figure 3.50 (a) The simulated porous structure using biased diffusion limited aggregation. The green line on the top is the initial HF/SiC interface. Dendritic black points are the formed pores. Blue dots uniformly distributed in the bottom are the simulated free holes. (b) Cross sectional SEM image of a porous 3C SiC sample.

Of course, the model we used here is oversimplified. There are a few more things we need to consider if we want to improve our simulation results.

(1) The real chemical reaction is not a one hole process, it takes seven holes to etch a SiC pair. This requires a detailed understanding of the chemical reaction route. This hasn't been done yet, to the best of our knowledge.

(2) Each grid stands for a lattice atom in this simulation. Si-Si bond length is about 5.4 Å.[92] The width of the total simulation area is about 160 nm. The scale of the simulation is therefore much smaller than the real porous morphology. A typical pore morphology is about 10-100 nm scale in our case, how to describe this is not easy.

(3) In the real etching, there are some preferential etching directions. This means that, in certain directions, the etching happens faster than in others. How to quantify this process and represent it by probabilities is not obvious.

(4) The field effect in this model is not considered. This is not a problem if the applied voltage and the drawn current are small. In many electrochemical etchings we performed, the actual current density could be as high as few hundred milliamps. The drifting of the holes inside the SiC is obvious and cannot be neglected. The modeling of the hot charge transfer is also challenging.

(5) In our nano columnar pore fabrication, the SiC lattice crystal is hexagonal instead of cubic. The holes move from lattice atom to lattice atom. It is necessary to define a new set of probable hole movement directions other than just x and y direction. We also need to find out the mobility anisotropy of holes in different polytypes.

(5) A two dimensional simulation does not truly resemble the real system (This is even true for the cubic crystal structure). We need a three dimensional simulation but this is not only difficult but also increases the work load of each simulation iteration greatly.

All the above considerations have to be taken to develop a more realistic simulation that can explain the pattern formation in the formation of the nano-columnar porous structure.

3.13 SUMMARY

Nano columnar pore formation is obtained on the C-face of n-type 6H and 4H SiC. It is found that a constant voltage condition, rather than constant current condition is needed for the uniform columnar pore formation. The voltage has to be optimized for the best columnar pore formation.

The experimental conclusions are summarized below:

(1) To form a nano-columnar porous structure in C-face SiC, an optimum voltage needs to be applied. (Section 3.2 and 3.3)

(2) The optimum voltage increases with the resistivity of the SiC material. The formed nano-columnar pore morphologies, however, are independent of the doping. The columnar pores are always around 20±5 nm diameter. The interpore spacing is about 40-60 nm. (Section 3.7)

(3) Surface conditions do not influence the columnar pore formation, which suggests that the surface patterning will neither improve nor change the nano-columnar formation process. (Section 3.4)

(4) Temperature will not influence the nano-columnar pore diameter in any obvious way. The higher temperature only increases the pore growth rate. The rate change is related to the faster reaction rate at higher temperature. (Section 3.5)

(5) The oscillation of the current during the pore formation is associated with the surface roughness and shows a unique frequency at about 0.6 Hz (Section 3.4). It is also found that the current oscillation at controlled temperature does not change with different voltages. This invalidates the application of current burst model to explain the porous SiC formation. (Section 3.5)

(6) HF concentration will change the columnar pore diameter and growth rate. This is related to the complicated HF chemistry which will change the oxide removal rate during the columnar pore formation. We believe at low concentration of HF, the pore growth is determined by the oxide removal rate by HF. In the cases of using high concentration of HF, the pore growth is determined by the charge transfer across the interface. The later one is the case we obtain the nano-columnar porous structure. In another word, to obtain nano-columnar porous structure, we ought to use an appropriately concentrated (2%-10%) HF electrolytic solution. (Section 3.6)

(7) It is observed that the current decay occurs during every porous formation process. When the nano-columnar pore forms, the exponent of the power lay decay relation is about 0.4. This is not a sufficient condition, which means that during some of the porous SiC formations, we observe ~0.4 exponent power

law current decays but the final pore morphology is not nano-columnar. (Section 3.2-3.6)

(8) It is also shown that values of γ (average number of holes needed to remove a SiC atom pair) can change greatly. However, in the highly concentrated HF, the values are about 7, especially during the nano-columnar pore formation. We will use this information to discuss the possible chemical reaction that happens during the nano-columnar pore formation. (Section 3.2-3.6)

(9) The nano-columnar pore formation is a reproducible process (Section 3.5-3.6). At larger voltages, the etching process becomes unstable and gives a large variation of experiment results. (Section 3.6)

The experimental observations reveal an interesting fact that in aqueous HF solution no matter how we change the experimental conditions, such as doping of the sample, etching voltages, polytype of the material, surface conditions, reaction temperature, and HF concentration, the resulting nano-columnar pore lattice remains the same (20±5 nm), if you ever obtain one. The formed columnar porous structures have almost identical pore diameter and center to center interpore spacing (40-60 nm).

Based on these experiments, we use the verified double layer model in the columnar pores to answer the following questions.

(1) What determines the columnar pores' geometry?

(2) What determines the columnar pores' dimension?

(3) What is the potential distribution during the pore formation?

(4) What is mechanism of the pattern formation in the nano-columnar pore formation?

The HRTEM study shows the important details about the columnar pore structure: a perfect SiC lattice in the pore wall; cylindrical pore wall; Hemispherical pore tip. Based on the TEM images, we then apply the cylindrical and spherical Poisson's equation to investigate the field at pore tips and pore walls. Our work showed that:

(1) The fast oxidation reaction rate of C-face and the favored spontaneous Helmholtz layer field direction for hole transfer are responsible for the columnar geometry during the nano-columnar pore formation. This qualitative explanation is what we know now to answer the question 1.

(2) Poisson's equations of planar surface, cylindrical surface, and spherical surface have been applied to discuss the potential and electric field conditions near the semiconductor surface. It is found that the porous formation could be divided into two phases: pore nucleation and pore formation.

For pore nucleation in the nano columnar pore formation, the SiC/HF electrolyte interface is planar. A deep inversion (with UV) or a large breakdown voltage (without UV) is needed for pore nucleation.

Once the pores appear, the interface geometry will change to cylindrical (pore wall) and spherical (pore tip). For the nano columnar pore formation, we suggest that at the pore tip, 3 V drops across the space charge region and large voltage drops on the Helmholtz layer to maintain a large charge exchange rate. The 3 V voltage drop near the SiC surface will pin E_F below E_{vs} and result a electric breakdown at the surface of the 10 nm radius pore tip. The large voltage we applied is required to satisfy the appropriate voltage drop across the Helmholtz layer and the electrolyte inside the pores to obtain a significant current. This explains why the pore diameter is fixed at about 20±5 nm no matter how we change the applied voltage.

We also suggested a maximum interpore spacing that can be obtained if the pore diameter is kept at 20 nm. This maximum value is due to the spontaneous band bending at the pore wall surface. The interpore spacing can be reduced by increasing the charge exchange rate under larger applied voltages. The minimum value is observed to be about 40 nm according to the experiments so far.

This study enables us to understand the reasons for the nano-columnar porous structure's unique dimension, which are also our answers to question 2.

(3) A simple circuit model is proposed to explain the current decay during the etching. The calculations do not agree with the experimental results. However, we did find that there is an appreciable voltage drop in the electrolyte inside the columnar pores during the etching. As the columnar pore grows, the voltage drop in the electrolyte inside the pores is increasing. Since the total voltage is a constant and the voltage at the pore tip space charge region is fixed at about 3 V, the voltage across the Helmholtz layer decreases as the etching goes on. Because the Helmholtz voltage determines the charge transfer rate, this slows down the etching rate.

In the example discussed in section 3.11.7 with 4H SiC doped at 1×10^{18} cm^{-3}, total 45 V is maintained during the etching. The voltage across the pore tip space charge region is kept about 3V. The voltage drop in the electrolyte inside the nano-columnar pores changes from 0 V to 20 V. The voltage across the Helmholtz layer therefore changes from 42 V to 22 V.

This study answers question 3.

(4) The biased diffusion limited aggregation model is used to predict the pattern formation in PSC. The latest result only resembles the porous structure in 3C SiC. To simulate the columnar pore growth in n-type hexagonal SiC, many improvements have to be made. The question 4 remains open so far.

4.0 COLUMNAR PORE GROWTH IN (11-20) FACE N-TYPE 6H SILICON CARBIDE

4.1 INTRODUCTION AND EXPERIMENTAL NOTES

After obtaining nano-columnar pores in C-face n-type 4H and 6H SiC materials, it appears that the cylindrical pore structure tends to form along the etching preferred crystalline direction in the photo-electrochemical etching. Earlier study[27] on the triangular pore formation in the n-type 4H and 6H SiC suggests that there are channels formed in the <11-20> directions under low electric field etching conditions. This result suggests that the <11-20> direction is an etching preferred direction and thus a-face n-type material etched under relatively high electric field may also produce columnar pores. To better understand the columnar pore formation mechanism and physics, we propose that by etching a-face material, we can investigate the following issues:

1. Unlike the basal plane material, where we can have Si-face or C-face, for A-face 4H or 6H SiC crystals, the crystalline structure of SiC is not polar. If we can fabricate columnar pores on a-face material, it will suggest that the columnar pore formation does not require a polar face.
2. If we succeed in fabricating the columnar porous structure in a-face SiC, it is then interesting to see whether we can vary the diameter of the columnar pores.

Before we address the pore formation in n-type a-face SiC, we have to clarify that it is very difficult and expensive to obtain a-face orientated and polished SiC crystals. The material resource is extremely limited. The a-face material used in this study is cut off from a 6H SiC boule using a diamond cutting saw. The samples are then mechanically polished with diamond lapping compounds. The surface polishing is finished with ¼ μm size diamond. Nickel ohmic contacts are then deposited onto the samples (see appendix B for details). The doping of the material is determined to be 8.2×10^{17} cm^{-3} by Van de Pauw four point measurements in our laboratory.

The electrolyte used in the etching process is 10% HF and 5% ethanol (mass percentage). We use a 1000 W Hg Xe Arc Lamp with multiple filters as the UV source to assist the electrochemical reaction by additional electron hole pair creation. The wavelength range of the UV illumination on the sample surface is 350-450 nm. The intensity is about 600 mW/cm^2 as measured by a Synrad Power Wizard^{TM} 2 laser power meter. Voltage is then applied across the two electrodes using a PAR 2273 Potentiostat/Galvanostat.

After anodization, samples are cleaned in acetone to remove the black wax mask. A Sartorius MC21S micro-balance is used to measure the mass loss of the sample due to the photo-electrochemical (PEC) etching. The sample is then "cleaved" by breaking the along a diamond scratch. Planar and cross-sectional scanning electron microscope (SEM) imaging are performed using a Philips XL30 FEG microscope at an operating voltage of 15 kV. The thickness of the porous structure is determined by the cross-sectional SEM measurement.

4.2 RESULTS AND DISCUSSION

For basal face samples, it is known that the critical etching condition that influences the columnar pore formation is the etching voltage. Therefore, a total of five samples were etched in order to find the possible optimum conditions that will produce columnar pores in the a-face SiC. The different voltages have been tested are 12, 13, 14, 15 and 20 V. The etching time was 10 minutes for all the experiments. Cross sectional SEM images of the formed pores are shown in Figure 4.1.

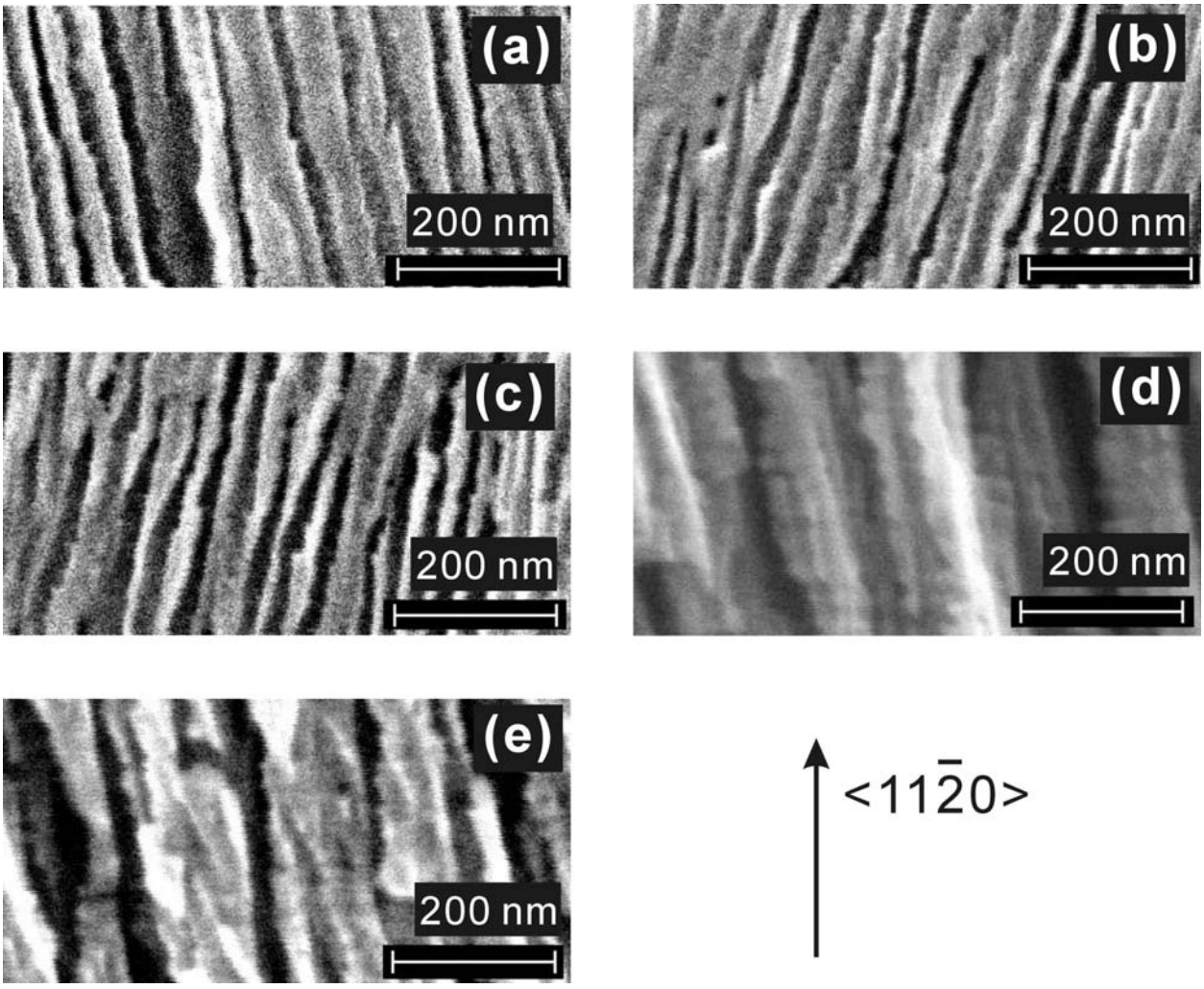

Figure 4.1 Cross sectional SEM images of the PSC etched on the a-face. The applied voltages are (a) 12 V, (b) 13 V, (c) 14 V, (d) 15 V and (e) 20 V.

From these SEM images we can see that the columnar pores are not uniform. Among the five experiments, the best columnar pores are formed under the voltage of 12 V. More samples will be preferred to test the etching voltage even lower. In this sample, the pore diameter is about 20 nm. With increased voltage, the pores become more irregular and the porosity increases. Filamentary porous structure is observed. Figure 4.2 shows the plots of the porosity, porous layer thickness, and γ (see section 3.2) dependence of the etching voltage applied.

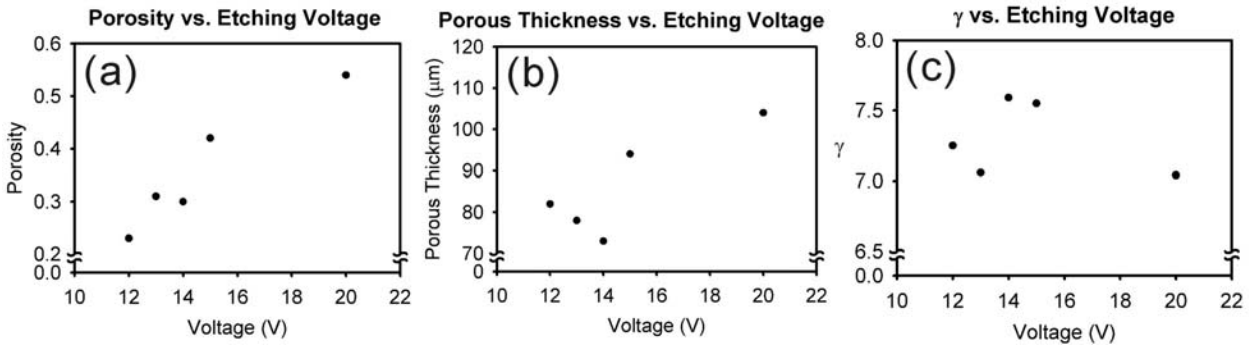

Figure 4.2 (a) Porosity, (b) porous layer thickness and (c) γ dependence on the applied etching voltage during the electrochemical etching of n-type a-face SiC material doped around 8.2×10^{17} cm^{-3}**.**

These experiments show that the porosity of the formed columnar porous structure is proportional to the applied voltage. The porous layer thickness does not have a clear trend with the increasing voltage. The layer thickness seems to decrease from 12 to 14 V, then rise when the voltage is larger than 14 V. The number of holes γ that are consumed to etch a SiC pair during the five experiments does not vary much. The values are between 7 and 7.6, which are not very different from the etchings that have been carried out on Si-face and C-face SiC samples.

The current-time curves during the etching process were also recorded. These curves are displayed in Figure 4.3. The shapes of the curves are very much like the current density – time curves observed during the etching of C-face and Si-face SiC. In general, higher voltage yields higher current density in the etching. There is a "linear" section in every curve on the log-log plot, which indicates a power law decay relation (Eq. 3.4).

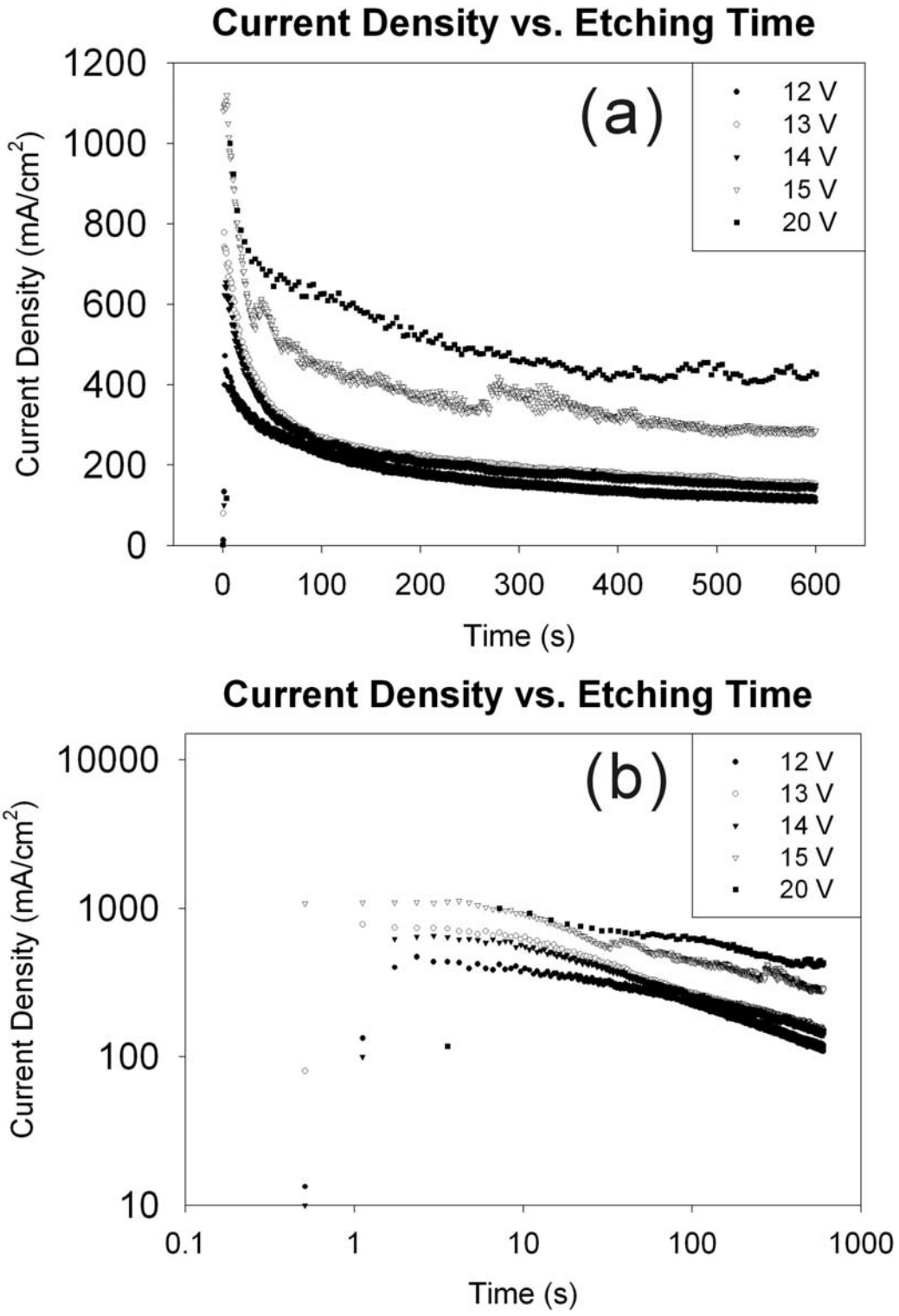

Figure 4.3 (a) Linear plot and (b) double log plot of the current density-time curves during the PECE of n-type A-face SiC. UV illumination is applied with the intensity 600 mW/cm^2.

We fit all the curves between 200 s and 600 s using the power law decay expression. The results for parameters A and β are shown in the Figure 4.4.

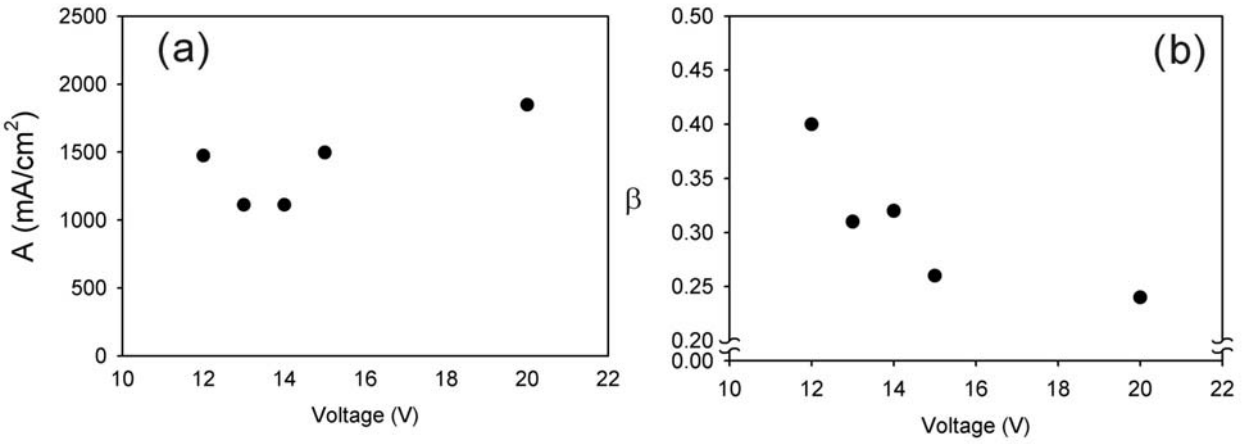

Figure 4.4 The parameter (a) A and (b) β vs. voltage plot. The results are obtained from the fitting of the current density-time curves between 200 and 600 seconds.

There is no clear changing trend of parameter a while increasing the etching voltage. However, the decay constant β clearly decreases while increase the voltage. The decaying constant β is about 0.4 for the best nano columnar structure at 12 V. β then decreases with increasing voltage. We may use a similar model in section 3.8.7 to explain this current decay.

Current oscillation is also observed during the electrochemical etching. To examine the oscillatory behavior, the residues from the fitting of the current density-time curves are plotted in Figure 4.5. The amplitude of the AC current signal is about 10 to 20 mA/cm^2, which is about 1% of the DC current density. It has to be pointed out that in the 20V experiment, the current measurement sampling period is about 4.6 s instead of 1.8 s as in other cases. The frequency of data recording is unintentionally set to be much lower than the other cases. The high frequency current oscillation signal therefore may not be recorded. This also reduces the sampling frequency in the FFT.

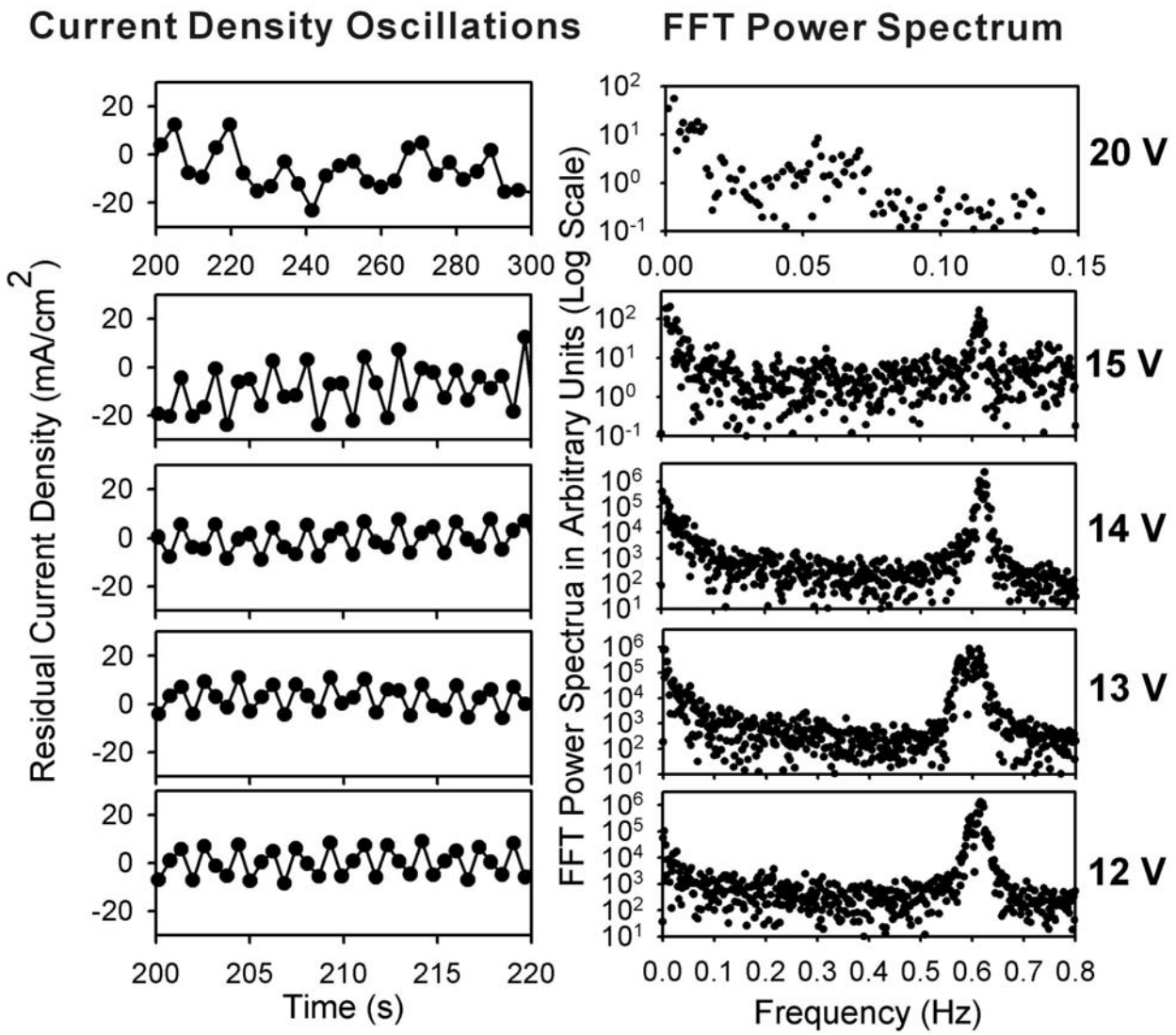

Figure 4.5 Current density oscillations observed during the PECE of a-face SiC is shown in the left column. The right column presents semi logarithmic plots of the FFT power spectrum of the current density from each experiment. The etching voltage used in each experiment is marked on the right side.

The power spectra from the FFT of the whole current density curves (except the first few seconds) confirm that this is not an isolated phenomenon. The characteristic frequency is maintained during the entire etching process. As a matter of fact, the oscillation frequency becomes less apparent with the increasing voltage (The power spectra peak to background ratio

is decreasing), while the oscillation frequency remains the same. According to the FFT plot, the frequency is about 0.6 s, which corresponds to a 1.7 second oscillation period.

Finally, we performed a current-voltage scan on the a-face SiC used in the above experiments. This helps us to have a better understanding of the interface properties between the a-face SiC and the electrolytic solution. Two scans are carried out in two different UV illumination conditions: 600 mW/cm^2 UV illumination and no UV illumination, as indicated in Figure 4.6 below.

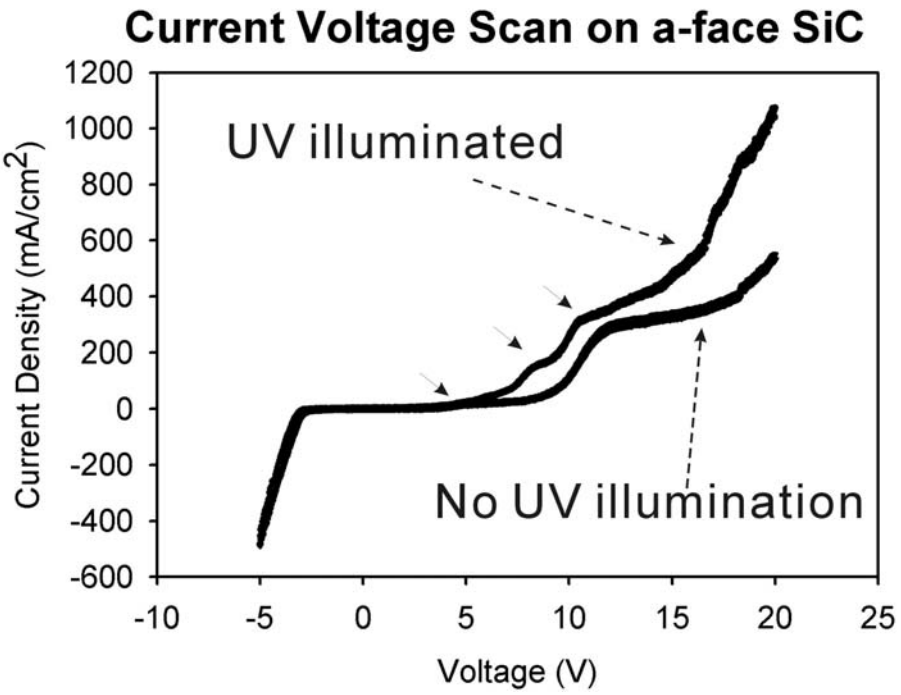

Figure 4.6 Current-voltage scans on an a-face SiC sample doped at 8.2×10^{17} cm^{-3} in aqueous 10% HF and 5% ethanol electrolyte. The kinks are marked with solid arrows on the UV illuminated I-V scan curve.

From the current density-voltage curves, it is found that the UV illumination increases the current density compared to the case without UV illumination. There are at least three kinks on the curve with the UV illumination and two on the curve without UV illumination. The kinks at

the largest voltage on both curves are around 10 to 12 V. These happen to be the voltage that we find producing the best nano columnar porous structure.

4.3 SUMMARY

Despite the difficulty of obtaining a-face SiC crystals, we studied the columnar pore formation in n-type a-face 6H SiC samples. Based on a limited number of experiments, we do find columnar pore formation in the a-face material. An optimum voltage has to be used in order to produce more uniform columnar porous structure. The pore diameter is about 20 nm, which is not different from the columnar pore formation in C-face SiC crystals. The study reveals that increasing the voltage increases the porosity. The porous thickness and γ do not have a clear relation to the applied voltage. SEM images confirm these results.

Current oscillations have also been observed during the etching processes. The periodic oscillation becomes less distinctive if the voltage is increased (vanishing FFT power spectra peak). The least noisy periodic oscillation is observed when we have the best columnar pore formation. It shows that the period is about 1.7 seconds.

Current-voltage scans were also performed on the a-face SiC materials used in the above experiments. Several kinks are observed on the curves both with and without UV illumination. The largest kink voltage is about 10-12 V. This voltage happens to be the optimum voltage among our experiments to produce the best columnar porous structure.

5.0 ELECTROCHEMICAL ETCHING ON P-TYPE SILICON CARBIDE

5.1 INTRODUCTION AND EXPERIMENTAL NOTES

Electrochemical etching on p-type 4H or 6H is relatively simple compared to n-type material, simply because it doesn't require UV illumination to provide the holes for the PECE reactions. However, p-type material is much more difficult to obtain than the n-type material, which is commercially available.

There are mainly three reasons we sometimes needed p-type PSC. First is the uniformity in porosity we believe p-type PSC possesses compared to n-type porous structures. However, our recently developed nano-columnar pore growth on n-type C-face crystals is also uniform in porosity. For many studies, like Raman scattering, Brillouin scattering, etc., uniformity of the porous structure is greatly preferred.

The second reason for fabricating p-type PSC is we don't need UV illumination during the etching. The fact that we use an Arc lamp as the UV source limits us in the etching time we can sustain in the n-type SiC porous fabrication. For p-type PSC, fabrication time can easily be a few hours or even 24 hours without any difficulties or practical problems.

Last but not the least, it is observed that, so far, we cannot electrochemically polish any n-type SiC material. For both Si-face and C-face etching on n-type material, it is found that we always have porous formation. The complete removal of SiC material, like what happens in Si or

other semiconductors, does not occur in our n-type SiC etching (the voltage range we have tried is from 0 to about 100 V in aqueous HF solution). However, for p-type SiC, this is not a problem. We've observed electrochemical polishing on both Si-face and C-face p-type material. Although the underlying mechanism remains unclear, this property of p-type material is very useful if we need a flat surface after electrochemical processing to study the interface properties.

For these reasons, this chapter presents discussions on the lab experiment observations in addition to the p-type porous paper published earlier from our group in J. Appl. Phys. 97 (4), No. 044908 (2005). We will discuss the details about the electrochemical polishing process. Doping effects on the p-type porous formation will be addressed.

The instrumentation we use to fabricate p-type PSC is not very different from what is used to etch n-type PSC. The anodization is conducted in a three-electrode cell where a SiC crystal is used as the anode and a platinum plate as the cathode. We use a saturate calomel electrode as a reference electrode. Aqueous HF mixed with ethanol electrolyte is used. The concentration will be specified later for different experiments. A Nickel ohmic contact is made on the back side of the SiC sample and protected by Apiezon wax. The front surface of the SiC sample is exposed to the electrolytic solution. Voltage or current is then controlled across the anode and cathode electrodes using a Perkin Elmer 263A Potentiostat/Galvanostat.

After anodization, samples are cleaned in acetone to remove the black wax mask. A Sartorius MC21S micro balance is used to measure the mass loss of the sample due to the photo-electrochemical (PEC) etching. The sample is then "cleaved" by breaking the sample along a deep scratch marked by a diamond pen. Planar and cross-sectional scanning electron microscope (SEM) imaging are performed using a Philips XL30 FEG microscope at an operating voltage of

15 kV. The thickness of the porous structure is determined by the cross-sectional SEM measurement.

5.2 ELECTROPOLISHING OF P-TYPE SILICON CARBIDE

Electrochemical polishing has been obtained on both Si-face and C-face p-type SiC. Although we use highly doped p-type SiC in both cases, it is found that for Si-face p-type 4H SiC, we need a relatively higher doped material ($p \sim 7.7\times10^{18}$ cm^{-3}), and for C-face p-type 4H SiC, the doping of the semiconductor has to be lower ($p \sim 7\times10^{17}$ cm^{-3}) in order to facilitate the electro-polishing process and avoid any porous formation. The 4H SiC samples we used all have an 8^{o} off cut towards <11-20>. 1% HF (mass percentage) mixed with 5% ethanol electrolyte is used for the electrochemical polishing experiments.

All the experimental information is listed in Table 5.1 below.

Crystal Face	Doping (cm^{-3})	Current Density (mA/cm^2)	Sample Area (cm^2)	Etching Depth (μm)	Mass Loss (g)	Porosity Calculated	Charge Passed	γ
Si-face	7.7×10^{18}	20	0.45	8	0.000975	0.84	16.2	6.9
C-face	7×10^{17}	20	0.48	9	0.001124	0.81	17.28	6.4

Table 5.1 Experimental data for electrochemical polishing of the p-type 4H SiC

The porosity calculated by mass loss doesn't equal to one (all the material is removed). We think this is because there is a slope around the etching edges and also the etching process is not as even as we think, we over evaluate the etching depth. The Charge that has passed through the sample during the etching process is calculated by multiplying the constant current with the 30 min etching time. Then γ can be calculated using the equation 3.4.

The cross section SEM images taken for both samples are shown in Figure 5.1. The etched Si-face is smoother than the C-face under the SEM resolution (better distinguished under AFM in the J. Appl. Phys. manuscript by Shu, CMU). The edge slope after etching is clearly seen on the cross section images for both cases. The voltage needed for etching the p-type material while maintaining the current density at 20 mA/cm^2 is about 2.71 V for Si-face and 2.95V for C-face samples, respectively. Figure 5.2 shows the voltage oscillations observed during the etching process for both crystal faces. To show the oscillation behavior better we only plot part of the complete etching curve from 1400 s to 1600 s. The FFT power spectrum of the voltage-time curve is shown in Figure 5.3. Both power spectra for Si and C face etching are noisy but have a peak at about 0.085 Hz, which corresponds to an oscillation period of about 12 s.

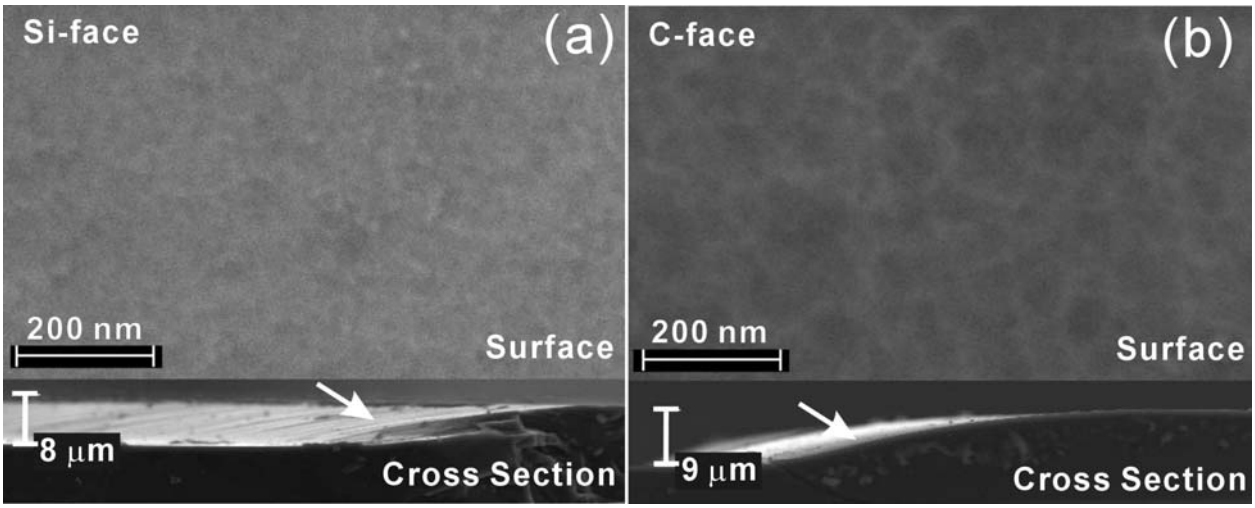

Figure 5.1 SEM images of electrochemically polished (a) Si-face and (b) C-face p-type SiC samples. The upper section of each image is the plan view of the sample surface and the lower view is the cross section showing the etching depth and the etching slope (indicated by the arrows).

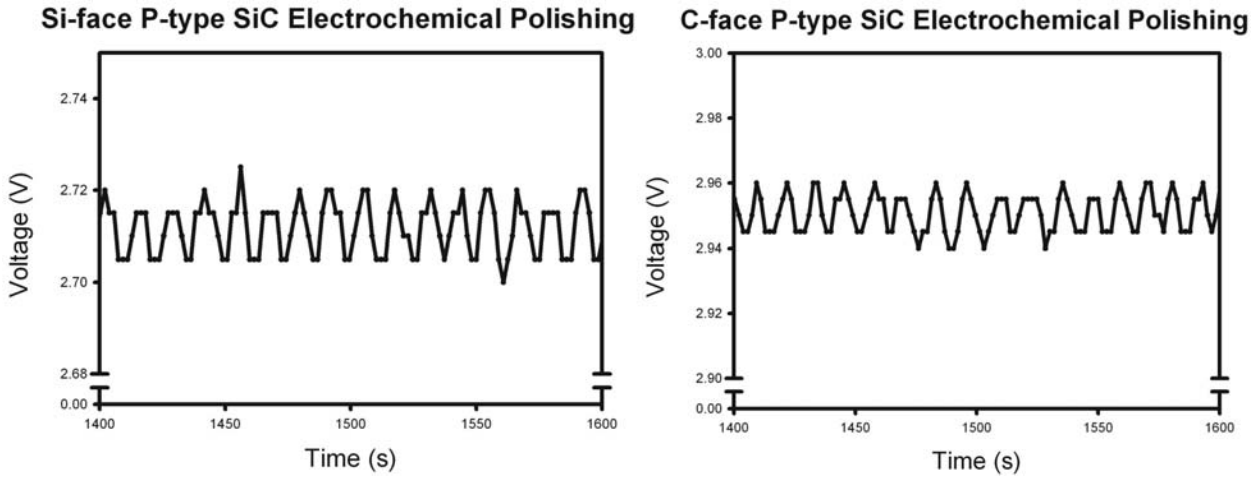

Figure 5.2 Voltage oscillation observed during the electrochemical polishing of p-type SiC.

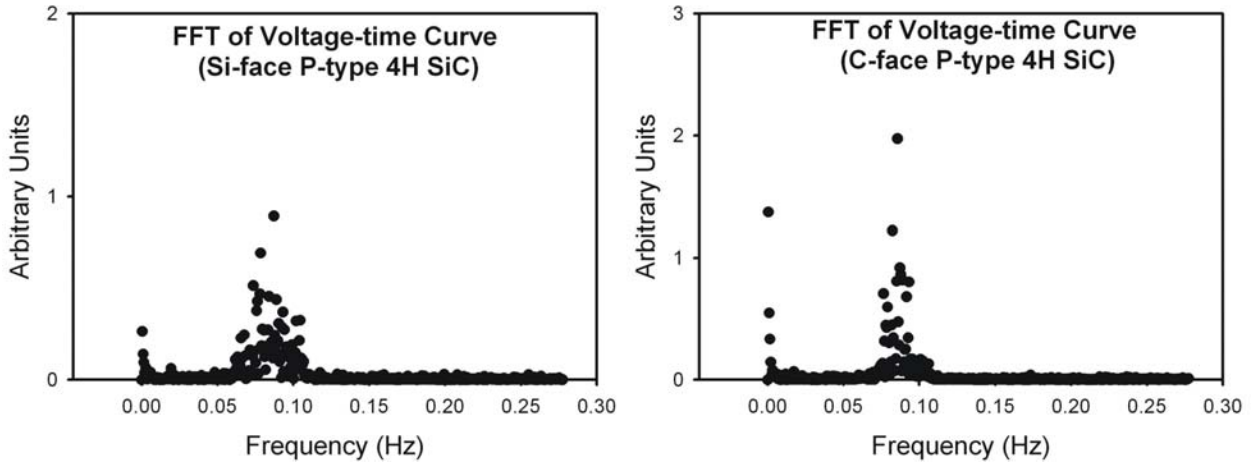

Figure 5.3 FFT of the V-t curves for electrochemical polishing of p-type 4H SiC**.**

5.3 ELECTROCHEMICAL ETCHING OF P-TYPE SILICON CARBIDE

It was found by Shor *et al.* then that, in order to have pore formation, the electrochemical etching on p-type SiC must be carried out on C-face rather than Si-face samples. The electrochemical etching of p-type SiC other than electrochemical polishing, has already been studied systematically in our laboratory[27]. Our early research has shown that on 2×10^{18} cm^{-3} samples, the

porosity depends on the current density that is used during the electrochemical etching. The formula as a result from the fitting of the experimental data is found to be $P = 0.686 j^{0.08}$, where P is the porosity and j is the current density. The predicted lowest porosity we can obtain with our current equipment is about 0.27 with the current density 10^{-8} A/cm^2, which implies an extremely slow etching rate.

During process of preparing p-type PSC samples for our collaborators, more extensive experiments have been carried out recently and interesting experimental observations have been recorded. In this section we will discuss the important ones, which we believe extend our knowledge of p-type SiC porous etching.

5.3.1 Systematic Current Density Dependence Study on More Highly doped (7×10^{18}cm^{-3}) p-type 4H SiC

In order to obtain a p-type PSC layer with lower porosity (< 0.5) with a reasonable etching rate, we performed electrochemical etching on higher doped 4H p-type SiC samples (p ~ 7×10^{18}cm^{-3}) with a 3^o off cut. The aqueous electrolyte used contains 10% HF and 5% ethanol by weight. Figure 5.4 shows the dependence of porosity, etching rate and γ dependence on the current densities.

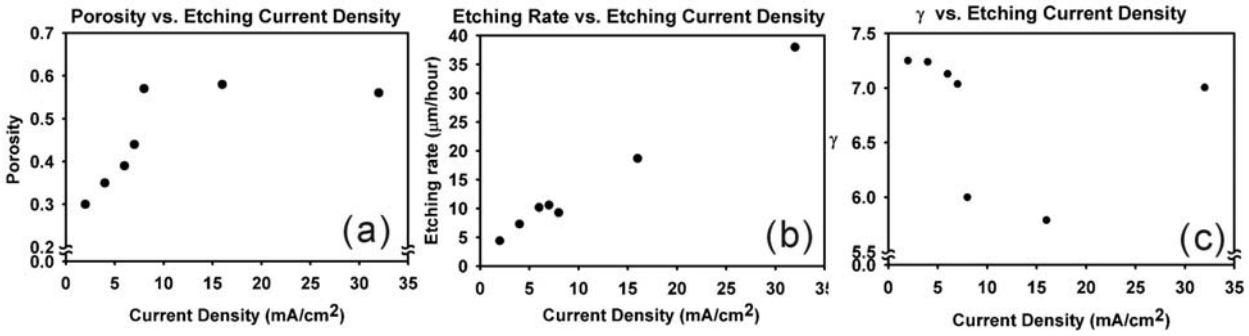

Figure 5.4 The current density dependence of (a) porosity, (b) etching rate and (c) γ of the electrochemical etching of p-type 4H SiC ($p \sim 7\times10^{18}cm^{-3}$).

It is found that the porosity can be as low as 0.3 with a reasonable etching rate at 5 μm/hr. Unlike the etching on lower doped material, the porosity has a maximum at about 0.6. The etching rate increases along with the current density. γ decreases in general with increasing current density when the current density is below 32 mA/cm^2. The increase of γ at 32 mA/cm^2 current density and the small kink in the etching rate plot are not yet understood.

The compliance voltages applied to maintain the current densities are displayed in Figure 5.5. Note that the etching time for each current density is not the same. The etching time is chosen so that the total charge that will flow through the sample is the same. The voltage curves show that the compliance voltage needed is a constant in the beginning of the etching process. The compliance voltage rises towards the end of the etching. The nature of the rising voltage behavior is not clear at this moment. The details of the Voltage-time curves are then shown in the Figure 5.5. No voltage oscillations have been observed.

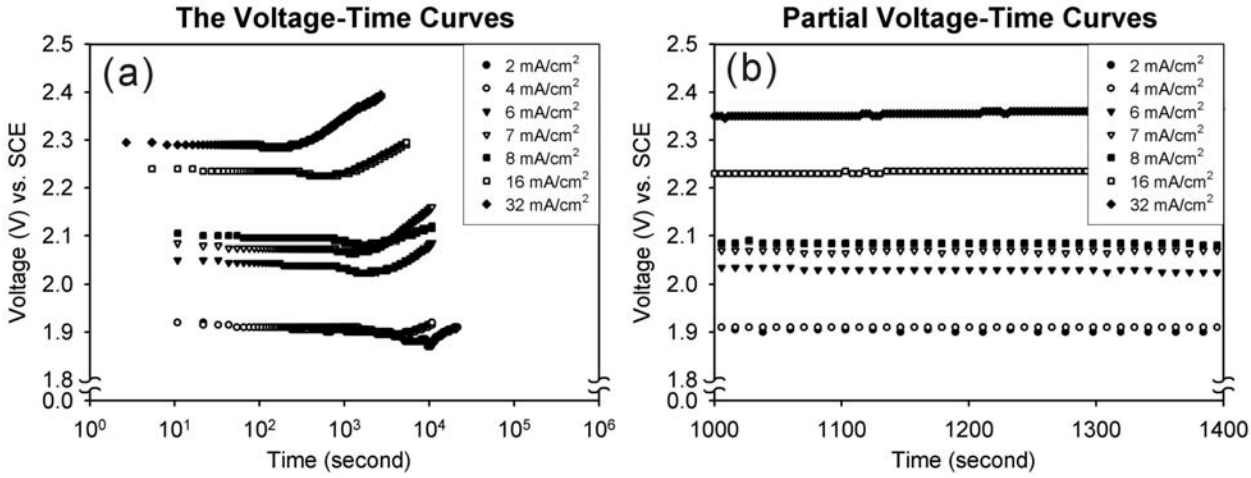

Figure 5.5 The (a) complete and (b) partial voltage-time curves recorded during the etching at each current density.

Figure 5.6 shows the cross sectional SEM images of the samples etched using different current densities. The SEM images are taken near the porous/bulk interface and thus reflect the porous structure towards the end of the etching. The porosity observed on the images is in qualitative agreement with the porosity obtained gravimetrically in Figure 5.4 (a). The porosity increases with the current density. The scale of the observed porous features appears to vary with increasing current density.

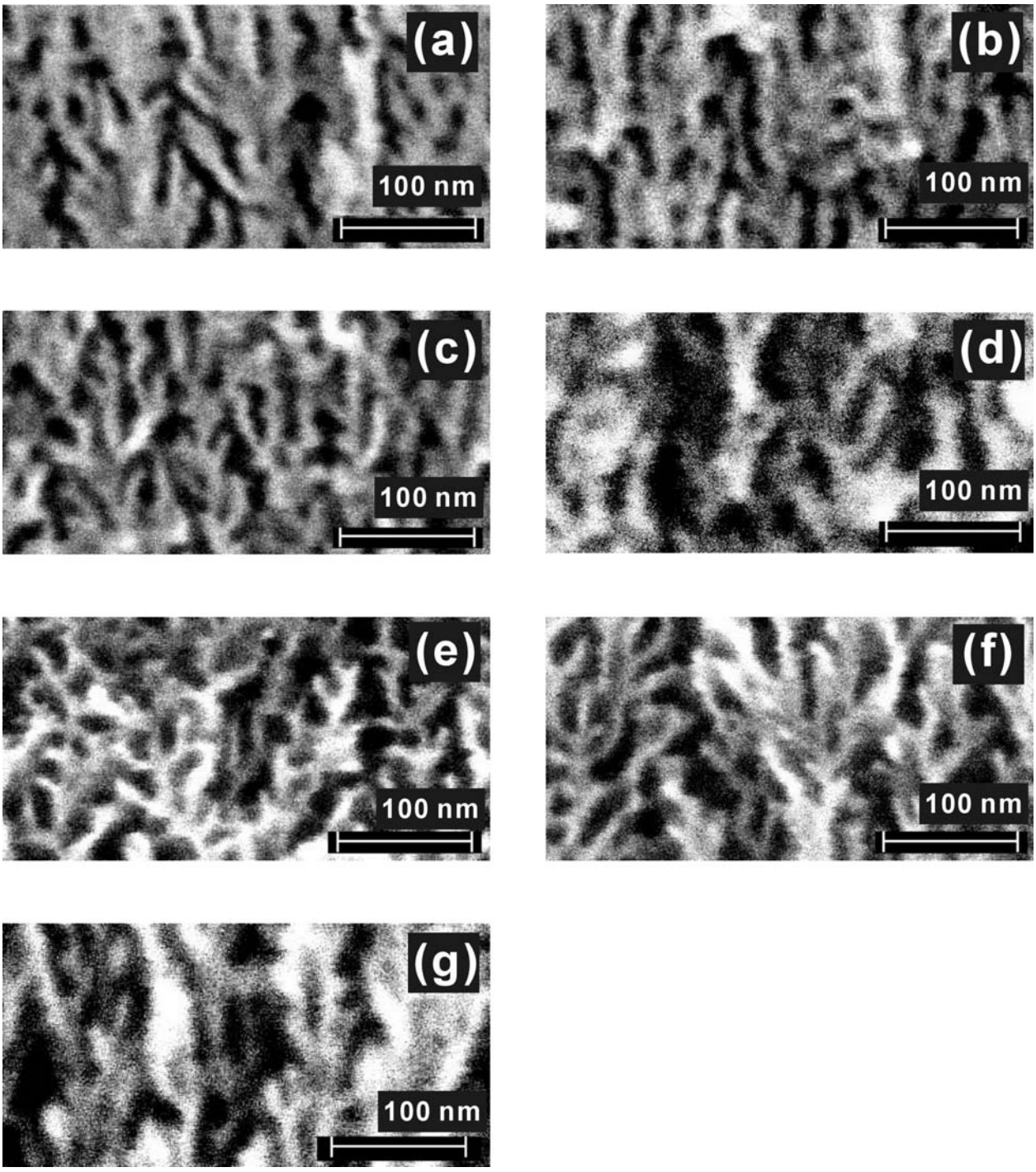

Figure 5.6 Cross-sectional SEM images of the porous structures etched at (a) 2 mA/cm^2, (b) 4 mA/cm^2, (c) 6 mA/cm^2, (d) 7 mA/cm^2, (e) 8 mA/cm^2, (f) 16 mA/cm^2 and (g) 32 mA/cm^2 on 4H p-type SiC doped at 7×10^{18} cm^{-3}.

5.3.2 Etching Time Study of the Electrochemical Etching of p-type 6H SiC doped at 2.3×10^{18} cm^{-3}

In the electrochemical etching, it is believed that holes participate in the reactions and create the voids inside the original bulk semiconductor. In the etching of p-type SiC, holes are supplied by either dopant or avalanche breakdown and therefore no UV illumination is necessary in contrast to the etching of n-type material. Since there is no light absorption decay during the pore formation, we used to believe[28] that the pores are generally uniform from the air/porous interface to the porous/bulk interface. In other words, there is no porosity gradient resulting from the etching process. To examine this, we performed 4 mA/cm^2 current density etchings on 6H p-type SiC doped at 2.3×10^{18} cm^{-3} with various etching time to study the relation between the porosity and the porous layer thickness. The aqueous electrolytes used in the experiments are 10% HF and 5% ethanol mixed by weight percentage.

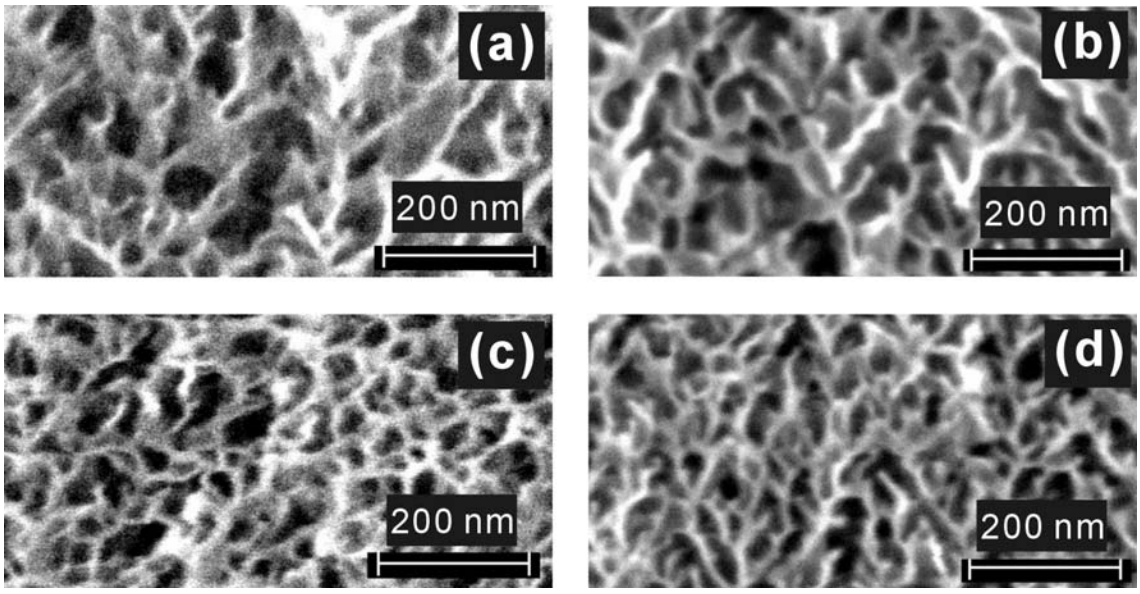

Figure 5.7 Cross sectional SEM images of p-type porous structure etched under 4 mA/cm^2 for (a) 4 hours, (b) 8 hours, (c) 16 hours and (d) 24 hours. Dark contrast is the pore.

A total of four experiments were performed with the etching times 4, 8, 12 and 16 hours. Figure 5.7 shows the cross sectional SEM images of the porous structure near the porous/bulk interface. This reflects the porous structure formed at the end of each experiment. Although the pore wall thickness seems to be the same in the four experiments, the size of the voids in between decreases along with the increase of the etching time, i.e. the pores are becoming smaller. This implies that the porosity is decreasing.

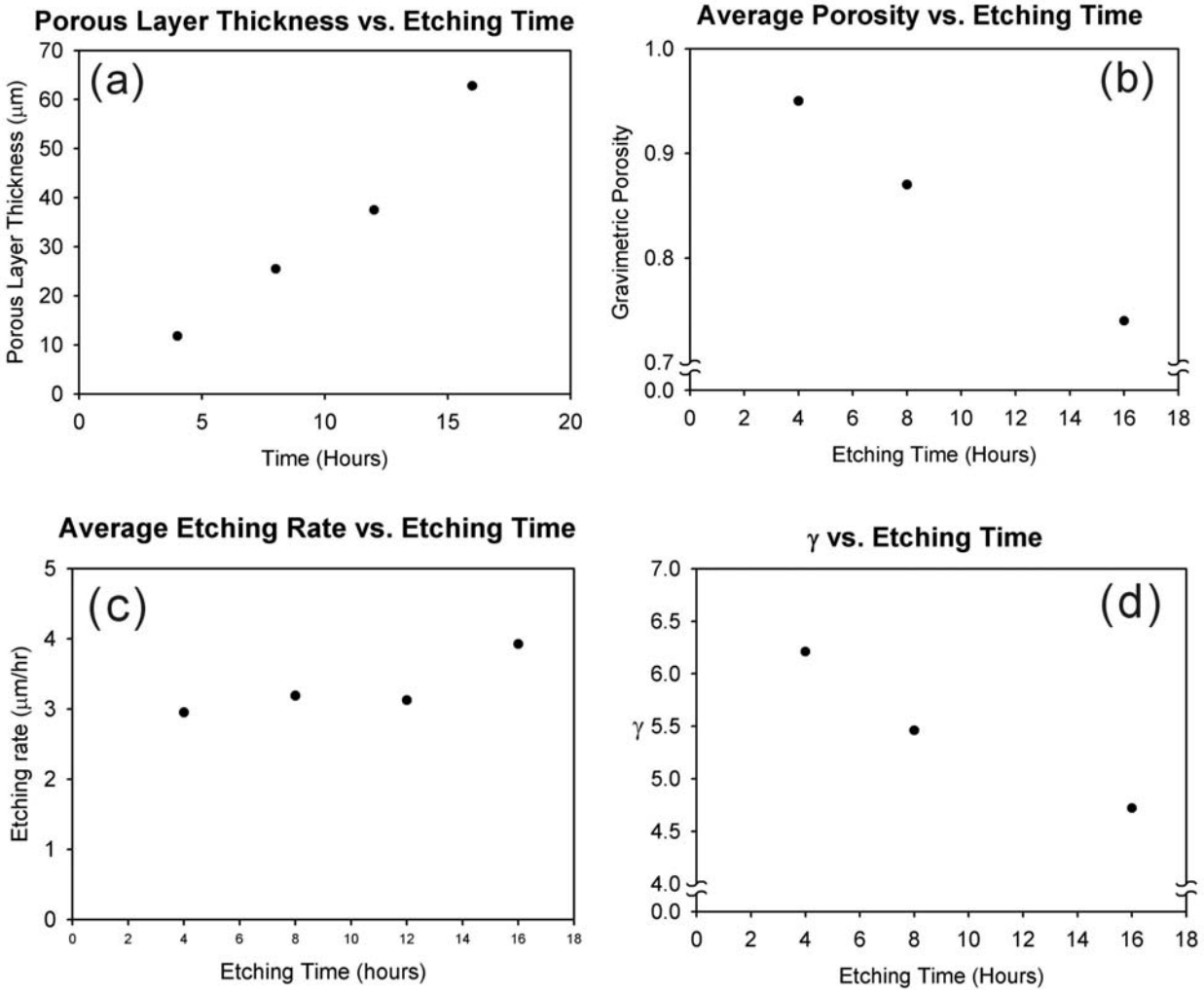

Figure 5.8 The (a) porous layer thickness, (b) porosity, (c) etching rate and (d) γ dependence on the different etching time under the etching current density 4 mA/cm^2. (Because the experiment with 12 hour etching was done without any microbalance to weigh the sample, the porosity and γ values are missing in plots (b) and (d))

More experimental data are presented in Figure 5.8. The porous layer thickness (Figure 5.8a) grows almost linearly with the etching time. Longer etching, however, leads to a decrease of the overall average porosity of the sample (Figure 5.8b). This is consistent with the SEM images. The average etching rate (Figure 5.8c) does not vary much when we extend the etching time, which suggests that the etching speed is nearly constant throughout the etching. The number of holes required to etch a SiC pair (γ) decreases from 6.2 to 4.7 (Figure 5.8d). The reason of this change of γ is not clear so far.

5.3.3 Doping Dependence of the Pore Formation in p-type SiC

From the lower porosities of p-type porous SiC presented in section 5.3.2, we learned that the material doping has a strong effect on the pore formation in p-type SiC. Although there are no designed systematic experiments designed, in order to study the doping effect qualitatively, we concluded some experiment results on different p-type SiC materials. In these experiments, we use the same electrolyte (aqueous 10% HF and 5% ethanol) and the same current density (4 mA/cm^2) during the electrochemical etching. Because these experiments were done for different purposes, the polytype and offcut of the material are different. Since the etching time may also be different in different experiments, we compare only the etching rate. The porosity and γ comparisons are then also qualitative. Results given for the materials doped at 1.9×10^{18} and 2.3×10^{18} cm^{-3} are the average values from several experiments. All the data are listed in Table 5.2 and plotted in the Figure 5.9 to examine the doping dependence.

Polytype	Off cut (^{o})	Doping (cm^{-3})	Etch Rate (μm/hr)	Porosity	γ
4H	8.00	7×10^{17}	2.7	0.95	5.8
6H	0.00	1.9×10^{18}	3.8	0.79	6.3
6H	3.80	2.3×10^{18}	3.4	0.89	6.2
6H	3.23	7×10^{18}	7.7	0.34	7.2

Table 5.2 Experimental results to compare the doping effects during the formation of porous p-type SiC.

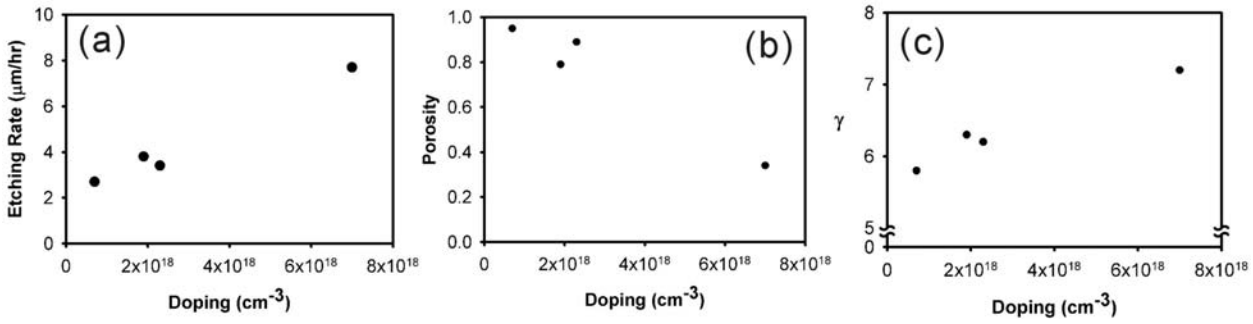

Figure 5.9 The dependence of the (a) etching rate, (b) porosity and (c) γ on the doping of p-type SiC.

In general, as we observe from Figure 5.9a, the etching rate increases with the doping. This is reasonable because we have more holes available to assist the electrochemical process. The average porosity decreases with the increasing doping. We think this is due to the higher etching rate along the etching direction that decreases the chances for lateral etching in the SiC. This suggests that if one wants to electropolish C-face p-type SiC, a lower doped material is preferred. If a low porosity porous sample is required, then higher doped material is necessary in order to maintain a reasonable etching rate.

5.4 SUMMARY

Experiments have been performed on p-type SiC materials. It is found that, unlike the n-type SiC material, for which electrochemical polishing has not been observed so far, the electrochemical polishing of p-type SiC can be done on both the Si-face and the C-face. A constant current etching condition is used during the polishing processes. A 12 s cycle compliance voltage oscillation has been observed during the etching.

The systematic current density study on more highly doped ($p \sim 7\times10^{18}$ cm^{-3}) p-type material reveals that we can obtain much lower porosity (<0.50) porous p-type SiC with a reasonable etching rate (~5 μm/hr). The porosity reaches its maximum value 0.6 at the current density larger than 16 mA/cm^2. SEM observation confirms this result. These new results on more highly doped p-type material extend our capability of fabricating p-type PSC to a wider porosity range.

It was believed that pore formation in p-type SiC is uniform. However, systematic experiments done by etching samples for different lengths of time demonstrate that there is a porosity gradient inside the porous structure. From the experiments, we discovered that the porous etching rate does not vary much during the etching. The average porosity decreases with increasing porous layer thickness, which indicates that the porosity decreases across the porous layer (surface to porous/bulk interface). The porosity is highest near the air/porous interface, which is the initial etching surface. The porosity drops when the pores are formed deeper inside the porous structure. This is also observed in the SEM images. The pore wall thickness is roughly the same, however the pore size is larger for the sample etched for shorter period of time.

We propose that this is possibly due to the diffusion of the HF electrolyte, which causes the decrease of the HF concentration near the pore tips.

The summarized experimental results from different experiments qualitatively shows the doping effects on the formation of pores in p-type SiC. They show that more highly doped materials will produce lower porosity porous samples. The etching rate increases with the material doping (amount of available holes for the chemical reactions).

APPENDIX A

PUBLICATION LIST

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3. "Raman Spectra of a 4H-SiC Epitaxial Layer on Porous and Non-porous 4H-SiC Substrates", M. J. Clouter, Y. Ke, R. P. Devaty, W. J. Choyke, Y. Shishkin, and S.E. Saddow, *Mater. Sci. Forum* 556-557, p. 415 (2007).

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11. "Modification of the Oxide/Semiconductor Interface by High Temperature NO Treatments: a Combined EPR, NRA and XPS Study on Oxidized Porous and Bulk n-type 4H-SiC", H.J. von Bardeleben, J.L. Cantin, I.C. Vickridge, Yongwei Song, S. Dhar, L.C. Feldman, J.R. Williams, Y. Ke, Y. Shishkin, R.P. Devaty and W.J. Choyke, *Mater. Sci. Forum* 483-485, p. 277 (2005).

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17. "Brillouin Scattering Studies of Surface Acoustic Waves in SiC", G.T. Andrews, M.J. Clouter, B. Mroz, Y. Shishkin, Y. Ke, R.P. Devaty and W.J. Choyke, *Mater. Sci. Forum*. 457-460, p. 653 (2004).

18. "Porous Structure of Anodized p-type 6H SiC", Y. Shishkin, Y. Ke, W.J. Choyke, and R.P. Devaty, *Mater. Sci. Forum* 457-460, p. 1471 (2004).

19. "Intrinsic Defects at the 4H-SiC/SiO_2 Interface: Identification of the Carbon Dangling Bond Center in Oxidized Porous SiC", J.L. Cantin, H.J. von Bardeleben, Y. Shishkin, Y. Ke, R.P. Devaty, and W.J. Choyke, *Phys. Rev. Lett*. 92(1), 015502 (2004).

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APPENDIX B

FABRICATION OF NANO-COLUMNAR POROUS SILICON CARBIDE

This appendix contains the details of the laboratory procedures and the related experimental equipment used to fabricate porous SiC (PSC). Based on and further developed from the initial instrumentation built by Y. Shishkin, two different setups are now being used in our laboratory for the PSC fabrication.

Figure B.1a shows a general schematic of the photo-electrochemical etching (PECE) experiment without temperature control capability but with a temperature monitor. Figure B.1b shows the schematic of the setup with the temperature control capability within 0.1 ^{o}C. A Teflon sample holder accommodating SiC pieces is placed into a Teflon or polypropylene chamber containing aqueous HF electrolyte mixed with ethanol. The current or voltage applied across the sample is controlled by a Galvanostat or Potentiostat respectively. The etching of the SiC is performed either without or with UV illumination on the sample surface. Filtered light from a Mercury/Xenon arc lamp source is used if the UV illumination is desired.

The following section contains information about the necessary instrumentation and how to utilize it to fabricate PSC.

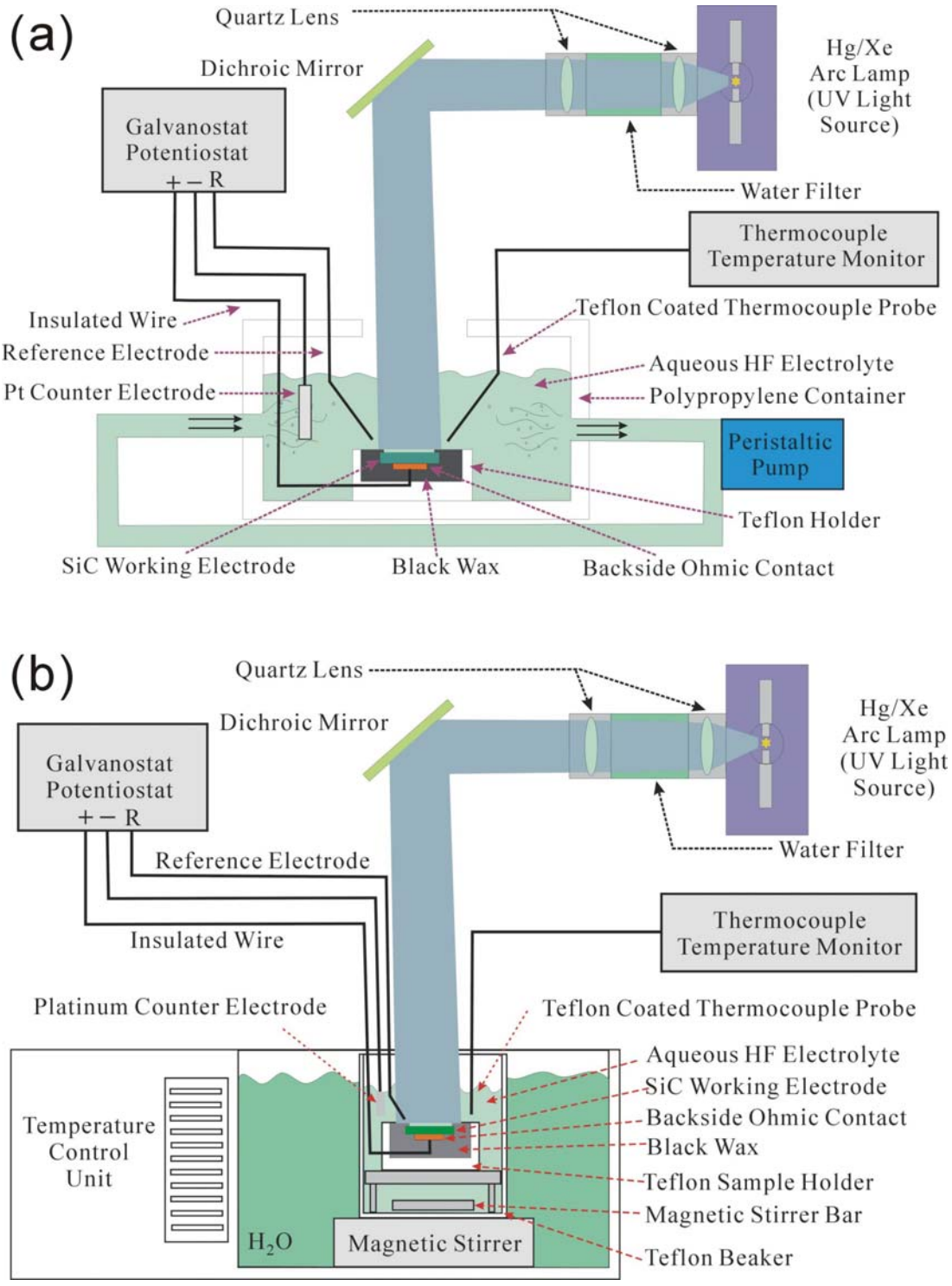


Figure B.1 Schematics of three electrode PECE setups (a) without temperature control and (b) with temperature control.

B.1 SAMPLE PREPARATION

The photoelectrochemical (PEC) reaction here needs an external power supply to provide the necessary additional voltage and current to etch the sample. A SiC crystal wafer piece is served as the anode in the electrochemical reaction cell. A good electrical contact to the semiconductor is thus needed so that reproducible results can be obtained. The ohmic contact made to the back side of the sample is an annealed Nickel film deposited onto the SiC surface in vacuum by e-beam evaporation. The following cleaning and preparation procedures are required to ensure the quality of the ohmic contact.

- Clean the sample with photo-spectrometric grade acetone in an ultrasonic cleaner for 10 minutes. Acetone removes most of the organic contaminations.
- Clean the sample with photo-spectrometric grade iso-propanol in an ultrasonic cleaner for 10 minutes. This process removes the acetone residue.
- Dip the sample into a 10% HF aqueous solution for 10 minutes. This will remove the silicon oxide from the sample surface.
- Choose the appropriate deposition technique depending on the type of doping. For p-type material, we use Al/Ti alloy (90%/10%) and thermal evaporation, for which pieces of the alloy are melted inside a tungsten coil heated using an electrical current of about 150 to 200 Amps. For n-type SiC, we use pure (99.99%) Ni evaporated by electron beam.

- Position the sample on the mask with the sample back side facing towards the metal source. The deposition mask is any thin metal sheet with holes of appropriate diameter. The hole layout should be made such that there will be at least two deposited contacts on each sample back (two contacts are required for the contact resistance check). The mask with the samples should be placed about 20 cm above the Ni source (e-beam evaporation) and about 15 cm above the Al/Ti source (thermal evaporation).
- Pump down the chamber. A pressure in the low 10^{-5} Torr range is good for nickel deposition. Base pressure in the 10^{-6} Torr range is recommended for the aluminum deposition.
- Deposit 1000-1500 Å (deposition rate at about 2 Å/second) of Ni if the sample is n-type SiC, and 2000-2500 Å (deposition rate at least 10 but no more than 20 Å/second) of Al/Ti if it is p-type SiC.
- Anneal the Ni contacts in a moderate argon flow (40-50 sccm) at 1000 ^{o}C for five minutes by rapid thermal annealing (RTA). The Al contacts should also be annealed by RTA in argon flow for five minutes, but at 950 ^{o}C. For RTA process, the samples are rapidly pulled into and out of the hot zone of the furnace, which is already at the desired annealing temperature.
- After the samples are pulled out of the hot zone in furnace, allow them to cool down for a few minutes in the quartz tube while maintaining the argon flow. After removing the samples, check the resistance between the contacts. Good contacts usually give a few ohms resistance for n-type and a few tens of ohms for p-type highly doped samples.
- The sample now is ready for mounting, which will be described in the next section.

B.2 BATH AND SAMPLE HOLDER

We use a home made polypropylene rectangular shaped box if a peristaltic pump is used, where the temperature of the electrolyte is monitored but not controlled. Alternatively, a commercial resin/Teflon beaker is used together with a magnetic stirrer with the temperature controlled. Both containers can sustain HF concentrations up to 50% by weight.

The sample holder was machined by Bob Giles, the machine shop specialist. Holders are made out of Teflon, which possesses low thermal and electrical conductivity and has excellent resistance to corrosion in hydrofluoric acid. In order to protect the ohmic contacts on the back as well as the edges during the anodization procedure, the samples are masked using Apiezon black wax. The masking is done next to a vent pipe by, first, applying molten wax to the edges of a sample. The sample is then placed onto a small copper plate which has an insulated wire attached to it, as shown in Figure B.2. Between the sample and the copper plate one has to put a tiny drop of silver colloidal solution to ensure an electrical contact. After that, molten black wax is carefully applied around the edges of the sample. In order to ensure a good leak-proof seal one has to soften the wax. This is done by blowing hot air onto the mount using a heat blower. The softened wax will seal the potential electrolyte leaks to the back side of the sample. After the wax has cooled down, you can place the holder into the bath. In order to remove the by-products of the electrochemical reaction from the neighborhood of the semiconductor/solution interface, a diastolic pump is attached to the bath through a flexible PVC hose resistant to HF. The pump can circulate the electrolytic solution without any direct contact with it. A reasonable setting for the circulation speed is 2 or 3, as read from the dial.

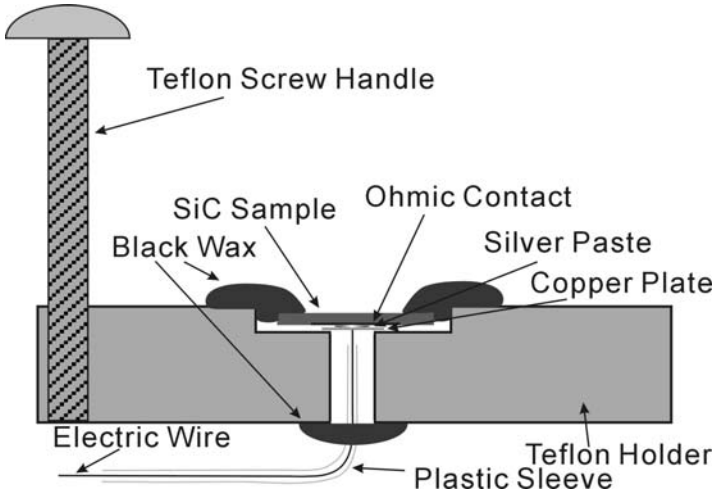


Figure B.2 Schematic of a sample holder.

B.3 TWO AND THREE ELECTRODE CONFIGURATION

For experiments conducted in the voltage range between 1-10 volts, a three-electrode cell is used, where a SiC crystal serves as the working electrode. In this case, an epoxy-body saturated calomel electrode (SCE) is used as a reference (Fisher Scientific, Cat. # 13-620-258). It has very large impedance so that no current can be drawn through it. All the potentials are given with respect to the SCE. A square 3 cm^2 platinum plate is used as an auxiliary counter electrode. Platinum is the material of choice for most electrochemical experiments.

The electrical control unit is essentially a current/voltage supply specifically designed for the three-electrode configuration. We have two instruments to choose from. For gentle regions of PECE we use a Perkin Elmer 263A instrument which can work in both potentiostatic and galvanostatic modes (refer to section B.7.1 of Y. Shishkin's dissertation to find out more about

the instrument). As a backup instrument, we also have a PWR-3 potentiostat manufactured by Bioanalytical Systems, Inc.

If higher voltage is needed, e.g., to separate a free standing porous membrane, a regular two-electrode power supply can be used. A Keithley 2425 Source/Meter or any other regular power supply can serve the purpose.

In the fabrication of nano columnar PSC, a voltage in the range of 10-100 volts is very often required. To serve this purpose, a PAR 2273 with a voltage divider shown in Figure B.3 is used in our laboratory. This instrument enables us to switch the electrode configuration between three electrodes and two electrodes conveniently. Impedance measurements that require a three electrode configuration can thus be followed by an etching procedure with two electrode etching.

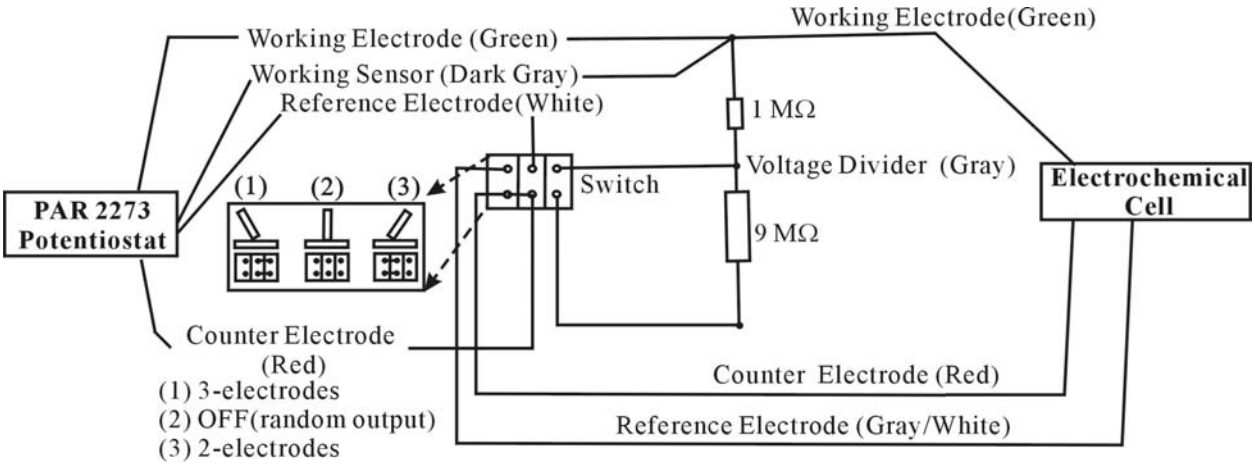


Figure B.3 The voltage divider used for the PAR 2273 Potentiostat.

B.4 POST TREATMENT OF SAMPLES AND SEM IMAGING

After anodization, the sample holder is carefully removed from the bath, thoroughly washed in deionized water, and air-dried. Next, the sample is removed by melting the Apiezon wax with a heat blower and cleaned with Q-tips in boiling acetone. Occasionally, the cleaning is done in toluene or trimethylchloroethylene under a fume hood if the surface of the porous sample is anticipated to be delicate and damage by Q-tip is to be avoided. All the cleaning is conducted under appropriate ventilation conditions to ensure safety. In particular, trimethylchloroethylene is carcinogenic, and any work with this solvent must be performed in the hood using special protective gear (apron, goggles, gloves, face mask). Usage of latex gloves is discouraged in the case of handling trimethylchloroethylene because latex quickly decomposes in trimethylchloroethylene.

The characterization of PSC is conducted using a Philips XL30 FEG Scanning Electron Microscope (SEM). Plan-view and cross-sectional SEM imaging are performed in the secondary electron mode at 5 to 15 kV. The instrument is located in the Material Sciences and Engineering Department. Consult the trained personnel of this laboratory to get familiar with the instrument in order to collect images of the necessary resolution, contrast, and brightness.

Plan-view imaging does not require any special preparation. Samples can simply be mounted on an SEM sample holder by means of a piece of sticky carbon tape. The tape not only holds the sample but also provides the electrical contact required to avoid charging effects. Due to high resistivity, one may expect charging to be a problem for samples of high porosity, resulting in somewhat worse image quality and image distortion effects. Use of an atomic Force Microscope (AFM) is recommended to examine the surface for these samples. Cross-sectional

imaging requires additional preparation. The samples are fractured in order to expose the porous structure in cross-section. For better control of the fracture line, it is recommended then one makes a scratch on the back of the sample with a diamond scriber.

B.5 FABRICATION OF FRAME SAMPLES

The term "frame sample" here is used to specifically describe a porous SiC chip as shown in Fig. B.4. The sample dimensions are usually 10 mm by 10 mm. The center pore area is purposely masked to be 5 mm by 5 mm before the etching process. The not etched SiC frame gives extra mechanical strength to the sample.

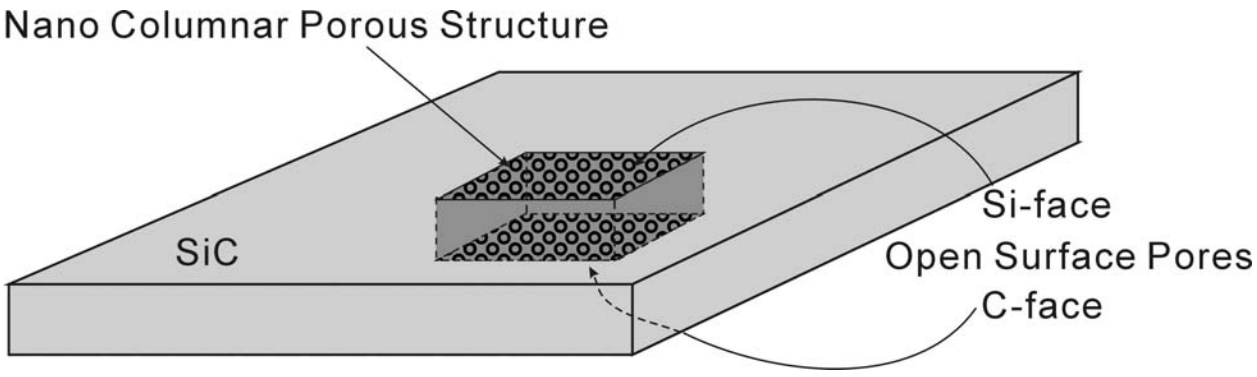


Figure B.4 Schematic of a frame sample.

The nano columnar porous SiC is found to form on only the C-face SiC so far. After the fabrication, the uniform columnar pores are sandwiched between the cap layer and the bulk SiC left from the etching process. In principle, one can remove the cap layer and obtain the uniform C-face surface pores of the nano columnar porous structure. However, some applications need

Si-face surface pores rather than C-face ones, so the polishing process must be applied on the Si-face. For the polishing to remove the cap layer from the C-face or bulk material from the Si-face, the techniques are similar. The critical condition that must be controlled other, than the surface smoothness, is the thickness of the material that has been removed.

The detailed polishing procedure could be found in Appendix D. The sample thickness should be measured using a micrometer. After the samples are mounted onto the sample holder, the total thickness of the samples and sample holder should be measured. This value will be used as the starting point. It needs to be kept in mind that the thickness is not uniform for each sample. An average has to be estimated by measuring the thickness at all samples' positions.

In the initial stage of polishing to flatten the sample surfaces using 30 μm diamond, the removed thickness has to be estimated every ten minutes, certainly more often than every 20 minutes. The etching rate greatly depends on the pressure, number of samples, and possible different SiC crystal qualities. The polishing rate is a case by case parameter and therefore can not be determined.

After using 6 μm diamond with polishing cloth, the rate of material removal is practically zero, judged with a micrometer. At this stage, no care needs to be taken for over polishing by removing too much material. The major concern is then to ensure the polishing quality in terms of the surface smoothness. The polishing should be carried out down to ¼ μm diamond to give the best surface quality. Based on our experience, the porous layer may not be uniform. If 20 μm of SiC needs to be removed, a total of 30-50 μm removal by polishing should actually be performed. The minimum sample thickness should be over 100 μm. Thinner sample usually doesn't hold and will crack even during the polishing.

The fabricated frame sample should look like the image in Fig. B.5.

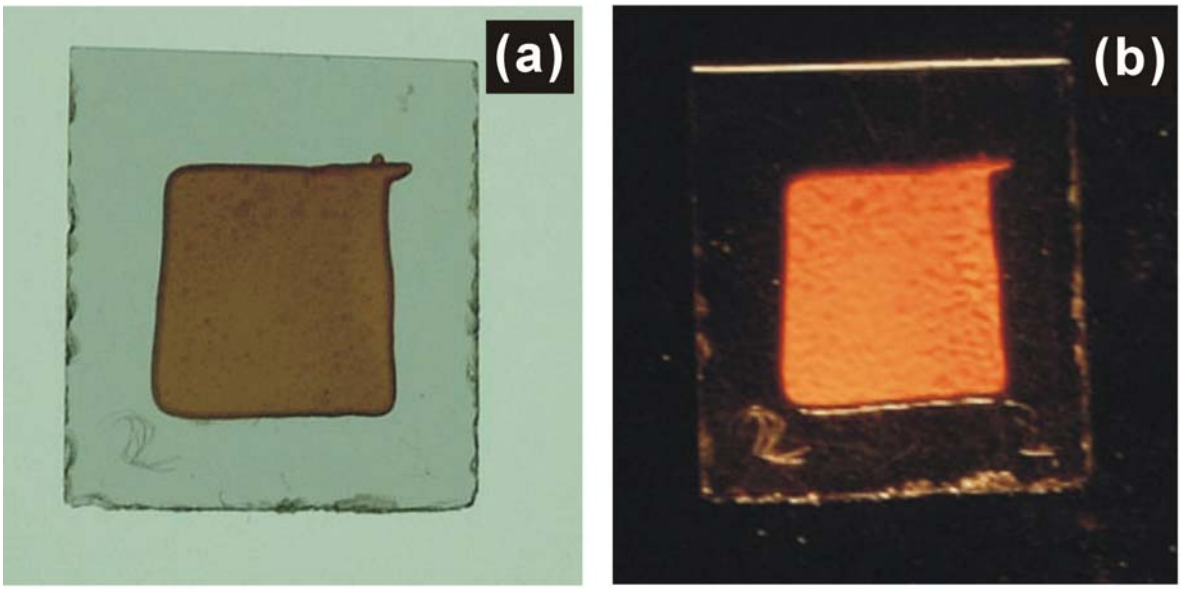


Figure B.5 Images of a typical frame sample fabricated in our lab. The images are taken with (a) front white light illumination and (b) back white light illumination.

B.6 ELECTROLYTIC SOLUTION FORMULE AND USAGE ESTIMATION

Aqueous HF Electrolyte Recipe

1. Properties:

   Density of 49%HF: 1.18 g/cm^3, volume=x ml

   Density of 90% ethanol: 0.79 g/cm^3, volume=y ml

   Density of H_2O: 1.00 g/cm^3, volume=z ml

   [HF] and [ethanol] are the concentrations in the units of weight fraction.

2. Formula:

$$\begin{cases} \dfrac{1.18\times 0.49x}{1.18x+0.79y+1z}=[HF] \\ \dfrac{0.79\times 0.9y}{1.18x+0.79y+1z}=[ethanol] \\ x+y+z=1000 \end{cases}$$

Iso-Propanol HF Electrolyte Recipe

1. Properties:

   Density of 49%HF: 1.18 g/cm^3, volume=x ml

   Density of 99.5% 2-propanol: 0.785 g/cm^3, volume=y ml

   [HF] is the concentration in the unit of weight fraction.

2. Formula:

$$\begin{cases} \dfrac{1.18 \times 0.49x}{1.18x + 0.79y} = [HF] \\ x + y = 1000 \end{cases}$$

N-Propanol HF Electrolyte Recipe

1. Properties:

   Density of 49%HF: 1.18 g/cm^3, volume=x ml

   Density of 99.8% 1-propanol: 0.802 g/cm^3, volume=y ml

   [HF] is the concentration in the unit of weight fraction.

2. Formula:

$$\begin{cases} \dfrac{1.18 \times 0.49x}{1.18x + 0.80y} = [HF] \\ x + y = 1000 \end{cases}$$

HF TBAP N-Propanol Electrolyte Recipe

1. Properties:

   Density of 49%HF: 1.18 g/cm^3, volume=x ml

   Density of 99.9% N-Propanol: 0.802 g/cm^3, volume=y ml

   Molecular weight of TBAP: 342 g/mol, mass=z g

   [HF] is the concentration in the unit of weight fraction.

   [TBAP] is the concentration in the unit of mol/liter.

2. Formula:

$$\begin{cases} \dfrac{1.18 \times 0.49x}{1.18x + 0.8y + z} = [HF] \\ \dfrac{z/342}{(x+y)/1000} = [TBAP] \\ \\ 1.18x + 0.8y + z = 1000 \end{cases}$$

HF TBAP MeCN Electrolyte Recipe

1. Properties:

   Density of 49%HF: 1.18 g/cm^3, volume=x ml

   Density of 99.7% Acetonitrile: 0.782 g/cm^3, volume=y ml

   Molecular weight of TBAP: 342 g/mol, mass=z g

   [HF] is the concentration in the unit of weight fraction.

   [TBAP] is the concentration in the unit of mol/liter.

2. Formula:

$$\begin{cases} \dfrac{1.18\times 0.49x}{1.18x+0.782y+z}=[HF] \\ \dfrac{z/342}{(x+y)/1000}=[TBAP] \\ 1.18x+0.782y+z=1000 \end{cases}$$

The Usage of Aqueous HF Solution

The formation of nano columnar pores in aqueous 10% *HF* solution requires the participation of *HF* to dissolve the SiO_2. We therefore need to estimate the usage of HF in each run so that we make sure that the experimental condition is within our error tolerance, which is around 5%.

The chemical reactions proposed are:

$$\begin{aligned} SiC+3H_2O+6h^+ &= SiO_2+CO\uparrow+6H^+ \\ SiC+4H_2O+8h^+ &= SiO_2+CO_2\uparrow+8H^+ \end{aligned} \quad \text{(B.1)}$$

The formed SiO_2 needs to be dissolved by HF so that the chemical reaction can proceed. The needed chemical reaction is then:

$$SiO_2 + 6HF = H_2SiF_6 + 2H_2O \ . \tag{B.2}$$

According to our measurements, about seven holes on average are consumed to remove one SiC pair. If reactions B.1 take place at the same rate as reaction B.2, six HF ions/molecules are then needed to remove the SiO_2 produced by removing the SiC pair. A single etching experiment will consume roughly around 20 C of charge in 30 minutes for a 1 cm^2 area sample. The formed porous layer thickness is about 130 μm. Based on these data, the number of HF ions/molecules used in each experiment is

$$\frac{20\ C}{1.6\times10^{-19}\ C}\times\frac{6}{7} = 1.07\times10^{20} = 1.78\times10^{-4}\,mol\,.$$

800 ml of 10% HF solution is often used in the bath. The total amount of HF in the solution is then estimated to be about 4 mol. Therefore, the reduction in HF concentration due to each experiment is so small that it can be neglected. At least 200 such runs are needed to cause a 1% decrease of the overall HF concentration. HF concentration reduction by evaporation is the major cause of uncertainty in the HF concentration error over a long period of time.

B.7 ERROR ESTIMATION

The experimental error needs to be estimated to evaluate the reliability of our data. The measurement instruments used in our lab are the Potentiostat/Galvanostat, Microbalance, and SEM microscope. Our Potentiostat/Galvanostat setups give about < 0.5% error in voltage and

current measurements. The accuracy of the Microbalance is 2 μg and therefore about 1% error for most weighing measurements. The SEM microscope gives about 0.5 μm error for the porous layer thickness measurements, and therefore gives about 1% error, too.

In our experiments, we often measure the voltage, current, passed charge, porous layer thickness, holes required to remove a SiC pair (γ), current density and porosity. Some measurement errors therefore can be estimated using the instrumental error above, for example, voltage, current, and pore layer thickness. The value of γ is determined by both mass loss and current measurements using the equation:

$$\gamma = N_{holes} / N_{SiC} = \frac{Q}{e} \Big/ \frac{V_p}{V_o} = \frac{Q}{e} \Big/ \frac{\Delta m}{\rho \cdot V_o} = \frac{Q \cdot \rho \cdot V_o}{e \cdot \Delta m}$$

Here, Q is the total electric charge flowing through the sample. e is the unit electric charge (1.6×10^{-19} C). N_{holes}=Q/e is the total number of holes that flowed. Δm is the mass loss in grams and ρ is the SiC mass density (3.21 g/cm^3). V_p, the pore volume, which is the total volume of SiC pairs removed by the PEC process, is then just Δm/ρ. V_o is the volume of a SiC pair, as determined below. N_{SiC}= V_p/V_0 is the number of SiC pairs chemically removed. Therefore, $N_{SiC} = \frac{\Delta m}{\rho \cdot V_o}$. For a 6H SiC single crystal, V_0 can be calculated by the following method. The 6H SiC unit cell volume is $\frac{\sqrt{3}}{2} a^2 c$ where a and c are the lattice constants. The measured values[93] are a = 3.08 Å, c = 15.12 Å. Since the unit cell contains six SiC pairs, each pair occupies an effective average volume: $V_0 = \frac{\sqrt{3}}{12} a^2 c = 20.7 \times 10^{-24} cm^3$. For each of the PECE processes, the total amount of charge is estimated by integrating the current-time curve. The number of holes

required to etch a SiC pair is then calculated. According to the rule of error propagation, the error of γ is therefore about 1.1%.

The current density measurements involve the current measurement and the area estimation. In our lab, for daily operation, the area of the sample is estimated using a normal ruler (named regular measurement). This can introduce an error large compared to the others. If we use a digital camera and travelling microscope with 1 μm resolution, we can perform much more accurate area measurements, which we call an accurate measurement. We then compare the difference between the regular measurement and the accurate measurement to give an estimation of error in the regular area measurements. The method of the accurate measurement is explained in the text below.

First the image of one sample is taken using a perpendicularly positioned digital camera. The accurate distance between two points on the sample is then determined using the travelling microscope. The sample image is then revised to add small grids using CorelDraw software (Fig. B.6) and printed out on letter size paper as large as possible. We then use a travelling microscope to determine the actual distance between A and B on the actual sample as shown in Figure B.6. Then the size of each grid square and the distance between A and B in the picture are measured using the travelling microscope so that a scale bar can be specified. In this case, the distance between A and B on the actual sample is 3.160 mm. On the picture, the distance between A and B is 145.05 mm. It is then determined that each grid represents 0.0872 mm. The number of the gird squares covered by the sample is counted to be 1081.5. The total area of the sample estimated this way is about 0.0822 cm^2. The area estimated by a simple ruler measurement is about 0.08 cm^2. The error is therefore 3%.

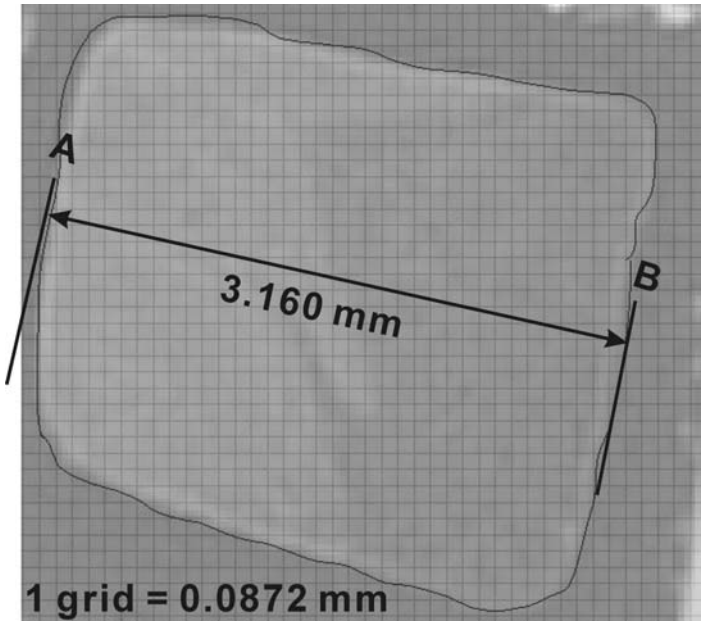


Figure B.6 Grid method to measure the sample area.

A total number of four different sample areas are estimated in this way independently. The largest error is about 5%. The samples used here possess a relatively small area around 0.1 cm^2. If the area, for example, is larger than 0.3 cm^2, which is actually true for most of the experiments, the relative error of the area measurements should be much smaller because the absolute error does not change for different sized samples. Therefore, we can safely say that the area measurements in our lab have an error smaller than 5%. We then estimate that the current density measurement error is about 5%.

The porosity is measured by weighing the sample and calculating the volume of the porous structure layer (area and thickness). For the mass loss measurements, the error is about 1%. The SEM thickness measurement gives another 1% error. The area estimation error is 5%. Based on the propagation of error, the error of the porosity measurement is about 5.2%.

The above estimations of errors for various measurements give us an idea of how accurate our measurements are. However, the experimental results sensitively depend on the

material doping, defects density, etc. The etching process itself is not stable for the high voltage etching experiments. The same etching conditions may give different experimental results. This kind of experiment variance, however, cannot be estimated quantitatively. This kind variation could be deemed as error in the measurements because it is often impossible to be distinguished this variation from the measurements error. Some initial efforts to understand the large experimental errors caused by the unstable electrochemical process have been made, as described in Chapter 3. Therefore, one has to be careful when working with the high voltage etching if any repeatable sample production is desired. Until now, the formation of the nano-columnar porous structure is deemed to be a reproducible process if the material properties (various defects and their density, doping, compensation, crystal orientation, stress level, polytype etc.) are consistent. In actual experiments, the thickness of the porous layer may vary from run to run by about 5 μm. The porosity measured is deemed to be identical within the instrument measurement error. If the doping varies within the sample or the wafer, the resulting porous structure may also not have a uniform thickness across the sample.

In conclusion, the error estimation for our experiments is very difficult due to the unstable process of the electrochemical reaction we perform. The measurement error is well within 5% if there is no large experiment variation due to the sensitive electrochemical process, especially if the etching voltage used is high. If the detailed SiC material properties listed above are changing, the experimental results are hard to predict. This means a calibration procedure is recommended before etching any new SiC wafer samples. It is usually true that for the samples cut off from the same wafer, the material properties are similar enough that the variation of the doping and the defects can be neglected.

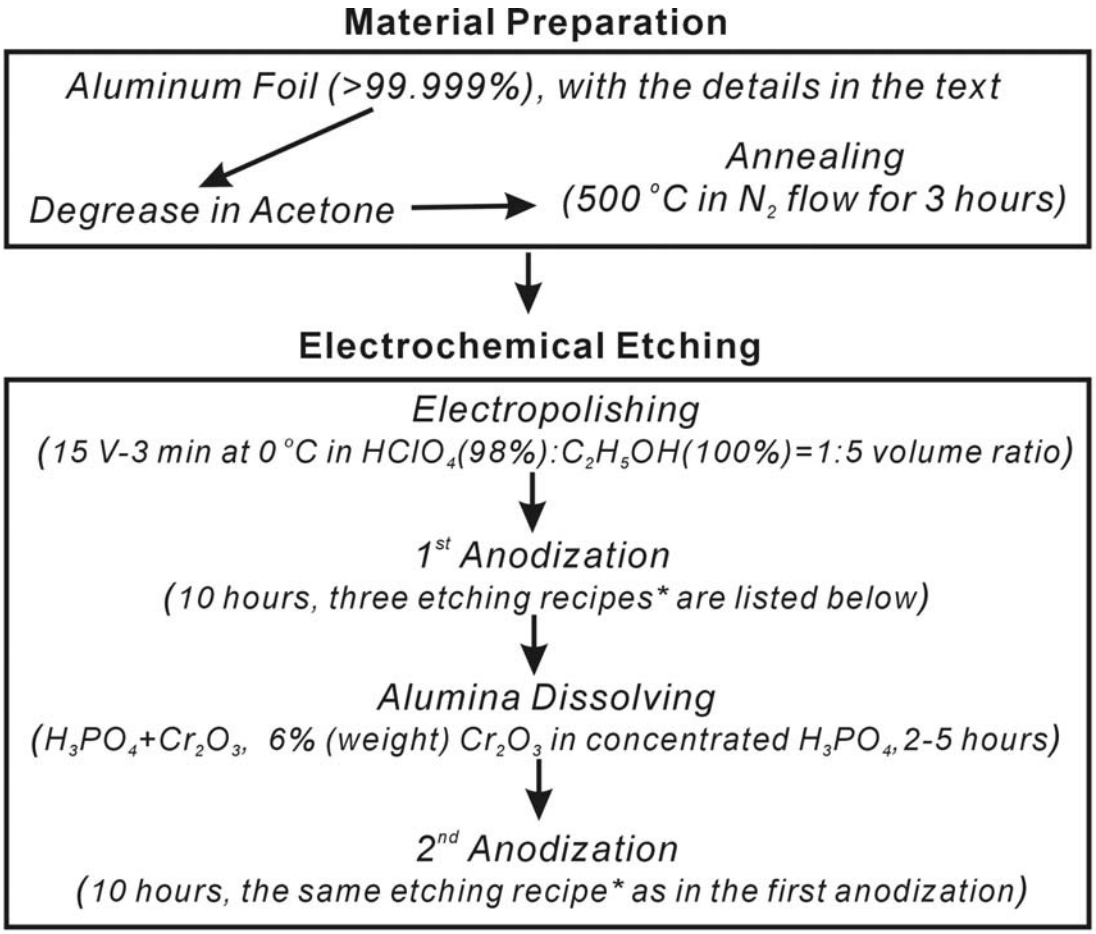
APPENDIX C

POROUS ALUMINA FABRICATION

Porous Al_2O_3 had once become our concern, simply because it was hoped that it could serve as a facial mask for surface pore nucleation and patterning, before the C-face nano columnar porous growth was discovered and controlled. Great effort has been devoted to repeating the well known technique.[37] In this appendix, we summarize the procedure for porous alumina fabrication. I'd like to thank Prof. Jianyu Liang at Dept. of Mechanical Engineering of WPI, who taught me all the detailed technical information[94].

It should first be pointed out that, to get well ordered porous alumina, good temperature control is needed, which could be realized by a thermo bath system (chiller and circulator). Very often, the desired reaction temperature is lower than the room ambient, for example, 10 ^oC. The tolerance of the temperature is about ± 0.1 ^oC. A Pyrex 1000 ml beaker is normally used to ensure sufficient quantity of the chemicals during the fabrication, which takes about 10 hours for each etching step. The potential supply that is needed in this case can be any two electrode regular power supply with a voltage range 0-200 V. We use a Xantrex 300-4 power supply to serve this purpose.

Figure C.1 shows is the flow chart of the lab procedure to fabricate the porous alumina.



***Etching Recipes**

Recipe	Electrolyte	Ingredient Amount	Water Volume	T (°C)	Voltage (V)	Typical Pore Spacing
1	0.3 M $C_2H_2O_4$	27 g	1000 ml	10	40	110 nm
2	1 M H_3PO_4	69 ml	931 ml	0	160	400 nm
3	0.5 M H_2SO_4	28 ml	972 ml	0	25	65 nm

Figure C.1. The flow diagram of porous alumina fabrication. Choose one of the three recipes according to the pore spacing desired.

TECHNICAL NOTES

1) ESPI (www.espi-metals.com) 5N, 0.01" thickness Al sheet is used as the substrate material. It is supposed to be a mechanically polished annealed Al sheet.
2) The use of the sample holder described for the PSC fabrication is prohibited because the high temperature needed to melt the black wax will destroy the formed porous alumina. To use a porous alumina free standing film on SiC, one has to use an O-ring sealed sample holder to avoid the high temperature.
3) To obtain a free standing film, we need to use $HgCl_2$ (2% by weight). The solution is made at 60 ^oC (Be aware of the toxic vapor) in the fume hood. The cooled down solution is then used. Fresh solution is recommended for each run. One can make a good amount for multiple runs. When separating the film, temperature lower than the room temperature serves the purpose better but room temperature also works. The film will separate after a while (in few minutes). Separation may cause a cracking problem, especially for films thinner than 1 micron.
4) The final film thickness is controlled by the second etching time. Usually one could use a longer etching time in the first stage such as 10 hr or longer, and use a much shorter time to grow the second layer. After removal of the first layer, one can continue etching for 1 hr to obtain a 2-micron thick film. The etching rate is about 2 um/hr (some times it is higher).
5) It is not necessary to do acid (diluted HCl or H_2SiO_4) etching before SEM. But doing so will give better picture because the acid etching will remove the surface Al_2O_3 and create a fresh surface.
6) It is not necessary to use current controlled etching. The result is similar to the potentiostatic etching.

7) If one wants to deposit a layer of Aluminum on top of any semiconductor, the base pressure should be at least 10^{-6} to 10^{-7} Torr range. Deposition rate is 0.1 um /min. Thicker film, such as 10-20 um thick, requires a Ti buffer layer (tens of nanometers) on semiconductor first.
8) To obtain a better ordered pore lattice, the first layer is needed to be removed. This procedure will leave a surface pattern on the Al substrate and the following second etching will initiate from these surface sites and gives a much better pore lattice. When removing the first layer of porous alumina, we use H_3PO_4+Cr_2O_3. H_3PO_4 alone can be used, too. You may need to increase the temperature to 60 ^oC speed up the chemical reactions.
9) You can have your anodization bath specially designed so you expose only the top surface to the electrolyte. The other way is to immerse the whole sample into the solution and protect the backside and the edges. When it is done the second way, one can use nail polishing and Teflon tape to protect the sample. It is cheap and simple.
10) Formed pore structure is shown in Figure C.2.

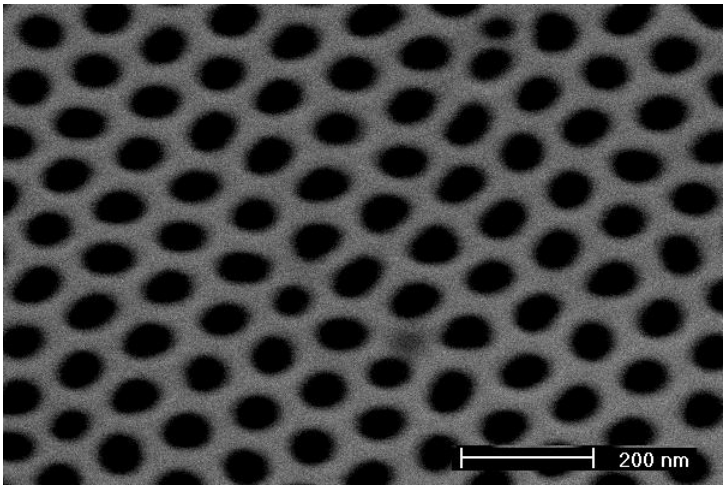


Figure C.2 Porous Al_2O_3 used as a mask in our lab.

APPENDIX D

MECHANICAL POLISHING OF SILICON CARBIDE

Mechanical polishing is a standard way in our lab to obtain an optically flat SiC surface. The basic procedures are presented below.

D.1 PREPARATION OF SAMPLES:

The SiC samples should be cleaned prior to polishing. The surface of the samples should be free of any kind of wax or particles. We can polish up to 20 1 cm × 1 cm samples with each polishing disk. All the samples one wants to polish on the same disk should have roughly the same thickness. The thickness difference has to be within 10 μm.

In order to reduce the probability of producing SiC chips during the polishing, we need to polish the corners and sides of each sample by hand using 30 μm diamond. The reason for doing so is explained in Fig. D.1. The ideal shape of the sample right before the mechanical polishing is illustrated schematically in Fig. D.1b:

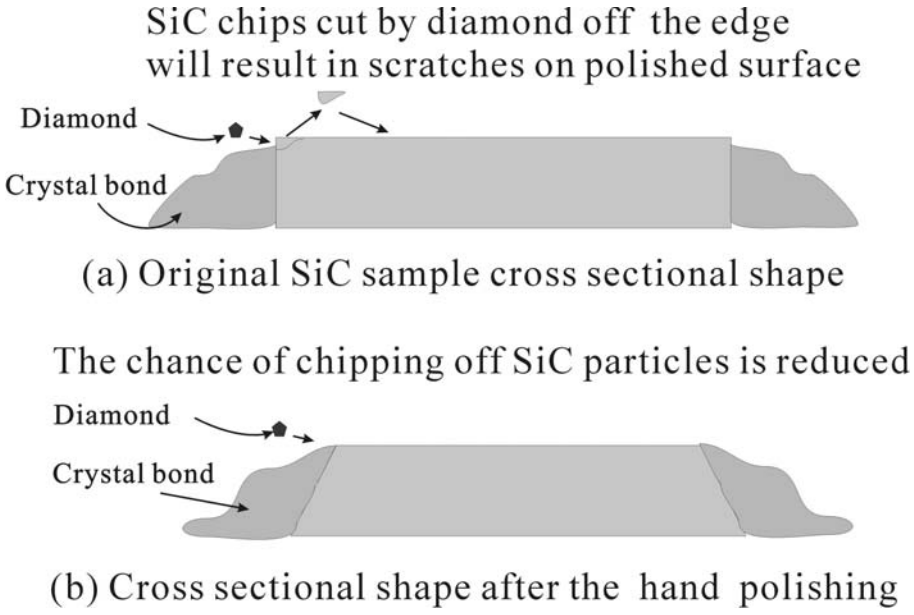


Figure D.1 (a) No bevels made before the polishing may cause chipping during the polishing. The chips will then scratch the sample surface. (b) Bevels made before polishing will reduce the chances of chipping during the polishing.

After making the bevel edges, clean the samples in boiled iso-propanol solution for ten minutes and rinse the samples in deionized water thoroughly. Make sure that there is no contamination of diamond lapping compound on the samples.

D.2 MOUNT SAMPLES

Mounting the samples is the most critical procedure of mechanical polishing. Because multiple samples will be polished each time, any inclination or non-leveled sample will affect the whole polishing. Not only a lot of time and diamond lapping compound will be wasted just to obtain a flat polishing surface for all the sample areas, but also some samples will be over

polished so that they are too thin for practical usage. Fig. D.2 shows some critical steps to mount samples.

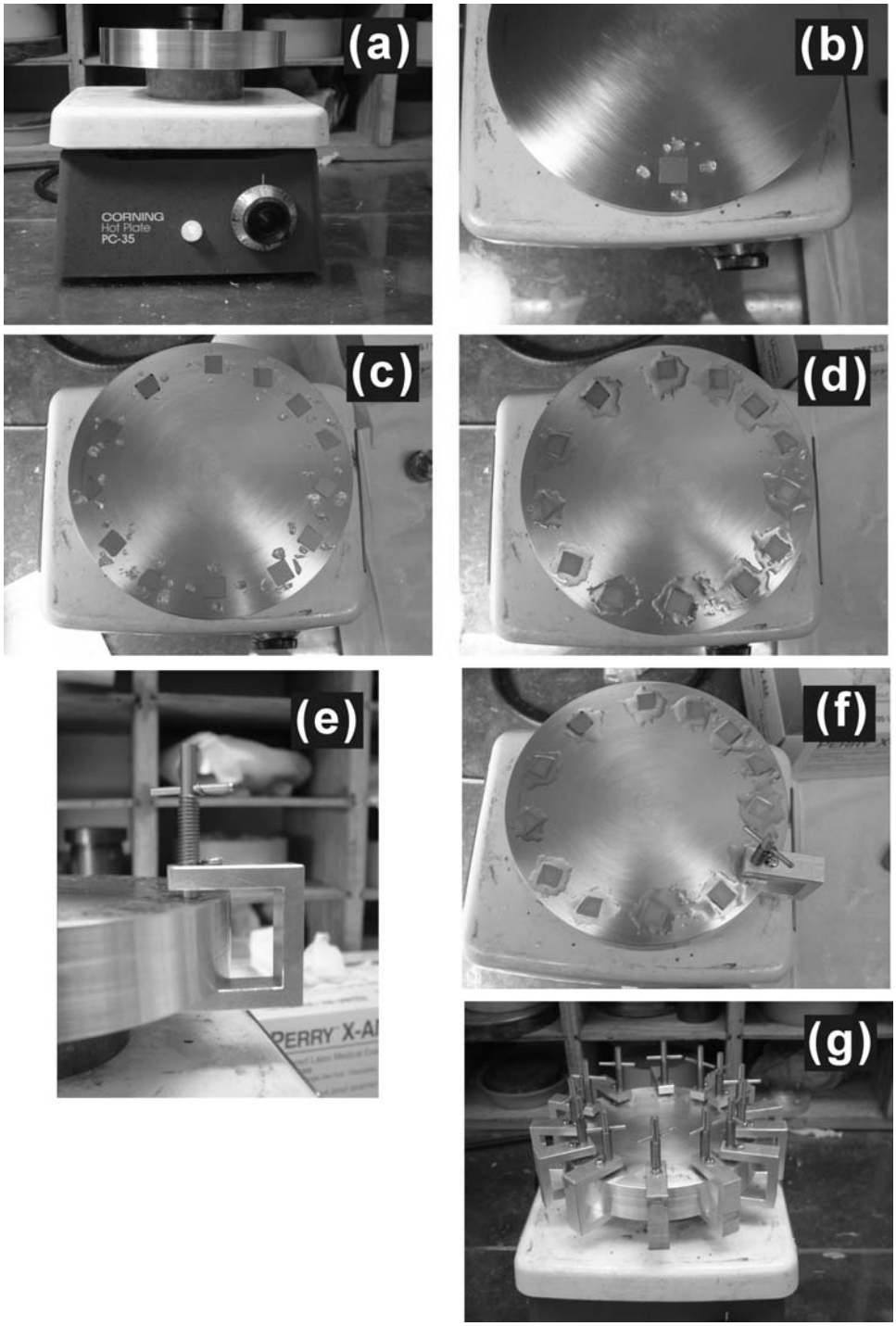


Figure D.2 Critical steps during the sample mount, as will be explained in the text.

1. Place the disks as shown in Fig.D.2a. Turn on the hot plate (Turn the knob to 4 and wait for ~20 minutes).
2. Place all the samples on the plate with the desired polishing surface up. Carefully place small pieces of crystal bond around each sample. (Fig. D.2b and c) (If one wants a double side polished sample after this polishing job, to distinguish the different surfaces after the polishing, it is highly recommended that one should scratch the back surface with a diamond scribe.)
3. After the crystal bond melts, use a Q-tip as a stick to spread it all round the samples. Make sure that all the edges of the samples are in good contact with the crystal bond. Any bubbles or gaps should be avoided. There should be no cement on the top of the sample surface (Fig. D.2d).
4. Carefully clamp samples in the center with spring loaded C-clamps (Fig. D.2e and f). The clamps are spring loaded. Use alcohol to clean the tips of the clamps first. This procedure favors the samples to sit tightly against the plate so they will be leveled nicely.
5. After clamping all the samples (Fig. D.2g), turn off the hot plate and let it cool down for more than 2 hours until it reaches the room temperature.
6. Take off the clamps.
7. Use acetone wetted Kim-wipes to carefully wipe off the part of the crystal bond higher than the sample surface. Also clean the sample surface if there is any cement contamination. The final height of the cement should be lower than the samples. This will give a very good initial polishing plane. (It is recommended to perform this operation in a fume hood). The reason for doing so and the final schematic diagram is shown in Fig. D.3.

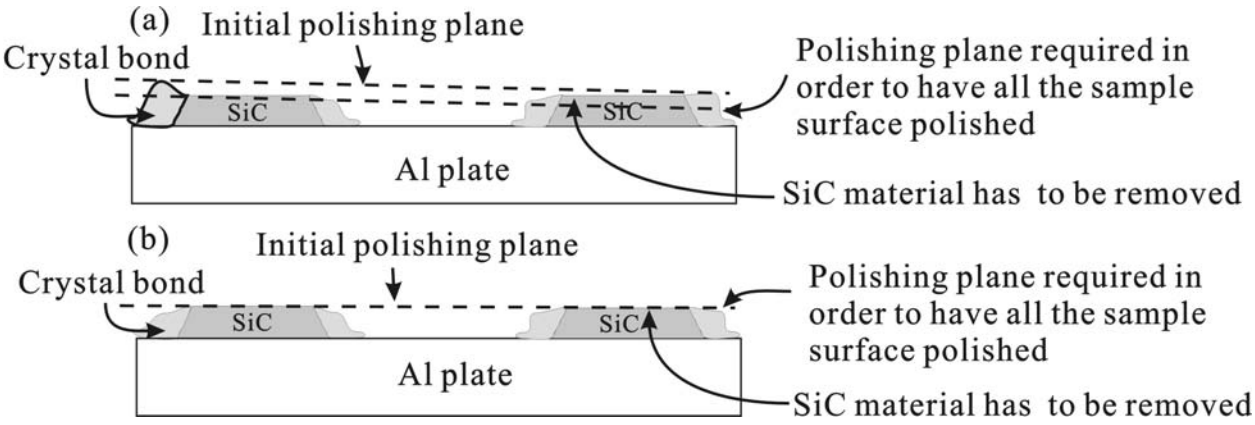


Figure D.3 (a) Schematic of a bad sample mount with a "big" (>0.5 degree) initial angle for mechanical polishing. (b) Schematic of an ideal sample mount so that almost no material is wasted during the initial stage of polishing.

D.3 POLISH SAMPLES

Paint four spots on the corners with any permanent marker (Fig. D.4). Record the initial polishing thickness.

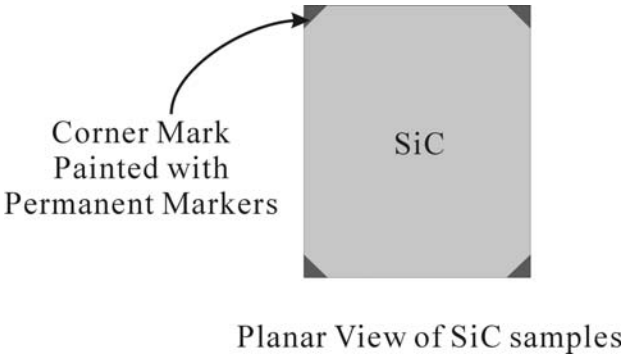


Figure D.4 The schematic of marking the samples prior to the polishing.

1. Turn on the polishing machine.

2. Install the polishing table for 60 μm diamond paste. Squeeze 2cm long 60 μm diamond lapping compound out of the syringe and dissolve the paste with kerosene. Add kerosene to fill the central hole on the back of the polishing disk as a necessary lubricant. Start polishing until all four marks on all the samples disappear. Record the polishing duration time. Measure the thickness loss due to this process if necessary. (Note: If the polishing speed is too low, increase the pressure by applying more lead bricks. Although more bricks will lead to larger pressure on the sample and in term faster polishing rate, one should be very careful not to crack the samples by the extra pressure applied.)
3. Clean the sample disk completely with the specific brush in cold soap/alconox water. This step should be carried out very carefully. Any cross contamination must be avoided. During this period, only the latex gloves and the kimwipes can be deemed as a diamond free media. After cleaning, record the thickness and calculate how much material has been removed. Check if the amount of material removed is normal.
4. Repeat this procedure for 30 μm followed by 15 μm diamond lapping compound. Cross contamination of diamonds with different sizes on polishing table or disks must absolutely avoided. This will determine the final polishing quality.
5. Switch to the 6 μm diamond paste polishing table. Polish using 6 μm diamond paste with polishing cloth applied until the surface looks like a perfect mirror. No visible scratches should be seen on the sample surfaces. Record the polishing duration time. Repeat the thickness measurement and check the amount of material removed.
6. Continue polishing using 3, 1, $\frac{1}{2}$ and $\frac{1}{4}$ μm diamond paste with polishing cloth in the order of decreasing diamond sizes. The polishing time should be the same as the 6 μm

diamond polishing time in order to get the best result. In case the 6 μm diamond polishing time is more than 24 hours, one just needs to do 24 hour polishing for each of the remaining steps. In many cases, according to experience, 8 hours of polishing is enough to get fairly good polished surfaces. Clean the polishing disk between each step. Use the correct polishing table for different size diamond paste. If necessary, check the thickness after each step to determine the amount of material removal.

D.4 REMOVAL OF SAMPLES

Put the plate on the hot plate setting and start to heat up the disk. Wait ~20 minutes until the crystal bond melts. Take off the samples. Turn off the hot plate. Clean samples using iso-propanol. The samples are now ready for use.

APPENDIX E

OPERATION AND MAINTAINANCE NOTES FOR THE E-BEAM EVAPORATOR AND VARIAN 936-60 LEAK DETECTOR

E.1 Operation Procedure for Varian 936-60 Leak Detector

Start-up after a long time standby (complete shut down status)

1. Set the following controls to the initial condition indicated below:

   Start/Reset/Vent Switch- RESET (on the front right corner of the top table)

Gross Leak Test – OFF	Filament on/off – OFF
Transfer Pressure – 20 millitor	Pumps (all three) – OFF
Leak – OFF	Pumping Mode – Service Pump
Reject Level – 10	Filament – 1
Calibrate – Full Counter Clockwise	Other Controls – As is

2. Plug the machine into an appropriate receptacle (3 pin socket). Connect the compressed air hose.

3. Turn on the switches for the roughing and fore pumps. Wait 10 minutes and turn on the switch for the Diffusion pump. Allow 20-25 minutes for the diffusion pump to warm up. Add liquid nitrogen to the cold trap.
4. Place the ELECTRONICS Circuit breaker in the ON position. When the SPECTROMETER TUBE PRESSURE indicator is in the green band, turn the PUMPING MODE switch to the OPERATION position. (Sometimes, the spectrometer tube doesn't indicate in the SERVICE PUMP mode. If so, one can just turn the pump mode to OPERATION and check the spectrometer tube pressure.). Set the FILAMENT on/off switch to the AUTO/RESET position.

Leak Checking

1. Set the Start/Reset/Vent switch to the VENT position.
2. Connect the piece to be tested to the test port and secure the connection.
3. Set the Start/Reset/Vent switch to the START position. If the Spectrometer tube pressure meter reading rises above the green band, the filament will turn off. Move the Start/Reset/Vent switch to RESET and then back to START.
4. When the TEST lamp lights, wait for the Leak Rate meter to come to rest. If the vacuum can not reach the required level, a gross leak check has to be considered.
5. Put the Range Selector switch in a position so that the Leak Rate meter shows downscale (the needle is indicating some small value on the meter in the scale but not below or equal to zero). Adjust Threshold and Volume to the values so that you feel comfortable.

6. Proceed with leak checking of your piece by carefully spraying helium gas around. Consult an experienced person if you don't know how to operate a Helium Tank.
7. After the leak is located, turn the Start/Reset/Vent switch to RESET and then to VENT. Remove the test piece from the test port. Insert the plug back and secure.

Shut-down

1. Set the Filament on/off switch to OFF.
2. Set the Electronics and Diffusion pump circuit breakers to OFF.
3. Wait at least 20 minutes to let the diffusion pump cool down.
4. Turn the Pumping mode switch to the SERVICE VENT position. Pour out the excessive liquid nitrogen. Put the cold trap back.
5. Turn the Pumping mode switch to the SERVICE PUMP position and wait until the test port pressure reads about 10 millitor.
6. Set the Rough and Fore Pump breakers to OFF.

E.2 OPERATION PROCEDURE FOR THE E-BEAM EVAPORATOR

Although the detailed step by step operation manual can be found in an appendix of Oleg Shigiltchoff's dissertation, due to some changes which have been made to the setup, we here present the revised step by step operation of the e-beam evaporator.

1. Preparation:

   a) Turn on the *compressed air valve*, *thermocouple vacuum gauge controllers (TC) 1* and *2,* and the *thickness monitor*.

   b) Place the *gate valve* above the mechanical pump to the OPEN position.

   c) Put the *Fore pump valve* switch on the front panel to the ON position.

   d) Allow pumping until the vacuum in the Fore pump line is lower than 1 milliTorr, indicated by *TC* 2 (At least 20 min pumping is preferred before turning on the diffusion pump).

   e) Meanwhile, clean the (SiC) samples using Acetone, Alcohol, and dilute HF solution 10 min each in ultrasonic cleaner. Rinse the samples thoroughly in deionized water afterwards. Dry the samples in air with kimwipes.

2. Load Samples:

   a) Place the *Hoist* switch to the UP position. Push the *Hoist Safety* button and move up the Bell Jar to open the chamber completely.

   b) Choose the correct mask plate. Position the samples onto the mask plate with the surface to be deposited facing down. Load the samples on the mask into the chamber onto the sample holder. Cover the samples with another Aluminum plate.

   c) Close the shutter so that it covers the samples completely.

   d) Place a quartz glass plate between the e-gun and the Bell Jar glass wall so that the possible deposition of metal onto the bell jar is shielded by the quartz plate.

   e) Put the Al shields inside the chamber to protect the glass jar from metal deposition. Carefully position the Aluminum shields so that they do not touch the e-gun leads and the glass Bell Jar will not hit the shield as it is lowered later.

f) Grease the L-gasket on the Bell Jar. Set the *Hoist* Switch to the DOWN position. Push the *Hoist Safety* Button to lower the Bell Jar all the way until it sits evenly on the metal ring. During this procedure, extra care should be taken to ensure that the Bell Jar does not crash into the Aluminum shield.

g) Close the *Vent Valve* if it is open.

3. Rough Pump: Close the *Fore Line Valve* on the front panel. Put the *gate valve* above the mechanical pump to the CLOSE position. Set the *Rough Line Valve* to the OPEN position.

   After the valve actually opens (a click should be heard), gradually open up the gate valve to avoid harsh pumping. The chamber vacuum should be pumped down below 1 milliTorr as indicated by *TC* 1 using the roughing pump.

4. Diffusion Pump:

   a) Close the *Rough Line Valve*. Open the *Fore Line Valve*. Turn on the cooling water for the diffusion pump on the back side of the evaporator. The water flow must be checked on the flow-meter. A comfortable fast spinning of the flow meter indicator should be observed.

   b) Turn on the *Diffusion Pump* switch. Wait 20 minutes.

   c) Fill the cold trap with liquid nitrogen until liquid N_2 pours out of the cold trap exhaust. Wait 20 minutes.

   d) If the Bar Jar chamber vacuum is above 1 milliTorr, switch back to the Rough Line pumping by closing the *Fore Line Valve* and opening the *Rough Line Valve*.

   e) When the vacuum is ready, close the *Rough Line Valve*. Open the *Fore Line Valve* and *Main Valve* to pump the Bell Jar Chamber using the diffusion pump.

f) After one hour of pumping with the diffusion pump, one can use the ion gauge to check the Bell Jar Chamber Vacuum. 2×10^{-6} Torr vacuum can be achieved by 2 hours of pumping if there is no leak. Usually a 1×10^{-5} Torr vacuum is good enough for Nickel or Gold deposition. For Aluminum, base pressure in 10^{-6} Torr is strongly recommended.

5. Evaporation:

a) When the chamber vacuum is ready, turn on the cooling water for both the thickness detector and the e-gun head. Turn on the e-gun power supply *Main Power* switch. The interlock light for the cooling water should be off.

b) Turn on the *High Voltage*. (Don't do this in low vacuum that is higher than 10^{-3} Torr or atmosphere).

c) Start to slowly turn up the *Emission Control* clockwise from 0 to about 100-150 μA. It should start with a click. This should be done very slowly. On the scale of the pot used to adjust the current, an average 2 increments is made per 10 seconds. Watch the metal piece in the crucible through the window in the aluminum shield and the protecting quartz plate.

d) As the metal piece melts, the deposition rate will be shown on the Sycon STM-100 thickness monitor (Parameters "Z-factor" and "Density" should be set prior to the deposition starts. See the manual on top of the rack). 1-1.5 Å/s rate is preferred. When the rate is reached, zero the initial reading and simultaneously open the shutter so that the samples are exposed to the evaporation source.

e) About 15-20 minutes are needed to deposit a 1500 Å thick metal layer. When the desired thickness is reached, close the shutter.

f) Turn down the e-gun *Emission Control* slowly counterclockwise all the way to 0.

g) Turn off the *High Voltage*.

h) Turn off the *Main Power* switch for the e-gun power supply.

i) Close the *Main Valve*.

j) Turn off the *Diffusion Pump*. Wait about 30 min for the chamber and diffusion pump to cool down.

6. Unload Samples and Shut down Evaporator:

a) Turn off the cooling water for the e-gun and thickness monitor.

b) Open the Vent Valve to vent the chamber. Note that the vent is connected to a Nitrogen gas tank. The valve of the gas tank needs to be opened. Set the gas flow regulator so that the pressure of the outgoing gas is low (smaller than 5 psi for sure) to avoid over pressuring the chamber. It should take about 10 minutes for the chamber to reach atmosphere pressure. Don't let the compressed Nitrogen flow over a long time, because it may cause condensation.

c) Open the Bell Jar chamber. Remove the aluminum shield. Remove the samples.

d) Take out the quartz plate. Clean off the deposited metal by using alcohol wetted Scotch Brite® pad.

e) Close the Bell Jar Chamber. Pumping down the chamber to 1 millitor with mechanical pump is optional.

f) After about 1 hour, turn off the cooling water to the diffusion pump.

g) Turn off the compressed air. Turn off all the gauge controllers and the thickness monitor.

E.3 TECHNICAL NOTES

Varian Leak Detector 936-60:

1. After a long time (over months) complete standby of the Varian 936-60 leak detector, a complete oil change for the two mechanical pumps is highly recommended. Changing the diffusion pump oil is optional. If it is necessary, use SANTOVAC 5 oil only.
2. If the filaments do not turn on, one can switch to filament 2 and try again. If both filaments are not working, disassembling the spectrometer tube is inevitable. Read the manual (on the rack above the furnace) carefully before taking off the spectrometer tube. When putting the ion source back, one should make sure that the longest leg of the ion source doesn't touch the chamber wall. After assembly, one should use an ohmmeter to check that this pin doesn't connect to the spectrometer tube wall.
3. If there is no response from the ion source emission, check the voltage between the test points TP1-TP4, TP2-TP4, and TP3-TP4. Make sure that the voltage is correct as specified in the manual. If the voltages are not right, check the breakdown diodes and the high power resistor since they are the likely ones that go bad. The troubleshooting should always follow the manual troubleshooting chart.
4. The standard calibrated helium leak source is functional for a very long time with a small amount of leak rate drop. If an accurate calibration is needed, contact Kurt J. Lesker or Duniway Company to do the calibration.
5. The company Duniway (Duniway.com) is a very useful knowledge source to work with Varian leak detectors.

6. The diagram in Figure E.1 showing the spectrometer tube is extremely useful.

Evaporator:

1. Great care should be taken when raising or lowering down the hoist. Don't push the *Hoist Safety* button for too long when the hoist is at the highest or lowest position. You may burn the motor if you do that. Lubricate the hoist as often as you can. Monthly lubrication is recommended.
2. Never turn on the high voltage for the e-gun power supply at low vacuum ($>10^{-3}$ Torr) or atmosphere. The paschen curve should be kept in mind. The vacuum should be better than milliTorr for safe operation of the e-gun.
3. If any over current is observed on current meter of the e-gun power supply, clean the e-gun head first to avoid any metal flakes shorting the circuits.
4. The copper pipe line under the table has been painted with Glyptal® to stop the leak in the machined brass parts and joints. The possible leak sources of the Chamber are:
    1) The O-ring on the side of the Main Valve connecting the valve pipe line,
    2) The O-ring under the metal ring.
    3) The O-rings on the feedthroughs on the stainless table,
    4) The O-ring on the front panel of the Main Valve,
    5) The O-rings of the e-gun feedthroughs.

    Check these o-rings first if any leak problem occurs. Do not use screwdrivers or any metal pieces to take off O-rings.

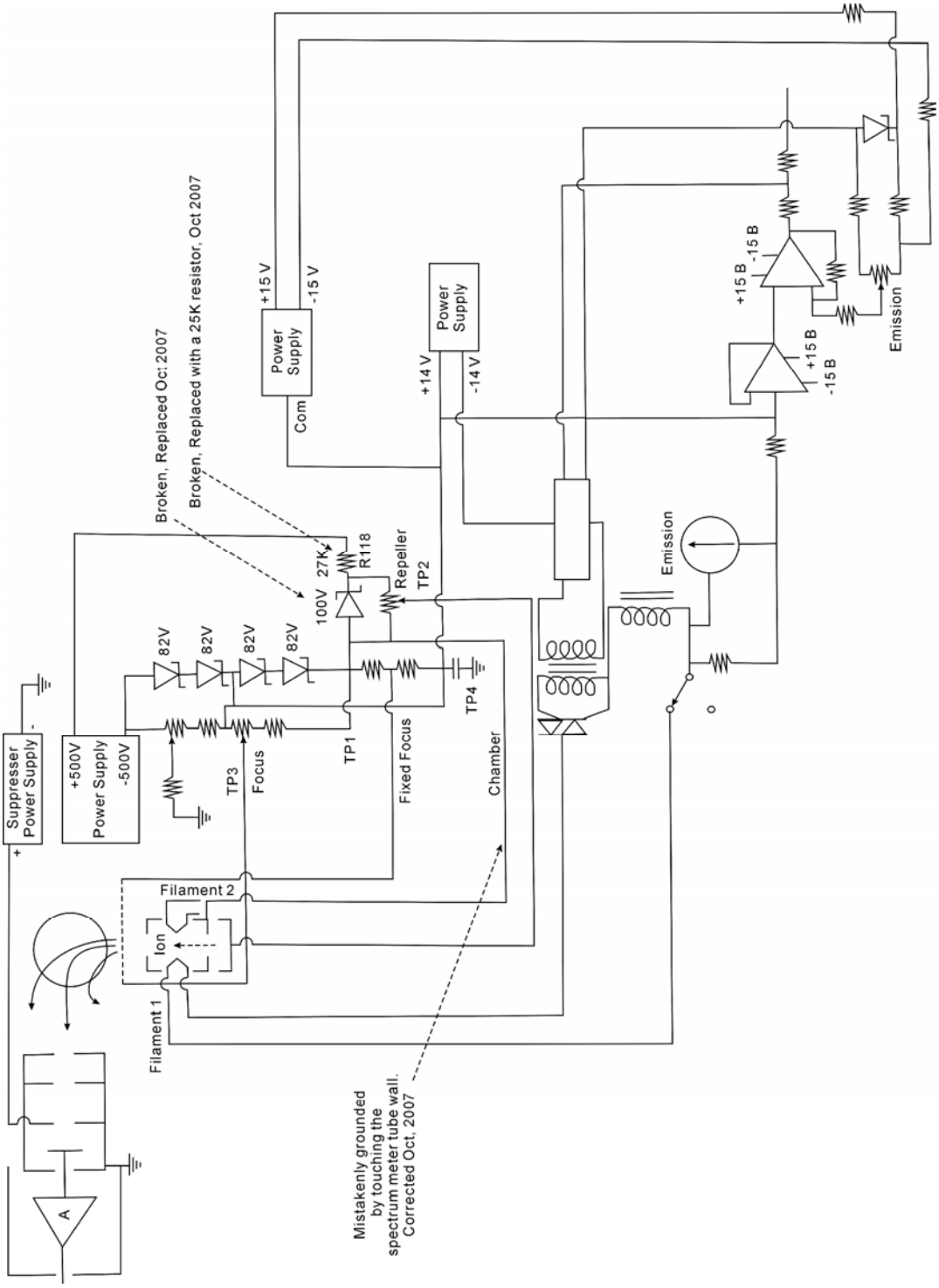


Figure E.1 Circuit diagram of Varian 936-60 leak detector mass spectrometer tube drawn by the electronic shop. This diagram is much more useful than the one in the manual to help finding the circuit problem.

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