ANALYSIS, DESIGN, AND OPTIMIZATION OF ANTENNAS ON CMOS INTEGRATED CIRCUITS FOR ENERGY HARVESTING APPLICATIONS

by

Minhong Mi

BS, Peking University, China, 1996

MS, Shanghai Institute of Technical Physics, Chinese Academy of Sciences, 1999

Submitted to the Graduate Faculty of

School of Engineering in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

University of Pittsburgh

2003

UNIVERSITY OF PITTSBURGH

SCHOOL OF ENGINEERING

This dissertation was presented

by

Minhong Mi

It was defended on

July 29th, 2003

and approved by

James T. Cain, Professor, Electrical Engineering Department

Ronald G. Hoelzeman, Associate Professor, Electrical Engineering Department

Raymond R. Hoare, Assistant Professor, Electrical Engineering Department

Michael R. Lovell, Associate Professor, Mechanical Engineering Department

Qing-Ming Wang, Assistant Professor, Mechanical Engineering Department

Dissertation Director: Marlin H. Mickle, Professor, Electrical Engineering Department

ABSTRACT

ANALYSIS, DESIGN AND OPTIMIZATION OF ANTENNAS ON CMOS INTEGRATED CIRCUITS FOR ENERGY HARVESTING APPLICATIONS

Minhong Mi, PhD

University of Pittsburgh, 2003

Radio frequency (RF) energy harvesting is a promising technology that finds applications in such products as Radio Frequency Identification (RFID) and Active Remote Sensing (ARS). In order to reduce the overall size and the manufacturing cost of the device, it is highly desirable to integrate the energy-harvesting antenna, onto the same monolithic CMOS integrated circuit as the functional circuitry. The focus of this dissertation is on the extension of the more traditional approach to antenna design while overcoming the many barriers to the design and analysis of tiny antennas that are fabricated on a CMOS die resulting in an extremely unfriendly environment. Specifically, the major challenges for building antennas on CMOS ICs have been identified. The Finite Element Method (FEM) was found to be the most suitable numerical method for the full-wave analyses of antennas on CMOS ICs after a comparison of the major numerical methods available for electromagnetic simulations. A complete power measurement system that requires no cable connection to the antenna under test has been constructed. It offers accurate measurement of the available power from the on-chip antennas with the help of the annealing approach to impedance matching, which was also developed in this research. The various design factors for antennas on CMOS ICs have been evaluated through both simulation

and experiments. It was concluded that the properly designed spiral antennas are good candidates for the on-chip energy-harvesting applications.

DESCRIPTORS

Antenna	CMOS Integrated Circuits
Energy Harvesting	Finite Element Method
Impedance Matching	RF measurement

ACKNOWLEDGEMENTS

There are a lot of people I am thankful to for the completion of my study at the University of Pittsburgh. But first of all, I'd like to express my sincere gratitude to my advisor, Dr. Marlin H. Mickle, for providing me with this great opportunity for exploring the wonderful world of RF and microwave microelectronics. Without his guidance, support, and perseverance, I would not have been able to enjoy so much fun.

I'd like to thank Dr. Qing-Ming Wang, Dr. James T. Cain, Dr. Williams W. Clark, Eric Reiss, Frank Marx, Fengting (Frank) Xu, and Dr. Yongping Ding for their assistance in the fabrication of the antenna chips at the John A. Swanson Microsystems Lab.

And last but not least, I would like to thank my parents for insisting on my going out of the small village to attend college. I thank my wife, Liqun Yin, for her unfailing love and support. And thanks to my son, Michael, with whom I feel happy and hopeful.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1.0 INTRODUCTION

The theory and practice of antenna design have supported and represented a mature discipline for many years. As the size of the antenna becomes extremely small compared to a wavelength, it is very difficult to test hypotheses compared to what was possible with the historical antenna development.

The reduced size magnifies the effects of approximations and simplifications that were not critical for antennas on the order of a wavelength. It has also been suggested that the tiny antennas may represent more of an integrated effect than an antenna. While this concept involves interesting physical phenomena, it is the subject of a research area that is just emerging.

The focus of this dissertation will be on the extension of the more traditional approach to antenna design while overcoming the many barriers to the design and analysis of tiny antennas that are fabricated on a Complementary Metal Oxide Semiconductor (CMOS) die, resulting in an extremely unfriendly environment.

1.1 Radio Frequency Energy Harvesting with Integrated Antennas

Power transmission by electromagnetic waves is a century old idea, but it did not attract too much attention from people until high frequency power sources were widely available in the 1930's. Since then, quite a number of developments in both technology and applications have followed [1]. Today, it is not only considered as an attractive means of transmitting power in space applications [2], but also found to be useful in a variety of commercial applications, such as Radio Frequency Identification (RFID) [3] and Active Remote Sensing (ARS)[4][5].

RFID systems use magnetic or electromagnetic fields for power supply and data exchange between data carrying device and the reader. These systems are more reliable and resistant to unauthorized copying or modification due to this unique characteristic. They are effective in manufacturing and other hostile environment where barcodes cannot survive. It is a technology that is beginning to conquer new mass markets, whose total market value is expected to reach $2.6 billion in 2005 [6].

An RFID system is always made up of two components [3]: the transponder, or the tag, and the interrogator, or the reader, as shown in Figure 1.1. The RFID reader provides the transponder with clock, energy, and reads, or writes, data to it. The transponder is only activated when it is within the interrogation zone of a reader. When activated, it sends the identification information stored on it back to the reader using the power supplied by the reader.

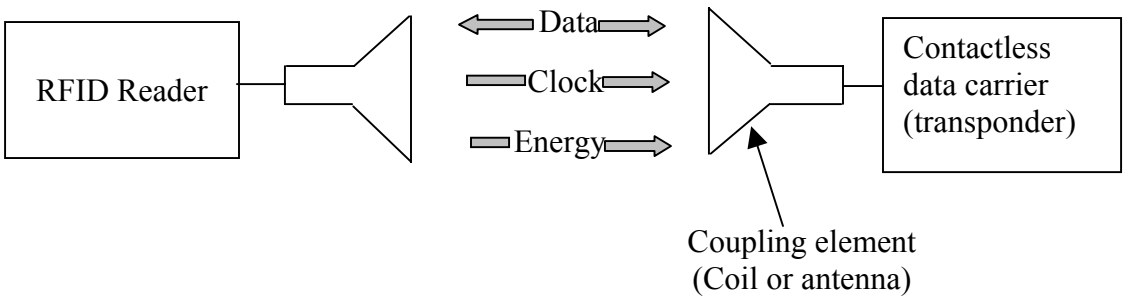


Figure 1.1 The RFID system (After K. Finkenzeller [3])

The RF powered active remote sensing system is similar to the RFID system in concept, but differs in that the ARS has an integrated sensor on the transponder and sends the measured data (*e.g.* temperature, motion, etc.), instead of identification information, back to the reader when activated.

Currently, the digital circuitry of an RFID tag is fabricated using a standard CMOS process. The coupling element in the form of a wound or printed metallic coil is fabricated separately and electrically connected with bond wires, or their equivalents, through an assembling process, which is fairly complicated and accounts for a considerable part of the total cost of a tag. The mechanical connections also make the product fragile and more vulnerable to mechanical failures. For some active remote sensing applications, a discrete coupling element may also be too big. Therefore, it is highly desirable to integrate the coupling element onto the same monolithic integrated circuit (IC) the digital logic circuitry (and the sensor for ARS) is built on. The resulting IC contains no connecting wires or batteries and relies solely on the Radio Frequency (RF) energy transmitted by the reader to power itself. In this dissertation, such an IC will be termed a Stand Alone System On Chip (SA-SOC).

If successfully implemented, the integration of the antennas onto the CMOS ICs will not only lead to a substantial reduction in the cost of RFID tags, but also make them more reliable and versatile, which will certainly help RFID systems find even larger markets, such as replacement for bar codes on merchandise in warehouse or supermarkets. It can also possibly bring some futuristic ideas, such as smart dust [7], closer to reality.

Most RFID systems use a scheme called “backscattering” to transfer information from the transponder to the reader. It works by varying the effective load connected to the energy-harvesting antenna and thus changing its monostatic or backscattering radar cross section (RCS). The reader monitors the change in the RCS of the tag and interprets it as the information sent by the tag. In this kind of system, the energy-harvesting antenna plays two roles, one as a receiving antenna, the other as a scatterer. The thorough investigation of the relationship between the scattering and transmission (radiation) characteristics of a given antenna is fairly involved [8]

and will not be given here. But generally speaking, a better transmitting antenna, and thus a better receiving antenna, should offer more room for the modulation of its effective RCS by changing the load connected to it. So the desired characteristics for the two different roles of an energy-harvesting antenna coincide. For the sake of convenience, only its role as a receiving antenna is addressed in this work.

RFID systems used to operate at relatively low frequencies, such as 13.56MHz. But recently, a few products that operate at the ISM (Industrial-Scientific-Medical) bands of 915MHz and 2.4GHz have emerged. For the antennas on CMOS ICs to work efficiently, an even higher frequency may be necessary. However, the highest frequency supported by the equipment in the labs in the School of Engineering is 915MHz, so all the work in this research had to be done at this frequency. As a consequence, the efficiency of some antennas we will see is much lower than that of a conventional antenna even if the antenna sizes exceed the economical limits for commercial applications considerably. Nevertheless, the methods and ideas presented are valid for higher operation frequencies.

The RF front end of an SA-SOC can be divided into three major blocks as shown in Figure 1.2.

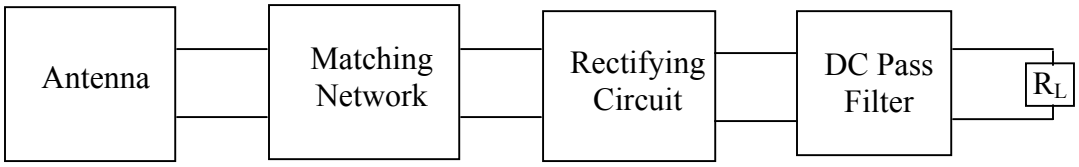


Figure 1.2 Block diagram of the front end of a SA-SOC

The antenna is the device that captures and delivers the RF energy. It is the subject of this research. The rectifying circuit and the DC pass filter convert the RF energy captured by the

antenna to DC voltage that drives the digital functional circuitry modeled by R_L in the diagram. The matching network is necessary to ensure maximum power transfer from the antenna.

With the structure shown in Figure 1.2, there is continuous DC power supply to the load R_L as long as the SA-SOC is within the interrogation zone of the reader. The power consumed by the load is always equal to that accepted by the rectifying circuitry. On the other hand, the so-called "charge pump" circuit has been utilized in some RFID systems, with which the RF energy captured in a long period can be accumulated and used for activating the digital circuits for a very brief period. This makes it possible for an SA-SOC to work in a much weaker electromagnetic field. In such devices, the power accepted by the rectifying circuitry is not necessarily always equal to that consumed by the load, although the total *energy* delivered and consumed should be equal as in the previous case. In this dissertation, no distinction will be made between the two types of systems since the antenna that delivers the highest power should be the one capable of delivering most energy in a given period of time.

1.2 Fundamental Parameters of Antennas

By definition, an antenna is "a means for radiating or receiving radio waves" (IEEE Std 145-1983). So the most important parameters that characterize the performance of an antenna are closely related to how good it is at delivering electromagnetic energy from the source into free space (transmitting antenna), or capturing electromagnetic energy from the free space and delivering it to the load (receiving antenna). The most prominent parameters include radiation pattern, directivity, efficiency, gain, polarization, input impedance, and bandwidth. The following are the definitions of these fundamental parameters and their desired values for energy-harvesting antennas. The definitions of the parameters are cited from [9].

1.2.1 Radiation Pattern, Directivity, and Gain

Antenna radiation pattern is defined as "a mathematical function or a graphical representation of the radiation properties of the antenna as function of space coordinates. In most cases, the radiation pattern is determined in the far-field region and is represented as a function of the directional coordinates. Radiation properties include power flux density, radiation intensity, field strength, directivity phase or polarization." Directly following this definition, we can derive such terms as power pattern and field pattern, which are graphs of the spatial variation of the power and electric (or magnetic) field along a constant radius, respectively. A convenient and most commonly used set of coordinates for plotting radiation pattern is shown in Figure 1.3

The radiation pattern of an antenna is often presented as a two-dimensional or three-dimensional plot with constant radius and varying θ and/or ϕ values.

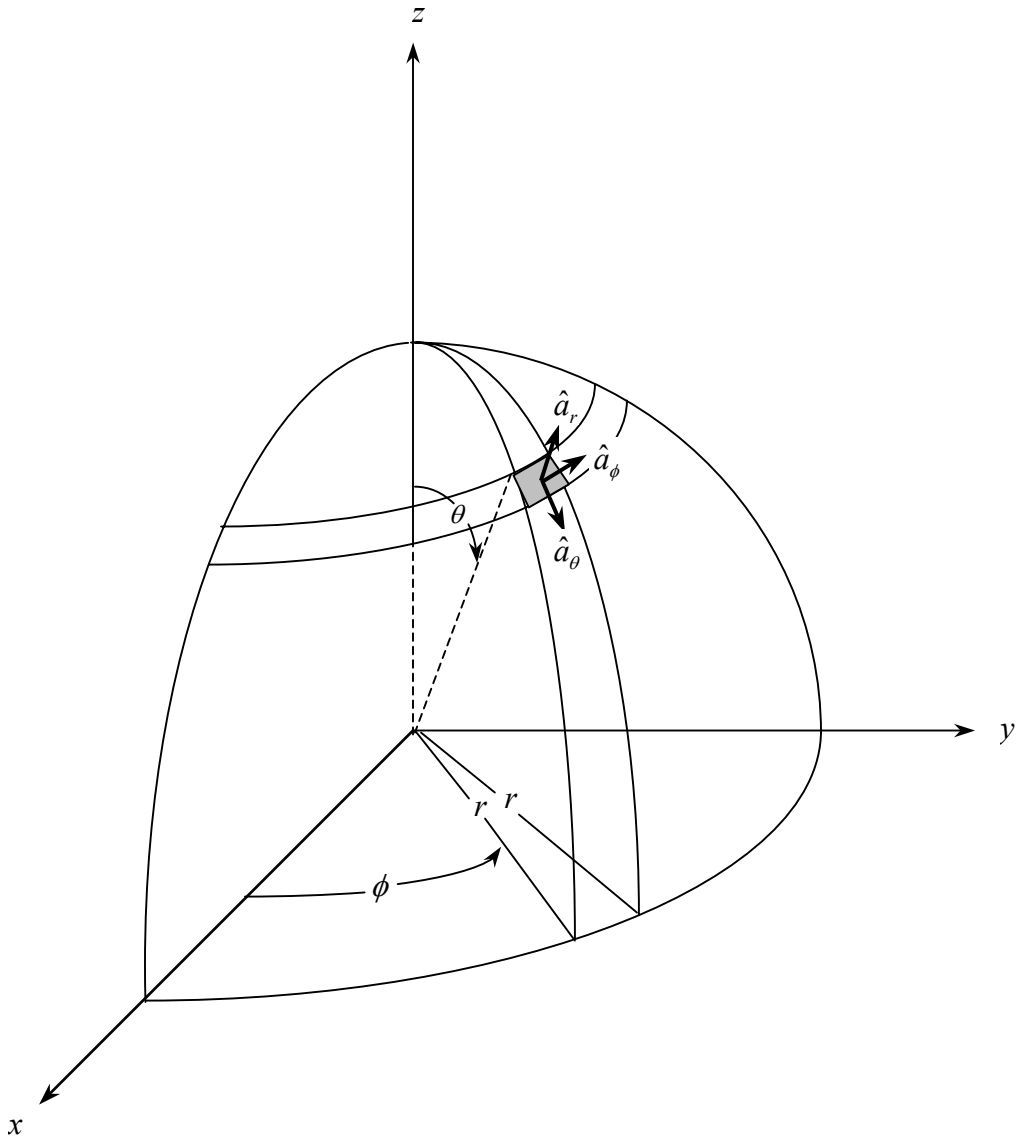


Figure 1.3 Coordinate system for antenna analysis

The directivity of an antenna is defined as "the ratio of radiation intensity in a given direction from the antenna to the radiation intensity averaged over all directions. If the direction is not specified, the directivity of maximum radiation intensity is implied." Simply put, the directivity of an antenna describes the properties of radiating or receiving electromagnetic waves more effectively in some directions than others. An antenna is said to be *isotropic* if it radiates equally in all directions. Otherwise, it is called *directional*. More specifically, an antenna is designated as *omnidirectional* if it has an essentially nondirectional pattern in a given plane and a directional pattern in any orthogonal plane.

Directivity only accounts for the directional capabilities of an antenna, and does not include the effects of the efficiency of the antenna. When the antenna efficiency is taken into consideration, the parameter becomes the gain of the antenna, which is defined as "the ratio of the intensity, in a given direction, to the radiation intensity that would be obtained if the power accepted by the antenna were radiated isotropically. When the direction is not stated, the power gain is usually taken in the direction of maximum radiation."

It is easy to understand that a directional antenna offers a larger detection range when everything is assumed equal and the maximum directivity is in the direction of the incoming wave. However, this places restrictions on the orientation of the antenna with respect to the incoming wave, which is not always possible for the energy-harvesting applications. For example, the orientations of the antennas are extremely difficult to control when the RFID tags are used for automatic checkout of merchandises in supermarket. On the other hand, omnidirectional antennas are less sensitive to the orientations, but they have shorter detection ranges compared to the directional antennas.

The radiation pattern depends mainly on the type and geometric shape of the antenna. So it is an important factor to consider when we choose the antenna type and shape for a given application.

1.2.2 Antenna Efficiency

Antenna radiation efficiency is defined as "the ratio of the radiated power to the total power accepted by the antenna". The radiation efficiency e_{cd} relates the gain of the antenna G and directivity D by

$$G = e_{cd} D \tag{1.1}$$

Antenna radiation efficiency only takes into account the losses within the antenna structure itself. It does not include losses at the input terminals. When such losses are considered, the parameter becomes the total efficiency e_0, which can be written as

$$e_0 = e_r e_c e_d \tag{1.2}$$

where e_r is the reflection (mismatch) efficiency, e_c is the conduction efficiency, and e_d is the dielectric efficiency. Usually it is very difficult to separate e_c and e_d, so they are often combined as e_{cd}, which is actually the radiation efficiency of the antenna.

The efficiency of an antenna is of great importance. It is even more critical for the antennas for energy-harvesting applications because it is the absolute power delivered by the antenna, instead of the signal to noise ratio, that is of significance for the SA-SOC. It is obvious that lower antenna efficiency leads to a tag with shorter detection range, or makes it totally unusable if the losses of the antenna are so large. Therefore, it is desirable to have high radiation efficiency, which, as we will see in the next chapter, is extremely difficult in the CMOS environment.

1.2.3 Antenna Polarization

The polarization of an antenna in a given direction is defined as "the polarization of the wave transmitted (radiated) by the antenna", which is further defined as "that property of an electromagnetic wave describing the time varying direction and relative magnitude of the electric-field vector; specifically, the figure traced as a function of time by the extremity of the vector at a fixed location in space, and the sense in which it is traced, as observed along the direction of propagation." Accordingly, the partial gain of an antenna for a given polarization in a given direction is defined as "that part of the radiation intensity corresponding to a given polarization divided by the total radiation intensity that would be obtained if the power accepted by the antenna were radiated isotropically." When the direction of the gain is not stated, the gain in the direction of maximum radiation is usually implied. Polarization may be classified as linear, circular, of elliptical.

In general, the polarization of the receiving antenna will not be the same as that of the incoming wave, and thus a reduction occurs in the amount of power extracted by the antenna from the incoming signal, which is commonly termed as polarization loss. The polarization loss can be taken into account by introducing the polarization loss factor (PLF), which is defined as

$$PLF = \left|\hat{\boldsymbol{\rho}}_w \cdot \hat{\boldsymbol{\rho}}_a\right|^2 \tag{1.3}$$

where $\hat{\boldsymbol{\rho}}_w$ and $\hat{\boldsymbol{\rho}}_a$ are the polarization vectors of wave and the antenna, respectively.

To ensure maximum power under all conditions, it is necessary to take the matching of polarization into consideration when designing the RFID system. For most applications, circularly polarized RF source should be used for the interrogator because the orientations of the

receiving antennas are hard to control. So use of a circularly polarized receiving antenna should give a 3dB boost in the signal level, compared to a linearly polarized one.

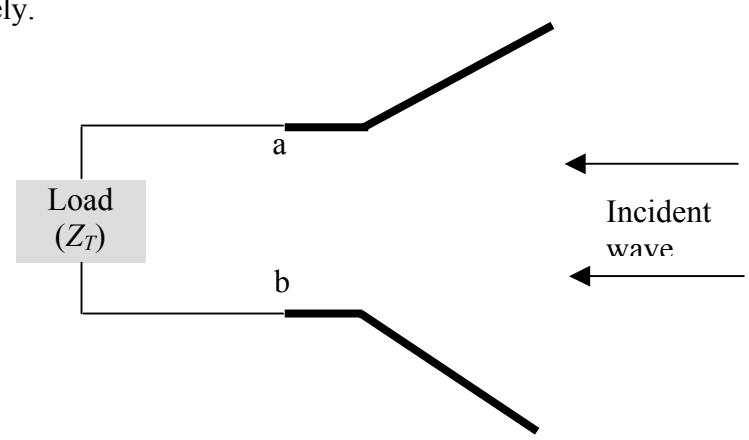
1.2.4 Input Impedance and Bandwidth

The input impedance of an antenna is defined as "the impedance presented by an antenna at its input terminals or the ratio of the voltage to current at a pair of terminals or the ratio of the appropriate components of the electric to magnetic fields at a point." In order to allow maximum power transfer, the impedance of an antenna must be matched to that of the source, or the load in case of a receiving antenna. Generally, the input impedance of an antenna changes as a function of frequency while the impedance of the source or load remains relatively constant. This limits the frequency range, within which a given antenna can operate because severe impedance mismatch outside the frequency range can make the percentage of power delivered from/to the antenna extremely low. That is the essence of the concept of antenna bandwidth, which is defined as "the range of frequencies within which the performance of the antenna, with respect to some characteristic, conforms to a specified standard." Because other antenna characteristics, like pattern, gain, and efficiency, do not change as rapidly as the input impedance, bandwidth of an antenna is usually determined by the impedance bandwidth, which is the range of the frequencies within which the input impedance is acceptable.

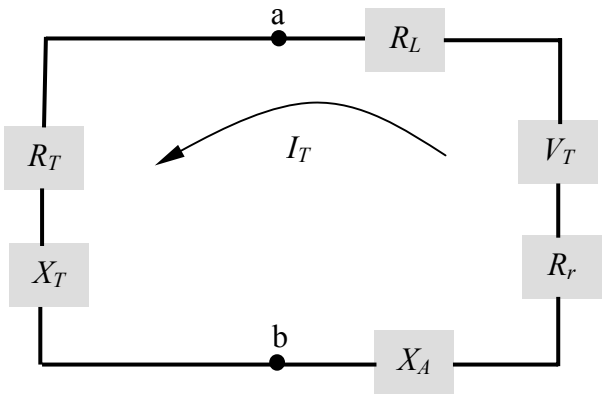
The input impedance of an antenna is usually defined at a pair of terminals. For a receiving antenna connected to a load that is shown in Figure 1.4 (a), the ratio of the voltage to current at the terminal designated as *a-b* defines the impedance of the antenna. It can be written as

$$Z_A = R_A + jX_A \tag{1.4}$$

where R_A is the antenna resistance while X_A is the reactance. The resistance part can further delineated into two components of R_r and R_L, which are the radiation resistance and the loss resistance, respectively.



(a) Antenna in receiving mode



(b) Thevenin's Equivalent circuit

Figure 1.4 Antenna and its equivalent circuit in the receiving mode (After Balanis [9])

In the Thevenin's equivalent circuit shown in Figure 1.4(b), V_T is the voltage induced by the incident wave, R_T and X_T are the resistance and reactance of the load. It can be easily shown that the power delivered to the load Z_T is maximized when the impedance of the antenna and the load is complex conjugate to each other, that is

$$R_r + R_L = R_T \tag{1.5}$$

$$X_A = -X_T \tag{1.6}$$

This is the well-known Maximum Power Transfer Theorem.

When the impedance of the antenna and the load are not matched, voltage reflection occurs, the severity of which is usually represented by the voltage reflection coefficient

$$\Gamma = \frac{Z_T - Z_0}{Z_T + Z_0} \tag{1.7}$$

where Z_{in} is the input impedance of the antenna, Z_0 is the impedance of the load, or the characteristic of the transmission line if the load is connected to the antenna through it. The reflection (mismatch) efficiency e_r is then defined as

$$e_r = (1 - |\Gamma|^2) \tag{1.8}$$

In addition to the strong dependence on frequency, antenna impedance is affected by such factors as geometry, method of excitation, and its proximity to surrounding objects. The input impedance of the load (the rectifying circuitry in the case of energy-harvesting) also varies with frequency and other factors like the input power level. So it is no wonder that ensuring the impedance matching between the antenna and the load under varied circumstances is extremely difficult. The primary way to perform impedance matching is to use a matching network, which can be composed of lumped circuit components or distributed microstrip lines. Since the impedance matching network must also be integrated on the same CMOS chip as the antenna and the rectifying circuit, its capability is oftenlimited because of the poor quality of the components and the limited available space. So it is necessary to take the input impedance of the antenna into consideration and possibly design the matching network at the same time with the

antenna. Or ideally, the antenna should be designed in such a way that its impedance is equal to the complex conjugate of the load and thus making the matching network unnecessary.

Since the SA-SOC is usually powered by an RF source at a single fixed frequency, the antenna does not necessarily have a wide bandwidth. However, it is crucial that the impedance of the antenna be stable and insensitive to changes such as manufacturing variations in geometry, presence of other objects in the nearby area, and temperature or humidity variations. This is necessary to ensure proper impedance matching under all conditions and thus a robust product.

1.2.5 Desired Characteristics of Energy-harvesting Antennas on CMOS ICs

All the above mentioned antenna parameters can be linked to the available power from the antenna by the concept of maximum effective area, which is defined as "the ratio of the available power at the terminals of a receiving antenna to the power flux density of a plane wave incident on the antenna from the direction of maximum radiation intensity". The maximum available power from an antenna P_{tm} is directly proportional to the maximum effective area A_{em}. In equation form, it can be written as

$$P_{tm} = A_{em} W_i \tag{1.9}$$

where W_i is the power density of the incident wave.

In [9], it was shown that the maximum effective area of a receiving antenna can be determined by

$$A_{em} = e_{cd}(1-|\Gamma|^2)\left(\frac{\lambda}{4\pi}\right)^2 D_0 \left|\hat{\rho}_w \cdot \hat{\rho}_a\right|^2 \tag{1.10}$$

where λ is the wavelength of the RF source, e_{cd} is the radiation efficiency, $\left(1-|\Gamma|^2\right)$ and $\left|\hat{\rho}_w \cdot \hat{\rho}_a\right|^2$ account for the losses due to impedance and polarization mismatches, respectively, D_0 is the maximum directivity, which is determined by the radiation pattern of the antenna.

It is clear from (1.10) that five factors, *i.e.*, operating frequency, radiation efficiency, impedance matching, directivity, and polarization matching, affect the maximum effective area. In order to maximize the available power from the antenna under a given condition, we must take all these five factors into consideration in the analysis and design of the energy-harvesting antennas. In addition, the antenna must fit in and be compatible with the unique environment provided by a CMOS fabrication process.

In summary, an ideal antenna on CMOS ICs for energy harvesting applications should have the following characteristics:

1. Be small enough to fit on a silicon die of a given area
2. Be compatible with the fabrication of CMOS circuitry on the same silicon substrate
3. Be capable of delivering enough power to the functional circuitry
4. Have an omnidirectional or hemispherical radiation pattern
5. Have a polarization pattern that is matched to that of the source
6. Have output impedance that is matched to that of the load under various conditions

1.3 Previous Works

The subject studied in this research is closely related to the structure called rectenna in the RF and microwave literature. Its early development and applications of before the 1980's is well documented in William C. Brown's review paper [1]. A rectenna is usually composed of a

simple dipole antenna connected to a discrete rectifying diode, with a low pass network in between to ensure the matching. When a large number of such rectennas are put together, they are capable of delivering DC power as high as several hundred watts. The frequencies of the RF sources are usually in the range of 3GHz to 40GHz. The recent interest in such structures is in their potential use for power transmission by microwave beams in space applications [2].

There have been very few reports on building rectennas on monolithic integrated circuits. No systematic study has been conducted in this field prior to this current work. Among the scarce reference sources available, the following are most closely related.

Strohm, *etc*. reported the successful implementation of rectennas on high-resistivity silicon wafers in [10], but the rectennas were used as sensors for the detection of millimeter wave signals at the frequency of 63GHz. In [11], integrated dipole antennas on silicon substrates were demonstrated for intra-chip communication, but the distance between the transmitting and receiving antennas is less than 5cm since they are both on a silicon die of 5.3cm×4.1cm. And again, the antennas are used for transmitting and receiving signals, instead of power.

A contactless smart card IC with integrated antenna was shown in [12]. It uses an on-chip magnetic coil and operates at the frequency of 13.65MHz. The chip needs to be put at a distance of less than 2mm from a strong magnetic source in order to get enough power and communicate effectively with the reader. Obviously, the magnetic coil is a near field antenna and works differently from the far field antennas studied in this research.

1.4 Organization of the Dissertation

This dissertation provides a complete review of the environment, the challenges, and the methods for analyzing, designing, measuring, and optimizing antennas on CMOS ICs. Its content

is centered about the methods for determining the key antenna parameters theoretically and experimentally, *i.e.*, through simulation and measurement, and ways of improving them.

Specifically, antenna design environment provided and the challenges imposed by the CMOS technology is first outlined in chapter 2, which is followed by a chapter on the analyses of the antennas on CMOS ICs. In chapter 4, the design considerations and procedures for the on-chip antennas are presented. Various ways for improving their performance are covered in chapter 5. Chapter 6 is a discussion over the methods for measuring the antennas on CMOS ICs. The experimental results are put into chapter 7. Finally, we summarize all the work and draw some conclusions in chapter 8 and chapter 9, respectively.

2.0 ANTEANNAS ON CMOS IC's: ENVIRONMENT AND CHALLENGES

CMOS processes are primarily engineered for the fabrication of integrated digital circuits on silicon substrates. Its low cost and amenability to device scaling have made it the dominant technology in today's commercial IC market. While other technologies, like GaAs and silicon bipolar, are still preferred in applications that require high gain and/or high operation frequencies, the lag in performance of CMOS technology is quickly shrinking with the emergence of new technologies like SiGe.

In the past two decades, CMOS technology has rapidly embraced the field of analog integrated circuits [13] and there has been a surge of interest in integrating passive components, such as inductors and capacitors, on CMOS ICs [14]. These continuing efforts have enabled the concept of system on chip (SoC), where all the components necessary for a complex mixed-signal system, no matter whether digital or analog, active or passive, are integrated onto a single silicon die.

The antenna might be the last component that will be integrated on the CMOS ICs. That's mainly because antenna is one of the few components the size of which is hostile to reduction and the conductive nature of the silicon substrates used in CMOS ICs is extremely detrimental to the antenna.

In this chapter, we will first take a quick look at the CMOS fabrication process, and then introduce the spiral antenna structure, which has been extensively studied in this research. Finally, we will go over the details of the challenges we face when we try to build antennas on CMOS ICs.

2.1 The CMOS Fabrication Process

A CMOS IC fabrication process usually starts with moderately to heavily doped silicon wafers. Using processing steps such as ion implantation, chemical vapor deposition (CVD), sputtering, optical lithography, and reactive ion etching (RIE), various materials are doped, deposited, and etched to form the active devices and the passive network of connections [15].

As an example, we show the cross-section and layer map of a two poly, double metal layer CMOS process (AMI_ABN process) in Figure 2.1.

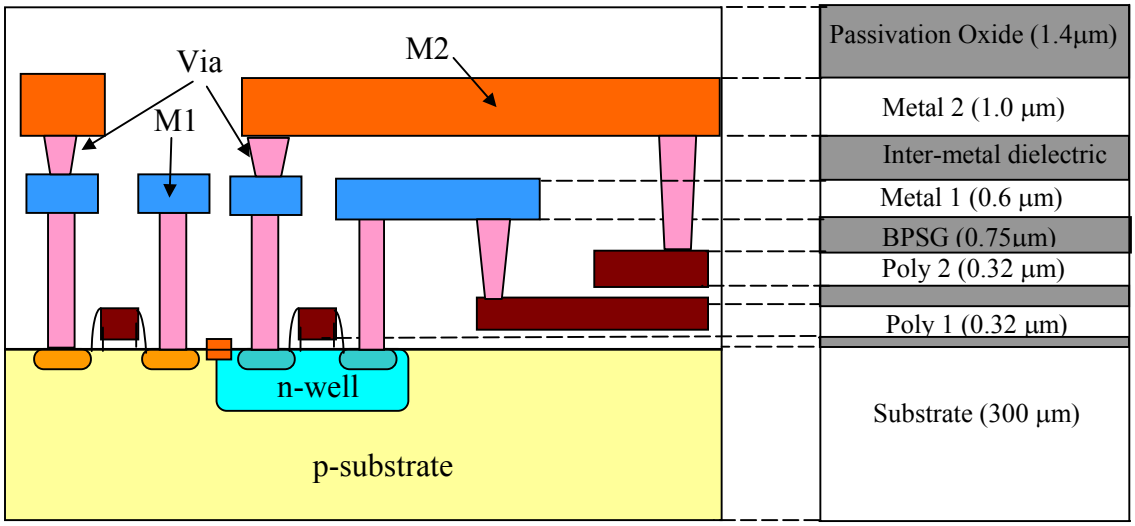


Figure 2.1 Cross-section and layer map of a two-poly, double metal layer CMOS process

As we can see from the figure, inside a CMOS IC, different materials form a layered structure on top of the silicon wafer, with vias made through the layers to construct the necessary connections. In this specific process, the sources and the drains of *n*-channel MOSFETs are constructed directly on the *p*-substrate while those for *p*-channel MOSFETs are built on previously implanted *n*-wells. The gates of the MOSFETs are usually made with poly-silicon

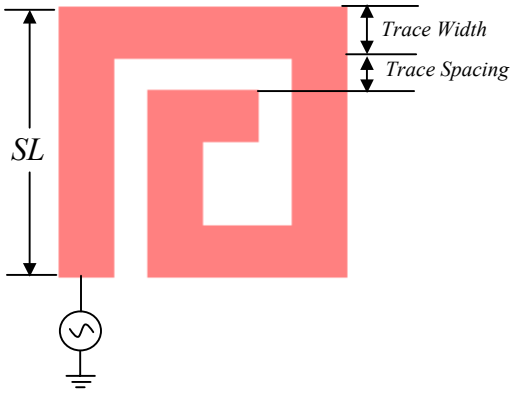
layers. After the MOSFETs are fabricated, the whole wafer is covered by certain dielectric material so that its surface is level and smooth. Contact holes are then made through it to connect the gates, sources, and drains of the MOSFETS to the first metal layer (M1), which is subsequently deposited on the top. The metal layer is patterned with photolithography to form the desired connections among MOSFETS. After the whole wafer is covered by another dielectric layer, a second metal layer (M2) is deposited on the top, which is also patterned and connected to the layer underneath using vias. For some modern processes, up to 8 metal layers can be made following the same procedure. The whole silicon wafer is usually covered by passivation oxide to prevent contamination before it is diced and the individual dies are packaged.

2.2 Spiral Antennas on CMOS ICs

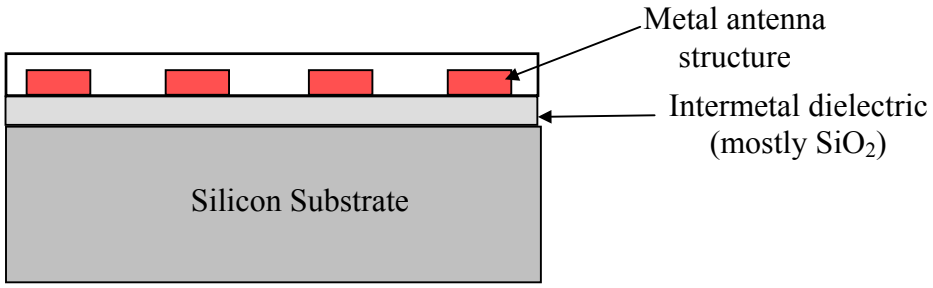
Although there exists a very rich literature of antenna shapes and structures [8], the planar nature of the CMOS chip structure reduces the choices for the antenna type to a fairly small set. A full discussion on the possible antenna structures is given in section 4.1.

Most of the analyses and experiments in this dissertation were done with the rectangular spiral antennas[1]. Its typical structure is shown in Figure 2.2. As we can see, the spiral is made of metallic rectangles connected to each other with the outside terminal connected to the source and the inner terminal open ended. It can be built with any available metal layer in a CMOS process. The reasons for choosing the spiral antennas as the subject of this study, the pros and cons associated with such a choice, and the detailed ground and feeding structure are all addressed in section 0.

[1] For the sake of conciseness, the rectangular spiral antennas will be addressed as spiral antennas in the following discussion. Therefore, the term spiral antenna implies rectangular spiral antenna, unless noted otherwise.



(a) Top view



(b) Cross sectional view

Figure 2.2 A spiral antenna with 1.5 turns

The sample spiral antenna shown in Figure 2.2 is assumed to be built on a silicon wafer with the thickness of 300μm. The dielectric (SiO2) layer thickness is 10μm. The aluminum layer used for building the spiral structure is 2μm thick. The square spiral has 1.5 turns. Its side length (*SL*) is 13mm. The metal trace width is 2.5mm while the metal trace spacing is 1.5mm. In the following sections, we will refer to this antenna as the sample antenna and it is the subject of various analyses.

2.3 Challenges for Building Antennas on CMOS ICs

There are at least two serious obstacles to the implementation of reasonably good antennas on CMOS chips. The first and foremost one is the stringent restriction on the physical size of the antenna, the other is the existence of significant losses in both the silicon substrates and the metal structure.

2.3.1 Size Matters

The economical reason for restricting the physical sizes of the antennas on CMOS chips is obvious since it is well known that the silicon die area is expensive. The gain of integrating the antenna on the chip will vanish if the chip with the antenna turns out to be too large. Unfortunately, as has been pointed out in [16], "antenna is one of the few components the size of which is related to the operating frequency." If the operating frequency of the system is fixed, size reduction of antennas can only be achieved with penalty factors.

There are quite a few good papers on the fundamental relationship between antenna sizes and their performances [17][18][19][20]. For the sake of completeness, a brief review of the

papers will be presented first. A discussion over their applications to the case of on-chip antennas then follows.

In Chu's classical paper [17], the entire antenna structure is assumed to be completely enclosed within a sphere of *2r* as shown in Figure 2.3. Here, an antenna structure includes not only the antenna itself, but also the transmission line for connecting the antenna and the oscillator (source). The antenna is considered small when *kr* is much smaller than 1, where $k=2\pi/\lambda_0$, is the phase constant. λ_0 is the wavelength at a given frequency in the free-space.

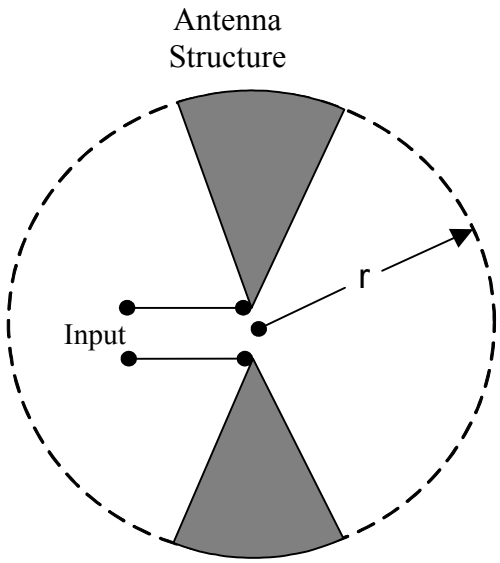


Figure 2.3 Biconical antenna within a sphere

According to [17], any radiating field can be written as a sum of spherical modes, all of which contribute to the reactive power, but only the propagating modes in the sphere add to the real radiated power. The quality factor of the n^{th} mode, Q_n, can be found from the ratio of the stored (reactive) to the radiated power. When *N* modes are supported, *i.e.*, propagating, the overall *Q* of the antenna is

$$Q = \frac{\sum_{n=1}^{N} \frac{a_n a_n^* Q_n}{(2n+1)}}{\sum_{n=1}^{N} \frac{a_n a_n^*}{(2n+1)}} \tag{2.1}$$

where a_n is the excitation coefficient of the n^{th} mode.

Higher order modes within a sphere of radius r become evanescent (below cutoff and not propagating) when $kr<<1$. They contribute very little to the radiated power. Therefore the Q of the system reduces to that of the lowest order mode supported by the small antenna. If it happens to be a TM mode, the Q of the system is then equal to

$$Q = \frac{1 + 2(kr)^2}{(kr)^3[1 + (kr)^2]} \tag{2.2}$$

A similar equation can be obtained for TE mode and the values of Q are halved when two modes, one TE and the other TM, are excited.

In Chu's original derivation of equation 2.2, it was shown that this result does not depend on the geometric configuration of the antenna. The shape of radiating element only determines whether TE, TM, or TE and TM modes are excited. Also, because the most favorable configuration was assumed for the antenna structure in his derivation, (2.2) presents a limit for the lowest Q that is achievable. The Q's of real world antennas can be very close to this limit, but will never reach it.

As we can see from (2.2), the Q of a small antenna varies inversely proportional to the cubic of its sphere r. It becomes higher and higher as the overall size of an antenna r becomes increasingly small compared to the phase constant k. Since the fractional bandwidth (FBW) of the antenna is related to the Q of the system by [20]

$$FBW = \frac{\Delta f}{f_0} = \frac{1}{Q} \tag{2.3}$$

When Q is much greater than 1, larger Q means narrower operational bandwidth. For example, the minimum Q for an antenna with r=2.2mm is roughly equal to 1.3×10^4 at 915MHz, which means a FBW of less than 0.1MHz. Such a small bandwidth makes it almost impossible to match the impedance of the antenna to that of the source.

On the other hand, the above results were obtained without considering antenna losses and thus are valid only for ideal (lossless) antennas. The Q of a real life antenna will be different from what's shown in (2.2) if the losses are taken into account.

According to the definition of quality factor,

$$Q = \frac{\omega \times \text{peak enery stored}}{\text{average power radiated} + \text{average power dissipated}} \tag{2.4}$$

it seems that increasing the dissipated power (antenna loss) will result in a smaller Q and hence wider bandwidth at first glance. Unfortunately, this reduction in Q is achieved at the cost of lower antenna efficiency because the efficiency of an antenna η is defined as

$$\eta = \frac{\text{Power radiated}}{\text{Power radiated} + \text{power dissipated}} \tag{2.5}$$

any increase in dissipated power inevitably brings down the efficiency of the antenna. For example, if we want to bring Q of the above said antenna to 100 and thus achieve a FBW of around 10MHz, the efficiency of the antenna will drop from 100% to less than 1%.

From the above discussion, we can see that there exists an awkward tradeoff between the above-formulated bandwidth and the radiation efficiency when the size of an antenna is much smaller than a wavelength. The antenna either has extremely narrow bandwidth or can become intolerably inefficient when it is too small compared to the wavelength at the operational frequency. And more often than not, we will see the latter result simply because the radiation powered drops roughly inversely proportional to r^3 while the loss terms drop roughly

proportional to r^2. The dissipated power eventually becomes dominant when the antenna size becomes smaller and smaller. This is particularly true and worrisome for antennas on CMOS chips because of the existence of excessive losses, as we will see in the following section.

Figure 2.4 shows the change in radiation efficiency as the size of the sample antenna is scaled up and down at 915MHz. As we can see from the figure, the efficiency of the sample antenna drops quickly as its size shrinks. The plot is based on the simulation results from Ansoft HFSS [21], an electromagnetic solver that is described in details in section 3.2.3.

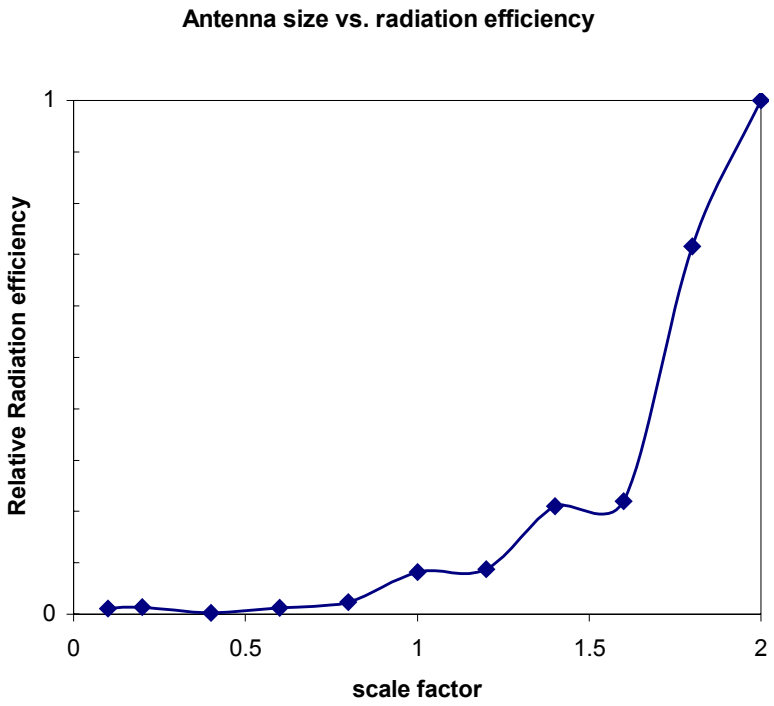


Figure 2.4 Relationship between antenna size and radiation efficiency

2.3.2 Losses of Antennas on CMOS ICs

Antenna losses can be roughly divided into two categories: the dielectric loss and the conduction loss. The losses in conventional antennas are usually quite small and account for only a few percent losses in radiation efficiency [22]. This is due to the fact that most conventional antennas are built on insulating dielectric materials and the metal structures are often made of very good conductors. For antennas built on CMOS technology, however, both dielectric and conductor losses exist and present a severe problem.

2.3.2.1 Substrate Induced Losses The most significant difference between the silicon substrates used for CMOS IC fabrications and the typical dielectric materials used for conventional antennas is their resistivity. The resistivity of the silicon substrates used for CMOS chips varies with its doping level, but is usually very low. It ranges from 10k Ω-cm for lightly doped Si (1013 atoms/cm3) to 10-3 Ω-cm for heavily doped Si (1020 atoms/cm3). It is easy to notice that even lightly doped silicon is fairly conductive compared to the commonly used dielectric materials for conventional antennas, such as alumina, whose resistivity is around 1019Ω-cm.

According to A. M. Niknejad [14], the substrate-related losses can be delineated into two types, depending on whether it is induced electrically or magnetically. As shown in Figure 2.5, electrically induced currents flow vertically or laterally, but perpendicular to the spiral segments. Magnetically induced eddy currents flow parallel to the device segments.

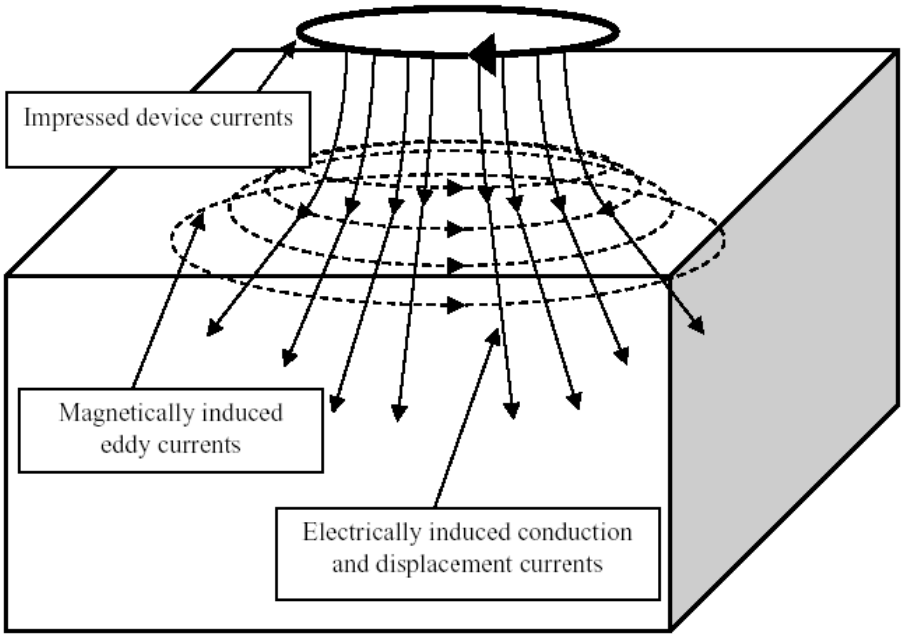


Figure 2.5 Schematic representation of substrate currents (After Niknejad [14])

Figure 2.6 shows the change in efficiency for the sample antenna described in section 2.2, as the resistivity of the substrate varies from 500 Ω·cm to 10k Ω·cm. The figure is based on the simulation results at the frequency of 915MHz obtained with Ansoft HFSS. In the simulation, the metal structure was assumed to be made of perfect conductor, so the effects of the conduction loss have been excluded from this analysis.

As we can see from the figure, the efficiency of the antenna changes significantly as the substrate resistivity varies slightly. We should remember that even the lowest resistivity simulated and shown in the figure (500Ω·cm) is extraordinarily high for a silicon substrate used for CMOS IC fabrication. Therefore, the resistivity range shown in the figure represents the very high end of what to be expected from standard CMOS processes. So the use of high-resistivity substrate is a must, not just a better option, for building an antenna with acceptable efficiency. However, the preparation of high resistivity silicon wafers requires extra processing steps, such as purification using the float zone method. Consequently, they are more expensive than the normal silicon wafers. There are also concerns for building active devices on high resistivity silicon substrates [10], but it has been shown to be viable if certain precautions are taken [23].

As a matter of fact, substrate induced losses have been the major obstacle to the integration of passive components, such as inductors, on CMOS chips. To reduce its negative impact on inductor quality factor, some researchers even suggested removing the silicon substrate underneath the device using micromachining techniques [24] [25].

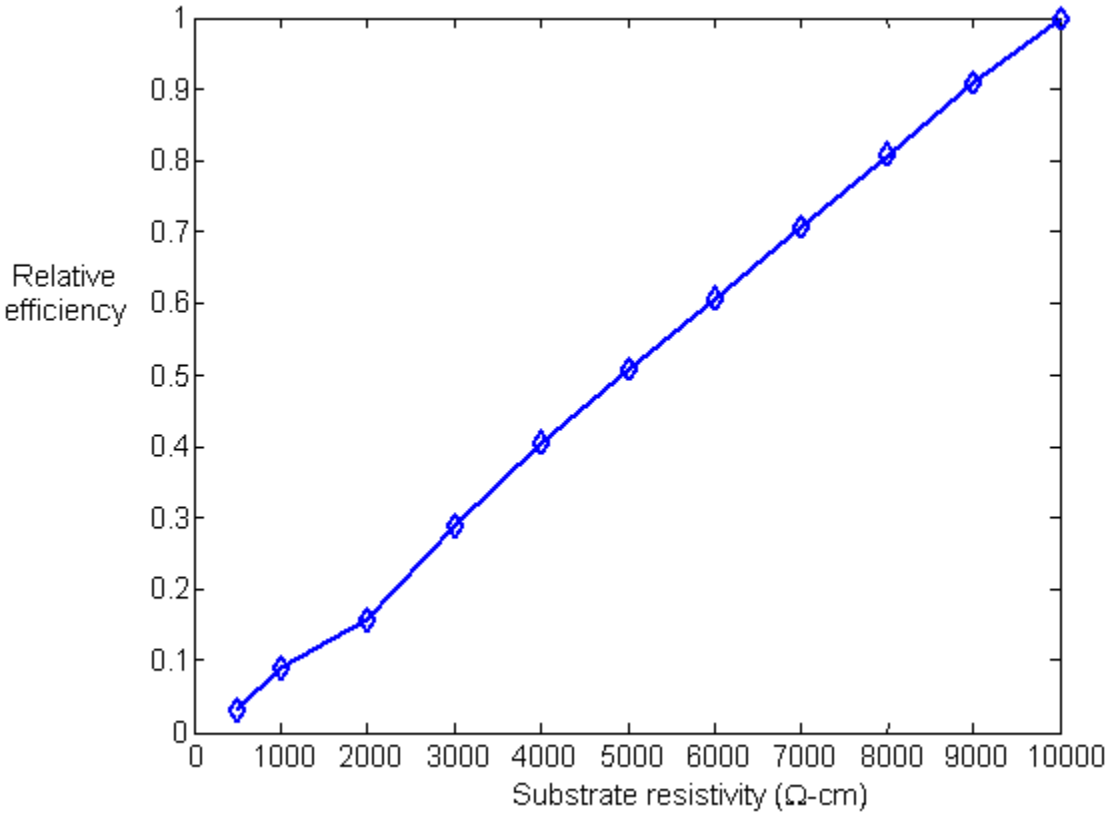


Figure 2.6 Substrate resistivity and antenna efficiency

2.3.2.2 Conductor Losses. Conductor losses occur in the form of heating in the volume of the conductors due to their finite conductivity. For a spiral antenna, conductor losses are of great concern because the metal traces are fairly narrow and thin. With the trace width being ten or twenty micrometers and total trace length close to $\lambda_0/4$ at 915MHz, the DC resistance of the spiral can easily reach tens of Ohms, which is extremely rare in typical antennas.

As the operating frequency increases, conductor losses increase due to the eddy currents [27]. This phenomenon is called skin effect when the eddy current is induced by the current flow inside the conductor itself and proximity effect when caused by nearby conductor carrying time-varying currents. The total current distribution in a conductor is a superposition of the original current flow in the conductor with the eddy currents caused by the skin and the proximity effects. The result is a reduction in the net current flow, which can be interpreted as an increase in the AC resistance.

Severity of the skin effect can be measured by the ratio of conductor thickness to a parameter called skin depth [28], which is defined as

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2.6}$$

where ρ and μ is the conductivity and permeability of the conductor respectively, f is the frequency of the current. Skin effect is usually thought to be negligible when the ratio of conductor thickness to skin depth is greater than one. At 915MHz, δ= 2.8μm for aluminum, which is more than twice the thickness of metal layers used in typical CMOS processes. So skin effect is pronounced at this frequency.

Eddy currents caused by the proximity effect are hard to determine analytically [28], but it is possible to show its significance using an electromagnetic solver with the method proposed

by C. P. Yue, etc. in [27]. It was shown that the proximity effect is negligible when the metal trace spacing is greater than 1μm at 1GHz.

Figure 2.7 shows the relationship between the antenna efficiency and the conductivity of the metal layer for the sample antenna based on the simulation results at 915MHz. The same simulator has been used as in the previous case. In the simulation, the metal layer is assumed to be thicker than the skin depth and the silicon substrate was assumed to be lossless.

It is easy to notice that the conductivity of the metal structure has a substantial effect on the efficiency of this particular antenna. This effect is expected to be more significant when the side length of the antenna shrinks and the metal traces become even narrower. Therefore, better conductors should be used whenever possible.

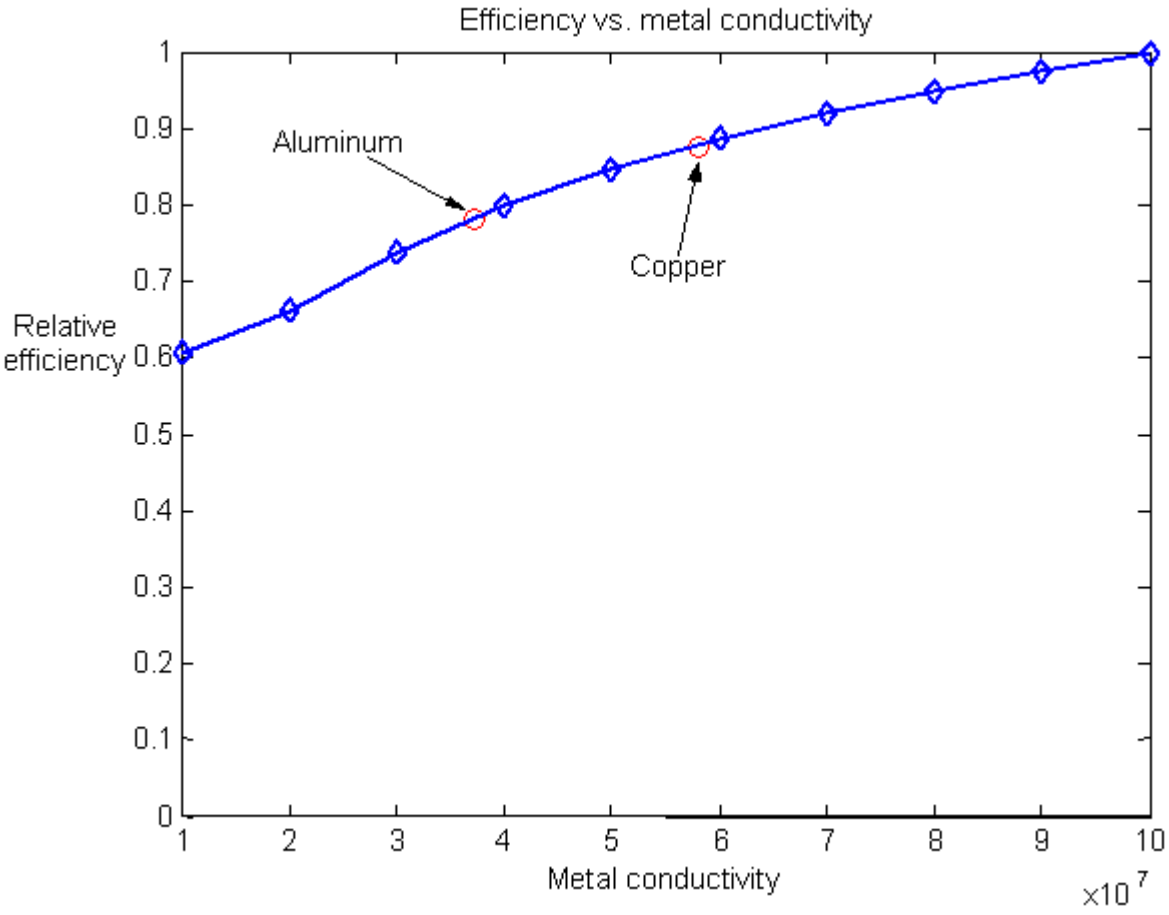


Figure 2.7 Metal conductivity and antenna efficiency

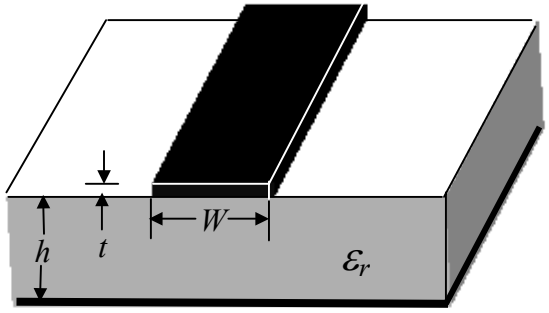
2.3.3 Other Effects of a Conductive Substrate

As we have seen in the previous section, the low resistivity of the silicon substrates used for CMOS IC fabrication brings about excessive losses, and thus low efficiency, to the antennas built on them. But that is not the only harmful effect that a conductive substrate may have. Other antenna parameters, such as input impedance and directivity, can also be adversely affected.

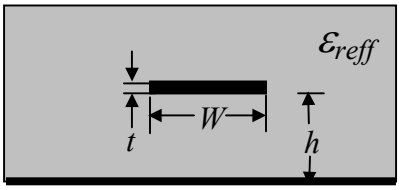
An antenna built on a silicon substrate can be considered as microstrip lines over a Si-SiO_2 system. According to [26], waves traveling along the silicon substrate can propage in three modes, depending on the doping level of the substrate. For a lightly doped substrate, the wave propagation behaves like a "quasi-TEM" mode. As the substrate is made heavily conductive, the wave is constrained to the oxide and the substrate acts like a lossy ground plane. This is the so-called "skin effect" mode of propagation. When the conductivity of the substrate is somewhere in the middle, the effective speed of propagation is orders of magnitude slower than propagation in free space, and this is the so-called "slow-wave" mode of propagation.

The dependence of wave propagation speed (mode) on the doping level of the substrate makes it difficult, or even impossible, to use the concept of effective permittivity, which is a convenient and widely used way to account for the fringing effects and the nonhmogeniety of dielectrics in the substrate. H. A. Wheeler introduced this term in 1965 [29], which is defined as the permittivity of a uniform dielectric material so that the transmission line of Figure 2.8(a) has identical electrical characteristics, particularly propagation constant, as the actual transmission line immersed in this uniform dielectric as shown in Figure 2.8(b). When the materials on both sides of the conductor are simple dielectric, i.e., non-conductive, the effective permittivity ε_{eff} depends on the permittivity of the dielectrics on both sides. It is also a function of the operating

frequency and tends to approach the permittivity of the substrate as the frequency increases [9]. Because the propagation constant does not depend solely on the permittivity of the materials around the conductor when they are semi-conductive such as silicon, the above statement may not be accurate any more.



(a) Microstrip line



(b) Effective permittivity

Figure 2.8 Illustration for the concept of effective permittivity

Since the input impedance is closely related to the way in which wave propagates from the port, it will be no surprise to see the variations in input impedance as shown in Figure 2.9. The results were obtained through simulations with Ansoft HFSS for the sample antenna shown in Figure 2.2. The numbers shown below the data markers are resistivity values of the silicon substrate in Ω-cm.

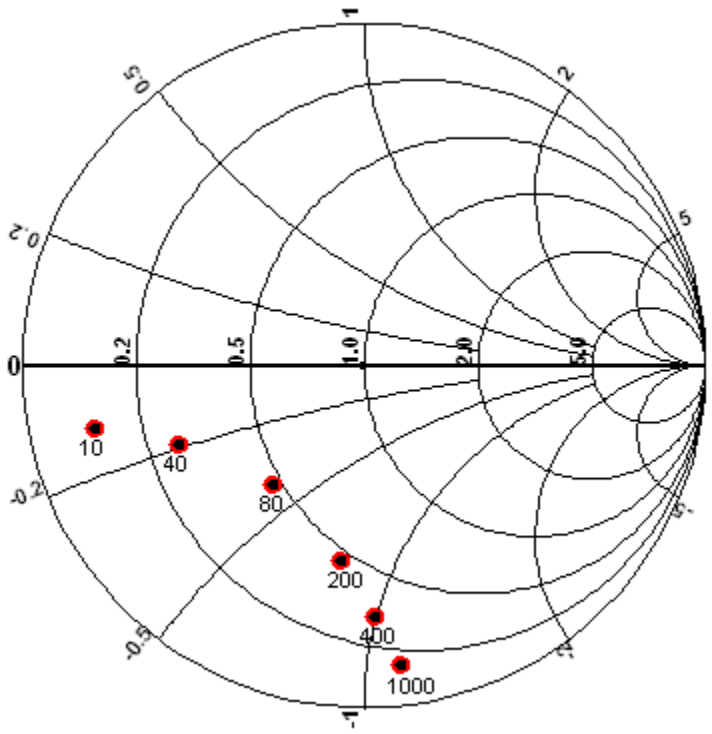


Figure 2.9 Effects of substrate restivity on input impedance of the sample antenna

Because the doping level of the silicon substrates used for CMOS IC fabrication is usually not strictly controlled, the resistivity may vary from wafer to wafer. As a result, the impedance of the antenna may also change. This will make the matching condition between the antenna and the rectifying circuit even more difficult.

3.0 ANALYSIS OF ANTENNAS ON CMOS ICs

Antenna analysis is important for at least two reasons. For one thing, it helps to reduce the time-consuming cut-and-try cycles by optimizing a particular design with parameter sweeping, which is crucial for designing antennas on CMOS chips because CMOS chip fabrication is expensive in terms of both money and time. For example, it takes up to 3 months to fabricate 5 CMOS chips with the size of 2.2mm×2.2mm at the minimum cost of $1,000 through the service of MOSIS [31]. A significant amount of time and money would be saved if the best design could be found using only analysis tools on computers. Furthermore, antenna analysis provides an understanding of the operation principles of antennas, which could be useful in the determination of limitations in the performance of an antenna, as well as in the development of new antenna designs.

Compared to other types of antennas, the analysis of spiral antennas on CMOS ICs is complicated by the presence of a non-homogeneous dielectric material behind the antenna and the complexity in the geometry of spirals. So a balance has to be reached between the complexity of the analysis method and the accuracy of the solution. Depending on how much simplification is used, antenna analyses can be put into two general categories: simplified, or reduced, analyses that maintain simplicity at the expense of accuracy and full-wave analyses that maintain rigor and accuracy at the expense of computational simplicity.

3.1 Full-wave Analysis of Antennas on CMOS ICs

Full wave analyses try to model the antenna structure by solving Maxwell's equations subject to certain boundary conditions. Most full wave analysis methods fall into two categories:

the analytical and the numerical techniques. Analytical techniques make simplifying assumptions about the geometry of a problem in order to apply a closed-form solution while numerical techniques attempt to solve fundamental field equations directly.

Separation of variables, series expansion, and conformal mapping are among the most commonly used analytical methods in solving EM-related problems [32]. Although the most satisfactory solution of a field problem is an exact mathematical one, and it is useful in checking solutions obtained from numerical methods, the complex geometric and material properties of antennas on CMOS chips defy the application of any analytical method. Therefore, an analytical solution to the spiral antenna problem was not pursued in this research.

The phenomenal increase of computational power of personal computers and the availability of vast amount of memory at increasingly cheaper prices have revolutionized the ways in which electromagnetic problems are analyzed. Computer solutions have greatly expanded the set of antenna geometries that can be accurately and efficiently modeled.

There are a variety of numerical techniques and programs available for the full-wave analysis of antennas. Ideally, a full-wave electromagnetic solver should provide a complete characterization of any structure. But in reality, each numerical technique is well suited for the analysis of a particular type of problem. The numerical technique used by a particular EM analysis program plays a significant role in determining what kinds of problems the program will be able to analyze. Therefore, it is necessary to compare the available numerical techniques and choose the most suitable one for the analysis of antennas on CMOS ICs.

3.2 Maxwell's Equations

Antenna theory, as well as its parent subject, electromagnetics, is governed by Maxwell's equations, as shown below, with certain auxiliary relations and definitions [30].

$$\nabla \cdot \vec{\mathrm{D}} = \rho \tag{3.1}$$

$$\nabla \cdot \vec{\mathrm{B}} = 0 \tag{3.2}$$

$$\nabla \times \vec{\mathrm{E}} = -\frac{\partial \vec{\mathrm{B}}}{\partial \mathrm{t}} \tag{3.3}$$

$$\nabla \times \vec{\mathrm{H}} = \vec{\mathrm{J}} + \frac{\partial \vec{\mathrm{D}}}{\partial \mathrm{t}} \tag{3.4}$$

where $\vec{D}$ is the electric displacement, $\vec{B}$ is the magnetic flux intensity, $\vec{E}$ is the electric field, $\vec{H}$ is the magnetic field, $\vec{J}$ is the electric current density, and ρ is the electric charge density.

Most time-varying electromagnetic problems involve steady-state AC fields varying sinusoidally in time. Other functions of time, such as the digital square pulses, may be considered a superposition of steady-state sinusoids of different frequency with the aid of Fourier Transformation. So it is advantageous to treat the time-varying quantities in (3.1)-(3.4) as phasors multiplied by $e^{j\omega t}$. By replacing $\partial/\partial t$ with $j\omega$, we have Maxwell's equations in phasor form as

$$\nabla \cdot \boldsymbol{D} = \rho \tag{3.5}$$

$$\nabla \cdot \boldsymbol{B} = 0 \tag{3.6}$$

$$\nabla \times \boldsymbol{E} = -j\omega \boldsymbol{B} \tag{3.7}$$

$$\nabla \times \boldsymbol{H} = \boldsymbol{J} + j\omega \boldsymbol{D} \tag{3.8}$$

After we put in the constitutive relationships $\boldsymbol{B}=\mu_r\mu_0\boldsymbol{H}$, $\boldsymbol{D}=\varepsilon_r\varepsilon_0\boldsymbol{E}$, and $\boldsymbol{J}=\sigma\boldsymbol{E}$, the Maxwell's equations in phasor forms become

$$\nabla\cdot\varepsilon_r\varepsilon_0\boldsymbol{E}=\rho \tag{3.9}$$

$$\nabla\cdot\mu_r\mu_0\boldsymbol{H}=0 \tag{3.10}$$

$$\nabla\times\boldsymbol{E}=-j\omega\mu_r\mu_0\boldsymbol{H} \tag{3.11}$$

$$\nabla\times\boldsymbol{H}=j\omega(\varepsilon_r\varepsilon_0+\frac{\sigma}{j\omega})\boldsymbol{E} \tag{3.12}$$

where μ_r is the complex relative permeability, ε_r is the complex relative permittivity, and σ is the conductivity of the media. μ_0 and ε_0 are the permeability and the permittivity of the free space, respectively.

Substituting $\boldsymbol{H}$ from (3.11) into (3.12), we have

$$\nabla\times(-\frac{1}{j\omega\mu_r\mu_0}\nabla\times\boldsymbol{E})=j\omega(\varepsilon_r\varepsilon_0+\sigma)\boldsymbol{E} \tag{3.13}$$

If we define the free space phase constant (or wave number) k_0 as

$$k_0^2=\omega^2\mu_0\varepsilon_0 \tag{3.14}$$

Equation (3.13) becomes

$$\nabla\times(\frac{1}{\mu_r}\nabla\times\boldsymbol{E})-(k_0^2\varepsilon_r-jk_0Z_0\sigma)\boldsymbol{E}=0 \tag{3.15}$$

where $Z_0=\sqrt{\frac{\mu_0}{\varepsilon_0}}$ is the characteristic impedance of free space.

As we will see later, (3.15) is the equation directly solved by some EM simulators.

It is sometimes convenient to recast Maxwell's equations of (3.1)-(3.4) in terms of the electric scalar potential Φ and magnetic vector potential function $\vec{A}$ [32].

From (3.1), it is clear that

$$\vec{B} = \nabla \times \vec{A} \tag{3.16}$$

and from (3.4) it follows that

$$\vec{E} = -\nabla\Phi - \frac{\partial \vec{A}}{\partial t} \tag{3.17}$$

After substituting (3.6) in (3.1), we have

$$-\nabla^2\Phi - \frac{\partial}{\partial t}(\nabla \cdot \vec{A}) = \frac{\rho}{\varepsilon} \tag{3.18}$$

Substituting (3.16) and (3.17) in equation (3.4), and using the vector identity

$$\nabla \times \nabla \times \vec{A} = \nabla\left(\nabla \cdot \vec{A}\right) - \nabla^2 \vec{A} \tag{3.19}$$

we get

$$\nabla\left(\nabla \times \vec{A}\right) - \nabla^2 \vec{A} = \mu\vec{J} - \mu\varepsilon\nabla\left(\frac{\partial\Phi}{\partial t}\right) - \mu\varepsilon\frac{\partial^2 \vec{A}}{\partial t^2} \tag{3.20}$$

When we invoke the Lorentz gauge, *i.e.*

$$\nabla \cdot \vec{A} = -\mu\varepsilon\frac{\partial\Phi}{\partial t} \tag{3.21}$$

Equations (3.18) and (3.20) then simplify to

$$\nabla^2\Phi - \mu\varepsilon\frac{\partial^2\Phi}{\partial t^2} = -\frac{\rho}{\varepsilon} \tag{3.22}$$

$$\nabla^2 \vec{A} - \mu\varepsilon\frac{\partial^2 \vec{A}}{\partial t^2} = -\mu\vec{J} \tag{3.23}$$

In the time period case, they become

$$\nabla^2\Phi + \omega^2\mu\varepsilon\Phi = -\frac{\rho}{\varepsilon} \tag{3.24}$$

$$\nabla^2 \vec{A} + \omega^2 \mu\varepsilon\vec{A} = -\mu\vec{J} \tag{3.25}$$

Using the relationship defined by equations (3.16) and (3.17), the electric and magnetic fields can be easily derived once the potentials $\vec{A}$ and Φ are solved for equations (3.24) and (3.25).

3.2.1 Method of Moments

The method of moments (or moment methods, MoM) is a technique for solving integral equations (IE's) by reducing them to a system of simpler linear equations. It uses a technique known as the method of weighted residue, which works by minimizing the difference (residue) between a certain trial function and the true solution.

In order to use the MoM to solve partial differential equations (PDE's) such as the Maxwell equations, it is necessary to derive the equivalent integral equations of the PDE's in the first place. This is usually achieved by constructing an auxiliary function known as the Green's function for that problem. The Green's function is the kernel function obtained from a linear boundary value problem and forms the essential link between the differential and integral formulations. Green's function is not available for all the problems with arbitrary boundary conditions. In order to derive the proper Green's functions, certain conditions must be met.

Most MoM programs solve equation (3.24) directly and calculate other quantities from its solution. Under the assumption that the dielectric layers and the ground plane extend infinitely, the integral equation corresponding to (3.24) can be obtained as

$$\Phi = \int -\frac{\rho}{\varepsilon} G(\vec{r}, \vec{r}\,')dv' \tag{3.26}$$

where $G(\vec{r},\vec{r}')$ is the proper Green's function, $\vec{r}$ and $\vec{r}'$ are the coordinates of source and field points, respectively.

Ansoft Ensemble [33] is the software package available for this research that uses the MoM to solve general EM problems. The basic quantities that it calculates are the surface currents. The far field radiation is calculated from the currents using the integral equation. The S-parameters at the input port are also derived from the current values, as well as the input impedance at the port. Like the other two methods we will discuss later, the MoM involves some form of discretization (meshing). But unlike the other two methods, only the surfaces of the conductors are discretized in the MoM. So the shapes used in meshing are usually two-dimensional, instead of being three-dimensional as in the other two methods. Figure 3.1 shows the triangle shape used in Ansoft Ensemble. For each triangle, Ensemble stores the components of the current that are normal to the three edges of the triangle. The current inside each triangle is the superposition of these edge values.

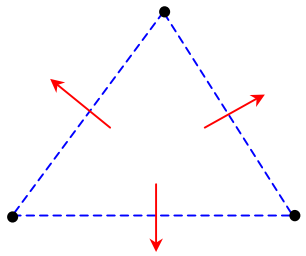


Figure 3.1 The triangular element used in Ansoft Ensemble

As an example, the meshing used and the gain pattern obtained for the sample antenna in Ansoft Ensemble are shown in Figure 3.2 and Figure 3.3 respectively.

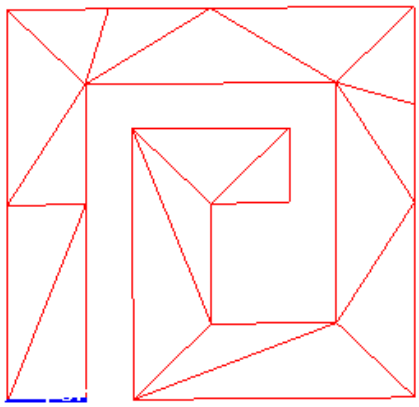


Figure 3.2 Meshing of the sample spiral antenna in Ensemble

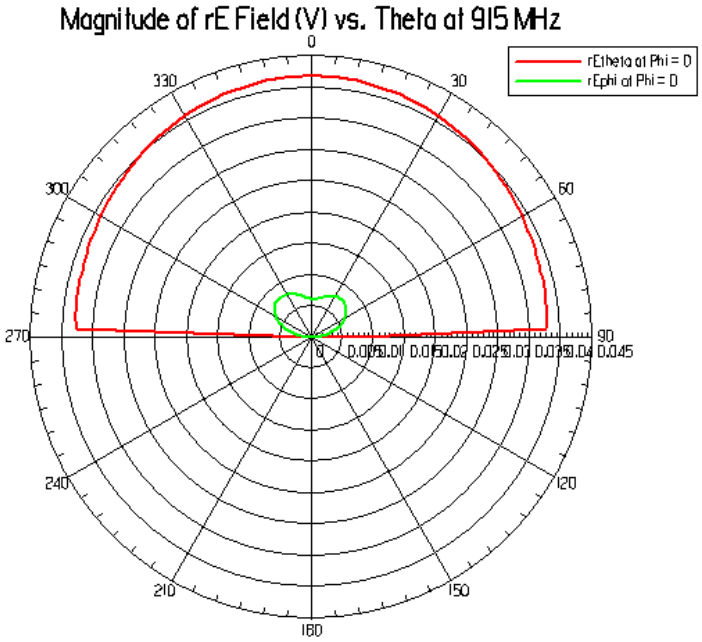


Figure 3.3 Gain pattern of the sample obtained with Ansoft Ensemble

It is easy to notice in Figure 3.3 that the simulated gain pattern shows no radiation in the lower hemisphere, which is unlikely since the spiral antenna is much smaller than a wavelength is size. This kind of discrepancy occurs because of the inherent assumption that the dielectric layer(s) and the ground plane extend infinitely under the metal layer, which are necessary for deriving the Green's function as mentioned earlier.

3.2.2 Finite Difference Techniques

Finite difference techniques have been developed in both the time domain and the frequency domain [34]. Because the Finite Difference Time Domain (FDTD) method is straightforward and by far more widely used, the other method, *i.e.*, Finite Difference Frequency Domain (FDFD), will not be discussed here. Despite its mathematical simplicity, FDTD is remarkably robust. Since its introduction by Yee in his original paper [35] in 1966, it has been used to solve a vast range of electromagnetic problems.

FDTD solves Maxwell's time dependent curl equations, *i.e.* equations (3.3) and (3.4), directly by implementing the space and time derivatives with simple central difference approximations. The region being modeled by FDTD is represented by two interleaved grids of discrete points. The electric field is evaluated on the points of one grid while the magnetic field is evaluated on points of the other grid. A basic element of the space lattice is shown in Figure 3.4, from which we can see that each magnetic field vector component is surrounded by four electric field components while each electric field vector component is surrounded by four magnetic field components.

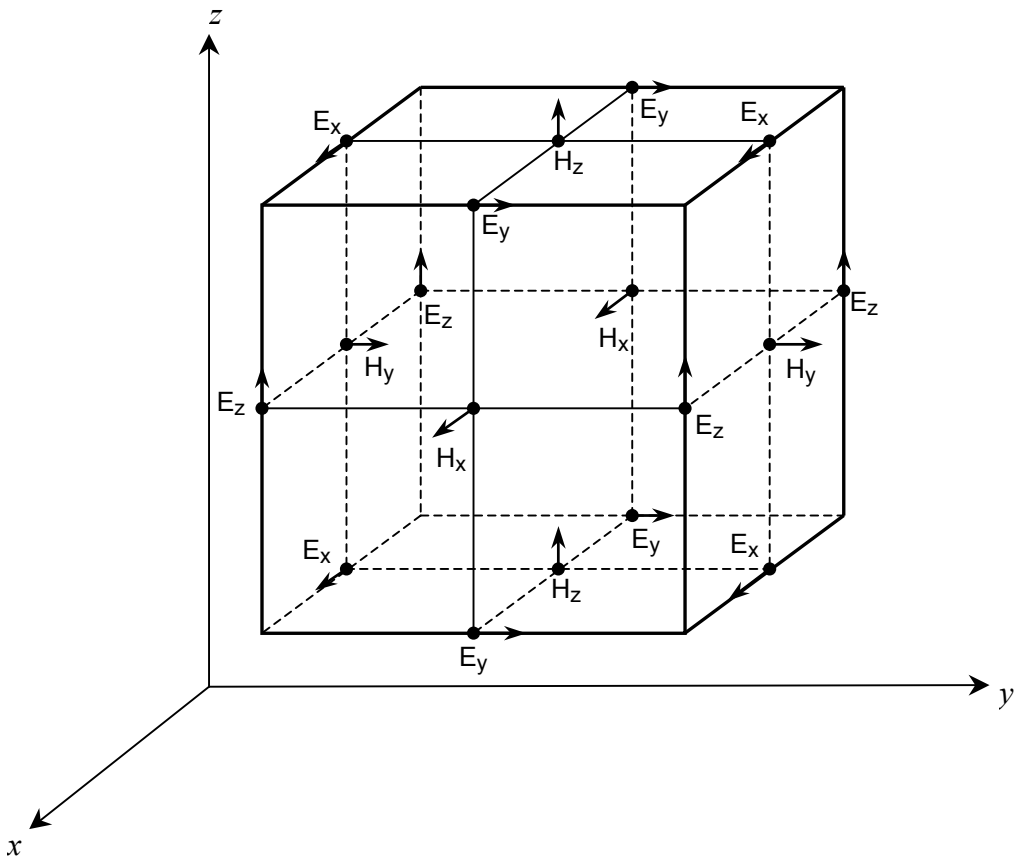


Figure 3.4 Basic element of the FDTD space lattice

Following Yee's notation, a grid point in the solution region is defined as

$$(i, j, k) = (i\Delta x, j\Delta y, k\Delta z) \tag{3.27}$$

and any function of space and time is defined as

$$F^n(i, j, k) = (i\delta, j\delta, k\delta, n\Delta t) \tag{3.28}$$

where δ=Δx=Δy=Δz is the space increment, Δt is the time increment, *i, j, k,* and *n* are integers. To ensure stability, the maximum time step should satisfy the Courant condition, which is

$$\Delta t \le \frac{1}{c\sqrt{(1/\Delta x)^2 + (1/\Delta y)^2 + (1/\Delta z)^2}} \tag{3.29}$$

It is obvious that equations (3.3) and (3.4) can be turned into six scalar equations:

$$\frac{\partial H_x}{\partial t} = \frac{1}{\mu}\left(\frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial y}\right) \tag{3.30}$$

$$\frac{\partial H_y}{\partial t} = \frac{1}{\mu}\left(\frac{\partial E_z}{\partial x} - \frac{\partial E_x}{\partial z}\right) \tag{3.31}$$

$$\frac{\partial H_z}{\partial t} = \frac{1}{\mu}\left(\frac{\partial E_x}{\partial y} - \frac{\partial E_y}{\partial x}\right) \tag{3.32}$$

$$\frac{\partial E_x}{\partial t} = \frac{1}{\varepsilon}\left(\frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} - \sigma E_x\right) \tag{3.33}$$

$$\frac{\partial E_y}{\partial t} = \frac{1}{\varepsilon}\left(\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} - \sigma E_y\right) \tag{3.34}$$

$$\frac{\partial E_z}{\partial t} = \frac{1}{\varepsilon}\left(\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} - \sigma E_z\right) \tag{3.35}$$

Using the finite difference approximations for space and time derivatives of second-order accuracy, we have

$$\frac{\partial F^n(i,j,k)}{\partial x} = \frac{F^n(i+\frac{1}{2},j,k) - F^n(i-\frac{1}{2},j,k)}{\delta} + O(\delta^2) \tag{3.36}$$

$$\frac{\partial F^n(i,j,k)}{\partial t} = \frac{F^{n+\frac{1}{2}}(i,j,k) - F^{n-\frac{1}{2}}(i,j,k)}{\Delta t} + O(\Delta t^2) \tag{3.37}$$

With the positioning of components shown in Figure 3.4, equations (3.3) and (3.4) can then be approximated by

$$\begin{aligned} H_x^{n+\frac{1}{2}}\left(i, j+\frac{1}{2}, k+\frac{1}{2}\right) = H_x^{n-\frac{1}{2}}\left(i, j+\frac{1}{2}, k+\frac{1}{2}\right) + \frac{\delta t}{\mu\left(i, j+\frac{1}{2}, k+\frac{1}{2}\right)\delta}\Bigg[E_y^n\left(i, j+\frac{1}{2}, k+1\right) \\ - E_y^n\left(i, j+\frac{1}{2}, k\right) + E_z^n\left(i, j, k+\frac{1}{2}\right) - E_z^n\left(i, j+1, k+\frac{1}{2}\right)\Bigg] \end{aligned} \tag{3.38}$$

$$\begin{aligned} H_y^{n+\frac{1}{2}}\left(i+\frac{1}{2}, j, k+\frac{1}{2}\right) = H_y^{n-\frac{1}{2}}\left(i+\frac{1}{2}, j, k+\frac{1}{2}\right) + \frac{\delta t}{\mu\left(i+\frac{1}{2}, j, k+\frac{1}{2}\right)\delta}\Bigg[E_z^n\left(i+1, j, k+\frac{1}{2}\right) \\ - E_z^n\left(i, j, k+\frac{1}{2}\right) + E_x^n\left(i+\frac{1}{2}, j, k\right) - E_x^n\left(i+\frac{1}{2}, j+1, k\right)\Bigg] \end{aligned} \tag{3.39}$$

$$\begin{aligned} H_z^{n+\frac{1}{2}}\left(i+\frac{1}{2}, j+\frac{1}{2}, k\right) = H_z^{n-\frac{1}{2}}\left(i+\frac{1}{2}, j+\frac{1}{2}, k\right) + \frac{\delta t}{\mu\left(i+\frac{1}{2}, j+\frac{1}{2}, k\right)\delta}\Bigg[E_x^n\left(i+\frac{1}{2}, j+1, k\right) \\ - E_x^n\left(i+\frac{1}{2}, j, k\right) + E_y^n\left(i, j+\frac{1}{2}, k\right) - E_y^n\left(i+1, j+\frac{1}{2}, k\right)\Bigg] \end{aligned} \tag{3.40}$$

$$\begin{aligned} E_z^{n+1}\left(i+\frac{1}{2}, j+\frac{1}{2}, k\right) = \left(1 - \frac{\sigma(i+\frac{1}{2}, j, k)\delta t}{\varepsilon(i+\frac{1}{2}, j, k)}\right) E_z^n\left(i+\frac{1}{2}, j, k\right) + \frac{\delta t}{\varepsilon\left(i+\frac{1}{2}, j, k\right)\delta}\Bigg[H_z^{n+\frac{1}{2}}\left(i+\frac{1}{2}, j+\frac{1}{2}, k\right) \\ - H_z^{n+\frac{1}{2}}\left(i+\frac{1}{2}, j-\frac{1}{2}, k\right) + H_y^{n+\frac{1}{2}}\left(i+\frac{1}{2}, j, k-\frac{1}{2}\right) - H_y^{n+\frac{1}{2}}\left(i+1, j, k+\frac{1}{2}\right)\Bigg] \end{aligned} \tag{3.41}$$

$$E_y^{n+1}\left(i,j+\frac{1}{2},k\right)=\left(1-\frac{\sigma(i,j+\frac{1}{2},k)\delta t}{\varepsilon(i,j+\frac{1}{2},k)}\right)E_y^n\left(i,j+\frac{1}{2},k\right)+\frac{\delta t}{\varepsilon\left(i,j+\frac{1}{2},k\right)\delta}\left[H_z^{n+\frac{1}{2}}\left(i,j+\frac{1}{2},k+\frac{1}{2}\right)\right.$$
$$\left.-H_x^{n+\frac{1}{2}}\left(i,j+\frac{1}{2},k-\frac{1}{2}\right)+H_z^{n+\frac{1}{2}}\left(i-\frac{1}{2},j+\frac{1}{2},k\right)-H_z^{n+\frac{1}{2}}\left(i+\frac{1}{2},j+\frac{1}{2},k\right)\right] \quad (3.42)$$

$$E_z^{n+1}\left(i,j,k+\frac{1}{2}\right)=\left(1-\frac{\sigma(i,j,k+\frac{1}{2})\delta t}{\varepsilon(i,j,k+\frac{1}{2})}\right)E_z^n\left(i,j,k+\frac{1}{2}\right)+\frac{\delta t}{\varepsilon\left(i,j,k+\frac{1}{2}\right)\delta}\left[H_y^{n+\frac{1}{2}}\left(i+\frac{1}{2},j,k+\frac{1}{2}\right)\right.$$
$$\left.-H_y^{n+\frac{1}{2}}\left(i-\frac{1}{2},j,k+\frac{1}{2}\right)+H_x^{n+\frac{1}{2}}\left(i,j-\frac{1}{2},k+\frac{1}{2}\right)-H_x^{n+\frac{1}{2}}\left(i,j+\frac{1}{2},k+\frac{1}{2}\right)\right] \quad (3.43)$$

As we can see from equations (3.38)-(3.43), the value of a given field component is written explicitly in terms of its value at previous time point and four field component values of the opposite kind around it at one half-time step before the current time point. Since all of these terms should be known by the time of current computation, once the boundary condition is given, the wave propagation from the excitation points throughout the grid can be actually simulated by alternatively calculating the electric and the magnetic fields at each time step using equations (3.38)-(3.43).

FDTD takes sampled analog signals at the excitation points as its input and the direct outputs from the solution are field strength values at the sampled space points. The excitation can take two forms: a pulsed one or a harmonic one. With a pulsed excitation, a pulse of finite width is launched into the computation region. Frequency domain results can then be obtained by applying a discrete Fourier transformation to the time domain results. With a harmonic excitation, a continuous sine wave source excites the computation region throughout a simulation. The frequency domain results are obtained directly from the time domain results

simply by observing wave magnitudes and phases since there is only one frequency for a sinusoidal signal.

The FDTD electromagnetic solver available for this research is part of a software package called APLAC [36], which was developed by the Nokia Research Center. Although the APLAC FDTD module did implement the basic calculations of FDTD and several absorbing boundary conditions (ABC's), many of the advanced features of a full-fledged electromagnetic solver, such as adaptive meshing and 3-D plotting, are not available. Even the calculations of some fundamental antenna parameters, such as directivity pattern, beam area, and antenna efficiency, were not implemented in the module itself. So it was felt that the APLAC FDTD module was a little underpowered for the simulation of the complex structures of the on-chip antennas. However, it should be meaningful to simulate one or two sample antenna configurations using this module so that the results from simulations using other software can be compared and validated. For this reason, the sample antenna shown in Figure 2.2 was simulated using this module.

The antenna was modeled using a grid of 100×100×50 cells with spatial resolutions of $\Delta x=1mm$, $\Delta y=1mm$, and $\Delta z=0.06mm$. The corresponding time step is $\Delta t=0.2ps$. The resolution along Z-axis was chosen such that five cells are occupied by the substrate height. Because the dielectric layer is much thinner than the wafer, modeling it will require a prohibitive number of steps in the Z-axis. As a consequence, it was neglected in the simulation. The metal parts are modeled as perfect electric conductors by setting the tangential electric field components to zero. Figure 3.5 shows the normalized radiated electric field (rE) components at 915MHz.

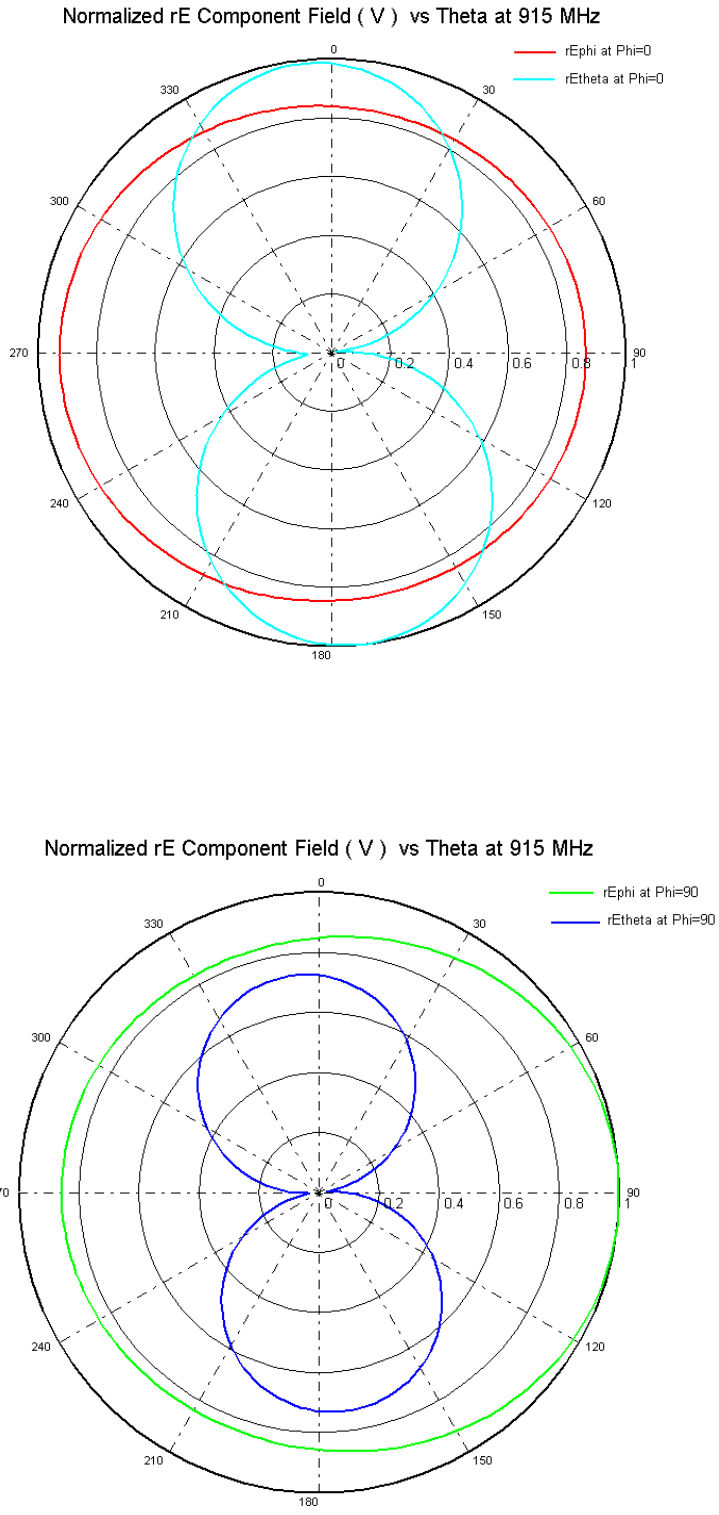


Figure 3.5 Radiation pattern of the sample antenna obtained with APLAC FDTD

3.2.3 Finite Element Method

The Finite element method works by breaking complicated shapes into small components (elements). It is widely used in civil and mechanical engineering to solve material and structural problems. Its major application in electrical engineering is to solve the complex electromagnetic problems such as the antennas.

The finite element analysis of any problem involves basically four steps [32]:

1. Discretizing the solution region into a finite number of elements
2. Deriving the governing equation for a typical element
3. Assembling of all elements in the solution region, and
4. Solving the system of equations obtained

In the first step, the solution region is divided into a number of small homogeneous pieces, or elements (hence the name finite element). The corners of the elements are called nodes. The most widely used element for the 3-D electromagnetic problems is the four-node tetrahedron, which is shown in Figure 3.6. The value of a vector field quantity (such as the H-field or E-field) at points inside each tetrahedron is interpolated from those at the vertices of the tetrahedron and/or those at the midpoint of selected edges that are tangential to a face and normal to the edge. As an example, the meshing of a spiral antenna using a tetrahedron in Ansoft HFSS is shown in Figure 3.7.

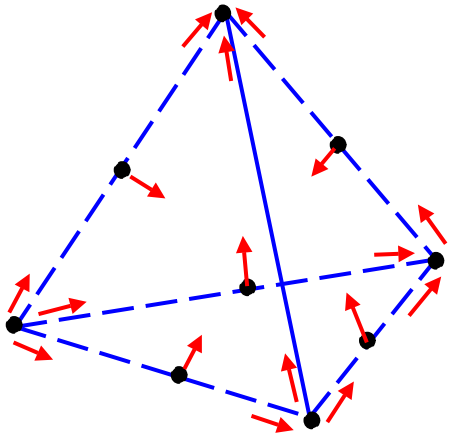


Figure 3.6 The tetrahedron element used in finite element analysis

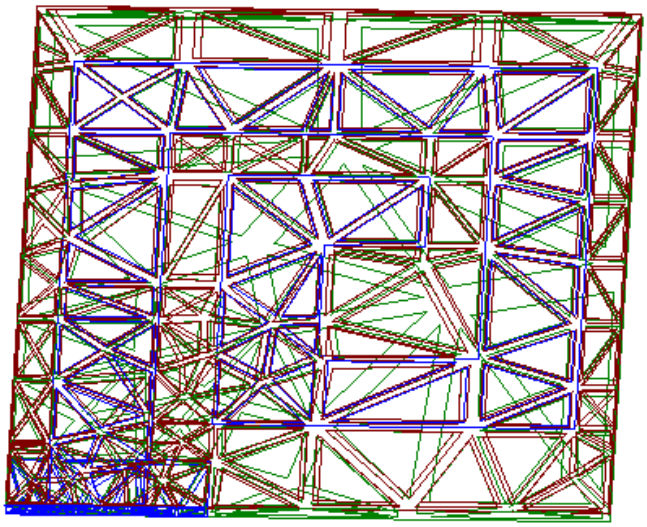


Figure 3.7 Meshing of a spiral antenna in Ansoft HFSS

The equation that is solved by most FEM simulators is (3.15). The variational technique is used to derive the governing linear simultaneous equations for one typical element from it, which works by minimizing or maximizing an expression that is known to be stationary about the true solution. In the derivation, certain approximation (interpolation as mentioned above) is involved, the order of which determines the number of unknowns of the resulting linear simultaneous equations. For a four-node tetrahedron element with the 0^{th} order approximation, a LSE with the dimension of six is obtained. With the 1^{st} order approximation, the resulting LSE has twenty unknowns.

As the third step, the linear simultaneous equations for each element are assembled into one large set of LSE's, which involves the conversion of local node numbers into global node numbers and the derivation of global coefficients from the local coefficients. The assembling process is necessary because most nodes are shared by two or more elements. The dimension of the resulting equation is approximately equal to the number of nodes, but the matrix that represents the system is generally sparse because each element only interacts with elements in its own neighborhood.

The final step in a finite element analysis is solving the large set of LSE's. This can be done through either the iteration method or the band matrix (matrix decomposition) method. The direct output from the solution is the electric field at each node. Other parameters, such as the magnetic field, the induced currents, and the power losses can be obtained from the electric field values. Unlike FDTD, where only the field components at the grid points can be found, the values of field components at any point within the solution region can be easily interpolated from the node values using the FEM.

As mentioned earlier, Ansoft HFSS was the FEM electromagnetic solver available for this work. It was felt that Ansoft HFSS is fairly versatile and powerful. Its 3-D modeler allows the creation of very complicated and intricate structures. The adaptive meshing capability relaxes the constraints on the maximum aspect ratio of the objects. Although only the basic electromagnetic field quantities are calculated in the initial FEM analysis, most of the important antenna parameters can be easily retrieved in the post-processor. Best of all, the use of macro language and the support for database make it much easier to model and compare antennas with similar structures but varied geometric or material properties.

In order to compare with the results obtained from APLAC FDTD simulations, we show the 3-D plot of total directivity pattern and 2-D plots of the radiate E-field patterns obtained with Ansoft HFSS for the sample antenna in Figure 3.8 and Figure 3.9, respectively.

As we can notice from the figure, the plots obtained with HFSS are very close to those from APLAC FDTD simulations.

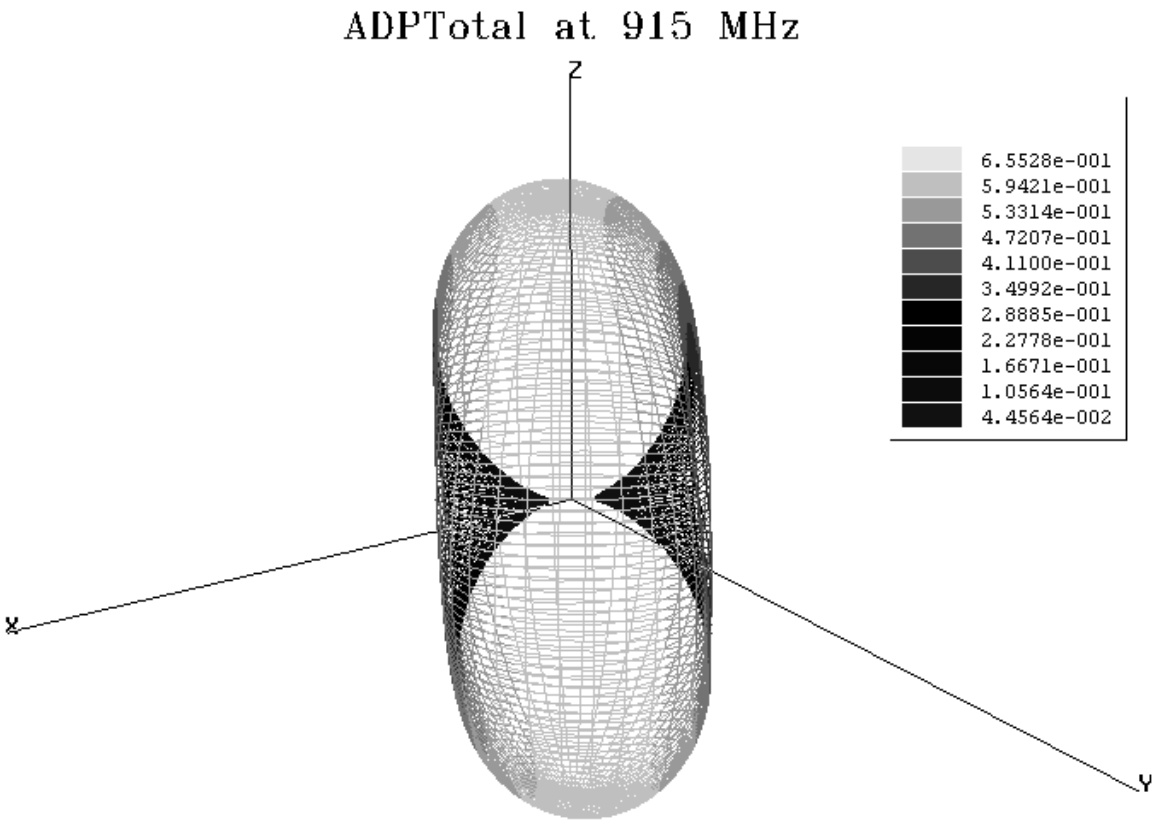


Figure 3.8 Total directivity pattern of the sample antenna from Ansoft HFSS simulation

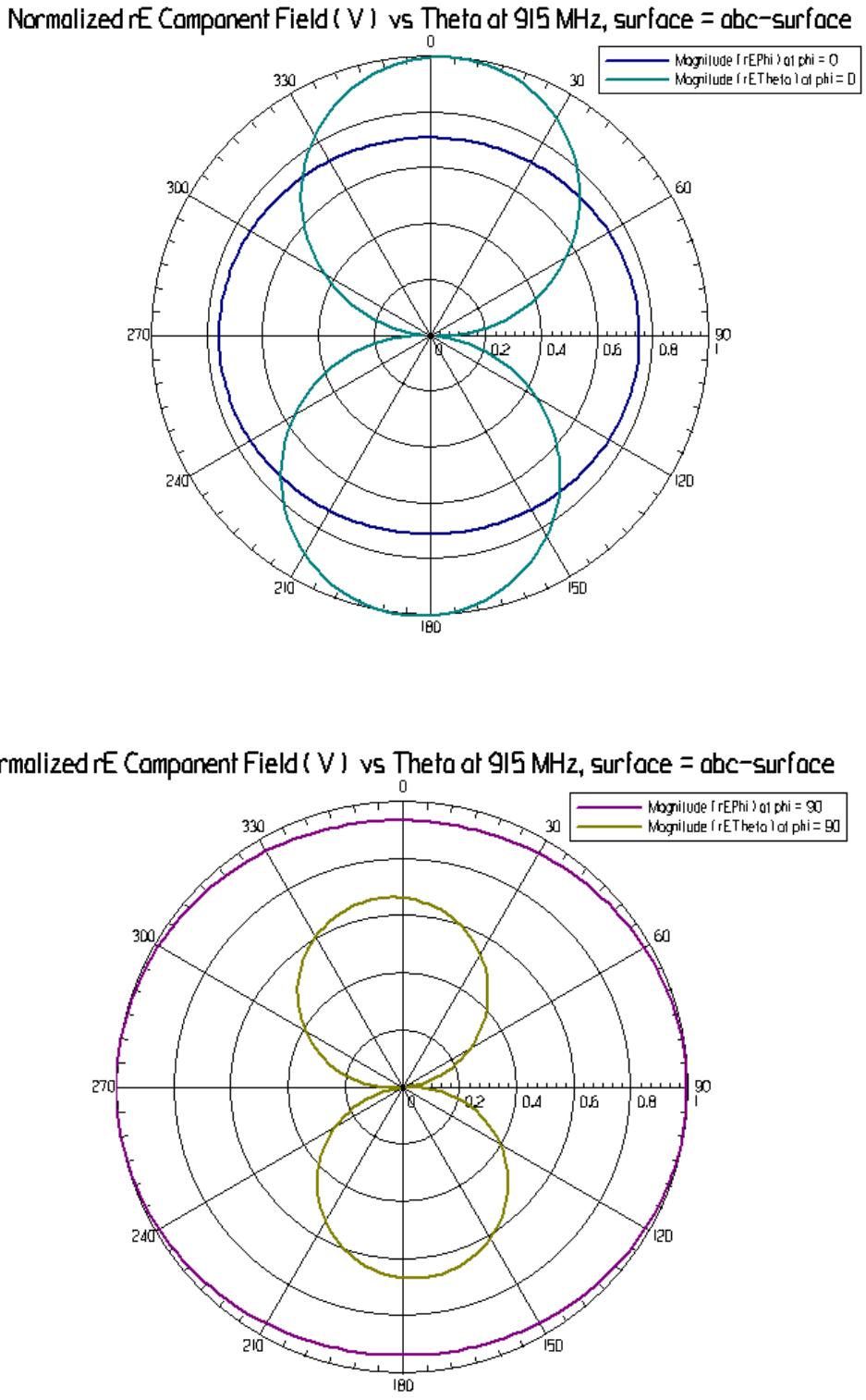


Figure 3.9 rE component field of the sample antenna obtained with Ansoft HFSS

3.2.4 A Comparison of the Three Numerical Methods

From the very brief review presented above, we can see that all the three numerical methods, i.e., MoM, FDTD, and FEM, have their own ways of attacking the same problem and possess distinct characteristics. As a result, there are pros and cons associated with each of them in their applications to the analysis of antennas on CMOS ICs.

One difficulty in applying FDTD or FEM to the antenna problem is that the region of interest is open or unbounded while the space over which finite difference scheme or meshing with finite elements can be applied is limited by the computer storage. So the solution region must be limited in some way and there will inevitably be an artificial boundary that separates the solution region and the unsolved open space. This boundary must be chosen in such a way that the solution region is big enough to enclose the radiator and can be extended to infinity without causing too much error. These artificial termination conditions are known as absorbing boundary conditions and have been the topic of considerable amounts of research efforts. They tend to become a less severe problem in modern software packages.

The MoM is more suitable for the analysis of open structure problems, such as antennas, because far field radiation can be easily calculated from the current distributions on the metal surfaces. The MoM is also computationally less involved because it only needs to solve the two-dimensional surface currents. Despite the fact that the planar structures of the CMOS ICs are amenable to the use of the MoM, the inherent assumption that the ground plane and the dielectric layers extend infinitely makes it unsuitable for the simulation of on-chip antennas studied in this research as we have seen in the simulation results for the sample antenna in section 3.2.1.

FDTD and FEM are similar in that no assumption of any form is made about the geometry of the structure being analyzed. So it is possible to model configurations that have

complicated geometries and many arbitrarily shaped dielectric regions in a relatively efficient manner. The mathematical derivation and hence the result obtained from them is a true solution to the physical model described by Maxwell's equations as long as there is enough memory and computation power available. However, even with the rapidly increasing memory and computational power available in today's computers, the need for the simulation of spiral antennas on CMOS ICs can still sometimes be unrealistic.

For FDTD, the spatial increment δ (grid spacing) must be smaller than the dimensions of the smallest features that need to be modeled and the volume of the grid must be great enough to encompass the entire object and most of the near field. Since the smallest dimension of the spiral antennas on CMOS ICs are usually in the order of several micrometers while the solution region must at least include the whole chip, which is on the order of millimeters, the number of elements can easily get into millions. However, even with only $100\times100\times50$ cells, the simulation of the sample antenna took more than five hours on a computer with a 1.4GHz processor and 512MB memory. We already mentioned that the thin dielectric layer was neglected in the simulation of the sample antenna because it would otherwise require too many steps in the Z-axis. The thickness of the metal layers is even hard to take into account since they are thinner than the dielectric layer. Although there exist some techniques for reducing the number of cells while maintaining the same level of accuracy, they are generally very difficult to realize and often unstable.

On the contrary, adaptive meshing, which means smaller elements for fine segments and bigger elements for less intricate parts, is much easier to realize in the FEM scheme. As a matter of fact, most advanced FEM programs, including Ansoft HFSS, have implemented this technique. Although it stops working when the aspect ratio of the structure exceeds a certain

level because of convergence problems, the range of geometric configurations that can be handled in FEM is already much larger than FDTD. For example, it is possible to model the thickness of the metal layers on a CMOS IC with Ansoft HFSS, which is significant because the thickness of the metal layers is less than the skin depth and thus their thickness affects the field solution.

In conclusion, Ansoft HFSS, which uses FEM, is the best program available for the full-wave simulation of antennas on CMOS ICs. It has been used extensively throughout this research to analyze various structures and effects of certain properties of the antenna.

3.3 A Lumped Circuit Model of Spiral Antennas on CMOS ICs

Unlike full-wave analysis that we discussed in the previous section, reduced analyses usually introduce one or more significant (but reasonable) approximations to simplify the problem so that design models and equations can be obtained. Although it is highly desirable to have such models for antennas on CMOS chips, the dependence of propagation constant on the doping level of the substrate makes such modeling attempts extremely difficult, if not impossible. In addition, the coupling among the segments adds to the complexity. So accurate physical models for spiral antennas on silicon substrate are not available in the antenna literature.

A lumped equivalent circuit model has been proposed and verified in this work. Although it does not lead to the much wanted antenna design equations, it does offer a rugged picture of the physical phenomena inside the antenna and the circuit can be valuable in the impedance matching between the antennas and the rectifying circuit.

Since the lumped circuit model is based on that for the on-chip spiral inductors, we will first review the lumped circuit model for spiral inductors on silicon substrates.

The most often seen inductor structure is as shown in Figure 3.10, which consists of a spiral on one of the metal layers and an output terminal (exit) in a different layer. A via connects the spiral and the exit. Although polygon and even circular spirals have been suggested by some researchers, the square layout remains the most popular choice because of its ease of fabrication.

The model shown in Figure 3.11 is the most widely used lumped circuit model for spiral inductors [29]. In the model, L is the inductance of the spiral, Rs is the series resistance of the metal, which includes DC resistance and the additional resistance at high frequencies due to the skin and the proximity effects. C_{br} represents the direct capacitive coupling between the two terminals of the inductor. The oxide capacitance between the spiral and the silicon substrate is modeled as C_{ox} while the capacitance and resistance of the silicon substrate are modeled by C_{SUB} and R_{SUB} respectively.

Although the various terms of L, R, and C's are clearly defined in the above model, they are very difficult to separate in measurements, or even simulations. This is mainly due to the fact that the losses and coupling effects in the spiral structure are distributed in nature, and thus it is difficult to apply the concepts of lumped resistance, inductance, or capacitance. Almost all the methods proposed for determining the component values in the model involve some form of data fitting. For example, all the values of L, C and R's are found by fitting to the electromagnetic simulation results in ASITIC [14], which is a popular inductor design and analysis tool developed at University of California at Berkeley. In a more physical model proposed by Yue, *et al* in [27], analytical expressions were derived for the calculation of L, R_S, C_{br}, and C_{ox}, but the calculation of C_{sub} and R_{sub} still depends on parameters extracted from prior measurements for a given process. Therefore the model is still somewhat empirical.

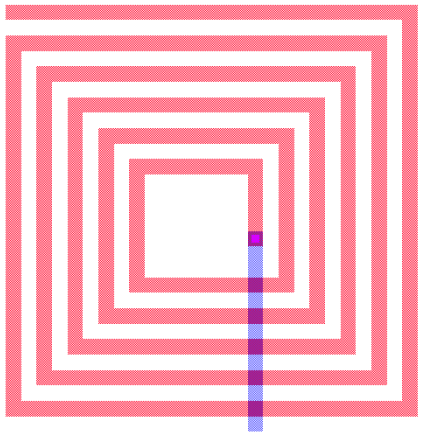


Figure 3.10 Layout of a spiral inductor

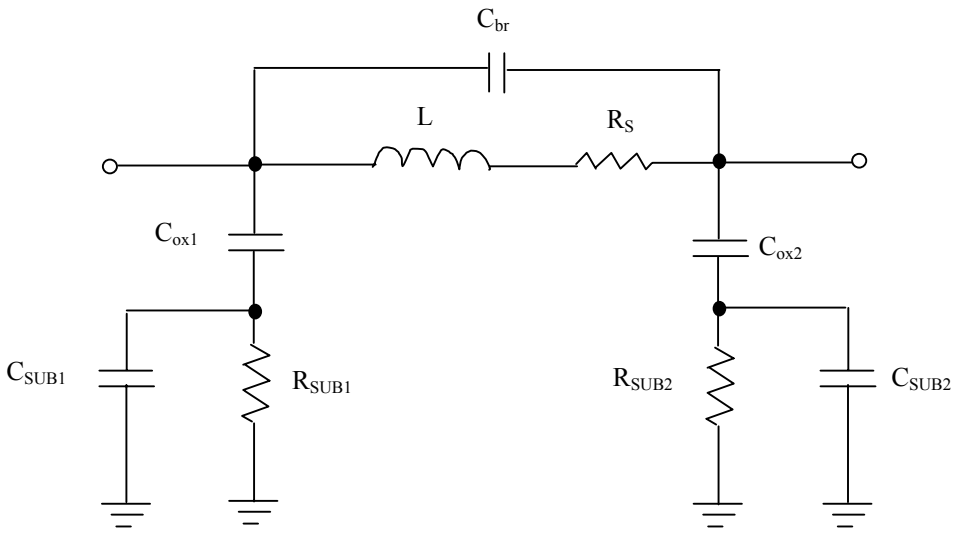


Figure 3.11 A lumped circuit model for the spiral inductors on silicon substrates

It is easy to notice the great similarity between the spiral antennas and the spiral inductors, with the only difference being the absence of the output terminal in the spiral antennas. So an equivalent circuit based on that for spiral inductors has been proposed and verified for the spiral antennas on CMOS ICs, which is shown in Figure 3.12.

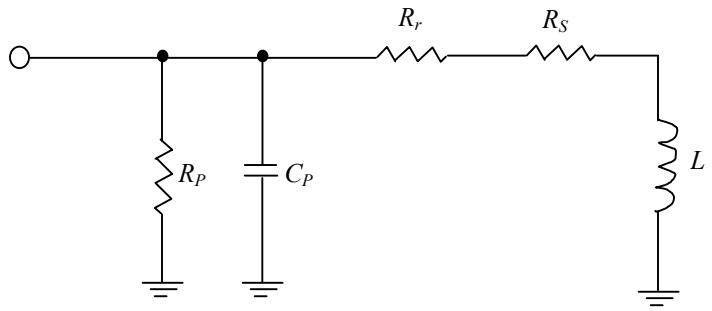


Figure 3.12 Equivalent circuit of spiral antennas on CMOS chips

The components in this equivalent circuit have similar meanings as those for spiral inductors, where L is the inductance of the spiral metal traces, R_S is the series resistance of the metal, C_P represents the capacitance between the spiral and the ground, R_P stands for the various losses in the substrate. The only difference is the addition of the radiation resistance R_r, which is assumed to be very small and has been omitted in the spiral inductor model. As in the case of the model for spiral inductors, the exact values for the components in the equivalent circuit are hard to determine physically. So some kind of data fitting must be employed in order to get the component values. In addition, there will be no way to differentiating R_r and R_S in the data fitting process are in series in the model. Therefore, they were treated as a whole, and denoted as R_S' in the model extraction.

An approach similar to the one used in [14] has been taken, in which we try to obtain all the component values through data fitting between the input impedance of the model and that from measurement or full-wave simulation. More specifically, we first measured the input impedance of the spiral antenna over certain frequency range centered about the operating frequency. The obtained measurement data were loaded into an optimizer with the equivalent circuit for the spiral antenna. The component values of the circuit were then optimized so that the input impedance of the circuit matches the measured value over the given frequency range.

4.0 DESIGN OF ANTENNAS ON CMOS ICs

Antenna design is the process of creating an antenna structure that meets certain performance specifications. For the energy-harvesting antennas, this means coming up with an antenna configuration that satisfies the requirements given in section 1.2.5. This includes the tasks of choosing the right antenna structure, the suitable material, the correct feeding method, and determining the proper geometric layout. Despite the fact that antenna engineering is sometimes considered to have established theory and design methods, it is still a very challenging task today. The primary reason is that the antenna parameters are interwoven, a change in the design might be beneficial to one parameter, but it can turn out to be deleterious to another. In addition, antenna performance is also very sensitive to many manufacturing and operational factors. A slight change in the performance requirement may necessitate a totally new design in some cases. So the design of an antenna often requires several trial and error iterations.

The planar nature of the CMOS chip structure has restricted our choices for antenna types to a small set. Time and intellectual property issues again held us from exploring too many antenna configurations. The design of antennas on CMOS ICs is further troubled by the lack of proper simplified models and design equations. In addition, there are no true tools available for antenna design. The electromagnetic solvers, such as Ansoft HFSS, are analysis, rather than design tools. We can simulate a specific structure with them, but it takes experience, or some times wild guesses, to come up with the initial design.

In this chapter, we will first take a look at the possible antenna structures on CMOS ICs, give the reasons for choosing the spiral structure, and then describe the process we took to design spiral antennas on CMOS ICs. A design example will be given at the end of the chapter.

4.1 Design Options for Antenna Structures on CMOS ICs

The CMOS process leaves little room for creativity when it comes to antenna structures. We must live with the following facts, whether we like them or not,

1. The overall dimension of the structure is small
2. The metal traces are thin and mostly in the same plane
3. There is always a conductive substrate underneath the metal structure[2]
4. The antenna can only be fed with microstrip lines

The degrees of freedom in the antenna structure are:

1. Whether or not to attach a ground plane to the back of the chip.
2. To use single or multiple metal layers
3. Whether the metal trace is wide or narrow (patch or wire)
4. Whether the wire forms a loop or is open ended

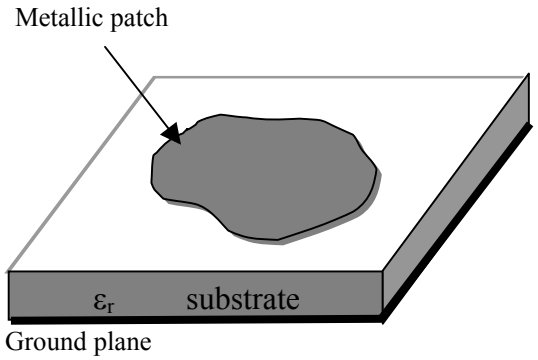
When there is a ground plane at the back of chip, the antennas become the so-called microstrip antennas. A loop antenna results when thin metal traces form a closed loop, either on a single metal layer or multiple layers. All other configurations can be categorized as wire antennas.

4.1.1 Microstrip Patch Antennas

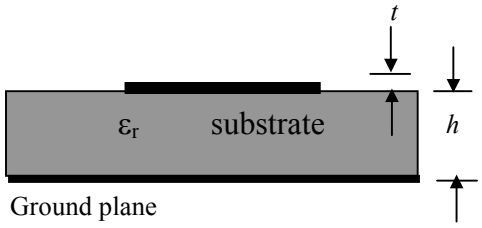
A microstrip antenna is a metallic patch printed on a thin, grounded dielectric material. It has attracted a lot of research interest recently because of its low-profile, low-cost, and easy integrability into arrays of with microwave integrated circuits [22].

[2] Although technically, it is possible to selectively remove the substrate underneath the antenna, the cost involved in such a technique prohibits its use in mass production.

The structure of a typical microstrip antenna is shown in Figure 4.1, which consists of a very thin ($t<<\lambda_0$, where λ_0 is the free-space wavelength) metallic strip placed on one side of a dielectric substrate and a ground plane on the other side.



(a) Microstrip antenna



(b) Side view

Figure 4.1 Microstrip antennas

The thickness of the dielectric for a microstrip antenna is usually a small fraction of the wavelength ($h << \lambda_0$, usually $0.003\lambda_0 \leq h \leq 0.05\lambda_0$). The metallic strip of a microstrip antenna can virtually be of any shape. But patches in the shape of square, rectangular, triangular, and circular are most commonly seen due to their relatively ease of analysis and fabrication.

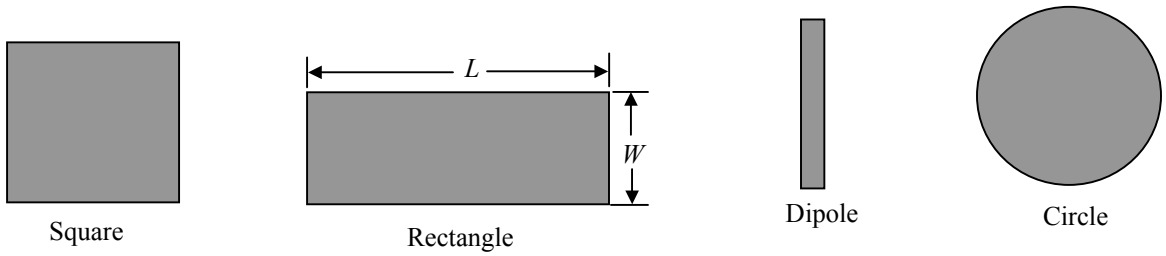


Figure 4.2 Basic microstrip antenna shapes

There are a variety of methods for connecting antennas to the source, which is termed *feeding* in antenna theory. The most commonly used feeding methods for microstrip antenna are probe (coaxial) feeding, which is shown in Figure 4.3, and microstrip line (coplanar) feeding, which is shown in. Figure 4.4

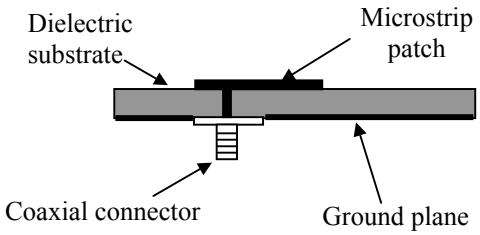


Figure 4.3 Probe feeding of a microstrip antenna

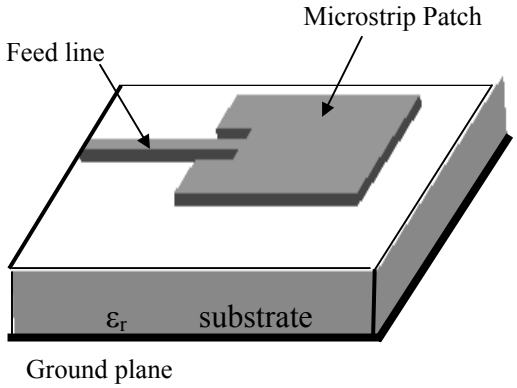


Figure 4.4 Microstrip line feeding of microstrip patch antennas

At the first look, it may seem that the CMOS process provides an amicable environment for the implementation of microstrip antennas. The metallic patch can be built with one of the metal layer of the chip while a conductor plane attached to the back of the chip, or even a lower metal layer, can serve as the ground plane. The feeding method is limited to microstrip line, but this is not a problem at all since the antenna and the source, or the rectifying circuits, must lie on the same substrate. However, in reality, there are several considerations that we need to take before we embrace this structure with full arms.

First, the thickness of the silicon wafers used for CMOS IC fabrication is usually in the order of 0.1mm to 1mm, which is less than $0.003\lambda_0$ at the chosen operating frequency of 915MHz. Since antennas require loosely bound fields to radiate into space, the radiation becomes increasingly weak as the distance between the patch and the ground plane drops, the aforesaid microstrip patch antennas are sure to be of low efficiency. This is especially worrisome if we take into consideration the existence of several significant loss mechanisms on CMOS chips, as explained in section 2.3.2.

For a microstrip patch antenna to resonate at the desired frequency, its largest dimension L must be roughly equal to $\lambda_g/2$, where $\lambda_g=\lambda_0/\sqrt{\varepsilon_{reff}}$ is the guided wavelength, ε_{reff} the effective relative permittivity. This leads to an antenna of around 10cm in length on the silicon substrates at the frequency of 915MHz. Even at 10GHz, the length of the patch is close to 10mm. This is obviously impractical when we consider the typical chip size of 1~2mm. Some researchers have suggested various size reduction techniques, such as using shorting posts and high dielectric materials [35][38], but none of them offers the required size reduction ratio, nor are they realizable in normal CMOS processes. So another difficulty in building microstrip patch antennas on CMOS IC's arises from the fact that the patch size allowed on a chip is usually too small to make it resonate.

For the above two reasons, microstrip patch antennas are not suitable for the on-chip implementation, at the frequency of 915MHz. But, at much higher frequencies, the silicon substrate will not be so thin compared to the wavelength, and the required patch length is also reduced, microstrip patch antennas on CMOS ICs may become feasible.

4.1.2 Loop Antennas

Loop antennas are widely used as receiving antennas in such devices as portable radios and pagers. The loops can take many different forms, some of which are shown in Figure 4.5. But generally, only rectangular or square loops are possible because of the requirement for Manhattan-style drawings in most IC fabrication processes.

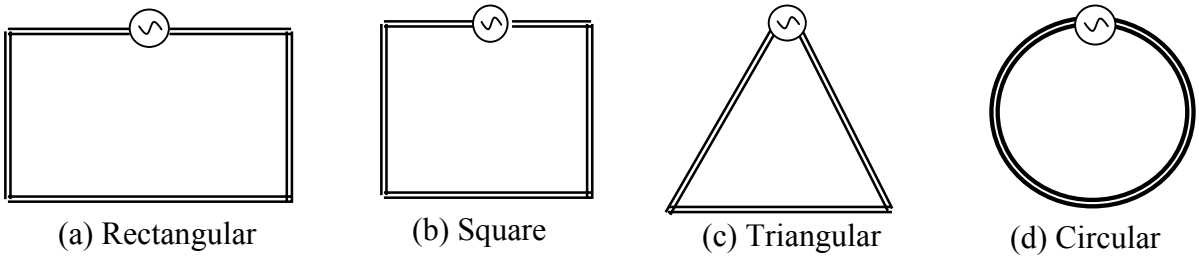


Figure 4.5 Typical configurations of loop antennas

Interestingly, loop antennas have essentially the same structure as on-chip inductors, many of the discussions on the possible layouts of inductors on CMOS ICs [14] should apply to the loop antennas. The number of turns for the loop antennas can be made fairly large if very thin metal traces are used, thus it is possible to achieve overall length (number of turns times circumference) close to the free space wavelength λ_0 for loop antennas on CMOS chips. But the perimeters of the loops are often a small fraction of λ_0 because of the stringent constraint on the overall chip size.

The field pattern of electrically small antennas of any shape is similar to that of an infinitesimal dipole [9], which is omni-directional in the loop plane, a desired characteristic for energy harvesting applications. But the radiation pattern, as well as the input impedance, is easily distorted by the silicon substrate under the loop antenna built on a CMOS chip. It also makes the analysis and modeling much more complicated.

The radiation efficiency of small loop antennas is usually very low. Even that of the discrete loop antennas used in many radios and pagers is often less than 50%. Since the common way to increase the efficiency of a loop antenna, i.e., to insert a ferrite core of very high permeability within the circumference, is not feasible on the CMOS IC, the only way to increase

the efficiency is to increase the perimeter and/or the turns. But this is also difficult because of the limited space available on a CMOS chip.

4.1.3 Wire Antennas

Among all the antenna configurations, wire antennas might be the most simple and easy to build. Virtually any kind of metal wire can be considered as an antenna, but the dipole antennas, in the form two straight wires, are most common because of their ease for analysis and fabrication.

The wire antennas built on CMOS ICs are different from their free space counterparts in that they are always backed by a conductive substrate. As a result, many of the antenna parameters differ.

4.1.3.1 Dipole Antennas. Most dipole antennas are the so-called half-wave dipoles, which are composed of two half wavelength long wires fed at a gap in the center. Unlike the free space dipole antennas, which are mostly cylindrical, the dipole antennas on CMOS ICs can only be built with flat metal traces as shown in Figure 4.6. The other difference between them is that antennas on CMOS ICs are always backed by a conductive silicon substrate, which often negatively affects its performance.

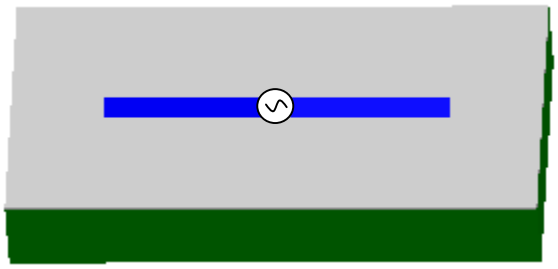


Figure 4.6 A printed dipole antenna on CMOS IC

Generally, it's not possible to build a half-wave dipole antenna on CMOS chips at low frequencies, such as 915MHz, because it exceeds 10cm in length. But it can become a good choice at higher operational frequencies because its compact geometry leads to significant savings in space. However, in [39], it was found that the input impedance of dipole antennas is easily distorted by a nearby object. This means the return loss due to impedance matching, and thus the performance of the whole system, can degrade when there is an object close to the antenna.

It's well known that dipole antennas have omnidirectional directivity pattern and are linearly polarized. This is confirmed by the simulation results shown in Figure 4.7 for a 6mm long dipole antenna assumed to be on the same substrate as the sample antenna shown in Figure 2.2.

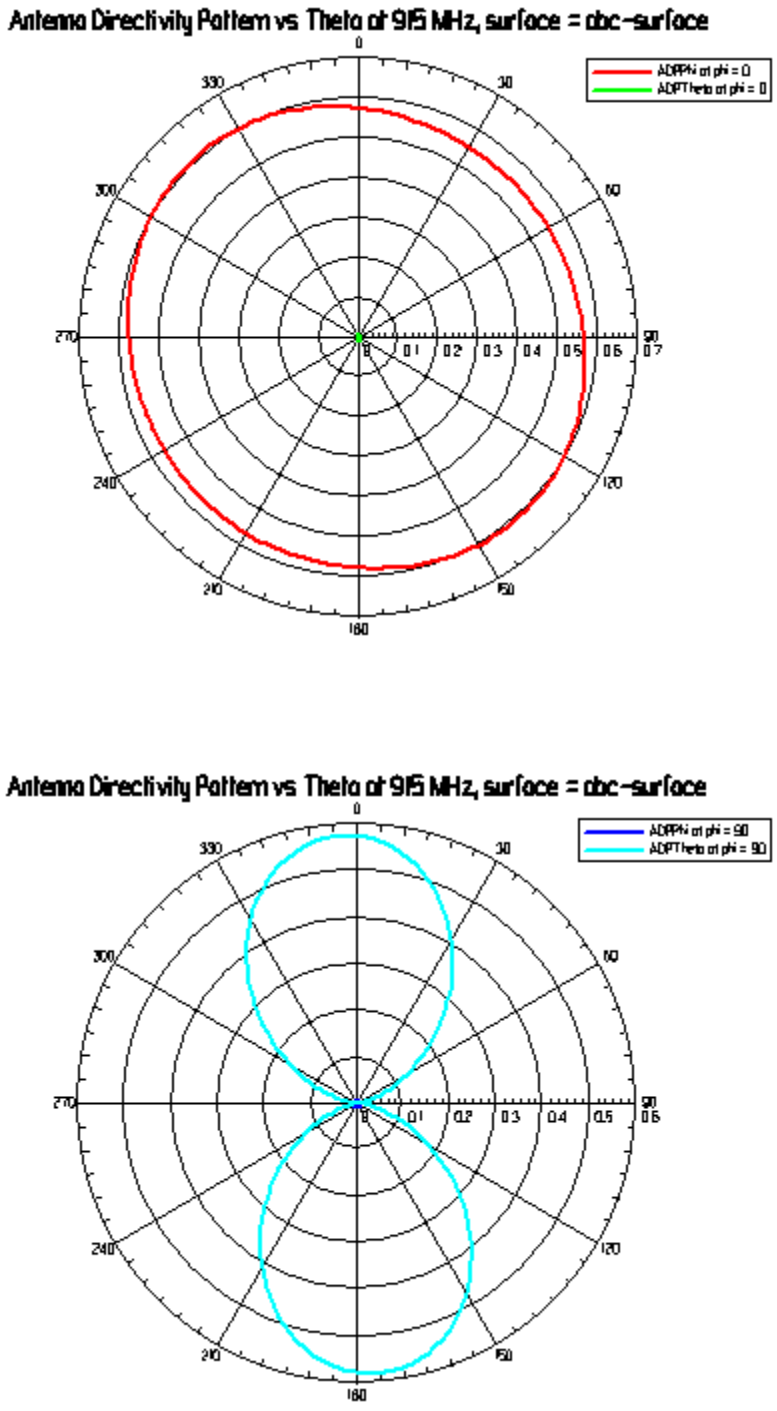


Figure 4.7 Directivity pattern of a dipole antenna on CMOS ICs

4.1.3.2 Meander Antennas. Other than the conventional dipole antennas shown in Figure 4.6, there is a class of the so-called modified dipole antennas. They are the results of continued efforts to make "shorter" dipole antennas. One example of such antennas is the meander antenna, which is shown in Figure 4.8.

Figure 4.8 A meander antenna on CMOC IC

As noted in the original paper that introduced the meander antenna [40], "In general, any attempt to reduce the physical size of monopole while preserving the same resonance frequency ends up with deficiencies such as bandwidth distortion, pattern distortion, and reduction in efficiency." The shortening ratios of the meander antennas and the effects of the reduced sizes were carefully studied in [41]. It was found that the radiation pattern of the meander antenna is similar to that of a conventional half-wave linear dipole antenna when the shortening ratio is about 30 percent. So a meander antenna may be a choice when the conventional dipole antenna will not fit in a small area.

4.1.3.3 Spiral Antennas. Spiral antennas were first reported in the antenna literature in the early 1960's [42] and drew considerable attentions recently because of their great potentials for the much wanted space savings and broader bandwidth in applications such as telecommunication systems [43][44]. Spiral antennas designed for telecommunication systems are usually composed of two interleaving spirals fed at the center as shown in Figure 4.9.

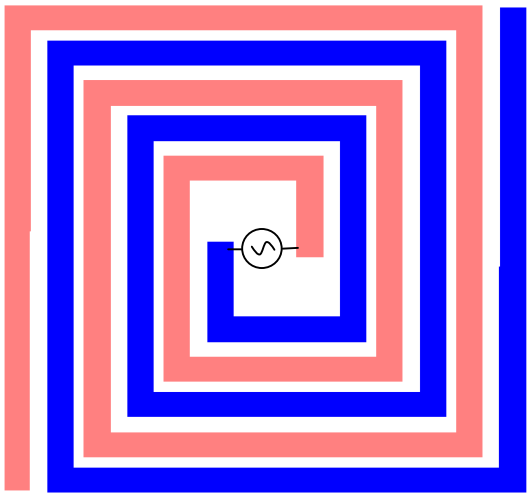


Figure 4.9 Dual spiral antennas

Like the printed dipole antennas described in section 0, the dual spiral antenna structures are balanced at the feeding. Since the operation of most digital circuitry requires a uni-polar (unbalanced) voltage source, a balanced-unbalanced transformer (balun) might be in order if the dual spiral structure is used for the energy-harvesting applications. That is one of the advantages of the spiral antenna studied in this work, which is composed of only one spiral fed at its outside terminal and thus unbalanced with respect to the ground.

The single spiral structure came from the idea of building a quarter wavelength whip antenna, as shown in Figure 4.10, in a small area by winding the whip into a spiral while still

keeping its total length at $\lambda_0/4$. Since the overall dimension of a chip is much smaller than a wavelength, spiral antennas on the CMOS chips are expected to have side length (*SL*) much shorter than those for telecommunication systems. So, it takes many more turns for a spiral antenna on a CMOS chip to have a total trace length of $\lambda_0/4$. As a matter of fact, multi-turn spiral antennas might be the only type of antenna that could possibly resonate at 915MHz within areas in the range of several mm^2. That's the major reason for choosing spiral antennas as the energy-harvesting antenna on CMOS chips.

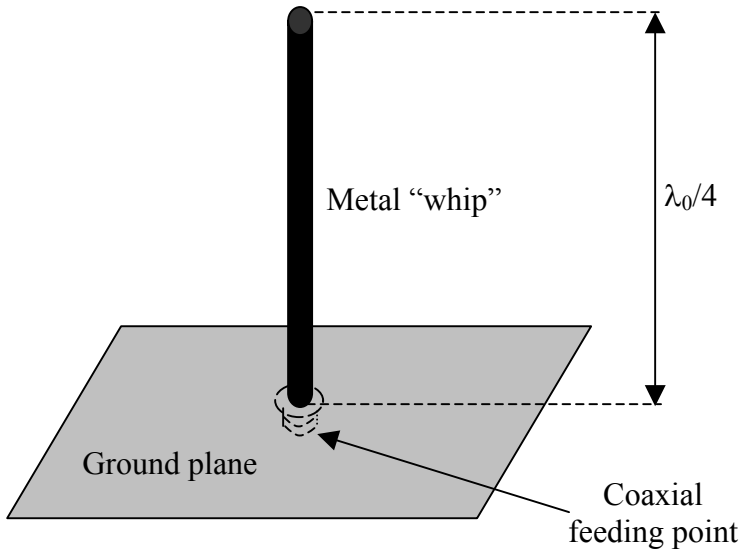


Figure 4.10 Quarter wavelength whip antenna

The single spiral antenna structure studied in this work is similar to other modified dipole antennas in that it is the result of efforts to reduce the overall length of a dipole antenna. So it suffers from the same distortions in directivity pattern, input impedance, and other parameters. Roughly speaking, the smaller the area, the more turns it takes, the more degradation is expected. So it is suggested that for the same total metal trace length, the number of turns for a spiral antenna should be kept as small as possible, or use conventional dipole antennas if higher operation frequencies are available.

At the early stage of this work, it was assumed that the ground plane should cover the whole back of the chip, which would make it a microstrip antenna according to the definition given in section 4.1.1. As explained earlier, the thin and lossy substrate makes such configurations extremely inefficient as radiators. In the later part of this research, the ground plane was removed from the back of the antenna. But a ground plane behind the circuit part of a CMOS chip is still necessary for the normal operation of the digital circuitry and the construction of the microstrip line feeding structure for the antenna. The resulting ground and feeding structure is shown in Figure 4.11, from which we can see that the back of the SA-SOC behind the circuitry is covered by a metal ground while that side behind the spiral is left open. It is found in both the simulations and the experiments that the size of the ground plane has a significant effect on the impedance, but little or no effects on the radiation efficiency or the directivity pattern of the antenna.

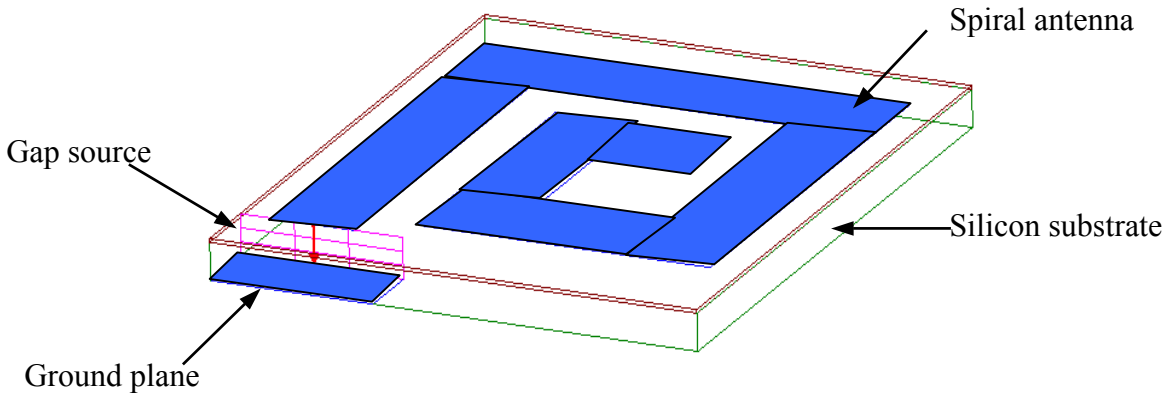


Figure 4.11 Ground and feeding structure of a spiral antenna

4.2 Design Procedure of Spiral antennas on CMOS ICs

Generally speaking, the goals of the design process of an energy-harvesting antenna should at least include the desired directivity pattern, polarization pattern, and input impedance based on the requirement of the specific application. However, the directivity and polarization patterns of the spiral antennas are very similar and do not vary much with such design parameters as the trace width and the trace spacing. So the major goal for the design of a spiral antenna on CMOS IC is that it resonates at the chosen operating frequency.

As mentioned in the previous section, the total trace length of the spiral antenna is chosen to be roughly equal to a quarter of the free space wavelength. As a rule of thumb, the side length of the spiral should be made as large as possible in order to increase the overall dimension of the antenna. The number of turns should be kept small in order to reduce the conduction losses. So the primary design variables are the metal trace width and trace spacing, which will be chosen in

such a way that the antenna resonates at the operating frequency. The major criteria for resonance is that the input impedance of the antenna is real, *i.e.*, reactance is close to zero, at the frequency.

The choice for the trace width and trace spacing in the initial design is somewhat arbitrary, but they were made equal in practice. Once we have an initial design with the total trace length equal to $\lambda_0/4$, it is put into full-wave simulation with Ansoft HFSS. The obtained input impedance of the antenna is compared to the desired value. If it is within an acceptable range, *e.g.*, the difference between the current resonant frequency and the target value is within 5% of the target resonant frequency, the design will be accepted, otherwise the trace width and spacing will be adjusted and the design is put back into simulation. Generally speaking, the trace width should be increased when the resonant frequency is higher than the target value, or decreased when the resonant frequency is too low. This iteration continues until the desired input impedance is achieved.

Although there exist a few papers that can be sourced to justify the choice for the single spiral structure [45], it is not backed by the majority of the conventional antenna theory. Therefore, the choice for such a structure and the corresponding design method that will be presented in the next section is mostly heuristic or experimental.

As a summary, the above considerations of the design process are organized in the diagram shown in Figure 4.12.

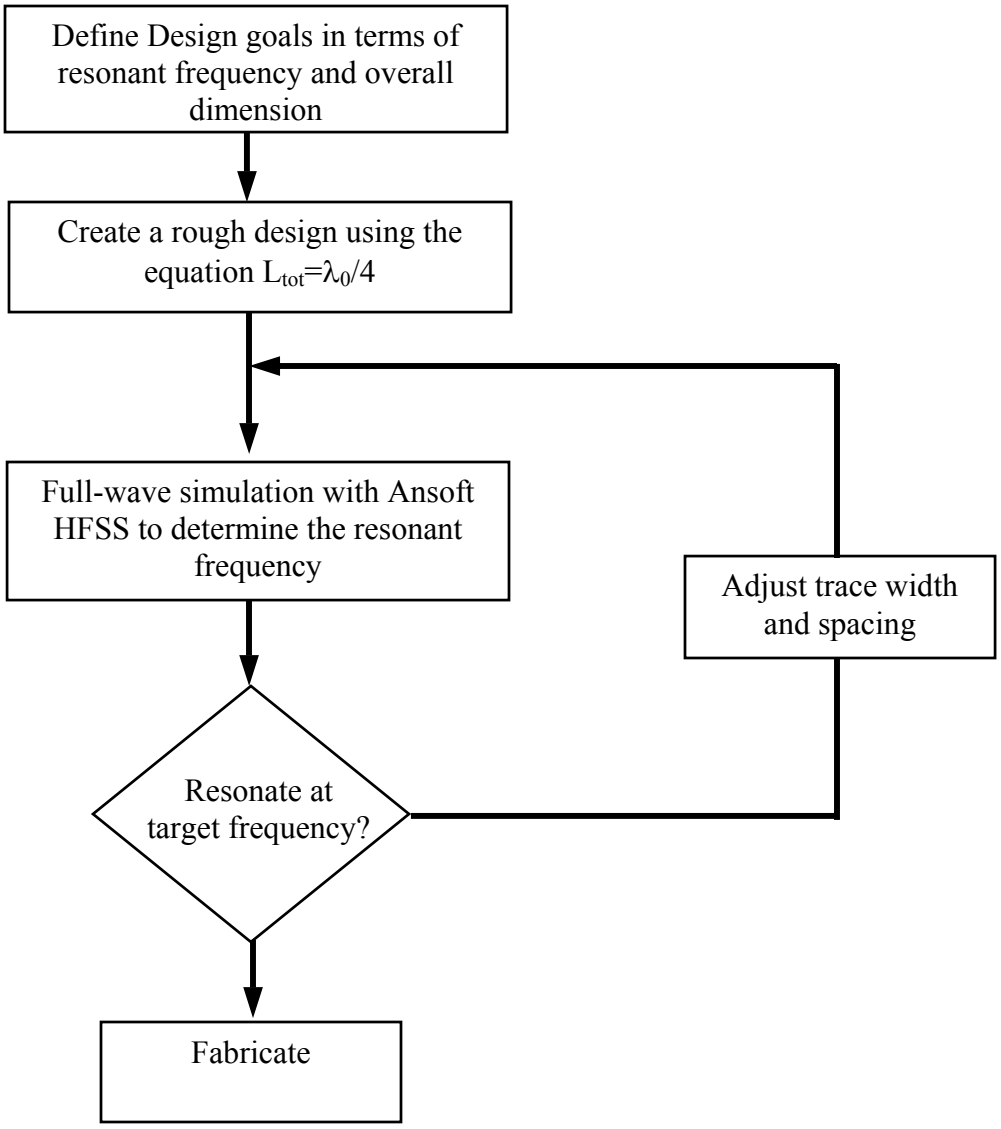


Figure 4.12 The design process of spiral antennas on CMOS ICs

4.3 A Design Example

In order to further illustrate the design procedure described in the previous section, the design process of the sample antenna shown in Figure 2.2 is given here as an example.

The material properties for each layer of the antenna structure are as given in section 2.2. The side length of the antenna is also predetermined to be 13mm. In the initial design, the trace width and the trace spacing were both chosen to be 2mm. To make the total trace length equal to a quarter wavelength, *i.e.,* about 80mm at the frequency of 915MHz, the number of turns needs to be 1.5. When we put the initial design into simulation with Ansoft HFSS, the resonant frequency was found to be around 950MHz. So the metal trace width and spacing were modified, and the design was again put into simulation. After several tries, we came to a design with parameters as given in section 2.2. The input impedance of the antenna at 915MHz is shown in Figure 4.13, from which we can easily tell that the antenna resonates at the given frequency.

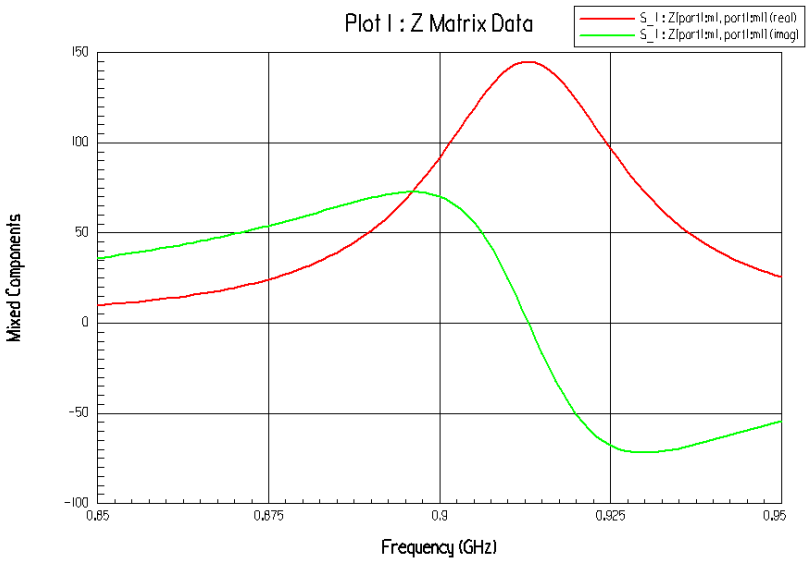


Figure 4.13 Input impedance of the sample antenna

5.0 OPTIMIZATION OF ANTENNAS ON CMOS ICs

As we have seen in section 2.2, CMOS technology does not provide a friendly environment for building antennas. Some characteristics of the CMOS process, such as the stringent restriction on the antenna sizes and the conductive nature of the silicon substrates, bring about problems that are not commonly seen in the conventional antennas. Some measures must be taken in order to minimize their adverse effects.

Among the five factors that affect the maximum effective area of an antenna as given in (1.10), the radiation efficiency is most severely affected by the harsh antenna environment on CMOS ICs. So enhancing antenna efficiency should be the focus of the optimization efforts, which are mainly ways to reduce the losses in the substrate and the conductor. The operating frequency, or equivalently the wavelength of the RF source, affect all four other factors, especially the radiation efficiency and the input impedance, so it is necessary to take all these effects into consideration when we try to determine the optimal wavelength. The exact impedance matching between the antenna and the load is generally difficult for antennas on CMOS ICs since there is no way to tune the matching after the fabrication is done. The level of difficulty for the matching depends on the chosen antenna structure and the operating frequency. So we should optimize them in such a way that proper impedance matching can be achieved at relative ease and under varying environmental conditions. The maximum directivity and the polarization should be regarded as design goals that are given for a specific application. In the following discussion, we will assume that best values of these two parameters can be achieved primarily through the choice of the antenna type and control of the antenna geometry in the design process and thus not considered as optimization variables.

5.1 Choosing the Optimal Frequency

It seems to be common knowledge in the antenna and microwave society that it becomes practical to integrate the planar antenna structures on silicon monolithic integrated circuits with dimensions on the order of several millimeters when the operating frequency is above 60GHz. The reasoning is that only at this frequency range, will the antenna size be comparable to the wavelength, and thus the antennas will have acceptable radiation efficiency and workable input impedance. However, the requirement on radiation efficiency should be less demanding when the antenna is only used in receiving mode and for short distance operations. For example, Singh *et al* have shown that an antenna can have satisfactory results at 5.98GHz with dimensions less than 10mm×10mm in [46].

According to equation (1.10), the maximum effective area, A_{em}, of an antenna is proportional to λ^2 when all four other factors are assumed constant. This suggests that a larger wavelength can actually lead to larger A_{em}. However, this conjecture is most likely false, especially for small antennas, because the other four factors can not be assumed to be constant when the incident wavelength changes. As a matter of fact, as we have shown in section 2.3.1, the efficiency of an antenna built in the same small area drops quickly when its overall dimension becomes increasingly smaller than the wavelength. The input impedance of the antenna also becomes much higher and less predictable, and thus makes optimal impedance matching less likely. As a result, A_{em} of the antenna may drop, instead. Nevertheless, it is obvious that there exists a tradeoff between the direct positive effects of the increased wavelength on A_{em} and its negative effects on the radiation efficiency and other factors, which lead to reduced A_{em}.

Generally speaking, higher frequency equipment is more expensive and delicate. High frequency waves may also require line of sight transmission. Both of these characteristics may be disadvantageous for the low cost applications like RFID. And of course, there is always the FCC. Some bands may simply not be available even if we feel they are the most suitable.

All of the above mentioned factors should be taken into consideration when we try to decide the optimal frequency for a given RF energy-harvesting application. Due to the complexity of the problem, it is very unlikely that we will be able to find the optimal frequency through simple simulation or analysis. Extensive experimental studies are necessary, which are beyond the scope of this research.

5.2 Reducing Substrate-related Losses

As we have shown in section 0, the conductive silicon substrate brings about heavy losses to the small antennas built on it and thus greatly reduces its radiation efficiency. Therefore, it is imperative to use high resistivity silicon. However, high resistivity silicon wafers cost more than the normal wafers. And generally speaking, the purer the wafer, the higher the price is. Consequently, it is advantageous to make certain changes to the antenna structure so that wafers with lower resistivity can be used. On the other hand, even intrinsic silicon, which has the highest possible resistivity, is fairly conductive compared to the dielectric materials used in normal antennas. Therefore, there is still a need and room for reducing the substrate related losses.

With the increase of the interest in integrating inductors on CMOS ICs, many researchers have proposed and demonstrated their ideas for reducing the unfavorable effects of the

conductive silicon substrates on the performance of the on-chip inductors. Most of those techniques are directly applicable to the antennas on CMOS ICs.

The obvious and straightforward way to reduce or even eliminate the losses associated with the conductive substrate is to simply remove it. Technically, this is possible with MEMS techniques such as selective etching [24]. Some researchers have even demonstrated the possibility of folding a planar metal structure with the surface tension of a meltable hinge as the action force, by which the two-dimensional antenna metal structure are turned 90 degrees and stand perpendicular to the substrate [47]. However, most of the MEMS techniques are complicated and costly. The resulting structures are often fragile. They may be utilized in some limited special applications, but they will not be good choice for mass production, at least in the near future.

Instead of selectively etching only the substrate underneath the metal structure, it is also possible to reduce the thickness of the whole substrate through grounding and/or polishing. In [49], it was shown that thinning of the silicon substrate leads to a higher Q and increased self-resonant frequency for on-chip inductors, when the chip is mounted on a lossless substrate, such as glass or quartz. However, it was also noticed in [49] that wafer thinning will have detrimental effects on Q if the chip is mounted on a metal substrate. For the small antennas built on the silicon substrates, the thinning of the wafer will certainly lead to a reduction of losses in the substrate, but it will also reduce the effective permittivity of the substrate, which in turn will lead to an increased guided wavelength λ_g. Since the resonant frequency of the antenna is a strong function of the guided wavelength, it is expected to vary as the wafer thickness changes. More specifically, the resonant frequency of the antenna will increase as the wafer becomes thinner. Alternatively, we need to increase the total length of the antenna so that it still resonates at the

desired frequency. This is often not desired since longer trace in the same area can only lead to a narrower trace width and thus more conduction loss.

Many researchers have also suggested inserting a metal ground so that the inductor is shielded from the substrate [48]. In order to reduce the eddy currents in the metal ground shield, perforations are made and thus make it the so-called patterned ground shield (PGS). It was found in [48] that the quality factor Q of the inductor could be increased with a proper PGS at the cost of reduced self-resonance frequency f_{SR}. For the on-chip antennas, the use of a ground shield placed so closely may further reduce the already weak radiation from the small antenna because the field will become tightly bound to the structure.

As we can notice from the brief description of the CMOS process in section 2.1, even the top metal layer, where the metal structure of the antenna lies, is very close to the conductive substrate because the metal layers and the dielectric layers in between are fairly thin (on the order of several μm's) in normal CMOS processes. So even though the inter-metal dielectric is a fairly good dielectric in terms of losses, it does not provide much insulation of the electromagnetic wave from the top metal layer to the conductive substrate. Therefore one way to reduce the substrate loss is to increase the thickness of the inter-metal dielectric so that the top metal structure is farther away from the conductive substrate. This method has been shown to be fairly effective for improving the quality factor of inductors on CMOS ICs [50]. It has been adopted by some analog friendly process, such as IBM *BlueLogic*^{TM} BiCMOS 5AM. But the extent to which this method will work is primarily limited by the thickness of dielectric one can get from a given process. The gain from the increase in the dielectric thickness is also expected to diminish as the metal structure is located further away from the substrate.

Figure 5.1 shows the changes in antenna efficiency and resonance frequency as the thickness of the dielectric between the substrate and the metal structure increases from a minimum of 5μm to a maximum of 60μm for the sample antenna shown in Figure 2.2. We can see that the efficiency of the antenna increases substantially as the thickness of the dielectric layer increases.

In standard CMOS processes, the inter-metal dielectric is mostly made of silicon dioxide (SiO_2), which has a much smaller permittivity (ε_r=3.9) than that of the substrate (ε_r=11.9), it is expected that the effective permittivity of the whole substrate decreases as the thickness of the inter-metal dielectric increases. This leads to an increase in the resonant frequency of the structure as shown in Figure 5.1, which is similar to the situation where the thickness of the silicon substrate is reduced. On the other hand, if we replace the silicon dioxide with high-permittivity materials, the resonant frequency of the same antenna should decrease. This might bring further benefits to the spiral antennas since the number of turns can be reduced because of the reduced total trace length needed.

For the ease of fabrication and minimal effects on the interconnections of active devices, only the inter-metal dielectric below the top metal layer should be changed. Generally speaking, thick inter-metal dielectric should not be very difficult to realize in commercial CMOS processes with minor changes at the very least, if any, additional cost. This is especially true if a CMOS foundry is dedicated to the production of the energy-harvesting chips.

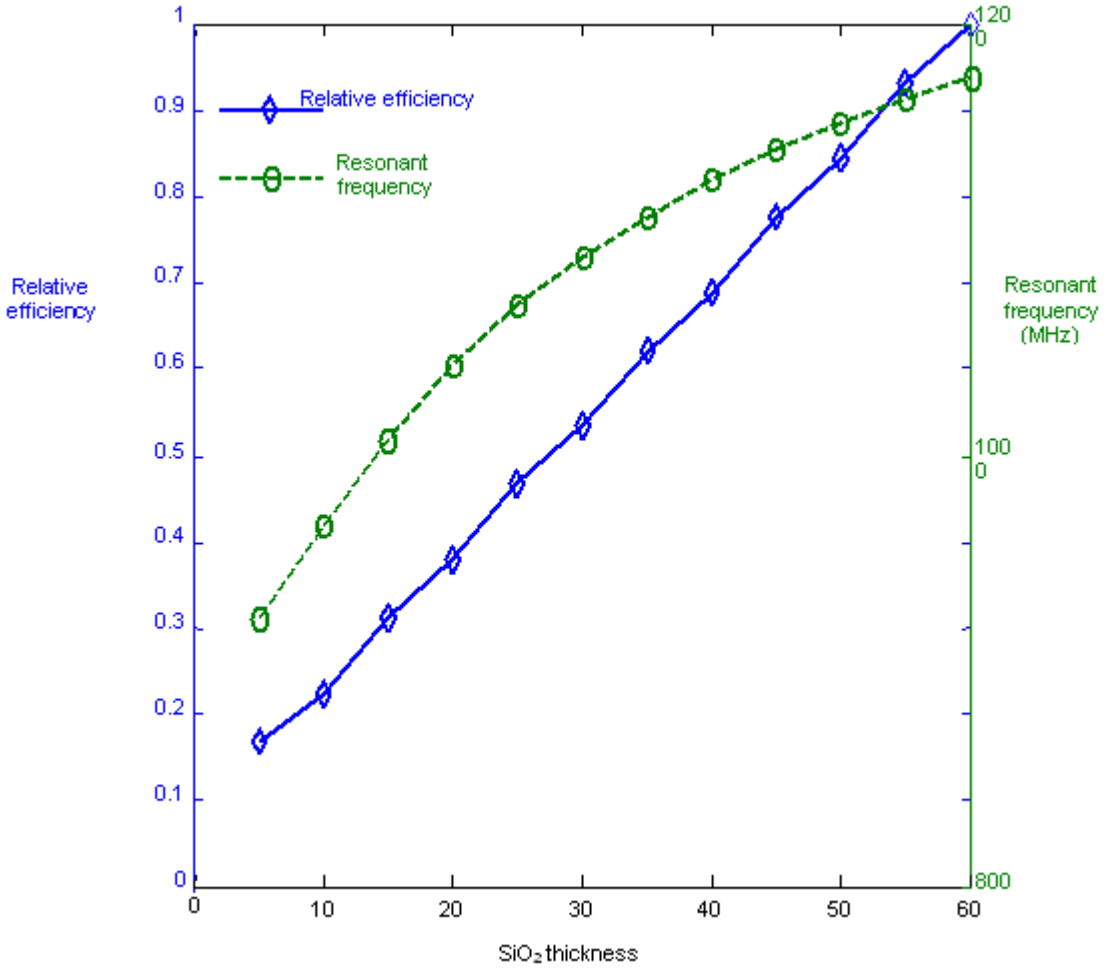


Figure 5.1 Effects of changing dielectric thickness

5.3 Reducing the Conduction Loss

To reduce the conduction loss of antennas on CMOS chips, better conductors or/and increased metal thickness should be used. However, the use of high conductivity metal, such as copper, or even gold, increases the fabrication cost considerably and may not be a good choice for low cost applications such as RFID. A thick metal layer is offered in some modern CMOS processes mainly for building on-chip inductors, which should work for antennas, too. But the gain from increasing metal thickness will diminish when the operating frequency is higher and the ac resistance becomes dominant due to the skin effect.

Due to the limited available fabrication resources, only the effects of changing metal thickness were verified with experiments. The results are presented in section 7.2.3.

6.0 MEASUREMENT OF ANTENNAS ON CMOS ICs

Measurement is necessary to prove that the specific requirements of an antenna, which are designed to conform to the specifications, are satisfied. All the antenna performance parameters listed in section 1.2, *i.e.* radiation pattern, gain, efficiency, polarization, and input impedance, deserve serious measurement efforts. But accurate measurement of most parameters for antennas on CMOS chips is generally difficult partly because the absolute values of the results are often small due to their small sizes and thus more vulnerable to systematic or random errors. One may say, the smaller the antenna size, the harder it is to determine its performance [51]. The most common problems with small antenna measurement include the coupling of nearby materials, the existence of unbalanced currents on the connecting cables, limited accuracy of the equipment, and so on. Even particular considerations are given to the measurement of small antennas, there may still be some cases where no effective method can be found [51].

Other than being extremely small, an antenna on CMOS IC is supposed to work by itself, which means no cable or wire connection of any form is made to it while it is in the working environment. When we try to connect it to the standard equipment using wires or cables, the field and the current distributions on the antenna are easily distorted. Consequently, the accuracy of the measurement may become comprised, or even nonexistent.

The accurate measurement of some of the parameters, such as the radiation pattern, requires fairly sophisticated equipment like antenna chambers or antenna ranges, which are not available in the departmental lab or readily available at other facilities. On the other hand, the figure of merit that is most important for the energy-harvesting antennas, its available power under given condition, is extremely difficult to measure using standard equipment because of the

cable connection problem mentioned earlier. As a result, certain unconventional method must be developed in order to get meaningful measurement results for the on-chip antennas in this research.

6.1 Measurement Setups

Generally speaking, the ideal measurement setup for the antennas on CMOS ICs should satisfy the following three conditions:

1. The feeding to the antenna should be the same as that in its actual use. The use of wire or cable connections should be avoided if possible.
2. The measurement should be accurate and stable.
3. The measured data should be easy to collect and analyze.

Since the maximum available power is most important for an energy-harvesting antenna, the setups we are going to discuss next are primarily for its accurate measurement. Some key antenna parameters, such as antenna directivity pattern, can be measured easily once the available power can be determined accurately.

6.1.1 Measurement Using Standard Equipment

Most RF measurement equipment, such as the vector network analyzer and the power meter, use coaxial cables to connect the devices under test (DUT). Because the on-chip antennas do not use probe feed, there is the problem of getting it connected to the cable.

One possible solution is to use a probe station, which is commonly utilized in the testing and measuring of impedance for integrated circuits. It works by bringing down a very fine needle into contact with the DUT. The needle and its connection to the cable can be calibrated following

standard procedures. Therefore, a probe station often offers high accuracy even in the frequency range of tens of GHz. However, while using the probe station, the DUT must be placed on a metal mounting holder, which acts as a large ground plane for the antenna and makes it impossible to build the feeding structure since it only has a ground plane underneath the feeding line and no metal ground plane behind the antenna structure itself. Furthermore, it is not possible to use a probe station to measure the available power from the antenna since it is usually bulky and not movable. Its metal frame will also interfere with the incoming wave.

The connection adapter used in this research is shown in Figure 6.1. The antenna chip is mounted on a printed circuit board (PCB) made from FR4-epoxy. A right angle PCB SMA-mounter is soldered to the back of the board. Its center pin is connected to the outside terminal of the spiral antenna with a bond wire while its ground shield is in contact with the small ground plane on the upper layer of the board.

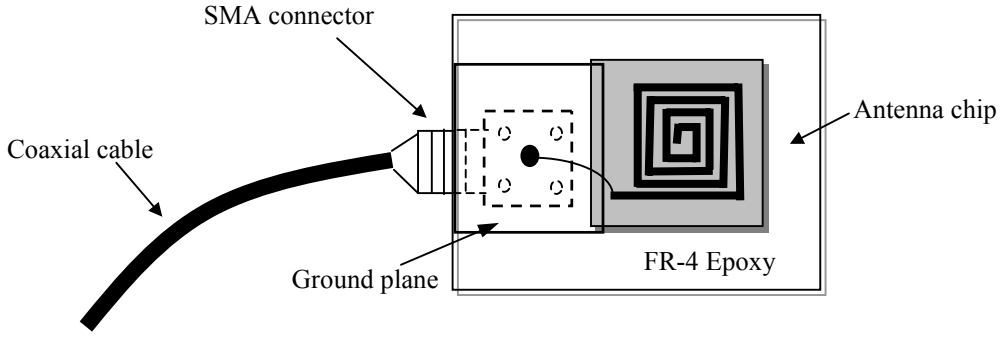


Figure 6.1 Measurement setup with cables

Obviously, the feeding to the antenna in the setup shown in Figure 6.1 is different from that in its actual use. So care must be taken in order to minimize the effects of such difference. It has been suggested in [46] that the use of two parallel bond wires help to reduce the inductance

of bond wire. In [52], it was shown that reducing the elevation of the bond wire from the ground plane helps to minimize its radiation effects. These suggestions were followed in this research.

The setup shown in Figure 6.1 can be used in the measurement of input impedance of the antennas. However, it is still not suitable for the measurement of available power from the antenna because there often exists a severe impedance mismatch between the antenna and the cable connection. The impedance of the on-chip antenna is usually much higher than the fixed impedance of 50Ω, 75Ω, or 300Ω for the cables and connectors. Because of this, the available power measured with the configuration shown in Figure 6.1 can be much lower than what to be expected when the antenna is connected to a matched load. The severity of the error, i.e., the difference between the measured power and the actual value, depends on the severity of the impedance mismatch. In addition, the antennas are often so small that their overall dimension is comparable to the length of the bond wire. There is a good chance that the bond wire itself is acting as an antenna.

6.1.2 Power Measurement with an Integrated VCO

The problem with the wire and the cable connections to the antenna forced us to look for a scheme that has integrated power sensors on the same silicon substrate as the antenna. The sensor can take place of the functional circuitry and the resulting chip should have the same RF front end as a working SA-SOC. Instead of transmitting stored information or physical measurement data to the receiver, it senses the power (voltage) available from the antenna and sends it back to the receiver.

One such sensor is the Voltage Controlled oscillator (VCO), which is a functional circuit whose frequency of the output signal depends on the control voltage. It was shown to be

effective for the measurement of available power from an on-chip magnetic coil [53]. It can be easily integrated on a CMOS IC [13], but the one to be used on a SA-SOC has the distinguished characteristic that the control voltage and the supply voltage are the same because they must both be connected to the DC output of the rectifier. If we obtain the relationship between the DC voltage and the oscillation frequency prior to the measurement, we will be able to determine the voltage on the IC by analyzing the frequency of the output signal from the VCO. Since the power consumed by the chip at a given DC voltage level is readily known, the voltage measurement quickly leads to the available power from the antenna. The output signal from the VCO is transmitted through an additional antenna, which is much smaller than the energy-harvesting antenna and is expected to have minimal effects on the energy-harvesting antenna.

The complete measurement setup is shown in Figure 6.2.

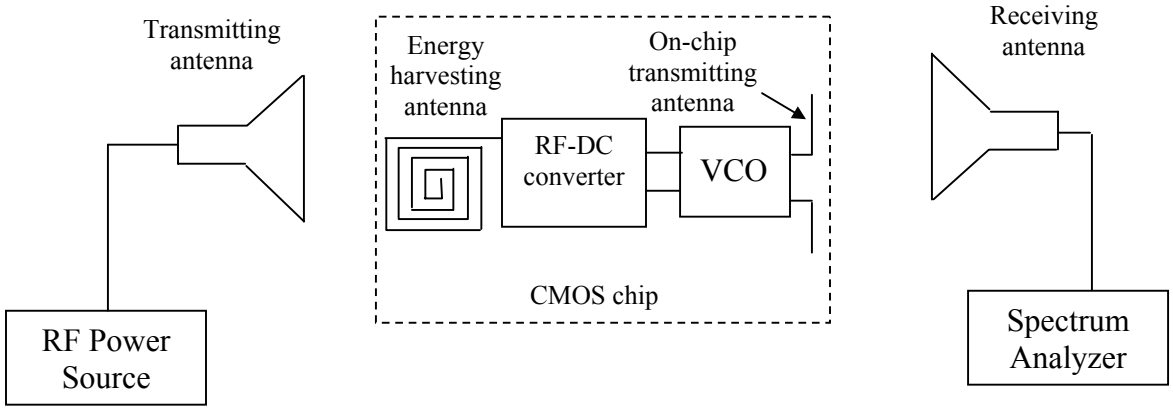


Figure 6.2 Measurement setup with an integrated VCO

The integrated sensor scheme is probably the best setup for the measurement of available power from the antenna in terms measurement uncertainty or measurement errors. However, its implementation poses a great challenge. First, the impedance matching between the antenna and the rectifying circuit on the CMOS IC is not tunable since everything is fixed after the chip is fabricated. This requires the matching to be first time correct, which is very unlikely due to the limited capabilities of the analysis and design tools. Therefore, an expensive trial and error process is unavoidable. Furthermore, most of the commercial semiconductor fabrication processes are optimized for the fabrication of digital ICs and often use highly doped silicon substrates, which are detrimental to the on-chip antennas. The few analog (most likely antenna) friendly processes are prohibitively expensive. As a result, it is very difficult to find a process that offers the desired specifications at an affordable price.

6.1.3 The Virtual Power Meter

The high cost of the CMOS IC fabrication and the difficulty in adjusting impedance matching lead to the development of a self assembled measurement system, which is given the name of Virtual Power Meter (VPM). The VPM follows the similar principle as presented in the single chip configuration with an integrated VCO. However, instead of the same silicon wafer, the antenna and the circuitry lie on the same printed circuit board (RF power sensor board). The details of its implementation and usage are given in appendix A. The RF power sensor board with an antenna under test and the detail of the bond wire feed are shown in Figure 6.3.

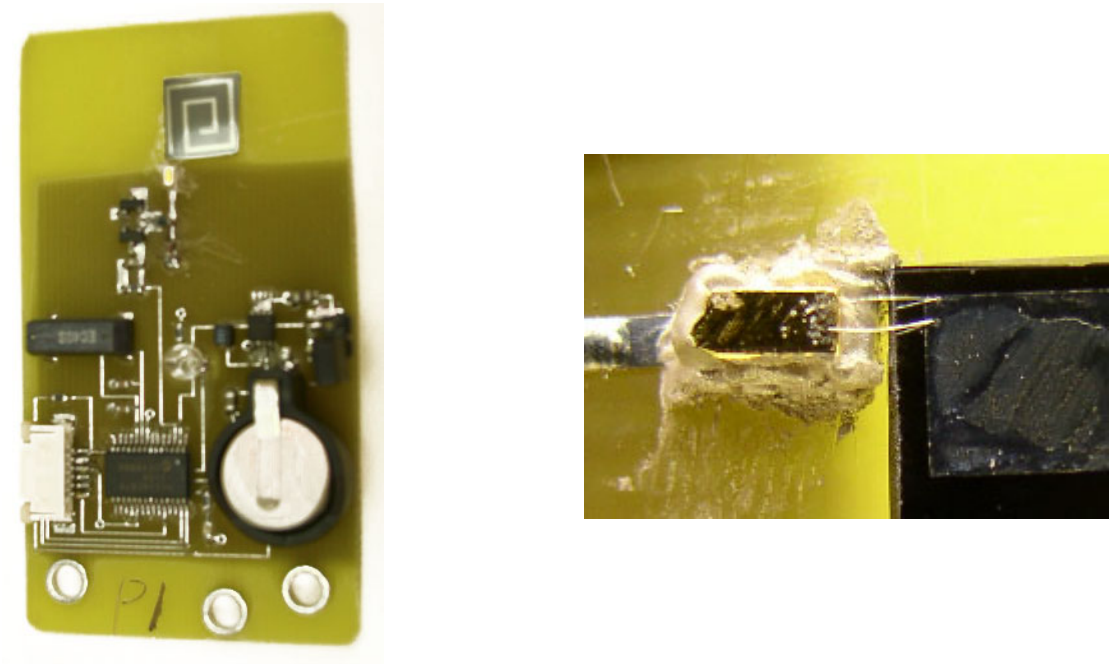


Figure 6.3 RF power sensor board setup

The most prominent advantage of the VPM setup is that it is much easier to match the impedance between the antenna and the rectifier. This is of great importance because it is only possible to get a fair comparison of the available power among different antenna designs when they are all matched to the rectifying circuit. Since the impedance of antennas usually differs, it is necessary to use different matching components for different antennas, which, as explained earlier, involves a try and error process that is not possible on the integrated circuit environment. On the board, changing the matching components is not a mission impossible any more. Using the technique described in the following section, matching is even possible without prior knowledge of the impedance of the antenna.

Because the detector circuit is not integrated on the same substrate as the antenna, a bond wire is necessary to connect them, which inevitably adds uncertainty to the measurement results. The measurement circuitry on the RF sensor board may also have some effects on the

performance of the on-chip antenna, although the board is designed in such a manner that its overall dimension is minimized and a ground plane shields the circuit components and the battery from the incoming wave. Although it is difficult to determine the complete set of effects of the test circuitry on the performance of the DUT, the results obtained in the experiments suggest that they appear to be minimal.

6.2 An Annealing Approach to the Impedance Matching

According to the maximum power transfer theorem, the impedance of the load should be made equal to the complex conjugate of that of the antenna in order to obtain the maximum power at the load. However, sometimes it is difficult to find out the exact output impedance of the antenna, especially when the overall size of the antenna is much smaller than the wavelength. So an annealing has been developed so that the maximum power transfer condition can be found without prior knowledge of the antenna impedance.

6.2.1 Description of the Method

The method was developed when we tried to match the impedance of the rectifying circuitry to that of the antenna with the virtual power meter setup. The schematic of the front end of the RF power sensor board used in VPM is shown in Figure 6.4. As we can see from the figure, the RF power received by the antenna is converted to DC by the voltage doubler circuit built with diodes D_1 and D_2. The inductor L_1, the capacitor C_1, and the three parasitic transmission lines TL_1, TL_2, and TL_3, construct the impedance matching network between the antenna and the voltage doubler. As the component values of L_1 and C_1 vary, the impedance

matching condition changes. The goal of the method is to match the impedance looking into the rectifying circuit Z_{Rct} to that of the antenna Z_{Ant}.

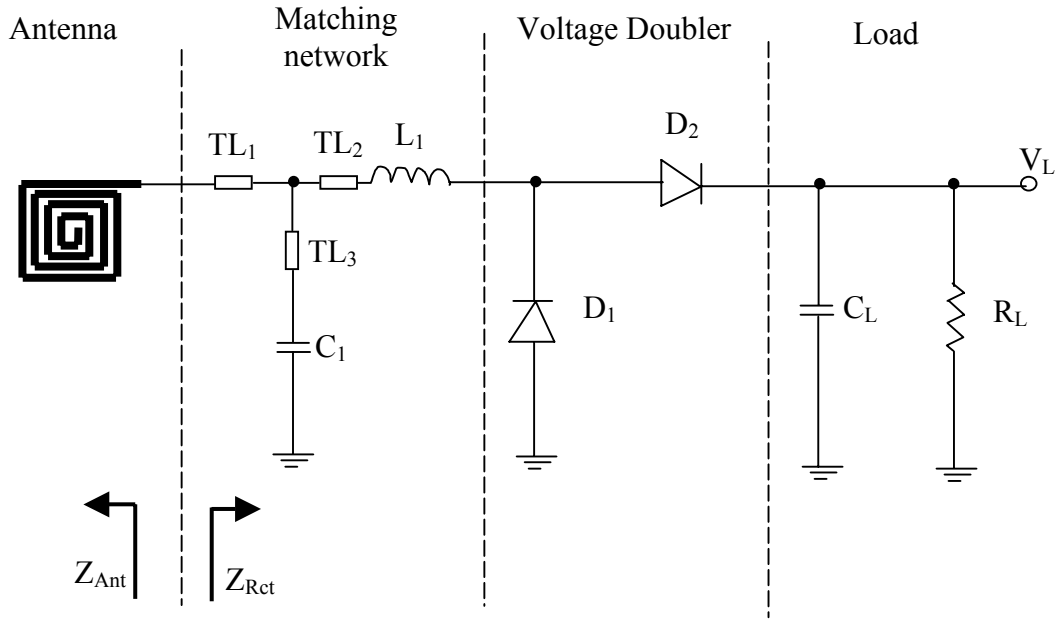


Figure 6.4 Impedance matching network

For a given antenna under the same testing condition, the DC voltage level V_L on the precision resistor R_L varies when the values of L_1 and/or C_1 are changed. So V_L is an indicator of the degree of matching between Z_{Rct} and Z_{Ant}. For each matching condition, *i.e.*, one combination of L_1 and C_1, in addition to V_L, the input impedance of the detector circuit Z_{Rct} is measured with an identical circuit board but without the antenna. If we plot the DC voltage level V_L on a chart that makes it easy to tell the corresponding value of Z_{Rct}, we will be able to visualize the change in the degree of matching as Z_{Rct} varies. Furthermore, if we find out that trend in the change of V_L by inspecting the plot, we can use it as the guide for choosing the component values of L_1 and C_1

in the next measurement. So even if we have to use random values for the components L_1 and C_1 at the beginning because of the lack of knowledge of Z_{Ant}, after several tries, we should be able to tell the general trend in the change of V_L and choose the component values of L_1 and C_1 in such a way that V_L goes higher. As more and more data points are collected and available for analysis, it becomes increasingly easier to observe the trend of the change in V_L. Eventually, this annealing process should lead us to the best matching condition, at least theoretically.

In reality, the achievable degree of matching is limited by the availability of the discrete component values of inductors and capacitors commercially available on the market. The other practical limitation to trying large number of component values is the technical difficulty in changing the tiny surface mount devices (SMD) of inductors and capacitors on the board with the extremely delicate bond wires only several millimeters away.

6.2.2 An Impedance Matching Example

In order to further illustrate the method described above, the matching of a sample antenna is given here as an example. The virtual power meter setup as described in Appendix A was used. The measurement of DC voltage V_L was taken with the on-chip antenna facing the transmitting antenna at a distance of 60cm. A total of 13 different matching conditions were tried in this example. The obtained data is shown in table 6.1 while Figure 6.5 shows the plot used for the analysis of the measurement results.

The data plot of Figure 6.5 utilizes a Smith chart for the easy presentation of a wide range of impedances. Each data point on the plot corresponds to the DC voltage measurement result under one matching condition. Its location is determined by the measured value of Z_{Rct}. The component values of L_1 and C_1 used to achieve that particular matching are printed below the

data marker. The color of the data marker represents the measured DC voltage level V_L, with red meaning higher voltages and blue for lower values.

Table 6.1 Measurement results for the impedance matching of a sample antenna

Measurement No.	L1 (nH)	C1 (pF)	Real(Z_{Rct})	Imag(Z_{Rct})	V_L (volts)
1	8.2	0	6.6	-12.2	0.92
2	15	0	9.7	23.3	1.74
3	18	0	13	58.8	2.44
4	22	0	19	105	3.92
5	27	0	30	169	3.68
6	27	1	512.8	348	1.48
7	27	2	33.4	-119.6	0.91
8	27	3	7.53	-44.6	0.35
9	18	2	34.3	68.8	2.52
10	18.0	3.0	61.40	56.00	2.06
11	22	1.5	108	163.9	4.07
12	22	0.5	31	124	4.26
13	22	0.9	45	137	4.5

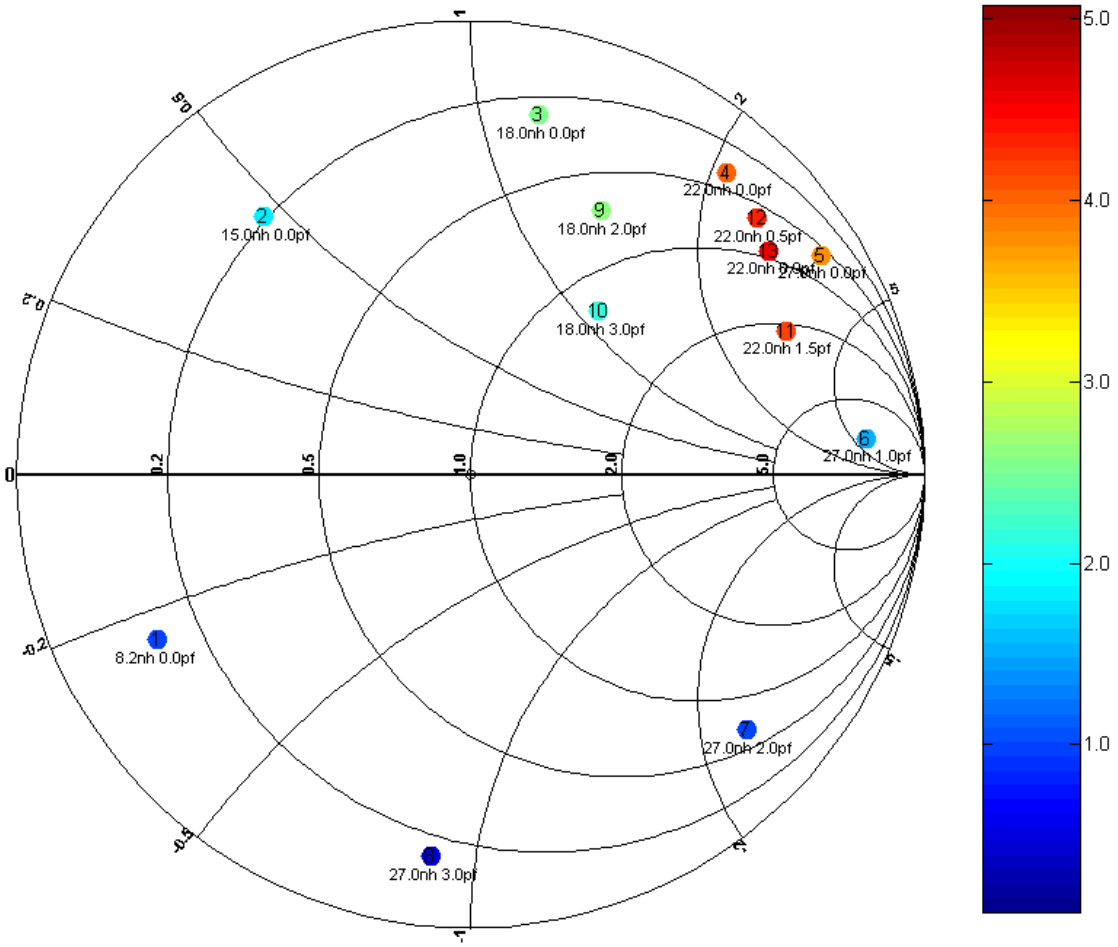


Figure 6.5 Voltage plot on Smith chart for the impedance matching of the sample antenna

As shown in Figure 6.5, the component values of L_1 and C_1 for the first 8 measurements were chosen in such a way that the impedance values spread evenly around the Smith chart. After inspecting the obtained plot, we noticed that the measured DC voltages are higher at data points 4 and 5. So in measurements No. 9, 10, and 11, we changed the component values of L_1, C_1 so that the value of Z_{Rct} is close to those for measurement No. 4 and 5. After adding them to the plot, it became even clearer that the best matching point should lie inside the triangular region enclosing data points 4, 5, and 11. This urged us to take measurements 12 and 13 as shown in the figure, from which we observed even higher voltages. As mentioned earlier, this annealing process can continue until the desired degree of accuracy is achieved. However, for the sake of argument, we will stop here and take the impedance value at data point 13 as that of Z_{Rct}.

6.2.3 Notes on the Annealing Approach

It has been shown that the annealing approach makes it possible to match the impedance of the rectifying circuit to that of the antenna even if the information about the impedance of the antenna is not available. This may not appear to be significant since the impedance of the antenna can be obtained with simulations using electromagnetic solvers like Ansoft HFSS. However, it is most likely that the simulation results for the antenna impedance don't match the real values very well due to the complexity of the on-chip antenna structure, proximate circuitry, and its small size compared to the wavelength. Often, they can only be used as a guide for the general region where the best matching is going to occur. So the annealing approach is still especially useful in order to achieve the best matching.

It has been suggested that the complex conjugate matching between Z_{Ant} and Z_{Rct} may not necessarily be the condition for getting maximum power from a receiving antenna [54]. The

reflection back from the load into the load due to impedance mismatch may cause the antenna to interact with the incoming electromagnetic wave in such a way that the power received by the antenna is increased. The annealing approach offers one way to find out the matching condition for maximum available power. The hypothesis can then be tested with the Z_{Rct} value obtained from measurement and the Z_{Ant} value from simulation, although the detailed research is beyond the scope of this dissertation.

6.3 Measurement of the Gain Pattern

The setups and the technique discussed in the above two sections are primarily for the measurement of available power from an on-chip antenna. It can be easily adapted to measure the gain pattern of the antenna. Although such a measurement will not be as accurate as one with sophisticated equipment, it at least gives us an estimation of the directive property of the antenna. On the other hand, even with the sophisticated equipment, the accuracy of the measurement may still be questionable due to the reasons given in the beginning of this chapter.

At the beginning of the gain pattern measurement, the impedance of the detector circuit is matched to that of the antenna using the annealing approach. Measurements of the available power from the antenna are taken while the orientation of the antenna is varied. Since the transmitting antenna we are using is highly linearly polarized, the gain pattern we obtain is the partial gain of the corresponding polarization.

The direct output from the measurement is the DC voltage response at the precision resistor on the RF power sensor board. The absolute values of the antenna gain can be calculated from the measurement results using the Friis transmission equation, which is

$$\frac{P_r}{P_t} = \left(\frac{\lambda}{4\pi R} \right)^2 G_{0t} G_{0r} \tag{6.1}$$

where P_t and P_r are the transmitted and the received power respectively, λ is the wavelength of the electromagnetic source, R is the separation between the two antennas, G_{0t} is the gain of the transmitting antenna, and G_{0r} is the gain of receiving antenna.

Table 6.2 shows the simulated and measured gain pattern of a sample antenna.

Table 6.2 Measured and simulated gain pattern of a sample antenna

Number of measurement	Polarization	Phi (degree)	Theta (degree)	Measured partial gain	Simulated partial gain
1	Theta	0	180	0.0224	0.039
2	Theta	180	180	0.0132	0.039
3	Phi	90	180	0.001	0.013
4	Phi	270	180	0.0012	0.013
5	Theta	0	90	0.0004	0
6	Theta	0	270	0.0007	0
7	Phi	90	90	0.0374	0.09
8	Theta	0	90	0.0062	0.068

6.4 Measurement of Antenna Efficiency

There are a number of methods for measuring antenna efficiency in the antenna literature, such as Wheeler's cap method, the Q factor method, and the directivity/gain method [56][57], among which, the Wheeler's cap method is the easiest to carry out and requires the least measurement set-ups. It was the only choice for the measurement of antenna efficiency with the available equipment.

The Wheeler's cap method is based on H. A. Wheeler's suggestion in [58] that enclosing the antenna with a conducting sphere with a radian length ($\lambda/2\pi$) in radius will eliminate the radiation resistance R_r from the input impedance without significantly changing the loss resistance R_L. So if we measure the input impedance of the test antenna with and without the cap. The efficiency of the antenna can then be calculated as

$$\eta = \frac{R_r}{R_r + R_L} = \frac{R_1 - R_2}{R_1} \tag{6.2}$$

where R_1 is the real part of the measured input impedance without the cap, R_2 is the real part of the part of the measured input impedance with the cap. However, this is the case when the loss of the antenna occurs in series with the radiation. For antennas with losses that occur in parallel with the radiation, the following equation should be used,

$$\eta = \frac{R_r \parallel R_L}{R_r} = \frac{R_1}{R_1 - R_2} \tag{6.3}$$

The experimental setup of Wheeler's cap method is shown in figure 6.7, which consists of the test antenna on a ground plane that can be completely enclosed by a metallic hemisphere. It was stated in [57] that the shape of the cap is not very important as long as it totally encloses

the antenna structure. But it was found in [53] that good contact between the cap and the ground plane, as well as centering the cap over the test antenna, was important.

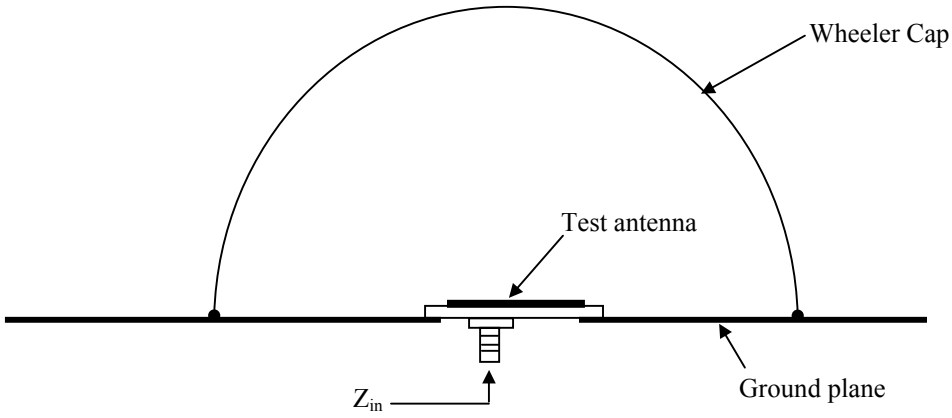


Figure 6.6 Test set-up of Wheeler cap method measurement (after D. M. Pozar [43])

Although the Wheeler's cap method was found to be of quite good accuracy in [57], there are at least two concerns for its accuracy when applied to the measurement of antennas. One is the inevitable problem of using bonding wires and connectors. The other is the complicated loss mechanism in the antennas on CMOS chips, which makes the equivalent circuit neither a series resistance-inductance-capacitance (RLC) nor a parallel RLC circuit as shown in fig. 3.3b. However, as mentioned previously, the Wheeler's cap method is the best measurement method with the currently available equipment, and was the method of choice for antenna efficiency measurements in this research.

7.0 EXPERIMENTAL RESULTS

As mentioned earlier, very few people have ever tried to integrate antennas on the same silicon substrate as the functional circuitry, especially at relatively low frequencies such as 915MHz. As a result, many of the analytical results given in previous sections have never been verified experimentally in the antenna literature. Therefore, it is necessary to design and carry out a series of experiments to verify these analytical results.

The experimental study carried out in this work can be roughly divided into three major parts. The first part mainly was done with antennas built on printed circuit boards (PCBs). It gave us a much better understanding of the operating principles of the small antennas and prepared us for the experiments with the antennas on the silicon substrates, which is part two of the experimental study. The experiments with the antennas on silicon substrates were very similar to those with PCB antennas, but they posed some challenges. First, the antenna chips had to be designed, sized, and fabricated as a part of this research. Secondly, there was a feeding problem because the antenna and the measuring are not on the same substrate. In the third part, a CMOS chip was fabricated with an energy-harvesting antenna and the power sensing circuitry (VCO) integrated on the same substrate. The chip was functional although the design was not necessarily optimal or the most desirable. However, it fully demonstrated the concept of power measuring with integrated sensor as discussed in section 6.1.2.

7.1 Experiments with PCB Antennas

The experiments with the PCB antennas were carried out using the virtual power meter[3]. The spiral antennas were similar to the ones described in section 0 except that they were fabricated on the FR-4 epoxy, instead of the silicon wafers. The target antenna (DUT) is built with the top metal layer with its last outside trace of the spiral connected to the detector circuit with a microstrip line. Since the antenna and the test circuitry are on the same FR4-epoxy substrate, there is no need for the bond wire feeds.

Obviously, the FR-4 epoxy substrates used for the PCB antennas is different from silicon. The copper used for building the metal layers on PCBs also differs from the aluminum used by most CMOS processes. However, the operational principles for the PCB antennas and the antennas built on silicon wafers should be the same. So the experiments with the PCB antennas not only helped us understand the small antennas better, but also augmented the results with antennas on silicon wafers.

As partly shown in Figure 7.1, more than twenty boards of different characteristics have been built and measured. Most of the design factors, such as the overall dimension of the antenna, the profile (shape), the metal trace width, the total conductor length, the conductor thickness, the existence, and the size of the ground plane have been experimented with using the PCB antennas. For the sake of conciseness, only the results for overall dimension, the metal thickness, and the ground plane property will be presented next. The results for antenna shape and metal trace properties are omitted since they are very similar to those obtained with antennas on silicon wafers as presented in the next section.

[3] The RF sensor board, the software program, and the annealing approach were developed as a part of this research.

Figure 7.1 The PCB antennas (boards) used in the experimental study

7.1.1 Effects of Antenna Size

Four antennas of a square profile but different sizes as shown in Figure 7.2 have been constructed to study the effects of overall antenna sizes. The impedance of the rectifying circuit Z_{Rct} has been matched to each of the four antennas using the annealing approach described in section 6.2. The DC voltage response measured on the precision resistor under the best matching condition is plotted in Figure 7.3. The impedance of the detector circuit at which the best matching with the antenna occurs is listed in Table 7.1.

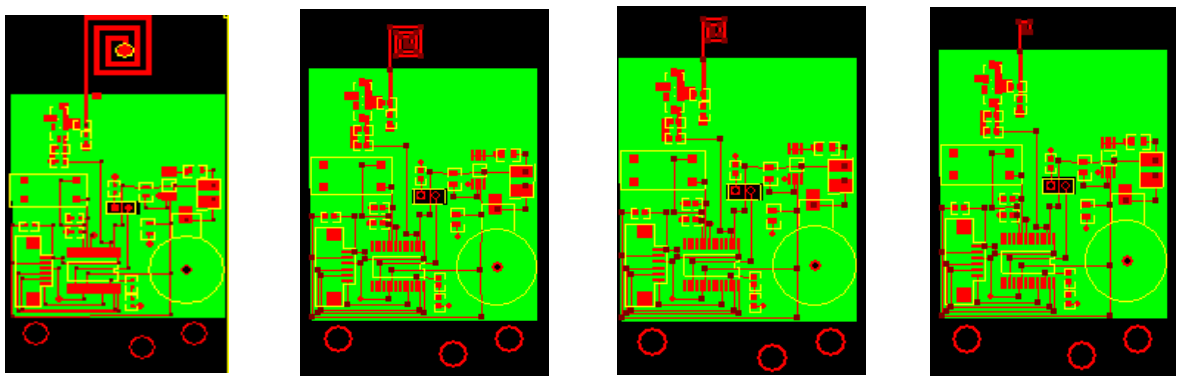


Figure 7.2 Square PCB antennas with different sizes

Table 7.1 Impedance matching for antennas of different shapes

Antenna name	Inductor L1	Capacitor C1	Resistance	Reactance
A	27.0nH	2.4pF	16Ω	-79Ω
B	39.0nH	0pF	440Ω	790Ω
C	39.0nH	0.2pF	1500Ω	-440Ω
D	39.0nH	0.3pF	675Ω	-830Ω

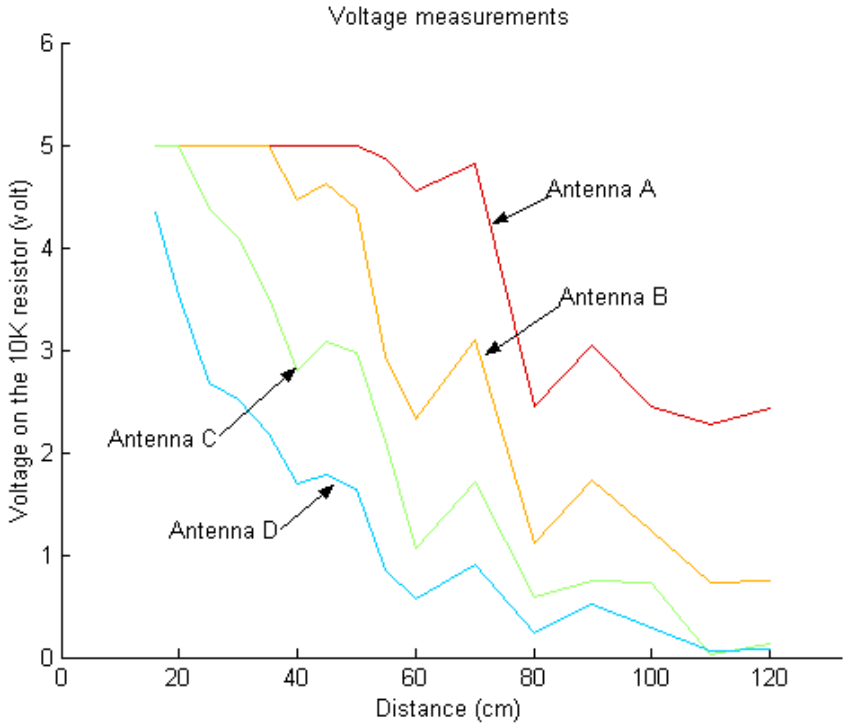


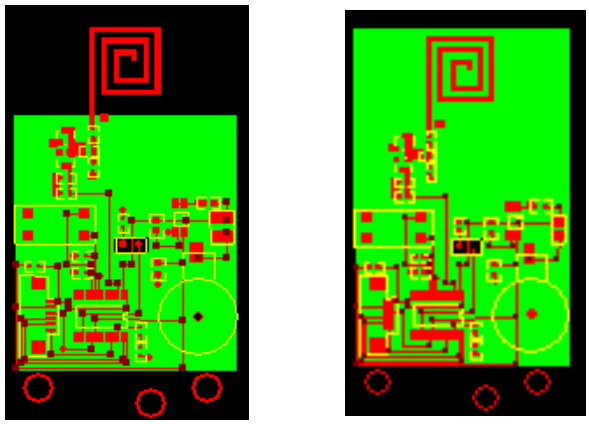
Figure 7.3 DC voltage response of the four square PCB antennas with different sizes

As we can see from Table 7.1, Z_{Rct} under the best matching condition is much higher when the antennas are smaller in size. This suggests that the input impedance Z_{Ant} of an antenna with smaller size is generally higher since the Z_{Rct} is supposed to be the complex conjugate of Z_{Ant} when they are matched. The low voltage levels observed for the smaller antennas in Figure 7.3 can be partially attributed to the difficulty of matching the higher impedance of the antenna as a slight change in the component value can lead to a major difference in Z_{Rct}. But the major reason is the one given in section 2.3.1, which is the reduced radiation efficiency of an antenna as antenna size drops.

It is easy to notice that the DC voltage response does not drop monotonously as the antenna is moved farther away from the transmitting antenna. The is mainly due to the fact that the electromagnetic wave reflected by the walls and tables around the measurement setup can easily create a zigzagged pattern of field strength along the path. Although the use of an anechoic antenna chamber can make the phenomenon disappear, it is not critical in the experimental study of this research because we are only interested in the relative scales of the voltage responses when we try to compare the performance of the antennas.

7.1.2 Effects of the Ground Plane

As mentioned in section 4.1.1, a closely placed ground plane behind the antenna structure can lead to extraordinarily low radiation efficiency. Since the thickness of the PCB or the silicon wafer is usually fixed for a given process, it is very likely that the ground plane is not located at the proper position if we simply put it on the back of the board or the wafer. At the frequency of 915MHz, it is usually too close because the thickness of a normal PCB is on the order of 1mm to 2mm, which is less than $0.006\lambda_0$.



Antenna A
(No ground plane)

Antenna B
(With ground plane)

Figure 7.4 Antennas with and without a ground plane

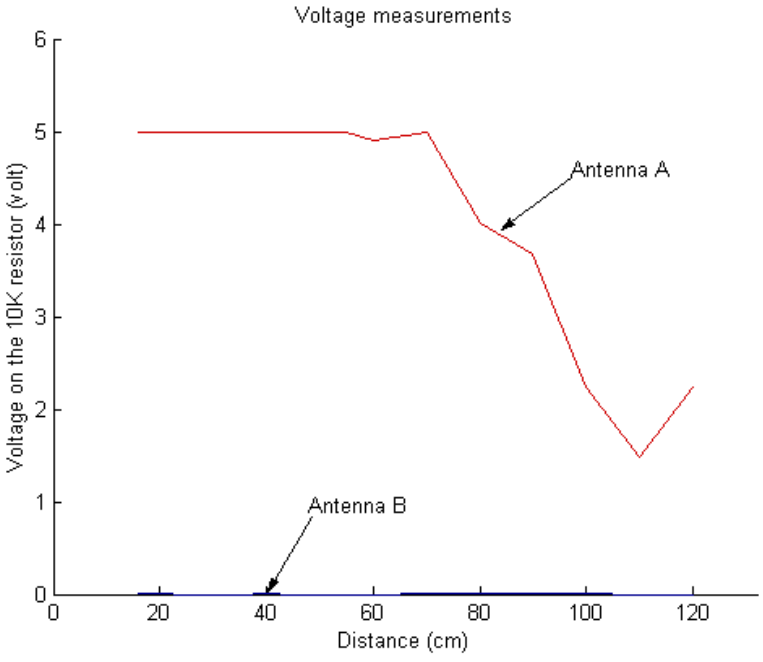
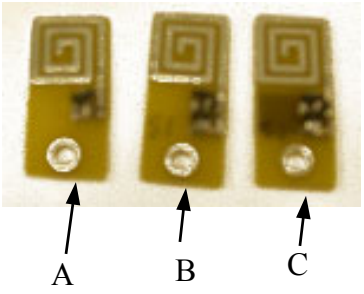


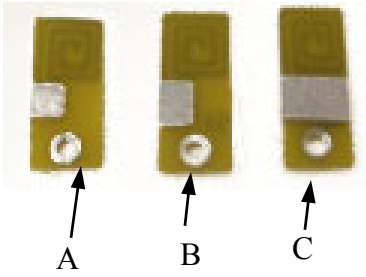
Figure 7.5 DC voltage responses of antennas with and without a ground plane

The experiments with the antennas shown in Figure 7.4 provided provisions for the testing of such effects. The two spiral antennas have exactly the same layout except that antenna B is covered by the ground plane on the back of the board. The DC voltage responses of the two antennas are shown in Figure 7.5. It is clear from the voltage response results that the ground plane is not a desirable feature for the PCB implementation. Because the thickness of a normal silicon wafer is smaller than a PCB, a ground plane directly put at the back of the antenna chip is expected to be even more detrimental.

However, some form of a ground plane at the proximity of the antenna is necessary to form the microstrip line feeding to it. The set of antennas shown in Figure 7.6 were constructed to study the net effect of such a ground plane. In order to reduce the size of the ground plane, a light emitting diode (LED), is utilized to indicate the power available from the antenna. This is a much more accurate measurement than the method with an integrated VCO. The impedance matching components are optimized so that the LED lights up at a distance as far from the transmitting antenna as possible. The distance is thus a surrogate for energy.



(a) Top side view



(b) Back side view

Figure 7.6 Antennas with proximate ground planes

It was observed that the LED lights up roughly at the same maximum distance of 70cm, which suggests that the maximum available power from the antenna is almost the same. However, as we can see from Table 7.2, the values of the matching components required to achieve the largest distances are different among the three boards. This suggests that the size of the approximate ground plane has an effect on the input impedance of the antenna.

Table 7.2 Impedance matching for antennas of different shapes

Antenna Name	Inductor L1	Capacitor C1
A	8.2nH	1.0pF
B	39nH	0pF
C	27nH	0.5pF

7.2 Experiments with Discrete Antennas on Silicon Wafers

The factors that we tried to study with the discrete antenna chips fabricated on silicon wafers include the antenna profile (shape), the geometric properties of metal traces for spiral antennas, and the thickness of the metal layer. The parameter we are most interested in, *i.e.*, the available power from the various antennas, is measured with the virtual power meter setup as described in section 6.1.3 and Appendix A.

The antenna chips were fabricated as a part of this research. A complete antenna chip fabrication process was developed as described in appendix B. More than 200 antenna chips were fabricated for the experimental study of this research and other related researches. Due to the limited fabrication capabilities available, the metal structures of the antennas were built directly on top of the silicon wafers. Although this makes the antenna structure unnecessarily

close to the substrate and possibly reduces its efficiency, it will have minimal effects on the validity of the obtained results since it is the relative changes that are being compared.

The picture of a wafer of antenna chips is shown in Figure 7.7. The layout of the photomask used in the fabrication is shown in Figure 7.8. It was designed with the Cadence Virtuoso layout editor [59]. A SKILL script has been created to facilitate the drawing of the spiral antennas. A total of 52 antenna layouts were created. Their physical dimensions are given in Table 7.3.

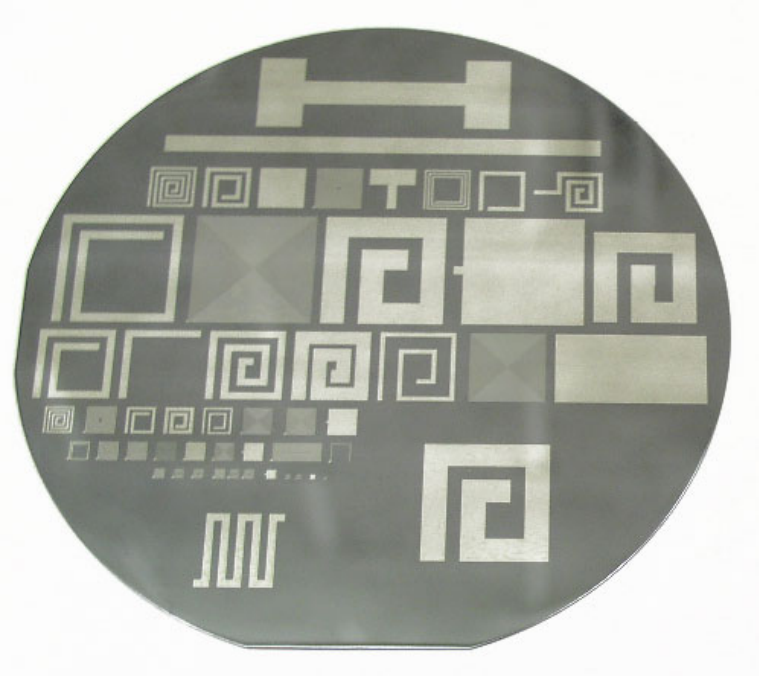


Figure 7.7 A complete wafer of antenna chips

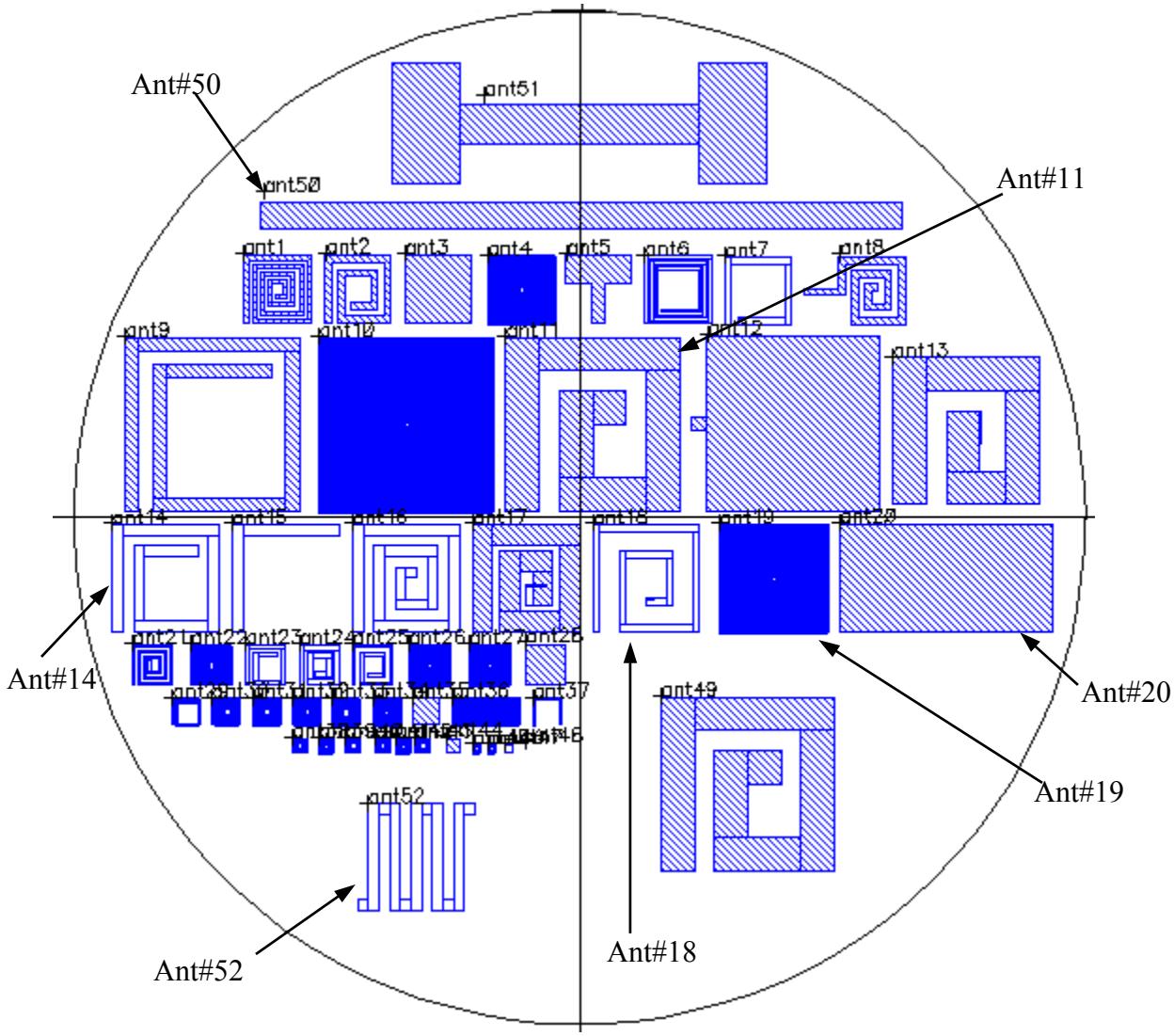


Figure 7.8 Layout of the photomask for antenna chip fabrication

Table 7.3 Physical dimensions of the antennas on silicon wafers

Antenna #	Side Length (μm)	Side Width (μm)	Trace Width (μm)	Trace Spacing(μm)	Number of turns	Total Length (μm)	Note
1	5000	5000	300	300	4	46100	
2	5000	5000	500	500	2	27500	
3	5000	5000					patch
4	5000	5000	60	60	20	212740	
5	5000	5000					T-shape
6	5000	5000	200	200	3	47800	
7	5000	5000	500	500	1	17500	
8	5000	5000	500	500	2.5	29500	side-feed
9	13000	13000	1000	3000	1.5	57000	
10	13000	13000	10	10	162	4237900	
11	13000	13000	2500	1500	1.5	49500	
12	13000	13000					patch
13	11000	11000	2500	1500	1.3	37100	
14	8000	8000	800	800	1.5	37600	
15	8000	8000	800	800	0.5	15200	
16	8000	8000	800	800	2.5	47200	
17	8000	8000	1500	500	2	35500	
18	8000	8000	500	1500	2	42500	
19	8000	8000	10	10	200	3207990	
20	8000	16000					patch
21	3000	3000	200	200	3.5	25000	
22	3000	3000	100	100	7	47500	
23	3000	3000	300	300	1.5	14100	
24	3000	3000	400	200	2	15800	
25	3000	3000	200	400	2	17200	
26	3000	3000	10	10	75	452990	
27	3000	3000	20	20	37.5	227980	
28	3000	3000					patch
29	2000	2000	100	100	1.5	10700	
30	2000	2000	100	100	5	21900	
31	2000	2000	50	50	10	41950	
32	2000	2000	20	80	10	43120	
33	2000	2000	80	20	10	40780	
34	2000	2000	10	10	50	201990	
35	2000	2000					patch
36	2000	5000	50	50	10	101950	
37	2000	2000	50	50	0.75	5950	
38	1000	1000	50	50	5	10950	
39	1000	1000	10	10	20	48790	
40	1000	1000	20	20	10	24780	
41	1000	1000	50	50	5	10950	same as 38
42	1000	1000	10	10	20	48790	same as 39

Table 7.3 (continued)

43	1000	1000	20	20	10	24780	same as 40
44	1000	1000					patch
45	500	500	10	10	12.5	12990	
46	500	500	10	10	10	12390	
47	500	500					
48	250	250	10	10	6	3350	
49	13000	13000	2500	1500	1.5	49500	same as 11
50	2000	48000					monopole
51	8000	27800					H-shaped
52	8000	8000			2		Meander

7.2.1 Effects of Overall Size

The effects of overall antenna size were analyzed again with the five antennas, *i.e.* ant#11, ant#16, ant#2, and ant#24, as shown in Figure 7.9. The detailed geometric parameters are summarized in Table 7.4. The DC voltage response measured on the precision resistor under the best matching condition is plotted in Figure 7.10.

Figure 7.9 Four antennas on Silicon wafers with different sizes

Table 7.4 Sizes of the four antennas shown if Figure 7.9

Antenna Number	Total Trace length	Physical Area
11	49.5mm	169mm^2
16	47.2mm	64 mm^2
2	27.5mm	25 mm^2
24	15.8mm	9 mm^2

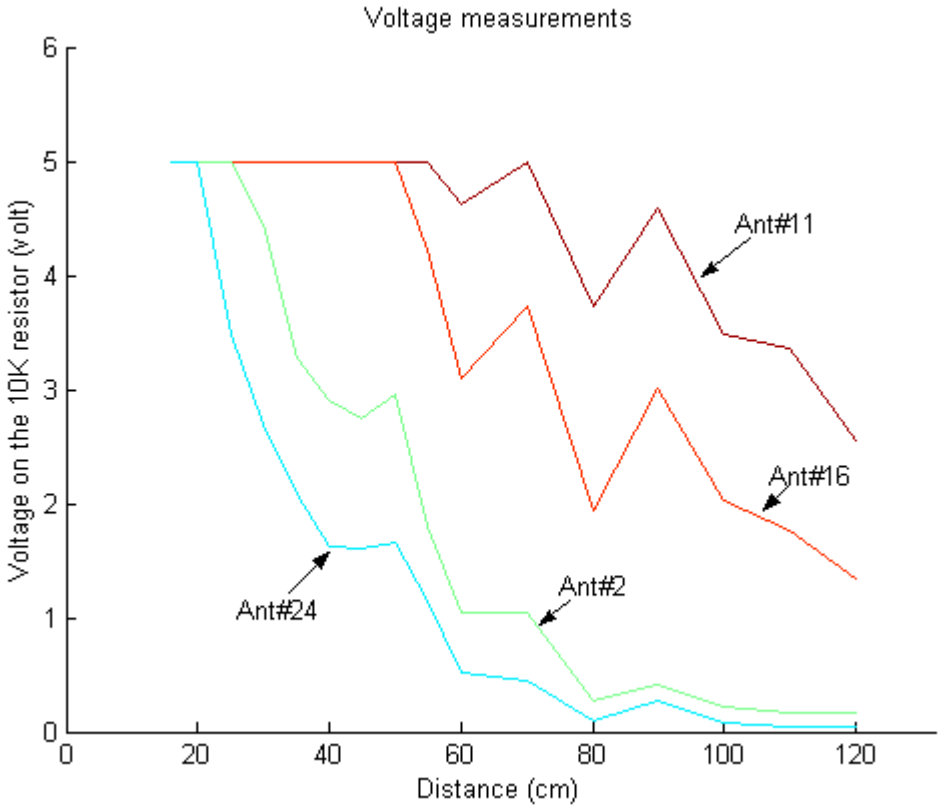


Figure 7.10 Voltage responses of the antennas with different sizes

As we can see from the results, the relationship between the overall antenna size and the voltage response is the same as that obtained with PCB antennas in section 7.2.1. As the antenna become smaller, the voltage response becomes lower. Although this is not a strict proof, the experimental results also show that the bond wire and the circuitry on the RF sensor board don't have a significant effect on the available power from the antenna.

7.2.2 Effects of Antenna Profile

The distinct effects of profile (shape) on the available power from an antenna can be analyzed with four configurations, (1) a monopole antenna (part of ant#50), (2) a patch antenna (half of ant#20), (3) a meander antenna (ant#52), and (4) a spiral antenna (antenna #16). The four antennas have the same length of 8mm. The patch, the meander, and the spiral antennas have the same width of 8mm. The width of the monopole antenna is 2mm. They were mounted on the same power sensor board using rubber cement and measured in turn. A picture of the four antennas is shown in Figure 7.11.

The voltage responses of the four antennas under the best matching conditions are shown in Figure 7.12.The impedance of the detector circuit at which the best matching was achieved is listed in Table 7.5, together with the matching component values.

Figure 7.11 Four antennas with different shapes

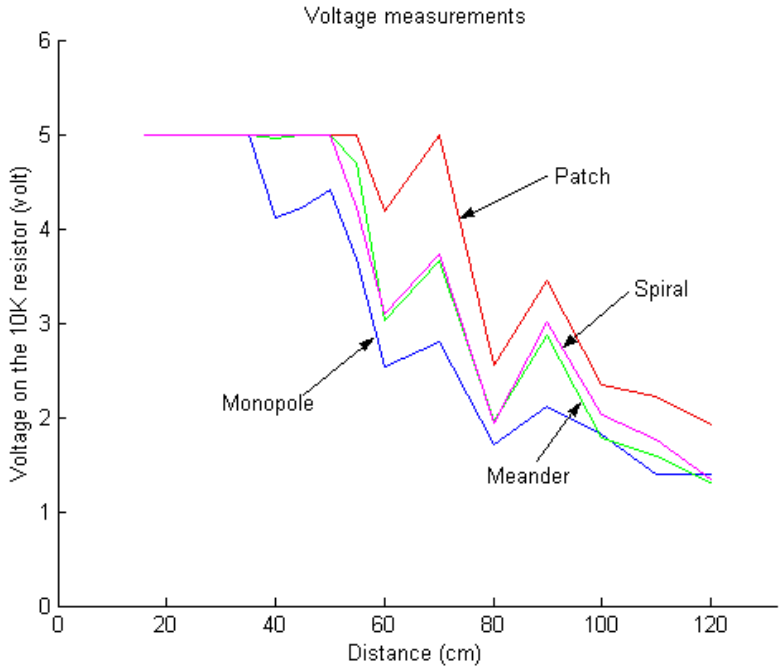


Figure 7.12 Voltage responses of antennas with different shapes

Table 7.5 Impedance matching for antennas of different shapes

Antenna Type	Inductor L1	Capacitor C1	Resistance	Reactance
Monopole	33nH	0.1pF	250Ω	565Ω
Patch	33nH	0pF	108Ω	389Ω
Meander	27nH	0.5pF	132Ω	325Ω
Spiral	27nH	0.7pF	207Ω	374Ω

As we can see from Figure 7.12, the patch antenna has the highest available power, and thus the largest gain. But a single patch antenna is usually linearly polarized, which is disadvantageous for most energy-harvesting applications due to the lack of a fixed orientation environment. The voltage responses of the meander antenna and the spiral antenna are very similar, suggesting that they have similar gains. Since the spiral antenna is not strictly linearly polarized and has some gain in the cross polarization, its voltage response is expected to improve if a circularly polarized RF source is used. The monopole antenna has the lowest voltage response, but it should be remembered that it is narrower than the other three antennas and thus has less die area.

7.2.3 Effects of Metal Trace Properties

Within the same area, i.e., the same overall dimension or size, the metal traces of the spiral antennas can have different numbers of turns, and/or different metal trace width and spacing. Six spiral antennas with the same overall dimension but different metal trace properties, *i.e.*, ant#14, through ant#19, have been used to study the effects of metal trace properties. As we

can see from the detailed parameters given in Table 7.3, ant#14, ant#15, and ant#16 have the same trace width and spacing but different numbers of turns. Ant#16, ant#17, and ant#18 have similar total trace length but different trace width and spacing. Ant#19 has the minimal trace width and spacing but largest total trace length. The six antennas are shown in while the DC voltage responses of the antennas under best matching conditions are plotted in Figure 7.14. The impedance of the detector circuit under which the best matching was achieved is listed in Table 7.6.

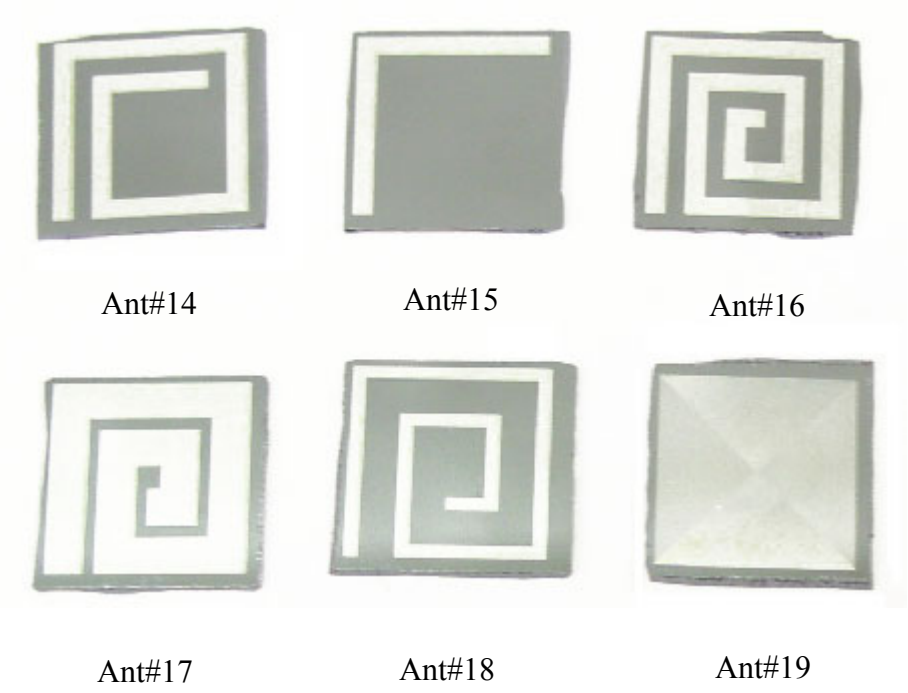


Figure 7.13 Antennas with different metal trace properties

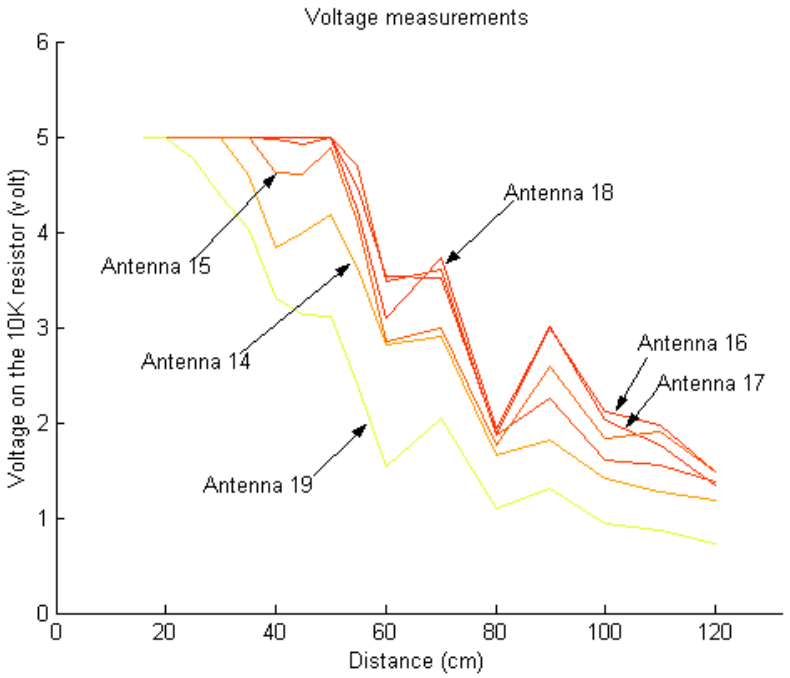


Figure 7.14 DC voltage response of antennas with different metal trace properties

Table 7.6 Impedance matching for antennas with different trace properties

Antenna Number	Total Trace Length	Inductor L1	Capacitor C1	Resistance	Reactance
14	37.6mm	27nH	0.8pF	307Ω	415Ω
15	15.2mm	27nH	0.5pF	132Ω	325Ω
16	47.2mm	27nH	0.7pF	207Ω	374Ω
17	35.5mm	27nH	0.5pF	132Ω	325Ω
18	42.5mm	27nH	0.6pF	150Ω	350Ω
19	320.8mm	33nH	0.1pF	250Ω	565Ω

As we can see from the results, the DC voltage responses for ant#14 through #16 increase in the order of their total trace length. However, larger total trace length alone does not make a better antenna because ant#19 actually has the lowest voltage response despite its much longer trace. The reason for this obvious degradation in performance can be attributed to the increased conductor losses as the metal trace becomes too narrow.

The difference in the voltage responses of antennas #16 through #18 is subtle. But it can be argued that the voltage response of antenna#18 is a little lower than those of the other two. This suggests that the metal trace width and spacing don't have a significant effect on the gain of antenna as long as the trace is not too narrow. Although the impedance of the detector circuit for achieving the highest voltage response for the four antennas differs significantly, the values of the matching components are very close. This is another indication of the difficulty in achieving optimal impedance matching to the small antennas.

7.2.4 Effects of Metal Thickness

As pointed out in sections 0 and 5.3, the finite conductivity of the metal used for building the antenna structure leads to losses, and thus reduces the radiation efficiency. Three wafers with the same geometric pattern but different metal thickness have been fabricated to verify this effect. Antennas with pattern #11 in the photo mask have been measured with the voltage responses shown in Figure 7.15. The thickness of aluminum layers for antennas A, B, and C is 0.24μm, 0.16μm, and 0.08μm, respectively.

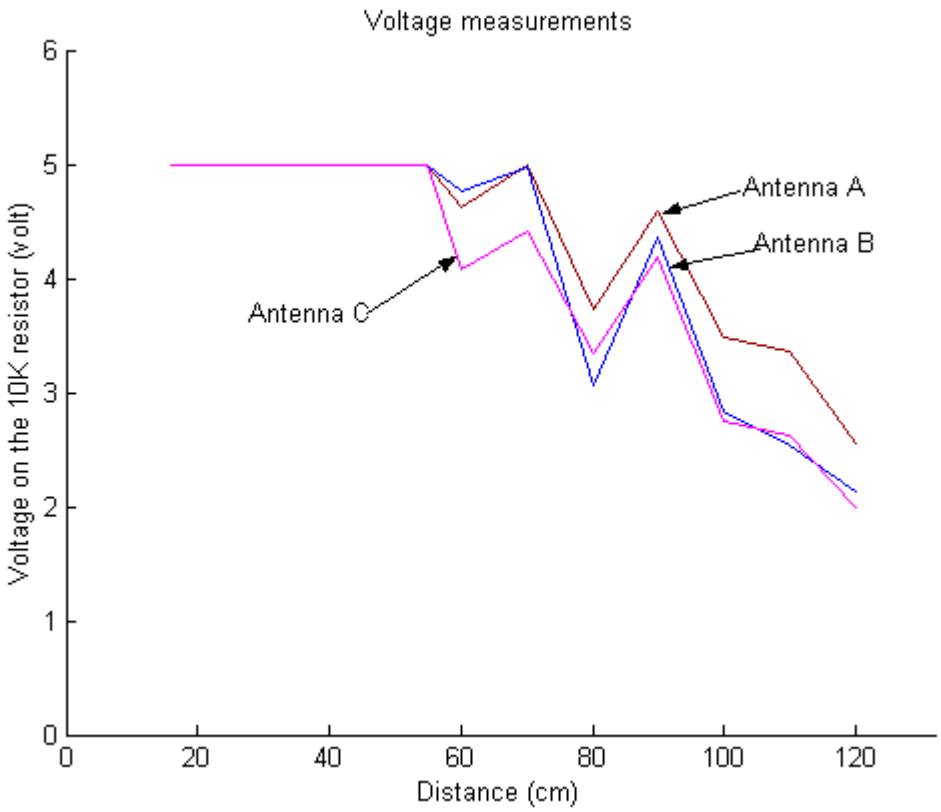


Figure 7.15 Voltage responses of antennas with different metal thickness

It is obvious from Figure 7.15 that the antenna with thickest metal layer has the highest voltage response. Because everything else is the same for the three antennas, we conclude that the antenna with thicker metal layer has higher radiation efficiency. However the gain from the increase in metal thickness is expected to diminish as the thickness approaches the skin depth. Interestingly, it was found in similar experiments with PCB antennas that thinner metal traces actually lead to higher voltage responses. But the metal used on the PCB antennas is copper, instead of aluminum, and the thickness of the PCB antenna is in the range of 50~230μm, which is much larger than the skin depth of 2.2μm at the frequency of 915MHz for copper.

7.3 A CMOS Chip with an Integrated VCO

A CMOS chip implementing the idea presented in section 6.1.2 was fabricated with the AMI_ABN process through the service of MOSIS. AMI_ABN is a double-poly, double-metal process with a minimum gate size of 1.5μm. Its layer map is shown in Figure 2.1. The physical layout of the chip is shown in Figure 7.16. The size of the chip is 2.2×2.2 mm^2.

The energy-harvesting antenna is a square spiral built with the 1μm thick top metal layer. It has 23.5 turns and a side length of 1560μm. The metal trace width is 17.8μm while the trace spacing is 13.6μm. The total length of the metal traces is about 78000μm ($\lambda_0/4$ at 915MHz)

The RF-DC converter is a voltage doubler circuit as shown in Figure 6.4. The capacitors were built with the two poly-silicon layers available in the process. The capacitance is designed and measured to 20pF. The two diodes are based on the Schottky barrier formed between the Aluminum metal layer 1 and the *n*-well. Its I-V curve is shown in Figure 7.17.

The VCO is of the so-called current starving type [60]. The measured relationship between the control voltage and the frequency of the output signal is shown in Figure 7.18.

The RFID functional circuitry is composed of a 125MHz oscillator and a digital block that continuously shifts out an 8-bit ID code in serial. The transmitting antenna is another spiral antenna with a side length of 610μm.

A few pads were included on the chip so that each functional block can be tested individually. As mentioned in the above description, both the voltage doubler and the VCO work. However we were not able to detect the signal from the chip when it is left in the electromagnetic field by itself.

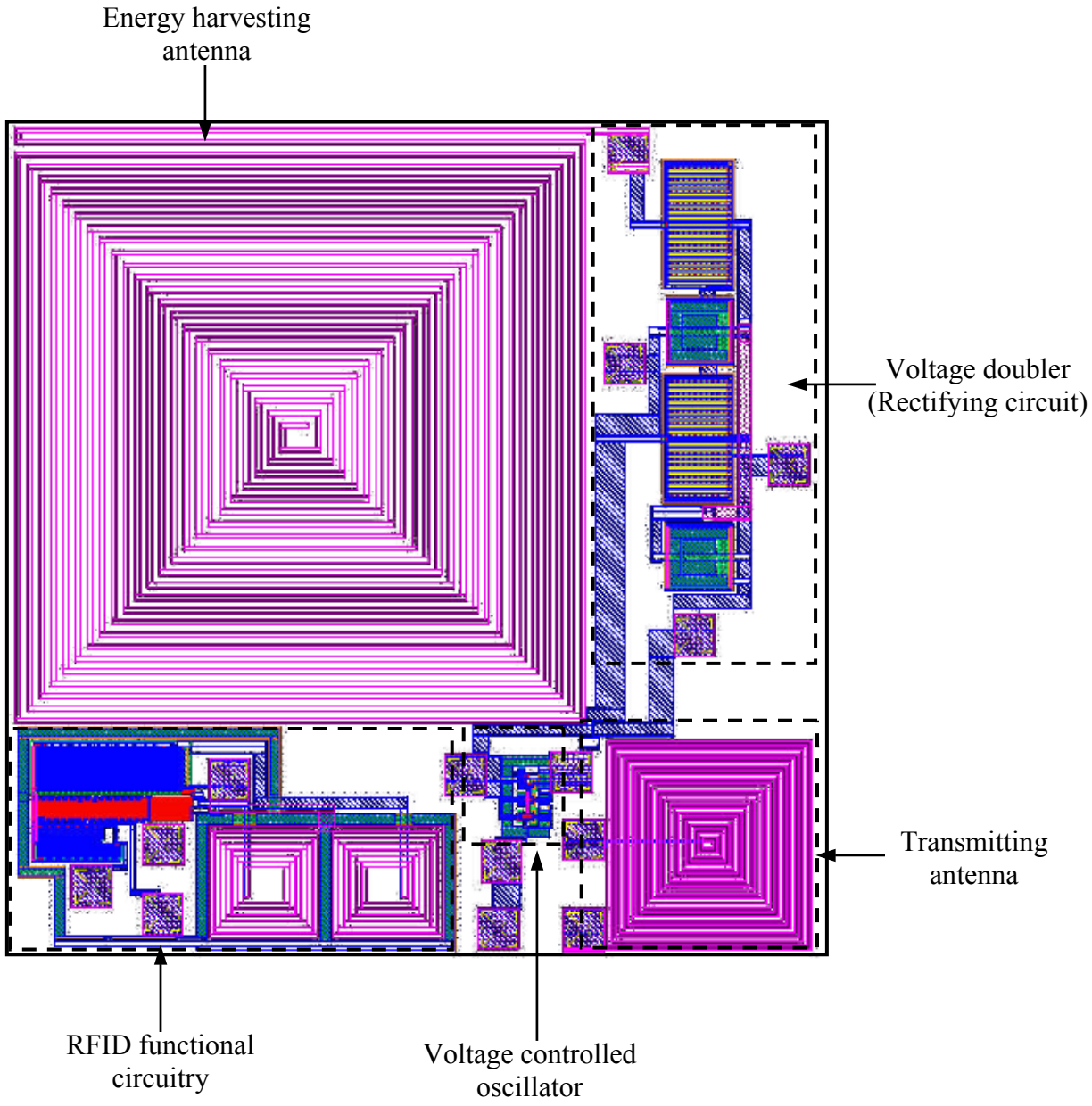


Figure 7.16 Device layout of the testing chip with integrated antennas and a VCO

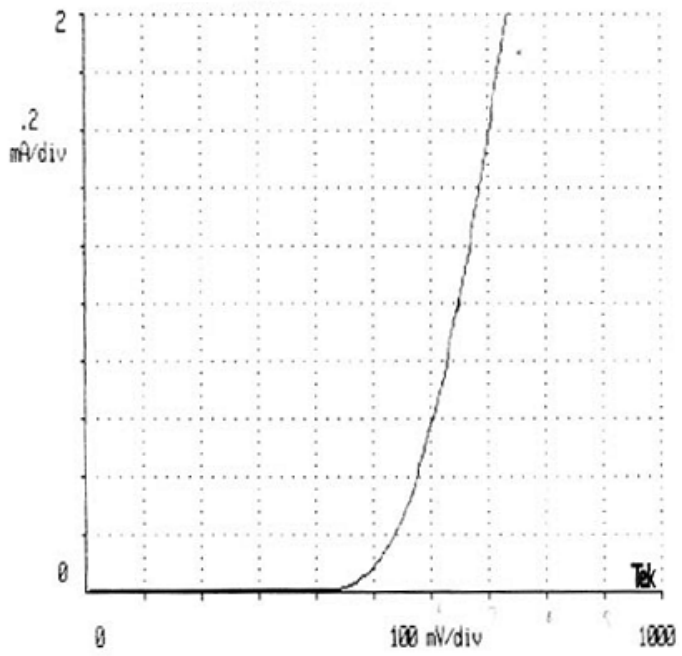


Figure 7.17 I-V curve of the Schottky diode on the testing chip

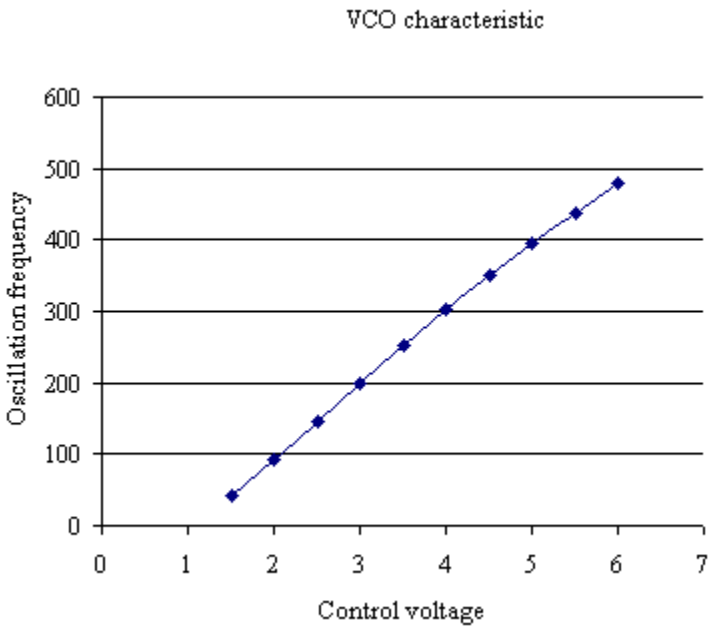


Figure 7.18 Frequency vs. voltage plot for the VCO

There are several possible reasons. First of all, the overall size of the spiral antenna may well be too small to harvest enough power for the circuitry on the chip. Secondly, with the resistivity being 2 Ω-cm, the silicon wafers used in the AMI_ABN process are so lossy that the antenna likely has an extremely low efficiency. The third reason could be the existence of impedance mismatch between the antenna and the rectifying circuit. So it is desirable to fabricate one or even more chips with larger antenna size, using high-resistivity wafers, but the high costs of both time and research funds were prohibitive. Finally, the sensitivity of the receiver in our laboratory lab may be insufficient to detect the weak signal from the VCO. However, the alternative setup with the virtual power meter and RF sensor board was quite satisfactory to accomplish the goals of the dissertation.

8.0 SUMMARY

In this dissertation, the fundamental parameters of the antennas on CMOS ICs for energy-harvesting applications were defined. The desired characteristics of such antennas were identified and summarized with the introduction of the concept of maximum effective area in section 1.2.5.

In section 2, the antenna environment on a typical CMOS process was reviewed. It has been shown with simulation results in this dissertation that the stringent restriction on the sizes of the antennas and the lossy nature of the silicon substrates used for CMOS IC fabrication pose major challenges for the integration of antennas on CMOS ICs. It has likewise been shown that the conductive silicon substrates make it difficult to apply the concept of effective permittivity and match the impedance between the antenna and the load.

Three popular numerical techniques for the full-wave analysis of antennas, i.e., MoM, FDTD, and FEM, have been reviewed and compared in section 3. It was found that MoM is not suitable for the simulation of the antennas studied in this research because of the assumption that the dielectric layers and the ground plane extend infinitely. The available FDTD package is underpowered because it lacks the capability of adaptive meshing, which is imperative to handle the largest aspect ratios of the on-chip antennas. It is concluded that FEM is more suitable for the analysis of antennas on CMOS ICs than the other two methods. The simulation results from the FEM electromagnetic solver, Ansoft HFSS, were found to be in good agreement with those from measurements. A lumped circuit model for the spiral antennas on CMOS ICs has also been proposed and verified.

In section 4, several antenna structures, which include the patch antenna, the loop antenna, the dipole antenna, the meander antenna, and the spiral antenna, have been compared for their suitableness of implementation on CMOS ICs. It has been shown that the spiral antenna is the most promising candidate. The details of the feeding and ground plane structure of the spiral antenna were then discussed. A heuristic design method for the design of the spiral antennas has been developed and illustrated with an example.

The factors that need to be considered for choosing an optimal operational frequency were discussed in section 5.1. The various techniques for reducing the negative effects of the conductive substrates, such as selective etching, wafer thinning, use of PGS, and increasing inter-metal dielectric thickness, have been identified in section 5.2. The effectiveness of the method of increasing inter-metal dielectric thickness was verified with full-wave simulations.

Section 6 is on the problems, challenges, and setups for measuring the antennas on CMOS ICs. The advantages and disadvantages of three measurement setups were discussed. The carefully designed and fully functional measurement system *i.e.*, the Virtual Power Meter, requires no cable connection and offers a convenient means of changing the impedance matching condition between the antenna and the detector circuit. The annealing approach I developed in the research made it possible to achieve the optimal matching condition without prior knowledge of the impedance values. It played a key role in the successful experimental study.

In section 7, the experimental results with antennas built on both PCBs and silicon wafers were presented. Various design factors such as the overall size, the shape, the metal trace properties, the existence, and the size of the ground plane were analyzed with the experimental results. It was confirmed that the maximum effective area of an antenna drops as the size of the antenna becomes smaller. It was also shown that properly designed spiral antennas are good

candidates for the on-chip energy-harvesting application. It was also shown that a ground plane behind the antenna is not a desired feature for the antennas on CMOS ICs at the chosen frequency of 915MHz. It has likewise been demonstrated that the proximate ground for antenna feeding has an effect on the impedance matching but does not have much influence over the gain. The experiments with three antennas of different metal thickness confirmed its effect on antenna radiation efficiency. A CMOS chip with an integrated energy-harvesting antenna and a VCO has been designed, fabricated, and tested. It demonstrated the functionality of concept of using VCO as a power sensor.

9.0 CONCLUSIONS

This dissertation is the first comprehensive study on the subject of antennas on CMOS integrated circuits for energy harvesting applications to appear in the antenna literature. All the important aspects of the analysis, design, optimization, and measurement of the on-chip antennas have been looked into by collecting the relevant previous knowledge and extending it to the special environment on CMOS ICs. Based on the extensive analysis and experiments carried out in this research. We draw the following conclusions:

1, It is challenging to build antennas on CMOS ICs mainly due to the stringent restriction on antenna size and the lossy nature of the silicon wafers used.

2, Properly designed spiral antennas are good candidates for the on-chip energy harvesting applications. The ground plane behind the antenna is not a desired feature at the frequency of 915MHz with normal silicon wafer thickness.

3, The finite element method is the most suitable numerical method for the full-wave analysis of antennas on CMOS ICs. The simulation results from an FEM electromagnetic solver are in excellent agreement with the experimental results despite the challenges brought by the complicated material and geometric properties of the antennas.

4, There are many ways to improve the performance of the antennas. Increasing metal thickness helps to increase the efficiency of the antenna when the metal thickness is less than the skin depth.

5, The virtual power meter developed in this research is an extension to the more traditional measurement instrumentation in that no cable connection to the DUT is

necessary and it is capable of measuring the available power from antennas with arbitrary impedance accurately.

6, The annealing approach to the impedance matching has been shown to be effective and crucial to the accurate impedance matching and the measurement of the performance of antennas on CMOS ICs. This method can also be extended to other cases where the impedance of the load is hard to determine in advance.

The research of integrating antennas, especially antennas for energy-harvesting applications, on the same silicon substrate as the functional circuitry is a new field that is just emerging. It is unlikely to have each aspect of this broad and new area covered in this pioneering work. As an old Chinese saying goes, we are showing off the bricks in the hope to see other people bring out their jades. The directions of future research I suggest include:

1. A systematic study on the optimal operating frequency for a given application.
2. A thorough investigation of the effects of metal thickness, especially when it is close to or greater than the skin depth.
3. A testing chip with an integrated power sensor built with a suitable CMOS process that is fully functional.
4. A fully functional RFID or ARS chip with an integrated antenna.

APPENDIX A

The Virtual Power Meter

The virtual power meter is a system developed for the measurement of available power from small antennas. As we can see from the schematic and the photo picture shown in Figure A.1. As we can see from the figure, the system is composed of three major blocks.

1, The transmitter, which includes an RF signal generator with an output power level of 5W at 915MHz and a linearly polarized patch antenna with directivity of about 6.

2, The RF power sensor board, which hosts the antenna under test (DUT), measures the available DC power, and sends out the data through an IR transmitter.

3, The data gathering and processing unit, which includes an IR receiver and a personal computer.

When the DUT is mounted on the RF power sensor board and put in the electromagnetic field created by the transmitting antenna, the RF power received by the DUT is converted into DC voltage on a precision resistor using a detector circuit. This DC voltage level is then digitized, framed, and transmitted through the IR link to the PC. Using previously obtained calibration data for the RF power sensor board, the DC voltage is converted into equivalent RF power available from the antenna. The results can then be displayed on the screen and saved.

A.1 The RF power sensor board

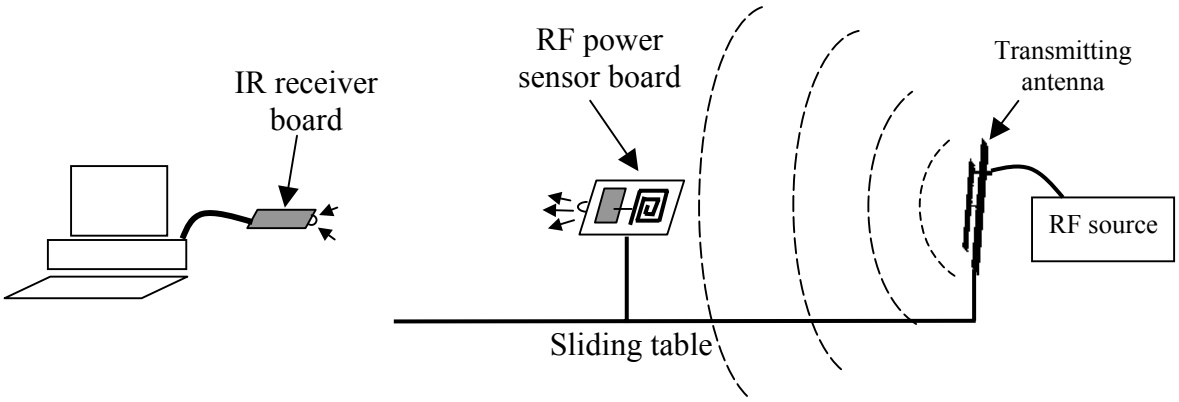
Besides the antenna and the detector circuit, the RF sensor board also holds the impedance matching network, a PIC micro controller, an IR transmitter, and a small battery. The schematic of the board is shown Figure A.2.

The PIC micro controller controls the operation of the board. It also has an integrated 12-bit A/D converter, which has been used for digitizing the DC voltage on the precision resistor. A voltage booster chip has been used to get the necessary operational voltage of 5V for the PIC from the battery, which has an output voltage of 1.5V. The details of the impedance matching network are given in section 6.2.2.

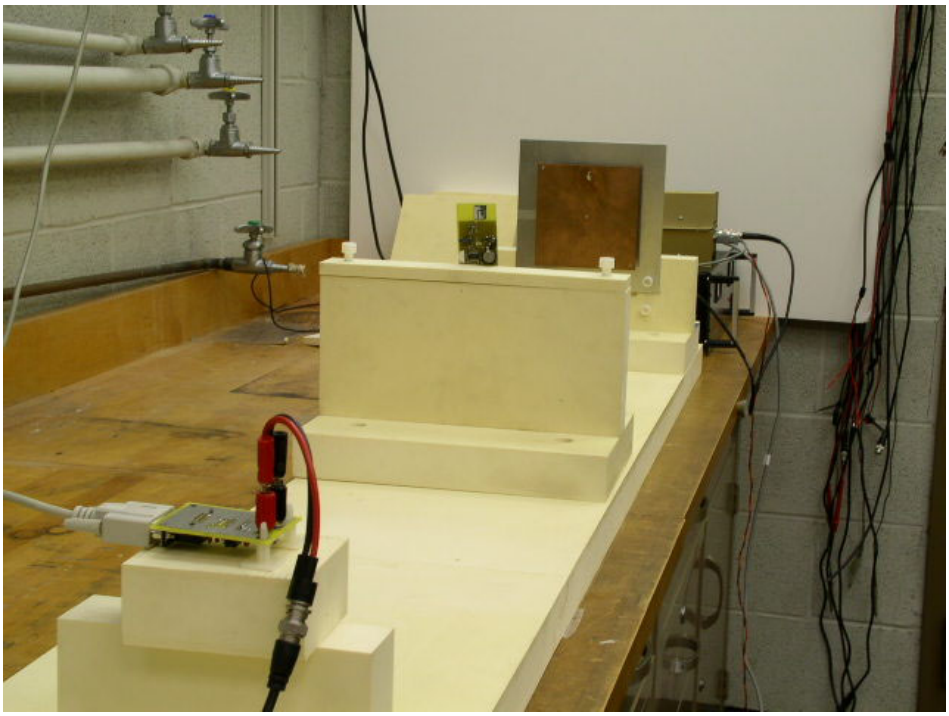
A.2 The software program

A software program has been developed to collect and analyze the measurement data using MATLAB. It has an easy-to-use graphical user interface (GUI) as shown in Figure A.3. The functions for the controls on the GUI should be easy to tell from their names.

The program can be run in two modes: the free run mode and the power-distance measurement mode. In the free run mode, the VPM is very similar to a conventional power meter, and it continuously measures and displays the RF power received by the DUT. The power-distance measurement mode is specifically designed to analyze the relationship between the RF power received by DUT and the distance from the transmitting antenna. Once in this mode, the computer is in control of the measurement process and asks for the user to move the DUT to the predetermined distances one by one. A curve of the RF power level vs. the distance can be plotted and saved automatically after the measurements at all the distances are done. An example of such curves is shown in Figure A.4. A Smith chart plot of the previous measurement results as shown in Figure 6.5 is also generated automatically.



(a) Schematic of the virtual power meter



(b) A photo picture of the virtual power meter

Figure A.1 The virtual power meter

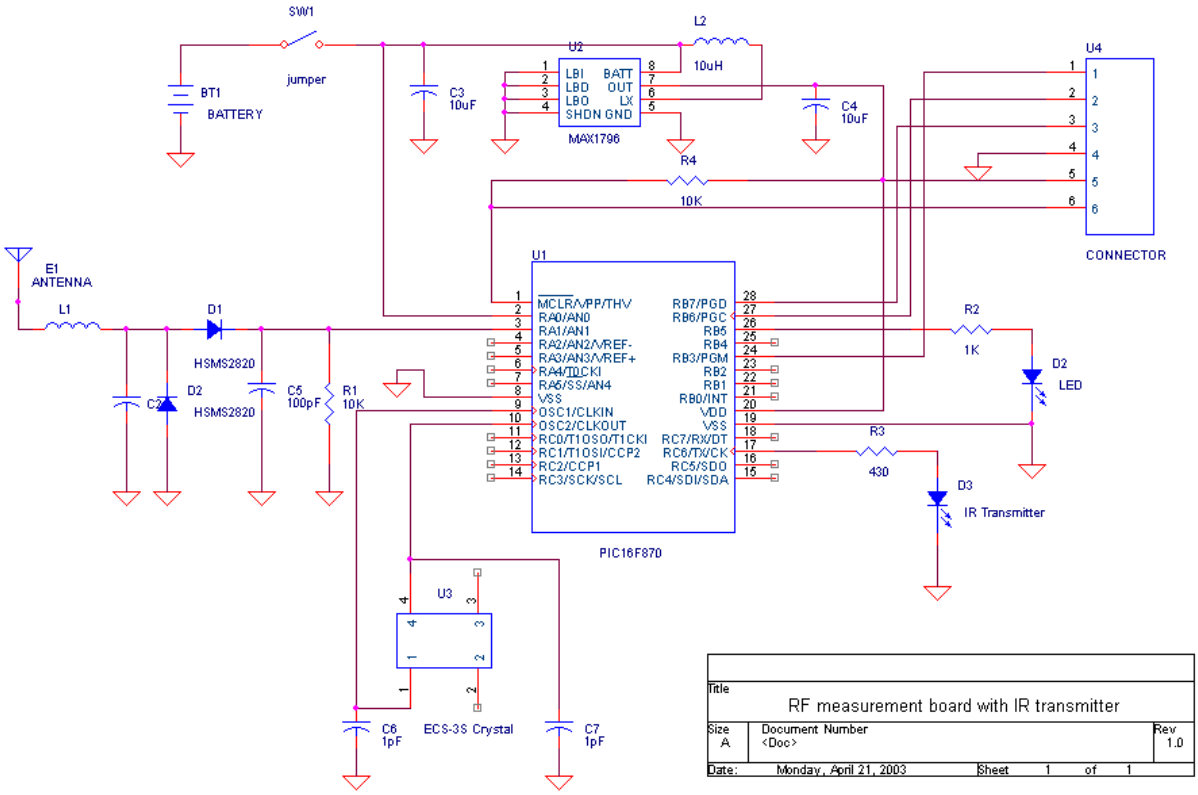


Figure A.2 Schematic of the RF power sensor board

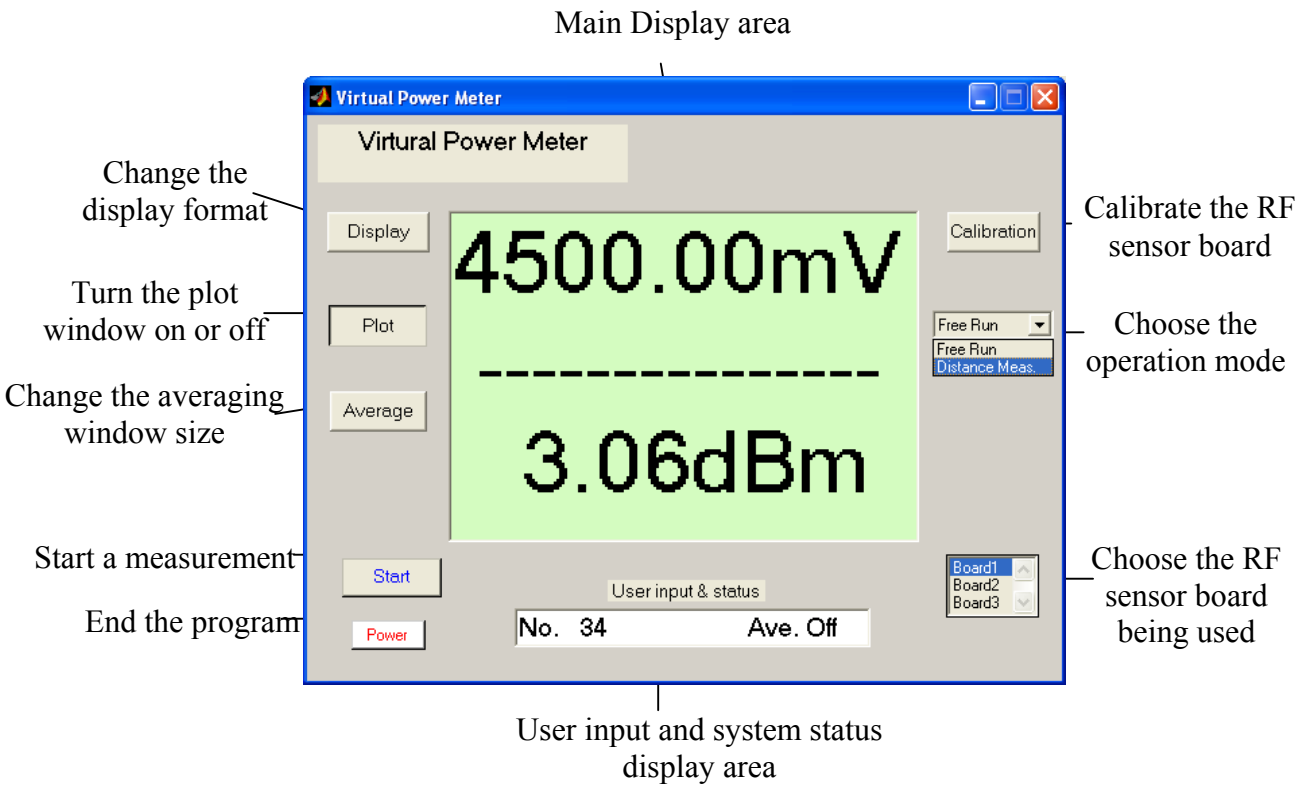


Figure A.3 Graphical user interface of the virtual power meter program

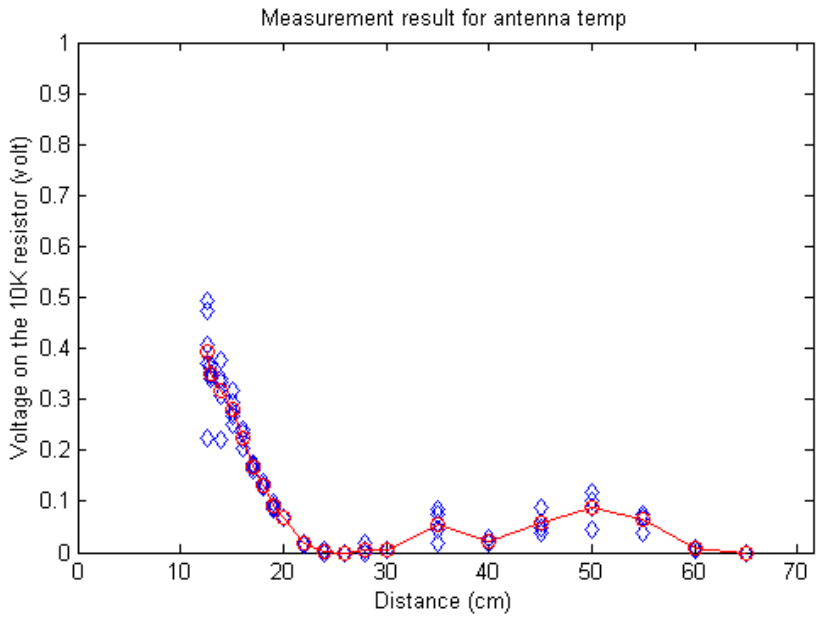


Figure A.4 A sample power-distance curve

A. 3 Calibration of the RF sensor board

As mentioned earlier, the quantity that is directly measured by the A/D converter on the RF power sensor board is the DC voltage on a precision resistor. Therefore calibration is necessary in order to get the equivalent RF power available from the antenna (DUT). However, the detector circuit on the sensor board is connected to the antenna through a microstrip line, so it is not possible to connect it to a standard reference power source for the calibration. Therefore, a replicated board with the same layout and circuit, but a standard cable connector is calibrated in lieu of the actual RF sensor board. The impedance matching network on the calibration board was tuned to the characteristic impedance of the cable, which is 50 Ω.

A Hewlett-Packard model E4421B signal generator has been used as the reference source in this research. The relationship between the DC voltage and the available power is obtained through 9^{th} order polynomial fitting with the discrete calibrated data points. A typical calibration curve is shown in Figure A.5, where the red markers and line are actual measurement results while the green line is the data-fitting result.

Once the calibration is done and the above said relationship has been established, the polynomials for the calibrated board are saved in a data file, which will be retrieved by the program to calculate the available power from the DC voltage data.

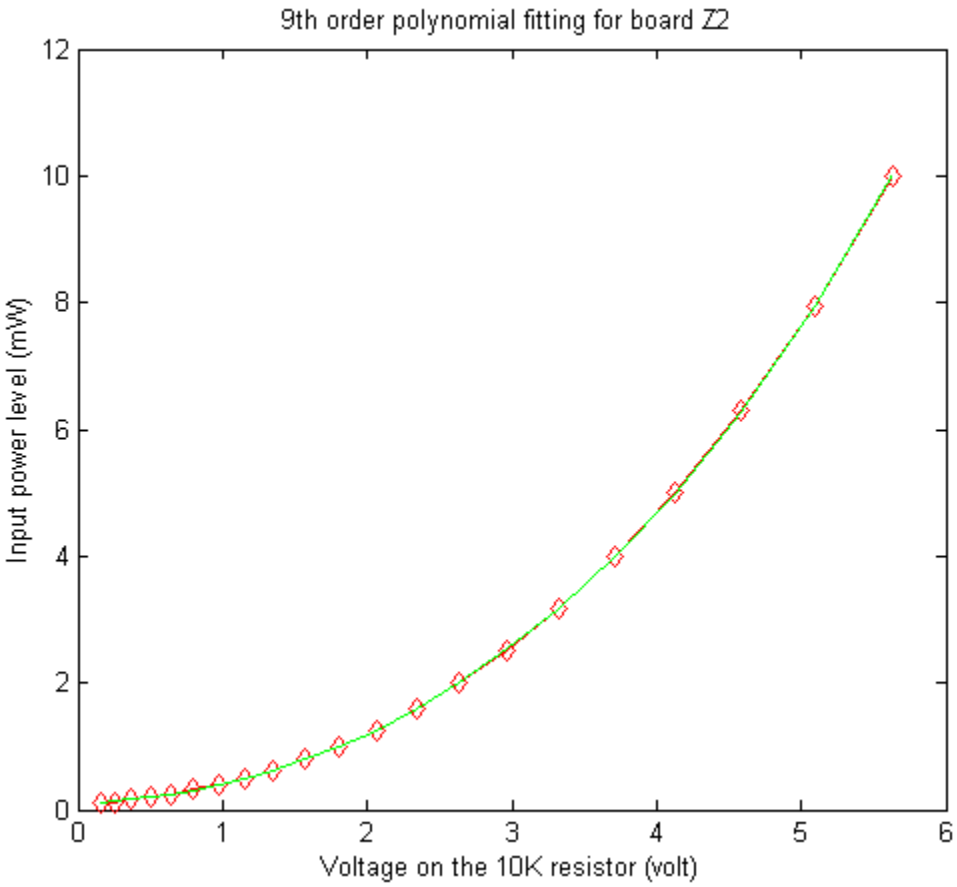


Figure A.5 Calibration and data fitting results

APPENDIX B

Antenna chip fabrication

The antennas for the experimental studies in this work were fabricated in the John A. Swanson Microsystems lab at the University of Pittsburgh, with the generous help from various professors and students associated with the lab.

The antenna chips are built on Boron doped *p*-type, 100 oriented, 3-inch silicon wafers. The resistivity of one type of wafers is 1-10 Ω-cm, which represents the normal wafers used for CMOS IC fabrication. That for the other type is greater than 10k Ω-cm, which represents the higher end of the silicon wafers available for IC fabrication. The metal used for building the antenna structure is Aluminum, which is sputtered and later patterned using photolithography. Its thickness is varied for some wafers in order to study the effects of the thickness on the antenna performance.

The whole antenna chip fabrication process can be roughly divided into 9 steps.

Step 1: Deposit aluminum film using sputtering

In this step, we deposit an aluminum foil on top of the silicon wafer using DC sputtering.

The sputtering system available in the lab is model ISE-OE-PVD-3000 from Innovative Systems Engineering, Inc. It has one deposition chamber and one manual load lock chamber. The deposition is done with one of the two available DC guns. The process gas used for the deposition is Argon at the pressure of 5mtorr. At a DC power level of 40W and room temperature, the deposition rate is around 1Angtrom/sec.

After the deposition, the wafer should be covered by a uniform aluminum film as shown in Figure B.1.

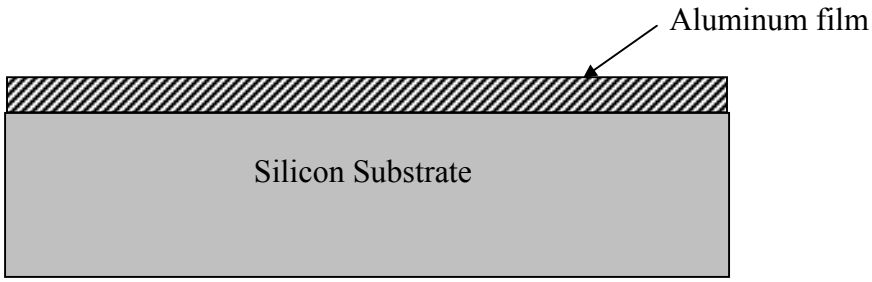


Figure B.1 The wafer structure after step 1

Step 2: Spin coat the wafer with photoresist

In this step, we apply a layer of photoresist on top of the aluminum foil.

The photoresist (PR) used in this fabrication is Microposit SC-1805 positive photoresist manufactured by Shipley, Inc. It was applied with a model RC-8 spin coater from Karl Suss. The obtained film thickness was about 0.5μm when the wafer was spun for 30 sec at a speed of 3500rpm. In order to increase the uniformity of the PR film, the adhesion promoter, HMDS, was first applied on the wafer with the same process prior to the application of the PR.

After this step, the wafer should have a structure as shown in Figure B.2.

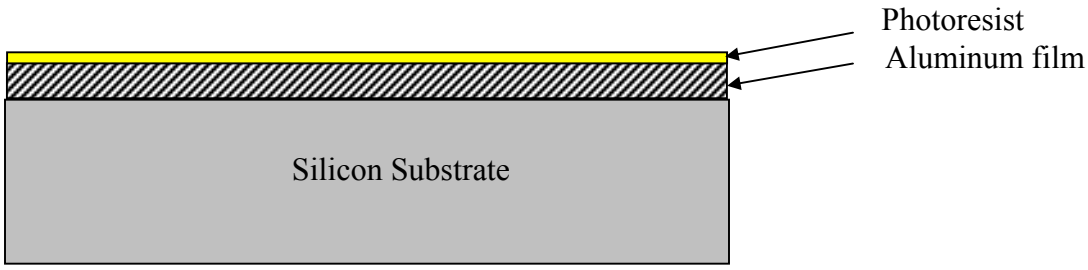


Figure B.2 Wafer structure after step 2

Step 3: Soft bake the photoresist

The PR is required to go through a soft baking process before it is exposed, which can be done with either a hot plate or a convection oven. In this fabrication, a convection oven was used to bake the wafer at 95°C for 30 minutes.

Step 4: Expose the photoresist to UV light

After soft baking, the PR is exposed to UV light using a Karl Suss model MA6 mask aligner. The UV source has a light intensity of 35.5mW/cm^2 at a wavelength of 365nm. The best exposure time was experimentally found to be 4sec. The soft contact exposure mode was used in this fabrication.

The photo mask was manufactured by Adtek Photomask, Inc. It was a clean field mask since positive photoresist was used for this fabrication. The mask uses an anti-reflective Chrome coating on a 4×4 inches^2 square soda lime glass plate. It has a minimal feature size of 10μm and critical dimension tolerance of ±1.0μm.

Step 5: Develop the photoresist

The exposed photoresist layer was developed using the MF-319 developer. At room temperature, the wafer was immersed in the developer for 60 sec. The wafer structure after developing is shown in Figure B.3.

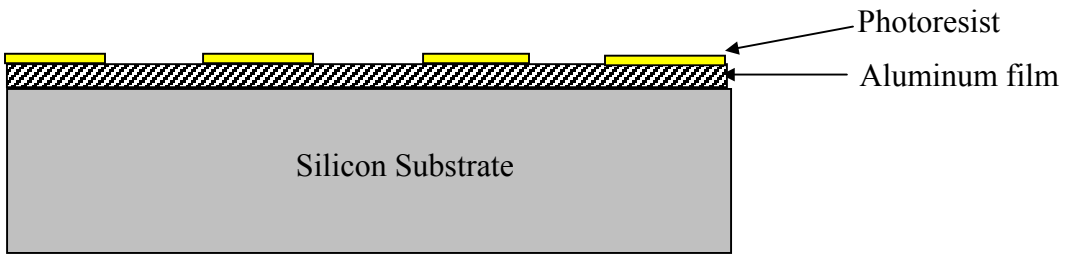


Figure B.3 Wafer structure after PR developing

Step 6: Hard bake the photoresist

The PR went through a hard baking process after it was developed. This was achieved by putting the wafer in a convection oven at 120°C for 30 minutes.

Step 7: Etch the aluminum film

In this step, the unwanted aluminum is removed from the wafer using a wet etching process. The etchant is a mixture of Phosphorous acid, Nitric acid, Acetic acid, and water with a ratio of 16:1:1:4.

The wafer is immersed in the etchant and consistently agitated for about 2 minutes at a temperature of 40°C. It is rinsed thoroughly with de-ionized (DI) water right after the immersion.

The wafer structure after etching is shown in Figure B.4.

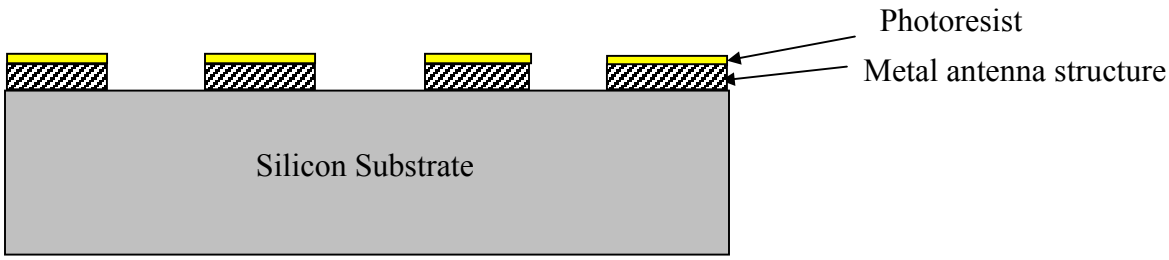


Figure B.4 Wafer structure after etching

Step 8: Remove the unexposed photoresist

In this step, the unexposed photoresist remaining on top of the aluminum structure is removed using Acetone.

After this step, the desired antenna structures are available on top the silicon substrate. The finished wafer structure is shown in Figure B.5.

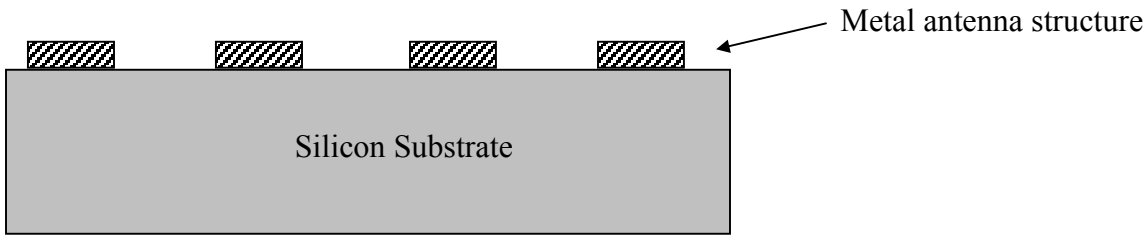


Figure B.5 Wafer structure after step 8

Step 9: Measure the aluminum thickness and cut the wafer into antenna chips

The aluminum layer thickness is measured with a Veeco Dektak^3 ST surface profiler. After the measurement, the wafer is cut into chips with a diamond saw or a glass scriber.

BIBLIOGRAPHY

[1] W. C. Brown, "The history of power transmission by radio waves," *IEEE Trans. on Microwave Theory and Techniques*, Vol. MTT-32, 1984, pp. 1230-1242

[2] T. Yoo and K. Chang, "Theoretical and experimental development of 10 and 35 GHz rectennas," *IEEE Trans. on Microwave Theory and Techniques,* Vol. MTT-40, 1992, pp. 1259-1266

[3] K. Finkenzeller, "RFID handbook, radio-frequency identification fundamentals and applications," *John Wiley and sons*, Chichester, 1999

[4] Apparatus for energizing a remote station and related method, U.S. Patent No. 6,289,237, University of Pittsburgh, Marlin H. Mickle, Kevin W. Wells, and Ronald G. Hoelzeman, September 11, 2001 (40 claims).

[5] Apparatus for energizing a remote station and related method, Continuation In Part, Serial No. 509/951,032, University of Pittsburgh, Marlin H. Mickle, Leonid Mats, Lorenz Neureuter, Minhong Mi, Dmitry Gorodetsky, Carl Taylor and Chad Emahiser, Filed September 10, 2001 (55 claims).

[6] "Global markets and applications for radio frequency identification equipment and systems", a report by the Venture Development Corporation, http://www.vdc-corp.com

[7] K. S. J. Pister, J. M. Kahn and B. E. Boser, "Smart Dust: Wireless Networks of Millimeter-Scale Sensor Nodes", Highlight Article in 1999 Electronics Research Laboratory Research Summary at University of California, Berkeley

[8] A. F. Stevenson, "Relationship between the transmitting and receiving properties of antennas," Quart. Applied Math. pp. 369-384, 1948

[9] C. A. Balanis, "Antenna theory: analysis and design," *John Wiley & Sons*, 1997

[10] K. M. Strohm, J. Buechler, and E. Kaspe, "SIMMWIC Rectennas on High-Resistivity Silicon and CMOS Compatibility," *IEEE Trans. on Microwave Theory and Techniques,* Vol. MTT-46, 1998, pp. 669-676

[11] B. Floyd, K. Kim, and O. Kenneth, "Wireless interconnection in CMOS IC with integrated antennas," *Digest of Technical Papers IEEE International Solid-State Circuits Conference,* ISSCC 2000, pp. 328 –329

[12] A. Abrial, J. Bouvier, M. Renaudin, P. Senn, and P.l Vivet, "A new contactless smart card IC using an on-chip antenna and an asynchronous microcontroller", *IEEE Journal of Solid-state circuits*, vol. 36, 2001, pp. 1101-1107

[13] B. Razavi, "Design of analog CMOS integrated circuits", *McGraw Hill*, 2001

[14] A. M. Niknejad and R.G. Meyer, *Design, simulation and applications of inductors and transformers for Si RF ICs*, Kluwer Academic Publishers, London, 2000

[15] S. A. Campbell, *The science and engineering of microelectronic fabrication*, 2nd ed. Oxford, 2001

[16] J. R. James, "What's new in antenna*?" IEEE Antennas and Propagation Magazine,* Vol. 32, 1990, pp. 6-18

[17] L. J. Chu, "Physical limitations of omnidirectional antennas," *Journal of Applied Physics*, vol. 19, 1948, pp. 1163-1175

[18] H. A. Wheeler, "Fundamental limitations of small antennas," *Proc. of IRE*, Vol. 35, 1947, pp. 1479-1484

[19] H. A. Wheeler, "Small Antennas", *IEEE Trans. on Antennas and Propagation,* Vol. AP-23, 1975, pp. 462-469

[20] R. C. Hansen, "Fundamental limitations in antennas", *Proc. of IEEE,* Vol. 69, 1981, pp. 170-181

[21] Ansoft HFSS, from Ansoft Corporation, Four Station Square, Suite 200, Pittsburgh, PA15219

[22] D. M. Pozar, "Microstrip antennas," *Proc. of IEEE*, Vol. 80, 1992 pp.79-91

[23] D. Beck, M. Herrmann, and E. Kasper, "CMOS on FZ-high resistivity substrate for monolithic integration of SiGe-RF-Circuitry and readout electronics," *IEEE trans. on Elec. Dev.*, Vol. 44, 1997, 1091-1101

[24] J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2μm CMOS RF amplifier." *IEEE Electron Device Letters*, Vol. 14, 1993, pp. 246-248

[25] J. M. Lopez-Villegas, J. Samitier, C. Cane, P. Losantos, and J. Bausells, "Improvement of the quality factor of RF integrated inductors by layout optimization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp.76-83, 2000

[26] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstrip line on Si-SiO_2 system. *IEEE Transactions on Microwave Theory and Techniques*, vol. 11, pp.869–881, 1971

[27] C. P. Yue and S.S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Trans. on Elec. Devices*, Vol. 47, 2000, pp.560-568

[28] H.A. Wheeler, "Formulas for the skin effect," *Proc. of IRE*, Vol. 30, 1942, pp. 412-424

[29] K. B. Ashby, W. C. Finley, J. J. Bastek, S. Moinian, and I. A. Koullias, "High Q inductors for wireless applications in a complementary silicon bipolar process," in *Proc. Bipolar and BiCMOS circuits and technology meeting*, Minneapolis, MN, 1994, pp. 179-182

[30] H. A. Wheeler, "Transmission-line properties of parallel strips separated by a dielectric sheet," *IEEE Trans. on Microwave Theory and Techniques,* Vol. MTT-13, 1965, pp. 172-185

[31] MOSIS Integrated Service Fabrication Service, http://www.mosis.org, USC information Sciences Institute, 4676 Admiralty Way, 7th floor Marina del Rey, CA 90292

[32] S. Ramo, J. R. Whinnery, and T. V. Duzer, *Fields and waves in communication electronics*, John Wiley & Sons, 1994

[33] Ansoft Ensemble, from Ansoft Corporation, Four Station Square Suite 200, Pittsburgh, PA15219

[34] M. N. O. Sadiku, *"Numerical techniques in electromagnetics"*, 2nd ed., CRC Press, 2000

[35] K. S. Yee, "Numerical solution of initial boundary-value problems involving Maxwell's equations in isotropic media," *IEEE Trans. on Antennas and Propagation*, Vol. Ap-14, 1966, pp.302-307

[36] *APLAC electromagnetic simulation manual*, APLAC Solutions Inc, 320 Decker Dr, Suite 100, Irving, TX 75062 USA

[37] R. B. Waterhouse, S.D. Targonski, and, D.M. Kokotoff, "Design and performance of small printed antennas," *IEEE Trans. on Antennas and Propagation,* Vol. 40, 1998, pp. 1629-1633

[38] T. K. Lo, Chun-on Ho, Y. Hwang, E. K.W. Lam, and B. Lee, "Miniature aperture-coupled microstrip antenna of very high permittivity," *IEE Electronics letters*, Vol. 33, 1997, pp.9-10

[39] P. R. Foster and R. A. Burberry, "Antenna problems in RFID systems", *IEE colloquium on RFID technology*, pp.3/1-3/5, 1999

[40] J. Rashed and C. T. Tai, "A new class of wire antennas," 1982 *IEEE Antennas Propagation Soc. Int. Symp. Digest*, Vol. 2, 1982, pp.564-567

[41] H. Nakano, H. Tagami, A. Yoshizawa, and J. Yamauchi, "Shortening ratios of modified dipole antennas", *IEEE Trans. on Antennas and Propagation,* Vol. AP-32, 1984, pp. 385-386

[42] W. L. Curtis, "Spiral antennas," *IRE Trans. on Antennas and Propagation*, Vol. Ap-8, 1960, pp. 298-306

[43] J. Ely, C. Christodoulou, and D. Shively, "Square spiral microstrip antennas for wireless applications," *IEE Micro. Sys. Conf., 1995,* pp. 229-232

[44] H. K. Kan and R. B. Waterhouse, "Small square dual spiral printed antennas," *IEE Electronics Letters,* Vol. 37, 2001, pp. 478-479

[45] R. Rudenberg, "The Reception of Electrical Waves in Wireless Telegraphy," *Annals of Physics (in German)*, Vol. 25, Leipzig, 1908.

[46] D. Singh, C. Kalialakis, P. Gardner, and P. S. Hall, "Small H-shaped antennas for MMIC applications," *IEEE Trans. on Antennas and Propagation*, Vol. Ap-48, 2000, pp.1134-1141

[47] G. W. Dahlmann and E. L. Yeatman, "High-Q microwave inductor on silicon by surface tension self-assembly," *IEE electronics letters,* vol.36, pp.1707-1708, 2000

[48] C. P. Yue, S. S. Wong, "On-chip inductors with patterned ground shields for Si-based RF ICs, " *IEEE Journal of Solid-state Circuit*, Vol.33, pp.743-752, 1998

[49] J. N. Burghartz, "Progress in RF inductors on silicon – understanding substrate losses," *Technical digest of International Electronic Device Meeting*, 1998, pp. 523-526

[50] C. M. Nam and Y. S. Kwon, "High-performance planar inductor on thick oxidized porous silicon (OPS) substrate," *IEEE Microwave Guided Wave Letter*, Vol. 7, 1997, pp. 236–238

[51] K. Hirasawa, M. Haneishi, *Analysis, design, and measurement of small and low-profile antennas*, Artech House, Boston, 1992

[52] H. Y. Lee, "Wideband characterization of a typical bonding wire for microwave and millimeter-wave integrated circuits," *IEEE Trans. on Microwave Theory and Techniques,* Vol. MTT-43, 1995, pp. 63-68

[53] J. Bouvier, Y. Thorigne, S. A. Hassan, S.A.; M. J. Revillet, P. Senn, "A smart card CMOS circuit with magnetic power and communication interface," *Digest of Technical Papers, IEEE International Solid-State Circuits Conference, 44th ISSCC*, pp. 296 –297, 474, 1997

[54] Private conversation with Professor. Marlin H. Mickle at the University of Pittsburgh

[55] *IEEE Standard Test Procedures for Antennas*, IEEE Std 149-1979, published by IEEE, Inc., 1979

[56] E. H. Newman, P. Bohley, and C. H. Walter, "Two methods for the measurement of antenna efficiency," *IEEE Trans. on Antennas and Propagation*, Vol. Ap-23, 1975, pp.457-461

[57] D. M. Pozar and B. Kaufman, "Comparison of three methods for the measurement of printed antenna efficiency," *IEEE Trans. on Antennas and Propagation*, Vol. Ap-36, 1988, pp.136-139

[58] H. A. Wheeler, "The radian sphere around a small antenna," *Proc. IRE*, 1959, pp.1325-1331

[59] Cadence Design Systems, http://www.cadence.com, 2655 Seely Avenue, San Jose, CA 95134

[60] Carl E. Taylor, "Using VCOs as RF measuring devices," MS thesis, Department of Electrical Engineering, University of Pittsburgh, 2003