# MEDIUM VOLTAGE DC NETWORK MODELING AND ANALYSIS WITH PRELIMINARY STUDIES FOR OPTIMIZED CONVERTER CONFIGURATION THROUGH PSCAD SIMULATION ENVIRONMENT

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With the advancement of high capacity power electronics technologies, most notably in high voltage direct current (HVDC) applications, the concept of developing and implementing future transmission networks through a DC backbone presents a realistic and advantageous option over traditional AC approaches. Currently, most consumer electrical equipment requires DC power to function, thus requiring an AC/DC conversion. New forms of distributed generation, such as solar photovoltaic power, produce a direct DC output. Establishing an accessible and direct supply of DC power to serve such resources and loads creates the potential to mitigate losses experienced in the AC/DC conversion process, reduce overall electrical system infrastructure, and lessen the amount of power generated from power plants, as well as other advantages. For the reasons listed, medium voltage DC (MVDC) networks represent a promising, initial platform for interconnecting relatively low voltage generation resources such as photovoltaic panels, serving loads, and supplying other equipment on a common DC bus bar. Future industrial parks, ship power systems, hybrid plug-in vehicles, and energy storage systems are all avenues for future implementation of the concept.

This thesis introduces an initial design and simulation model of the MVDC network concept containing renewable generation, power electronic converters, and induction machine loads. Each of the equipment models are developed and modeled in PSCAD and validated analytically. The models of the represented system equipment and components are individually

presented and accompanied with their simulated results to demonstrate the validity of the overall model. Finally, the equipment models are assembled together into a meshed system to perform traditional preliminary studies on the overall power system including wind speed adjustments, load energizing, and fault-clearing analysis in order to evaluate aspects of various operational phenomena such as potential overvoltages, system stability issues, and other unexpected occurrences.

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## THESIS NOMENCLATURE

| Symbol | Physical Quantity |
|---|---|
| A | Amplitude of Signal; Swept Area of Wind Turbine |
| a, b, c | Phases of Power System |
| C | General Capacitance |
| $C_p$ | Power Coefficient of MOD-2 Turbine |
| D | Diode Label, Duty Cycle |
| $f_s$ | Switching Frequency |
| $G_R$ | Gear Ratio |
| $G_\eta$ | Gear Efficiency |
| $I_a$, $I_b$, $I_c$ | Line Current |
| $I_g$ | Input Current to DC/DC Converter |
| $I_L$ | Average Current through Inductor |
| $I_p$ | Peak DC Current in DC/DC Converter |
| $\dot{KE}$ | Kinetic Energy Rate of Fluid |
| L | General Inductance |
| $L_l$ | Leakage Inductance of Transformer |
| M | Normalized Output over Input Voltage |
| m, $m_a$ | Modulation Index |

| Symbol | Physical Quantity |
|---|---|
| $\dot{m}$ | Mass Flow Rate |
| $m_f$ | Modulation Frequency |
| N | Neutral Point in Converter Circuit |
| n | Inverter Levels, Turns Ratio, Harmonic Number |
| P | Pole Pairs of Machine, General Power |
| $P_{mech}$ | Mechanical Power of Machine |
| $P_a$ | Instantaneous Power in Switch |
| PF | Power Factor |
| $P_{out, norm}$ | Normalized Output Power of DC/DC Converter |
| $P_{SW}$ | Average Power Dissipation in Switch |
| $P_{WIND}$ | Power in Wind |
| Q | Semiconductor Device Label |
| R | General Resistance |
| S | Packaged IGBT with Diode |
| s | Slip of Machine |
| T | General Torque, Output Torque of Wind Turbine |
| $T_e$ | Electromagnetic Torque |
| $T_m$ | Mechanical Torque |
| $T_s$ | Switching Period |
| $V_a$, $V_b$, $V_c$, $E_a$, $E_b$ | Line-to-Ground Voltage |
| $V_{ab}$, $V_{ac}$, $V_{bc}$ | Line-to-Line Voltage |
| V, $V_{DC}$, $V_g$ | Average DC Voltage |

| Symbol | Physical Quantity |
|---|---|
| $V_o$ | Voltage Across Magnetizing Branch of Machine |
| $V_p$ | Primary Voltage of Transformer |
| $V_s$ | Secondary Voltage of Transformer, Switch Voltage |
| $V_W$, $E_s$ | Velocity of Wind |
| $W_{ON}$ | Switch Dissipated Energy while ON |
| $W_{OFF}$ | Switch Dissipated Energy while OFF |
| $X_s$ | Normalized Reactance of DC/DC Converter |
| Y | Y Winding of Transformer |
| $Z_{th}$ | Thevenin Impedance |
| $\alpha$ | Firing Delay Angle in Rectifier Circuit |
| $\beta$ | Blade Pitch Angle |
| $\Delta$ | Delta Winding of Transformer |
| $\phi$ | Power Factor Angle, Phase Shift |
| $\rho$ | Density of Fluid |
| $\omega_e$ | Excitation Frequency of Machine |
| $\omega_r$ | Electrical Rotor Speed |
| $\omega_{rm}$ | Mechanical Rotor Speed |
| $\upsilon$ | Velocity of Fluid |
| $\gamma$ | Tip Speed Ratio of Turbine Blade |
| m | Magnetizing Branch Parameter |
| s / 1 | Stator Parameter |
| r / 2 | Rotor Parameter |

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# 1.0 INTRODUCTION

Corporate research centers and universities around the country are beginning to consider the use of DC in future transmission and distribution system applications. Recent developments and trends in electric power consumption indicate an increasing use of DC-based power in end-user equipment such as computers, televisions, and other appliances. DC systems are currently employed at lower voltages in telecommunication equipment, shipboard power systems, and traction systems. Electrical energy production from some renewable energy resources, including solar, is at DC.

As was the case at the turn of the 20$^{th}$ century, a justification in using AC compared to DC will need to be evaluated as the current electric grid begins to make drastic changes in the United States. In 2006, EPRI published a presentation that established a few points that made the case for DC applications in the 21$^{st}$ century [1]. Today, advances in the technological developments and applications are in the area of electronics with applications in transportation systems (electric vehicles and magnetic levitation trains). Equipment is increasingly being operated with DC and thus requires an AC to DC conversion with the current grid set-up. We are living in the era of the newly emerging micro-grid, which are distributed generation systems (such as photovoltaic systems) that produce DC power. Finally, solutions for integrating renewable energy with storage devices are attempting to be developed at the utility scale to deliver DC power.

Power electronics technology is an efficient, powerful, and a reliable solution for integrating the large amounts of renewable generation into the existing infrastructure. Renewable integration is a mandate set forth by the United States government with a deadline by 2030. Growing developments in the area of power electronics, including the application of novel semiconductor devices, have unlocked the potential for higher capacity, faster switching, lower-loss conversion and inversion devices. In recent years the advent of silicon carbide solid state electronic devices, which have lower switching and conduction losses compared to silicon devices, has made DC/AC conversion more promising in the near-term timeframe. Virtually all voltage and current ratings are possible by utilizing series and parallel combinations of discrete semiconductors. These factors combine to form an opportunity for the development and further deployment of DC technology throughout the electric grid at all levels from transmission through distribution to end-use. An inspiring quote for the research work to be presented is found below:

> *"Up until now we've just been connecting wind farms to the grid. What we need to be doing is integrating them. Power electronics will enable us to do this by controlling the power flows. It's a solution that's starting to be used, but nowhere near to the extent that will be needed in the future."* [2]

## 1.1 MEDIUM VOLTAGE DC NETWORK

High Voltage Direct Current (HVDC) has proven its merit over high voltage alternating current (AC) transmission for long distance power delivery applications. HVDC advantages include a decreased right-of-way clearance, improved control, power factor correction, less infrastructure,

and reduced losses [3]. Underwater and underground transmission of DC avoids excessive capacitance and dielectric heating effects in the cables. HVDC also provides an asynchronous link for strong, but instability-prone AC power systems and advanced systems can provide black-start capability. The HVDC cost of AC/DC conversion and DC/AC inversion terminals has steadily decreased as the voltage ratings, current capacity, efficiency, and cost of solid state electronics in these converters have decreased over the years, along with continued improvements in overall system design and construction. These factors, other attributes of HVDC technology, and the emerging applications of DC resources and supply establish the potential for a paradigm shift in the future development of transmission and distribution systems to one with a larger overall DC infrastructure.

The need for MVDC technology development has been driven by the liberalization of the energy market which has led to innovations and installations of large scale wind farms, solar farms, fuel cells, battery storage, and distributed generation. In addition, small end-use consumers are employing these same types of systems and devices at a scaled level which have a number of DC interfaces. There are certainly potential increases in efficiency that can be realized by employing a MVDC supply, but with an overall increase in complexity, technical requirements, and end-user protective devices, thus requiring R&D for MVDC technology.

Considering all of these various aspects and applications, MVDC is feasible and technically advantageous, and certainly economically attractive especially where there is a concentration of wind or solar generation combined with local loads. The specific distribution of renewable and potential DC sources at the medium voltage substation level will determine the economics and therefore the selection of DC versus AC. Applications for DC integration are numerous for green energy integration (i.e., solar and wind) generation, fuel cells, battery

storage, and other forms of energy resources. These are all rapidly increasing and they all employ/require a DC integration link of some kind. The same is true of the various loads that are being employed today by consumers, including the advancement in electric vehicles and more sensitive power electronics based loads, many of which are operating at low voltage DC levels.

A preliminary general set-up of a proposed MVDC substation layout with representative energy supply, distributed resources, and loads is displayed in Figure 1.1. The model consists of renewable energy resource integration (including wind and solar), energy storage (in a general form of a battery), and other applications (e.g., electric vehicle integration) at direct medium voltage connection. Generic blocks in the model represent various converter technologies for interfacing the medium voltage bus with associated generation resources and loads. Finally, an overall control system that builds intelligence into the network will be eventually designed to regulate the output power of the various generation resources and deliver power to the loads within the framework and design of the MVDC substation concept.

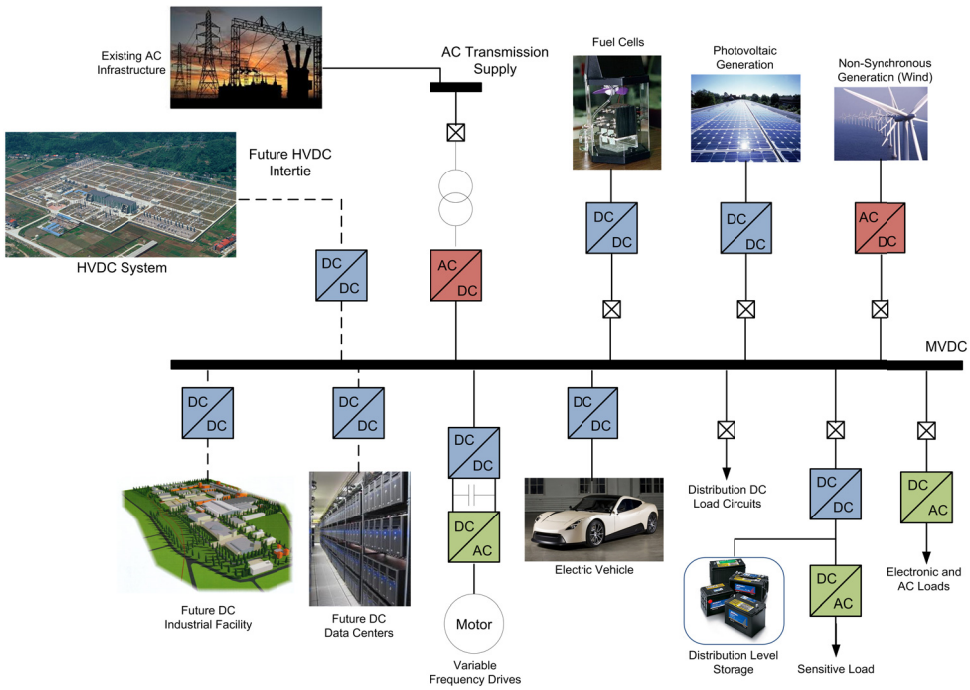


**Figure 1.1** Medium Voltage DC Substation

## 1.2 OBJECTIVES OF RESEARCH

To this point, the overall MVDC concept can be found in the literature in some general forms similar to the diagram in Figure 1.1. However, to date, there exist no complete models or simulations that account for the entire system. Certain aspects and individual components of the MVDC system have been modeled, such as the bidirectional DC-to-DC converter, due to its growing popularity for interfacing renewable resources to the electric grid.

A holistic MVDC framework requires more detailed development, since most efforts to-date focus more attention on the various components. The proposed concept herein is to integrate a portion of the MVDC model, while at first validating sections of the network through a piece-wise process. The ultimate build-out of this work will also address the interactions of the different types of converters with the electric machines found on the DC bus, as well as investigating aspects of the dynamic changes of the intermittent renewable generation resources, as two examples of a complete treatment.

Figure 1.1 contains many components that require sophisticated modeling techniques and cannot be expected to be completed in the allotted time frame for master's thesis research. Instead, a number of components from Figure 1.1 will be modeled in the MVDC network found in this document. These devices include two multilevel DC-to-AC inverters, a six pulse AC-to-DC rectifier, two induction machines, a bidirectional DC-to-DC converter, and the intermittent renewable generation resource being wind. The objective of this work is to build and validate the model composed of the latter components, and to run preliminary studies to quantify and identify undesired effects upon disturbing the network that can then be used to make improvements to the overall design. This work, essentially, is a preliminary study and base case

used for a larger, multiple year development of the overall MVDC network found in Figure 1.1. The objectives of the work to follow, therefore, include:

- Literature survey of state-of-the-art power electronic converters and control including inverters, rectifiers, and choppers used for high power applications and renewable integration;
- Design of various converter configurations based on those found in the literature that appear applicable and proven practical in an industrial setting;
- Numerous algorithms exist for controlling the semiconductor devices in the converters. Restrictions were placed on pulse width modulation techniques opposed to space vector modulation techniques. Selection of a pulse width modulation method for the converters will be determined based on a total harmonic distortion metric;
- Implementation of multiple generation resources into the model including a wind turbine with governor and equivalent voltage source representing the utility, which naturally dispatch depending on load demand;
- Assemblage of a system composed of different types of power electronic converters, machines, and generic resistive load with renewable generation in the PSCAD environment;
- Evaluation of the equipment interactions using analysis techniques used in industry. For this study, only fault-clear techniques and load energizing methods are evaluated. These studies will help evaluate overvoltages and extreme power demands of all loads on the network. They will also help identify design criteria, adjustment of parameters, and future research initiatives for this medium voltage DC initiative;

- The outcome of this work will provide a platform for future expansion of the network model that has been validated mathematically and through simulation.

## 1.3 THESIS ORGANIZATION

Chapter 2 provides a thorough treatment of the types of high power semiconductor devices used regularly in the power industry including the silicon controlled rectifier (SCR), gate turn-off thyristor (GTO), and insulated gate bipolar transistor (IGBT). This chapter also provides the theoretical foundation for the number of power converters described in this work. Thorough treatments of the neutral point clamp (NPC) and flying-capacitor (FC) multilevel inverters are provided along with standard control strategies for these types of inverters. Following the discussion of the inverters, the reader will get a feeling for the operation of a six pulse bridge rectifier as well as the bidirectional DC-to-DC converter. The difficulty with power converter operation is understanding which semiconductors are being switched at any moment in time and realizing that the devices are switching at a very fast rate. With this statement, the fundamentals found in Chapter 2 are essential for understanding the validation procedures presented in Chapter 4.

Chapter 3 provides the necessary principles and a review of the electric machines found in this work. Wind turbines, which have found popularity in the European countries, are increasingly being installed throughout the United States. Chapter 3 provides enough of the theory for understanding how the wind turbine was modeled in PSCAD. The AC drive configurations found in the wind turbine system are also described for the interested reader.

With the suitable amount of theory provided in Chapters 2 and 3, Chapter 4 addresses the MVDC network development. Here, the reader will find the details of how all the converters, machines, and wind turbine system are modeled with elaborated detail. The use of PSCAD schematics and output waveforms are used, when appropriate, to clarify and bridge any gaps that might still exist after reading Chapters 2 and 3. This chapter also provides extensive details showing how the theory presented in Chapters 2 and 3 aligns with what has been obtained through simulation so that the model's validity is established.

Chapter 5 provides the preliminary studies used to evaluate and optimize the converter placements in the developed model. Various disturbances are applied to the network to show the dynamic behavior of the MVDC network. Finally, Chapter 6 provides a discussion of the conclusions developed throughout this study and future work that our team at the University of Pittsburgh will be evaluating in the coming years.

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# 2.0 POWER SEMICONDUCTORS AND CONVERTER TOPOLOGIES FOR HIGH POWER APPLICATIONS

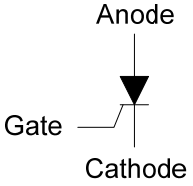
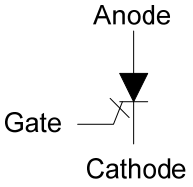
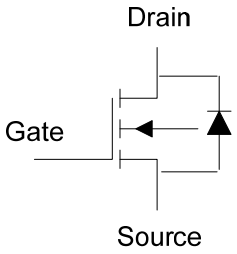
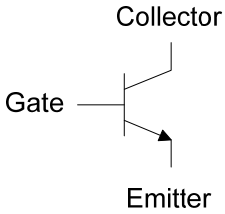
The principles of high power semiconductor devices and power electronics converters including multilevel inverters, rectifiers and bidirectional DC-to-DC converters and associated control are presented in this chapter. These essential discussions will provide the foundation for understanding the complexity and sophistication of the power electronics modules found in the MVDC network developed with PSCAD.

## 2.1 HIGH POWER SEMICONDUCTOR DEVICE CHARACTERISTICS AND REQUIREMENTS

Before the details of the most common power converter topologies used in high power applications can be explained and evaluated, a discussion of the power semiconductors used in the converter units themselves should be touched upon. The semiconductors, as we will see, are the critical components and driving mechanisms for obtaining the appropriate power conversion. To understand power converters and their operation, a general idea of the power semiconductor options, state of the device technology and trends, and the circuit concepts used in a utility or industrial setting are essential prerequisites.

The objective of this section is to give only general information about the power semiconductors used in the modeling of the medium voltage DC network. These devices include the silicon-controlled rectifier (SCR), gate turn-off thyristor (GTO) and the insulated gate bipolar transistor (IGBT). A comprehensive summary of these devices and a few other commonly used devices are found in Table 2.1.

**Table 2.1** Summary of Power Semiconductors used in Power Converters and Drives [4]

| Device | Symbol | Applications | Power Range / Freq. |
|---|---|---|---|
| SCR |  | High Power, Multi-Megawatt Power Systems | 100 MW to 1 GW<br>Frequency: < 100 Hz |
| GTO |  | High Power, Multi-Megawatt Traction and Controlled Systems, Power Systems | 1 MW to 100 MW<br>Frequency: < 500 Hz |
| Power MOSFET |  | Switching mode power supplies and small power actuators / drives | Up to 10 kW<br>Frequency: < 1 MHz |
| IGBT |  | Medium power industrial drives, machine control, inverters, converters, and active filters | Up to 500 kW<br>Frequency: < 100kHz |

### 2.1.1 Voltage and Current Carrying Capabilities of Common Power Semiconductors

A converter is an assembly of valves and other equipment, and each valve in turn is an assembly of power semiconductor devices along with snubber circuits (damping circuits) as needed, and turn-on / turn-off gate drive circuits. The device ratings and characteristics have a significant leverage on the cost, performance, size, weight, and losses in all power device applications.

Voltage and current ratings of the semiconductor devices have a significant impact on the total number of devices used in the converter as well as the cost of all the surrounding components. The highest blocking capability along with other desirable characteristics is in the range of 8-10 kV for thyristors, 5-8 kV for GTOs, and 3-5 kV for IGBTs [5]. The useable device voltage will be about half the blocking voltage capability after overvoltage and redundancies are taken into account, thus requiring multiple devices to be connected in series and, in the case of excessive fault currents, in parallel. Figure 2.1 provides a visual of the common semiconductor devices under discussion and their respective current and voltage ratings.

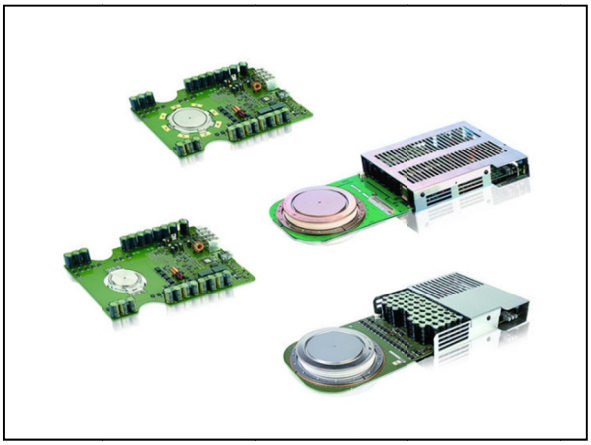
### 2.1.2 Semiconductor Switching Losses

Apart from the voltage withstand (blocking voltage) and current-carrying capabilities of the power devices, the most important qualities to evaluate when justifying the application of a semiconductor device include the conducting or ohmic losses, switching frequency, and switching losses. Traditionally, electrical engineers have a strong understanding of conduction losses because, essentially, they are the $I^2R$ losses throughout the system. The focus of this discussion will provide a general overview of common switching losses but will not go into the

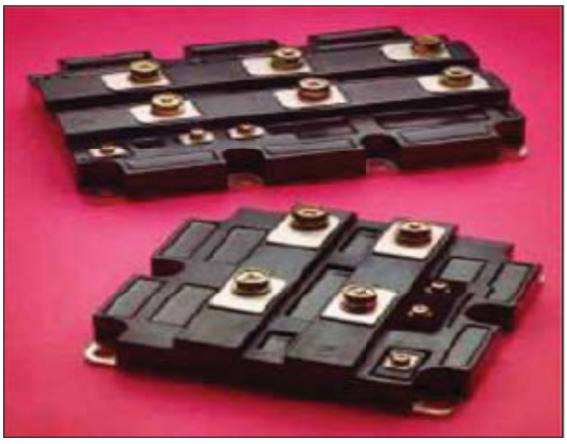
depth and explanation required to minimize these losses because this area of power electronics is a very rich subject.

12 kV, 1.5 kA SCR

6 kV, 6 kA GTO



6 kV, 6 kA IGCT/GCT



4.5 kV IGBT

**Figure 2.1** Physical Semiconductor Devices [6]

To set the groundwork for the discussion of switching loss, a classical DC/DC converter known as the boost converter will be used to capture switching loss fundamentals. The boost converter, shown in Figure 2.2, is classified as a switched mode power converter, as compared to a linear regulator, because of the continuous switching of the semiconductors. Referring to Figure 2.3, assuming ideal conditions, a single-pole double-throw switch has ideally replaced the semiconductor devices. As can be seen, the switch can be in two states. When the switch is in

position 1, the MOSFET of the converter is conducting (ON) and the diode is non-conducting (OFF). The circuit describing this state is illustrated in Figure 2.4. When the switch is in position 2, the MOSFET is non-conducting (OFF) and the diode is conducting (ON) as illustrated in Figure 2.5.

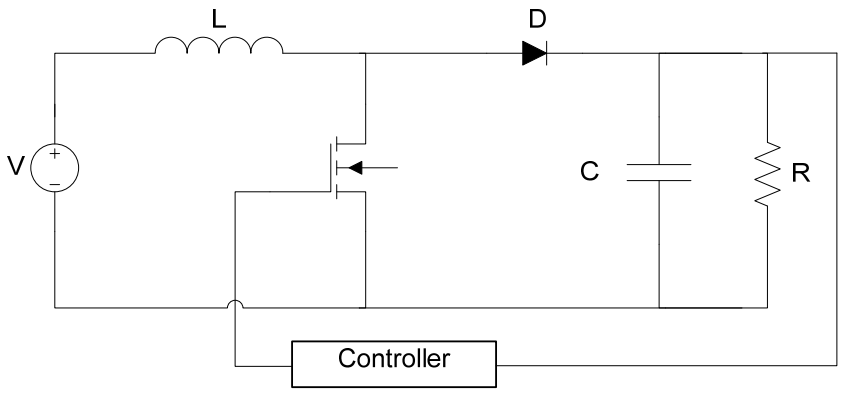



**Figure 2.2** Ideal Boost Converter

Besides the physical operation of the converter, it helps to reflect on the energy transfer between the inductor and capacitor. When the converter is in position 2 (Figure 2.5), the stored inductor energy is driving the circuit and allowing there to be an output voltage across the load while the capacitor is being charged by the input voltage source. When the converter is in position 1 (Figure 2.4), the stored energy in the capacitor, energy obtained while in position 2, contributes entirely to the output voltage seen across the load while the inductor, connected directly to the input voltage source, begins to store magnetic energy in preparation for the next switching transition.

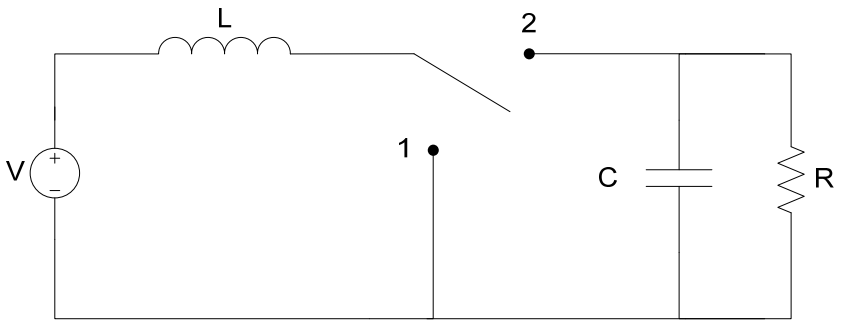



**Figure 2.3** Semiconductors Replaced with Ideal Switch in Boost Converter

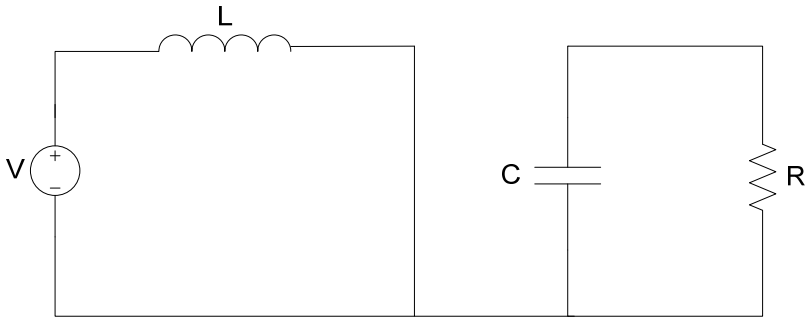



**Figure 2.4** Converter Circuit when MOSFET is ON and Diode is OFF (Position 1)

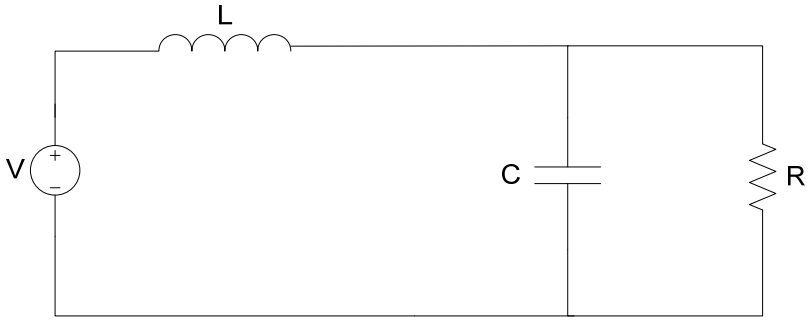



**Figure 2.5** Converter Circuit when MOSFET is OFF and Diode is ON (Position 2)

From the previous discussion, the converter consistently switches between states 1 and 2. The purpose of the controller in Figure 2.2 is to coordinate when the MOSFET should be ON and OFF. An ideal pulse width modulated signal seen across the MOSFET is found in Figure 2.6. When the switch is in position 2, the MOSFET, although not shown in the diagram but

physically is still in the circuit, develops a voltage drop across its terminals equal to the input voltage.

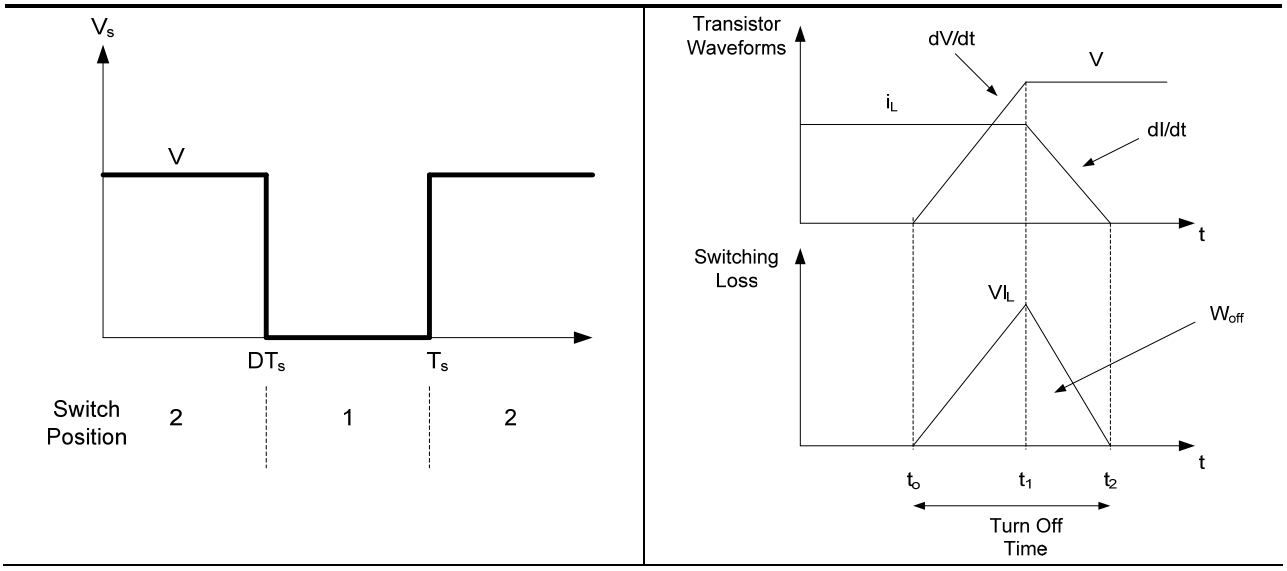



**Figure 2.6** PWM Voltage across MOSFET in Ideal Circumstances (L) and Reality (R) [7]

Thus far, ideal conditions of the power semiconductors have been emphasized. For practical applications where semiconductors do not turn ON or OFF instantaneously, this requires manufacturers to quantify the performance of the power semiconductor devices with various metrics. There are power requirements for the gate of the semiconductor, estimates of the current rate of change, *di/dt*, and voltage rate of change, *dv/dt*, capability and measurements for the turn-on time and turn-off time of the device. A realistic representation of a power MOSFET under a switching transition from ON to OFF states is shown in Figure 2.6. With the assumption that the ramp rates are linear, the average power dissipated by the transistor can be calculated with (2.1).

$$P_{SW} = \frac{1}{T_s}\int p_a(t)dt = \left(W_{on} + W_{off}\right)f_s \tag{2.1}$$

### 2.1.3 Performance Characteristics of the SCR and GTO

**SCR.** The silicon-controlled rectifier (SCR), developed by GE in 1958 and shown schematically in Figure 2.7, is the lowest cost per rated kVA and is capable of controlling the greatest amount of power. In utility DC transmission line applications, series-connected light-triggered SCRs are employed in inverters and rectifiers that interface the utility system to DC transmission lines which can carry about 1 kA and 1 MV [7]. The device is widely used in cycloconverters, high-voltage DC systems and Static Var Compensators (SVCs).

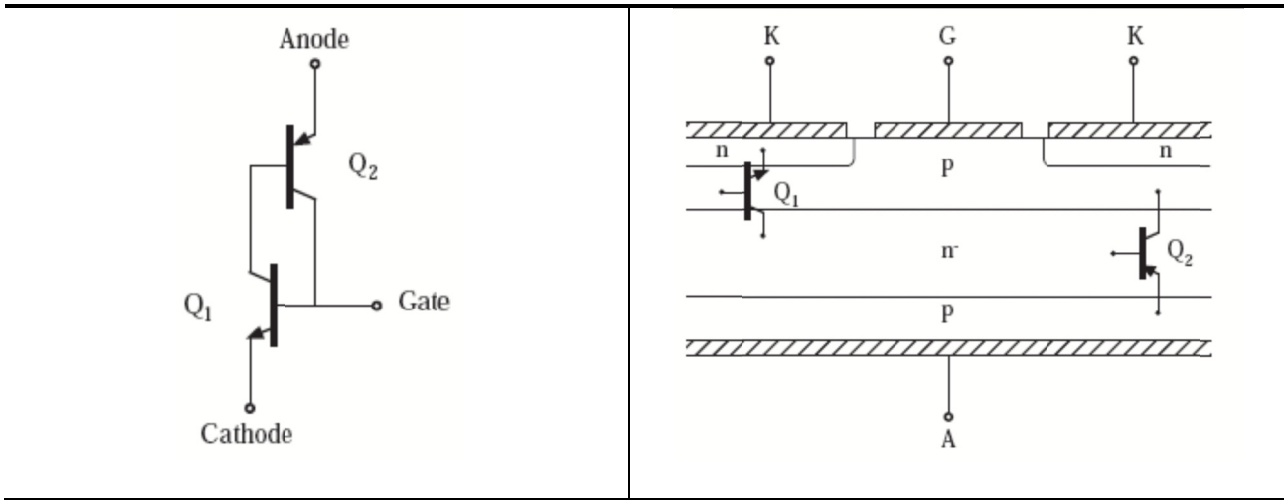



**Figure 2.7** Equivalent Circuit of SCR (L) and Cross Section of SCR (R) [7]

The SCR is capable of blocking both positive and negative anode-to-cathode voltages. The device is turned ON when the applied anode-to-cathode voltage is positive. This applied potential causes $Q_1$ to turn ON, due to a positive gate current, which in turn supplies base current to $Q_2$ and causes this effective transistor to turn ON. According to [6], the turn-on time is 14 μs. While in the ON state, the SCR can be modeled as a forward-biased diode junction in series with a low-value on-resistance. Regardless of the gate current, the device cannot be turned OFF except if a negative anode current (zero current crossing) or negative anode-to-cathode voltage is applied to the terminals of the semiconductor [7].

During the turn-off transition, the rate at which the forward anode-to-cathode voltage is reapplied must be limited to avoid retriggering the SCR. After the first zero crossing of the anode current, it is necessary to wait for a period of time before reapplying positive anode-to-cathode voltage to allow the minority stored charge to be actively removed from the depletion region via negative anode current. This period of time is minimized in inverter-grade SCRs [7]. The total turn-off time for the device is roughly 1200 μs [6].

**GTO.** The discussions on the gate turn-off (GTO) thyristor will be limited to the *conventional* GTO without the recent advances made in other devices using the GTO structure. The GTO, developed by the Japanese since the 1980s, is a SCR but fabricated with modern techniques allowing the device to take on a smaller, compact size.

The GTO is a latch-on device but it is also a latch-off device. The required gate current for turn-off is quite large. The gate current pulse for turn-on may be 30 A (3-5% of rated device current) for 10 μs for a 1000 A device, but the turn-off gate current would be 300 A (30-50% of rated device current) or larger for 20-50 μs. The voltage required to drive this current is about 10-20 V [5]. The energy required for turn-off is not very large, but, when considering the number of valves and turn-off events in a converter, the economic liability of the GTO becomes a significant factor to consider for the circuit designer.

Compared to the IGBT discussed next, the GTOs principal handicap is the relatively large gate turn-off drive requirements, emphasized earlier. This issue results in long turn-off time, and lower *di/dt* and *dv/dt* capability resulting in more costly turn-on and turn-off snubber circuits. Due to its slow turn-off, the conventional GTO is found in voltage-sourced converters operating under pulse width modulation (PWM) techniques using a relatively low frequency (a few hundred hertz). The major benefit to the GTO is its lower forward voltage drop. The GTOs

forward voltage drop is about 50% lower compared to an IGBT of the same rating. This is mainly due to the cathode area, divided into circular islands, being 50% less compared to a traditional thyristor [5].

### 2.1.4 Performance Characteristics of the IGBT

The insulated-gate bipolar transistor (IGBT), developed by GE in 1983, is a device that is part way to being a thyristor but is designed to not latch into full conduction equivalent to a voltage drop of one junction. The device also has an integrated MOS structure with insulated gate, like a MOSFET, as shown in Figure 2.8.

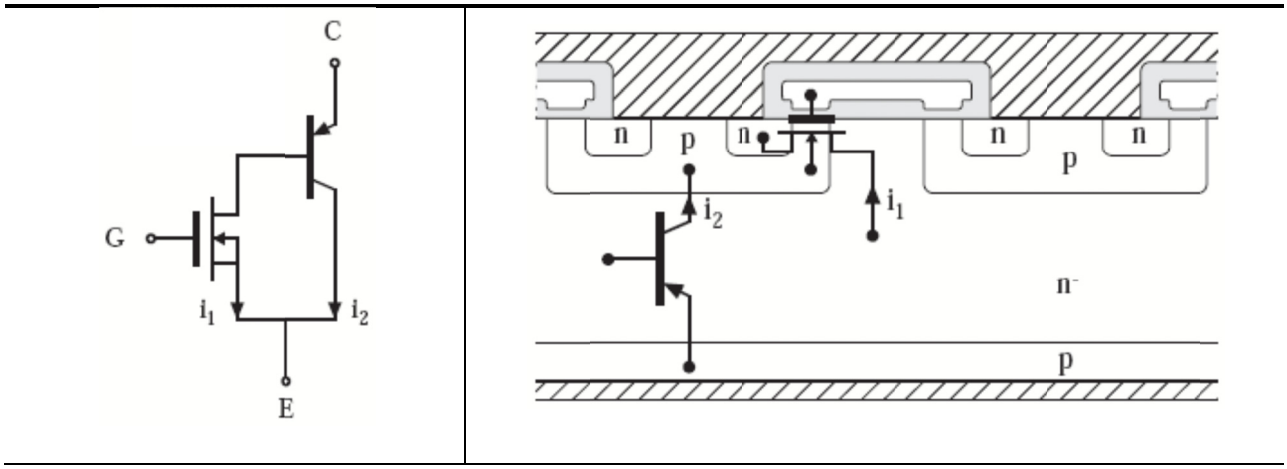



**Figure 2.8** Equivalent Circuit of IGBT (L) and Cross Section of IGBT (R) [7]

The advantage of the IGBT is its fast turn-on (1 μs) and turn-off (2 μs) times because the IGBT is a majority carrier device [6]. For this reason, the IGBT has been used in PWM converters operating at high frequency. Being a transistor based device, the IGBT has a higher forward voltage drop compared to a thyristor based device like a GTO. The major advantages of the IGBT in high-power applications are its low-switching losses, fast switching, and current-

limiting capability. The current-limiting capability is extremely valuable in voltage-sourced converters due to the potential presence of fault currents that can rise to high levels very rapidly. The IGBT has become the workhorse for industrial applications and has reached sizes capable of applications in the range of 10 MW or more [5].

### 2.1.5 Concluding Remarks on High Power Semiconductor Technology

The optimum power semiconductor device would have a low on-state voltage drop (such as a thyristor) as well as low gate-drive requirements and fast turn-off (like the IGBT). There are a number of devices in the marketplace that are replacing the conventional GTOs. These devices include the MOS Turn-Off Thyristor (MTO), Emitter Turn-Off Thyristor (ETO), and the Integrated Gate-Commutated Thyristor (IGCT). A nice comprehensive summary of the ratings, as of 2006, of various devices, including the state of the art devices previously mentioned, in comparison to each other is found visually in Figure 2.9.

The device capabilities have steadily increased since 2006. For example, ABB has increased its IGCT ratings from 6 kV / 3 kA to 6.5 kV / 3.8 kA and, recently, developed a 10 kV rated IGCT [29, 30, 31]. The device is expected to be on the market by 2012. Current research in power semiconductor device technology has been focused on self-powered ETO designs. A self-powered design implies that no external power supply or isolation transformer is necessary for powering the gate drive circuit resulting in lower system cost and simplified structure design. Current self-powered ETO designs are rated for 4.5 kV / 4 kA applications [32].

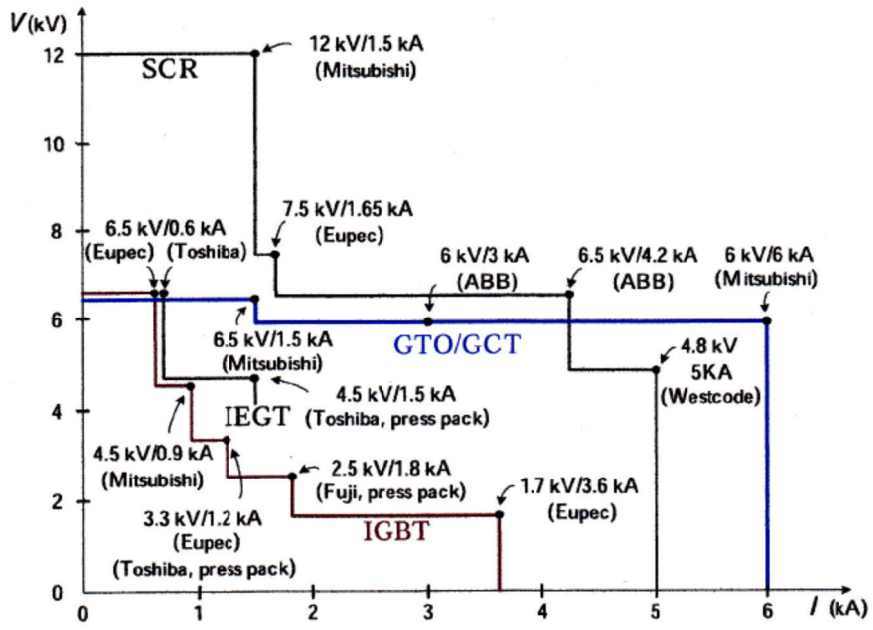



**Figure 2.9** Summary of Power Semiconductor Voltage and Current Ratings [8]

## 2.2 PRACTICAL MULTILEVEL VOLTAGE-SOURCED INVERTER TOPOLOGIES AND CONTROL

The primary function of a voltage-sourced inverter (VSI) is to convert a fixed DC voltage to a three-phase AC voltage with variable magnitude and frequency. VSI will, without question, be used more often in transmission and distribution systems in the future. The implemented VSIs for high voltage DC (HVDC) applications have been based on two or three-level technology, where a level represents a voltage state (DC positive voltage, DC negative voltage, or zero) of the output voltage waveform [9].

The idea of using multiple voltage levels to build the AC output voltage from the inverter due to the constraints of the power semiconductor ratings was proposed in the 1980s. Advantages of a multilevel approach include better power quality, electromagnetic compatibility,

low switching losses, and high voltage capability. The disadvantages of the multilevel inverters are the larger number of switching semiconductors required to perform the power conversion and the fact that the DC side voltage is supplied by capacitors or isolated voltage sources [10].

With advances in semiconductor technology, the multilevel concept has been taken from theory into practice by many of the top manufacturers in the electric drives business. Multilevel inverters, in general, are considered the state-of-the-art power conversion systems for high-power and power quality demanding applications [11]. For this reason, two of the most common multilevel inverter topologies, including the neutral point clamped (diode-clamped) topology and flying-capacitor design, will be discussed in this section of the thesis as well as the three common PWM techniques for switching the semiconductors in these converters.

### 2.2.1 Fundamentals of Multilevel Inverters

Multilevel converters are power conversion systems composed of an array of power semiconductors and capacitive voltage sources that, when properly controlled, can generate a multiple-step voltage waveform with variable and controllable frequency, phase and amplitude [11]. The number of levels, *n*, of a converter, previously referred to as a state in the output waveform, is defined as the number of steps or constant voltage values that can be generated by the converter between the output terminal and any internal reference node (the DC-link node) within the converter.

A qualification of a multilevel converter to be referred to as being multilevel is that each phase of the converter has to generate at least three different voltage levels. Figure 2.10 contains three inverter structures. The topology on the far left is an inverter, but it is not a multilevel

inverter because the output is that of a classical voltage source inverter. The middle and far right topologies are three and five-level topologies and are classified as multilevel inverters.

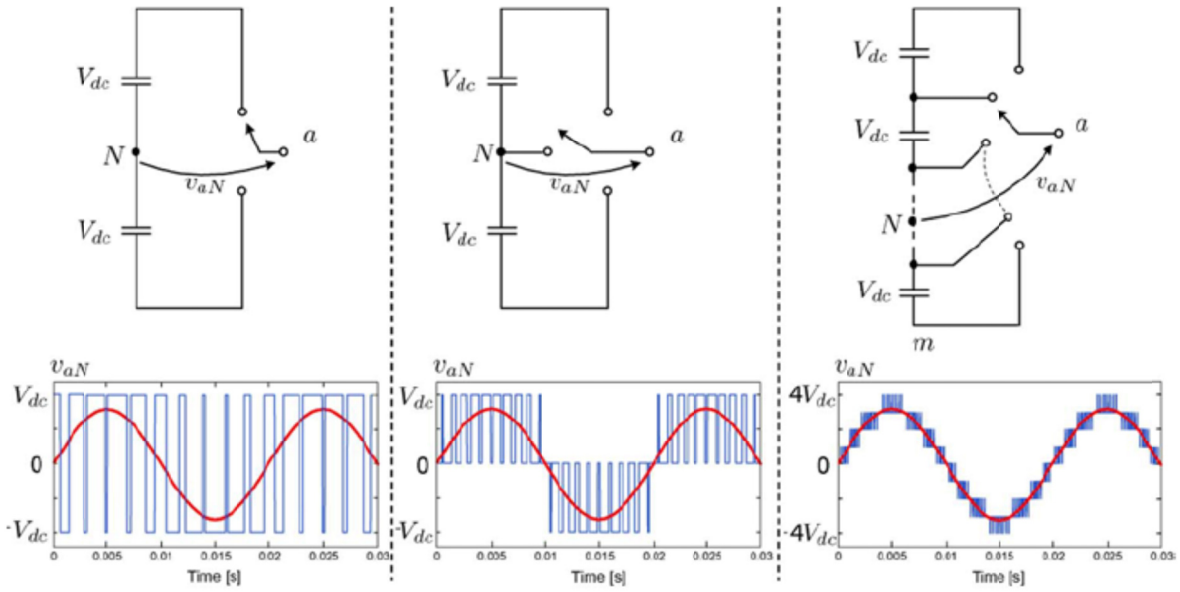



**Figure 2.10** Definition of a Multilevel Inverter [11]

The number of levels is always defined by the number found in the line-to-neutral voltage output, which are equally distant from each other. When considering a three-phase system, the levels of one phase are combined with those of the other phases generating $(2n - 1)$ voltage levels in the line-to-line voltage waveform, where $n$ is the phase to neutral voltage levels. The levels that are produced by the inverter add a new degree of freedom, from the control perspective, giving more alternatives to generate the desired output waveform. For this reason, multilevel inverters have the capability of improving power quality resulting in lower voltage distortion and reduced $dv/dt$ as described earlier [11].

There are many ways for combining the power semiconductors and capacitors to generate the multilevel output voltage. However, only some topologies have been adopted in practice,

and two of three will be discussed in extensive detail next because they are used in the model development of the MVDC network described in Chapter 4.

### 2.2.2 Neutral Point Clamped (NPC) Inverter

A three-level neutral point clamped (NPC) inverter, also known as a diode clamped inverter, is found in Figure 2.11. The NPC inverter can generally be configured as a three, four, or five-level topology, but only the three-level inverter has found wide application in high-power medium voltage drives [8]. For the purposes of explaining the NPC inverter, we will focus on the three-level design, but the details of the five-level NPC will be shown because it is this inverter topology that was chosen to be implemented in the medium voltage DC network.

The three-level NPC inverter is composed of two traditional two-level voltage source inverters stacked on top of another with minor modifications per phase leg. The two-level inverters are connected by two clamping diodes to form the neutral point, thus dividing the DC-link voltage in two. The advantage of connecting the semiconductors in this fashion allows the power devices to block only half of the total converter input voltage.

A brief note on the control of the switches is worth mentioning here, although elaborated upon in more detail in section 2.4. There are only two control signals per phase, which are complementary in nature to avoid a DC-link short circuit. The gate signal is binary in nature, represented by a zero for the OFF state of the switch and a one for the ON state. Table 2.2 provides the three different switching states of the three-level NPC inverter with associated voltage outputs. Figure 2.12 is a visual interpretation of Table 2.2 and provides the current flows in the NPC inverter that are required to obtain the desired voltage outputs indicated in Table 2.2.

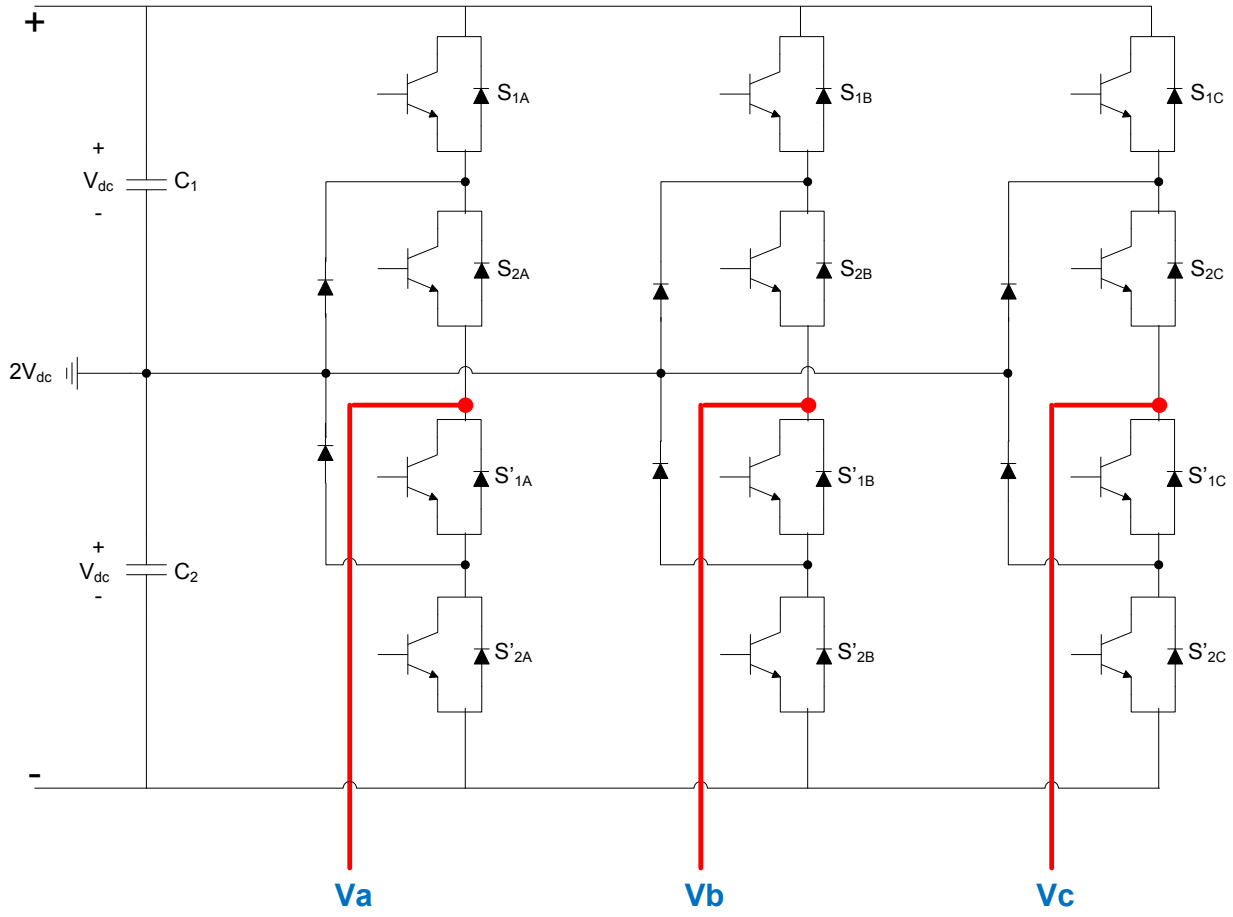



**Figure 2.11** Three-Level Neutral Point Clamped Power Circuit [11]

**Table 2.2** Binary Switching States for the Three-Level Neutral Point Clamp Inverter [11]

| | $S_1$ | $S_2$ | $S'_1$ | $S'_2$ | Voltage |
|---|---|---|---|---|---|
| I | 1 | 1 | 0 | 0 | $V_{dc}$ |
| II | 0 | 1 | 1 | 0 | 0 |
| III | 0 | 0 | 1 | 1 | $-V_{dc}$ |

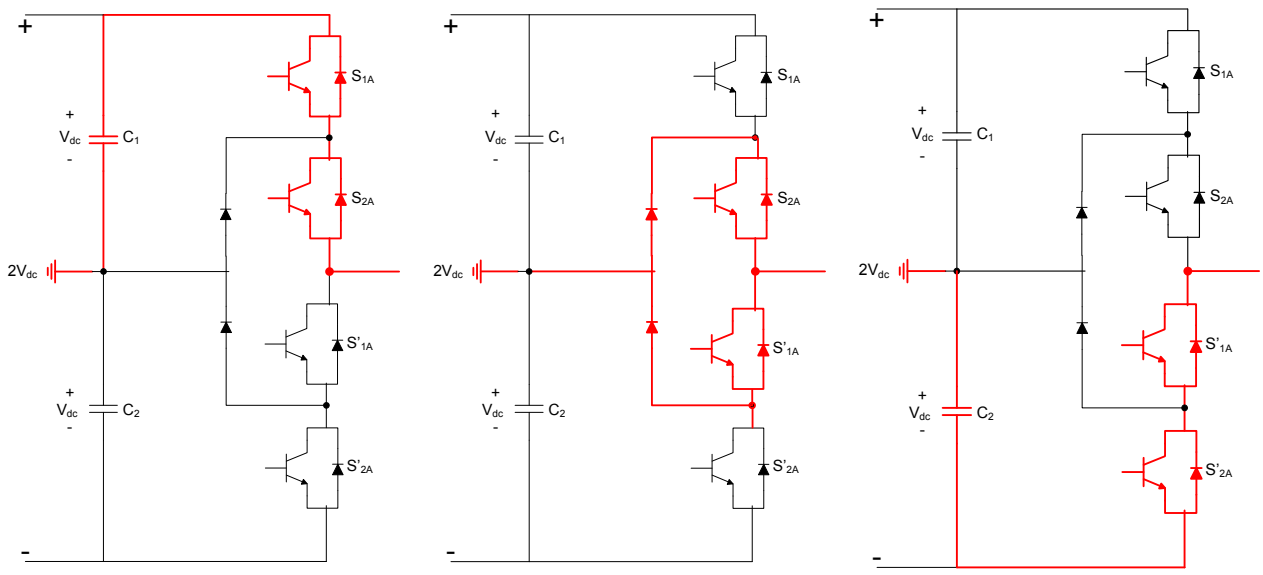



**Figure 2.12** Three-Level Neutral Point Clamped Switching States [11]

Figure 2.13 provides a five-level NPC inverter composed of four capacitors labeled $C_1$, $C_2$, $C_3$, and $C_4$. If a DC voltage is applied across the terminals of the inverter, the voltage across each capacitor will be $V_{DC}$ / 4, and each device voltage stress will be limited by the clamping diodes to $V_{DC}$ / 4.

In general, each active switching device is required to block a voltage level of $V_{DC}$ / ($n$-1) and the number of diodes required for each phase will be ($n$-1) x ($n$-2). When $n$ becomes sufficiently high, the number of diodes required will make the system impractical to implement. If the control strategy for the switches is based on PWM, the diode reverse recovery of the clamping diodes becomes the major design challenge in high-power applications [12].

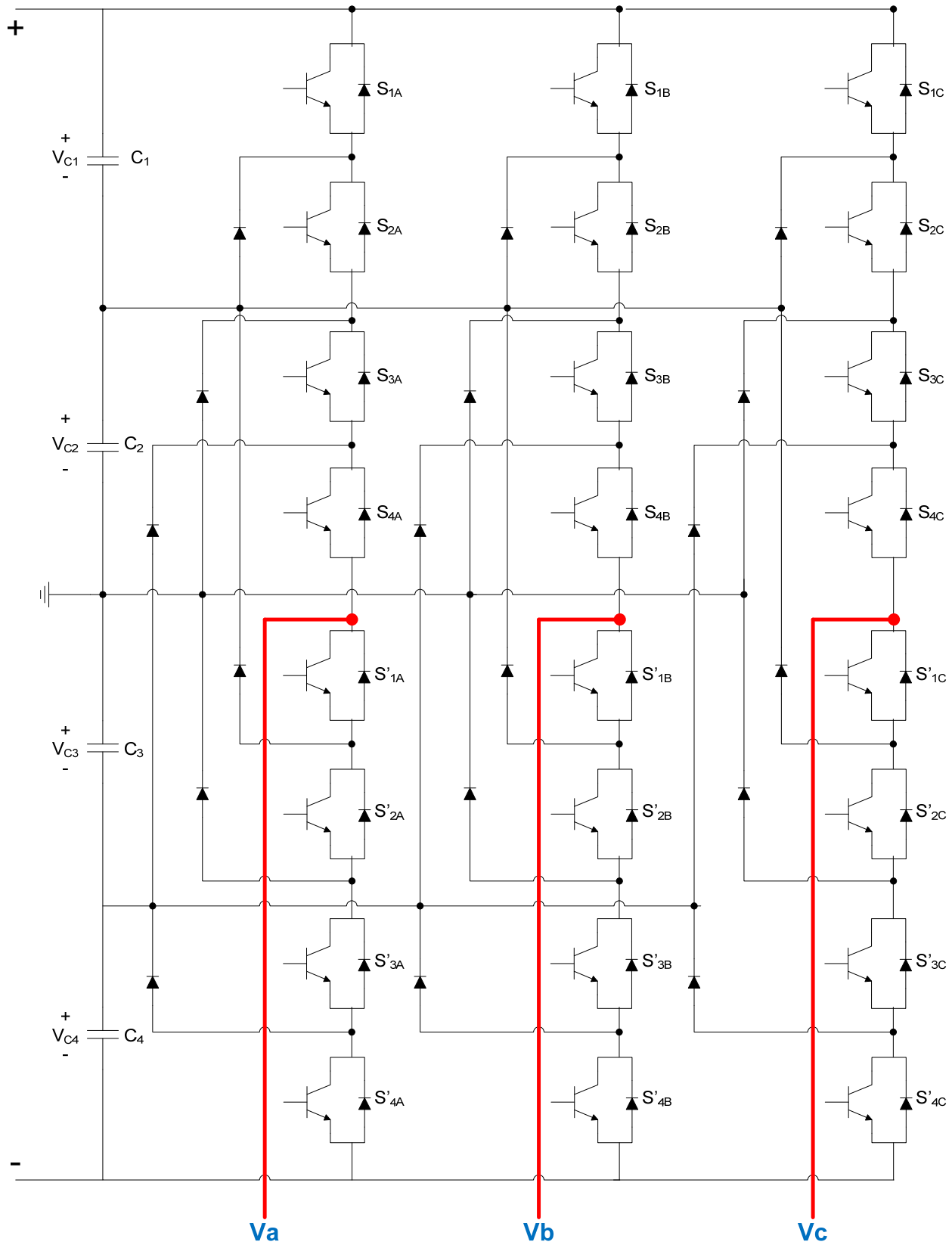



**Figure 2.13** Five-Level, Neutral Point Clamped Inverter [11]

**Table 2.3** Binary Switching States for the Five-Level Neutral Point Clamp Inverter [12]

| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S'_1$ | $S'_2$ | $S'_3$ | $S'_4$ | Voltage |
|---|---|---|---|---|---|---|---|---|---|
| I | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | $V_{dc}/2$ |
| II | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | $V_{dc}/4$ |
| III | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| IV | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | $-V_{dc}/4$ |
| V | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | $-V_{dc}/2$ |

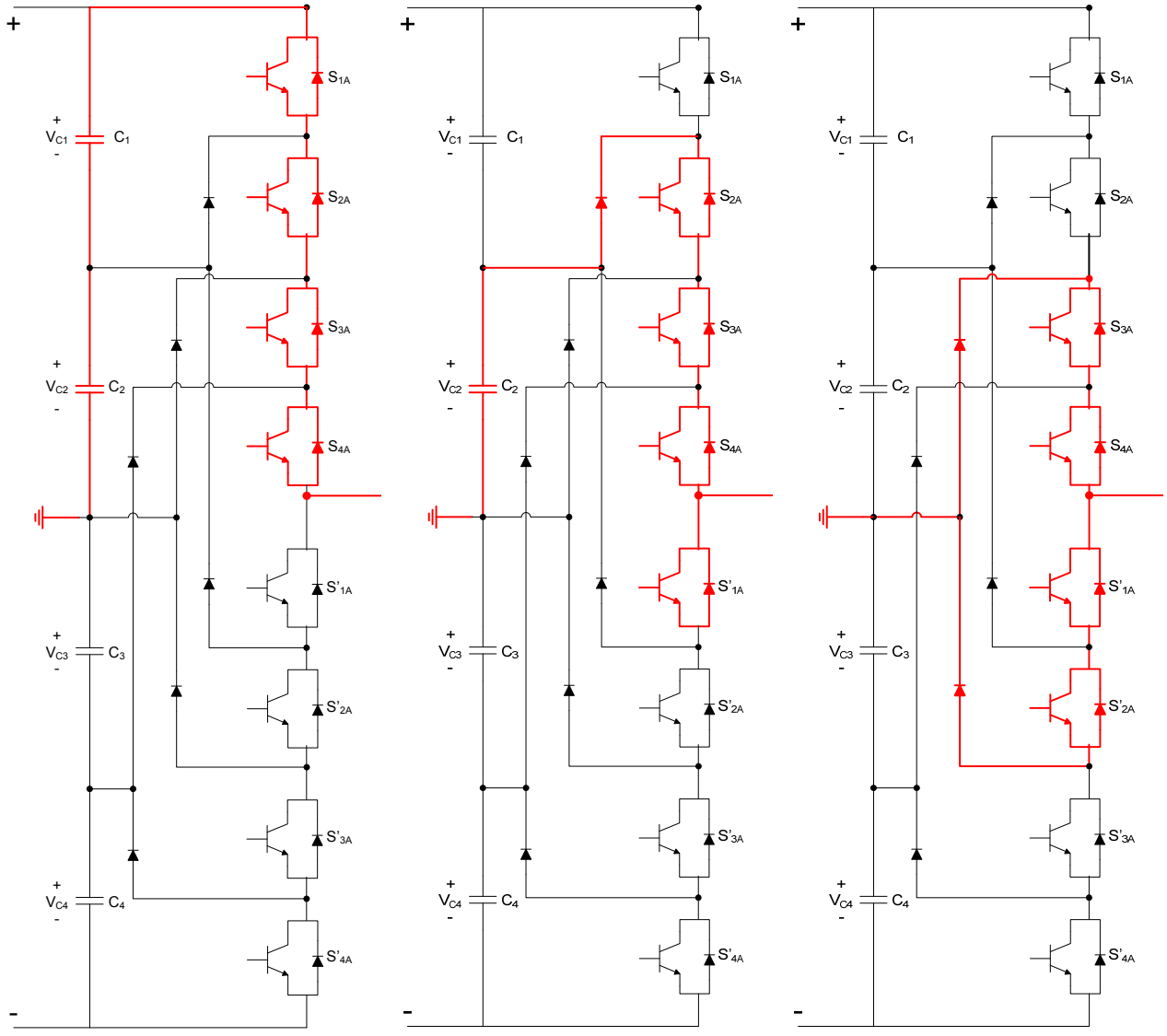



**Figure 2.14** Five-Level, Neutral Point Clamped Switching States (States I-III shown)

Table 2.3 provides the five different switching states of the five-level NPC inverter with associated voltage outputs. Figure 2.14 is a visual interpretation of Table 2.3 and provides the current flows in the NPC inverter that are required to obtain the desired voltage outputs indicated in Table 2.3.

### 2.2.3 Advantages and Disadvantages of the NPC Inverter

The NPC inverter offers many features that make it a prime candidate for many power conversion applications. Each of the switching devices withstands $V_{DC}$ / ($n$-1) of the total DC voltage during switch commutation, hence, there is no dynamic voltage sharing problems associated with this converter. The line-to-line voltage waveform is composed of (2$n$-1) levels leading to lower total harmonic distortion, THD, and *dv/dt* compared to a classical two-level inverter operating at the same voltage rating and switching frequency [8].

The NPC also has drawbacks including the additional clamping diodes, complicated PWM switching pattern design, and possible deviation of the neutral point voltage causing an unbalance in capacitor voltage as the number of output voltage levels increases. The deviation of the neutral point voltage results from unbalanced DC capacitors due to manufacturing tolerances, inconsistency in switching device characteristics, or unbalanced three-phase operation. If the neutral-point voltage deviates too far, an uneven voltage distribution takes place leading to premature failure of the switching devices and an increase in the THD of the inverter output voltage [8].

In practice, the three-level NPC topology is used due to the voltage drift phenomena of the capacitors for inverters designed with more than three levels. Capacitor voltage deviations depend upon the net real power exchange between the AC and DC sides of the NPC inverter. It

has been theoretically shown that no PWM strategy can guarantee the voltage balance of the capacitors for a NPC inverter having more than three levels for *all possible operating conditions*. Figure 2.15 provides the regions for which the capacitors remain balanced (stable blue region) for a *n*-level ($n > 3$) inverter. Mathematically, the boundary is defined by (2.2), where *m* is the modulation index (discussed in section 2.2.5) and cos ϕ is the power factor [13].

$$m = \frac{\sqrt{3}}{\pi \cos\phi} \tag{2.2}$$

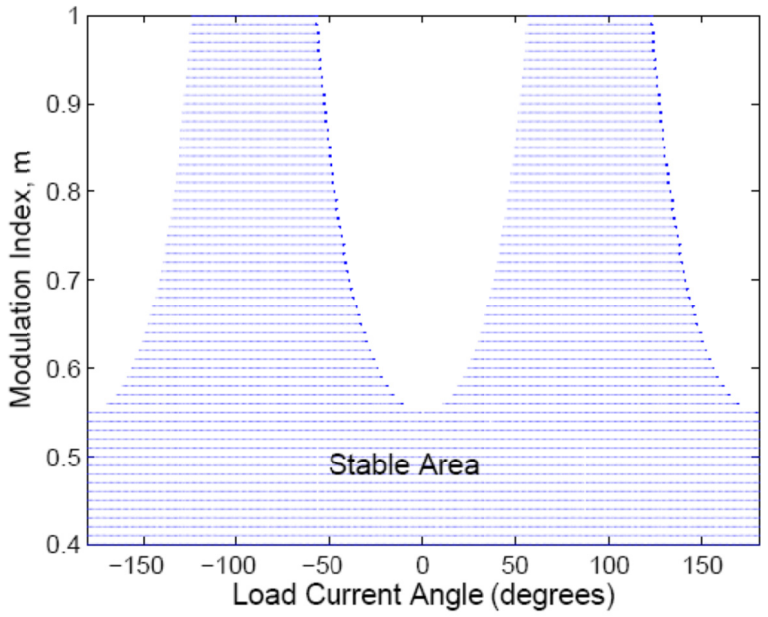



**Figure 2.15** Voltage Balancing Region for a n-level NPC Inverter [13]

In [13], the author developed a space vector modulation (SVM) technique, a more advanced mathematical algorithm for switching the semiconductors compared to PWM, which balances the capacitor voltages for a five-level NPC inverter. One of the main drivers for going beyond three levels is because such a configuration has been widely considered as a potential candidate for transformerless reactive power compensators. Clearly, when designing the inverters for the medium voltage DC network, Figure 2.15 will be of great importance.

### 2.2.4 Flying-Capacitor Configuration (Capacitor Clamped Inverter)

A five-level, flying-capacitor (FC) multilevel inverter topology is shown in Figure 2.16. The obvious difference between Figure 2.13 and Figure 2.16 are the capacitors, serving the role of the diodes in the NPC configuration, which clamp the voltage across the semiconductor device. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an *n*-level inverter will require a total of [(*n*-1) x (*n*-2)]/2 clamping capacitors per phase in addition to (*n*-1) DC bus capacitors (like the NPC inverter) [12].

The switching strategies for obtaining the five voltage states in the output of the inverter are found in Table 2.4. Because the circuit configuration is more eye appealing compared to the NPC configuration, switching state circuit diagrams capturing the current paths will not be emphasized in this document.

After reviewing Table 2.4, it would be obvious that the voltage synthesis of a five-level, FC inverter has more flexibility than a NPC inverter. There are more redundant switching states (multiple possibilities for achieving an output voltage level), a typical property of multilevel inverter designs. This asset of multilevel inverter designs is referred to in the literature as voltage level redundancy [12]. This attribute is used for control and optimization purposes especially when designing for fault tolerance in a converter.

### 2.2.5 Advantages and Disadvantages of the FC Inverter Topology

The main and probably the most important difference between the NPC topology and the FC topology is that the FC has a modular structure and can be easily extended to achieve a higher number of voltage levels and higher power ratings [12]. Individual valves are

**Table 2.4** Binary Switching States for the Five-Level Flying Capacitor Topology [12]

| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S'_1$ | $S'_2$ | $S'_3$ | $S'_4$ | Voltage |
|---|---|---|---|---|---|---|---|---|---|
| I | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | $V_{dc} / 2$ |
| II | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | $V_{dc} / 4$ |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | |
| III | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| IV | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | $-V_{dc} / 4$ |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | |
| | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | |
| V | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | $-V_{dc} / 2$ |

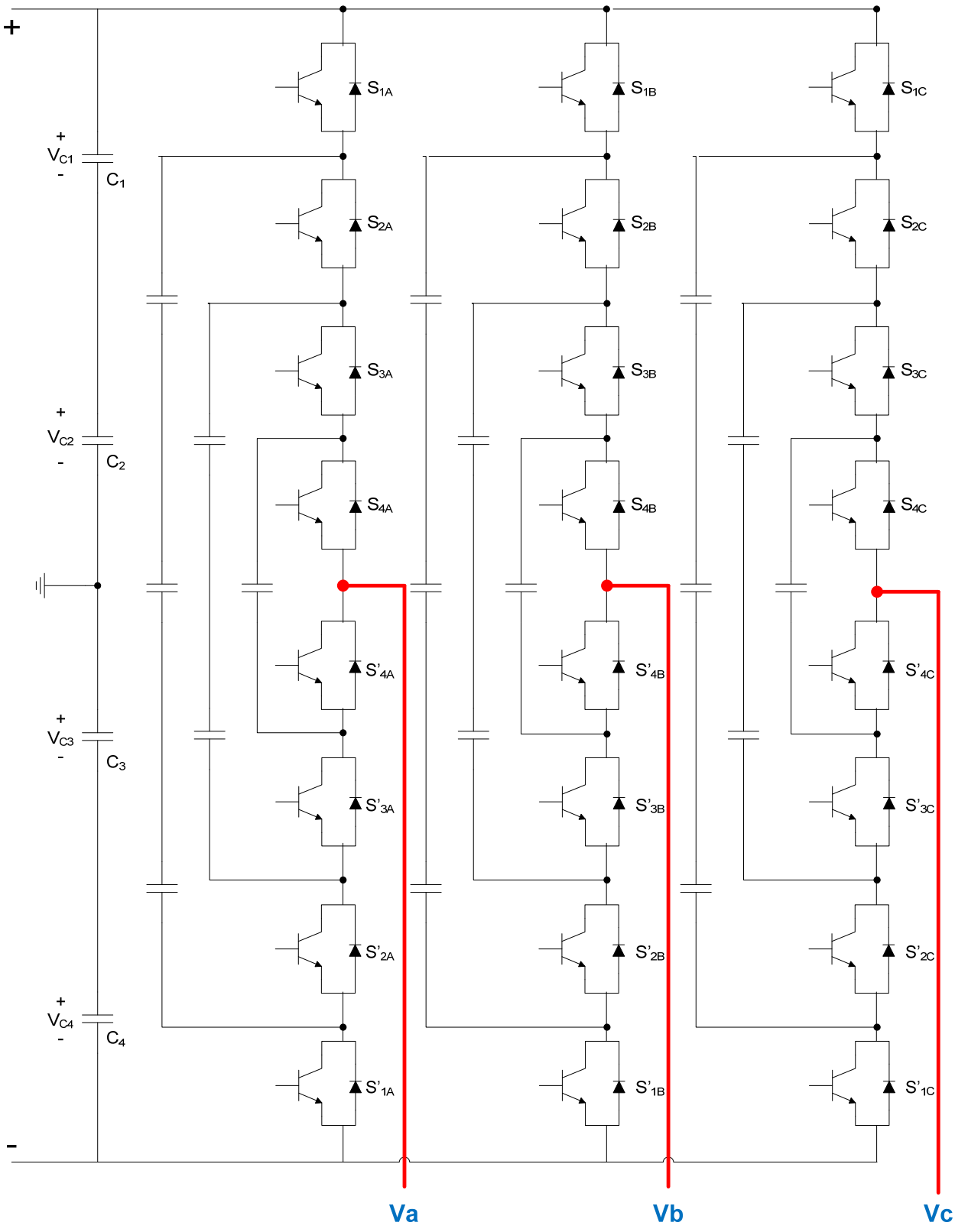



**Figure 2.16** Five-Level, Flying-Capacitor Multilevel Inverter Circuit Topology [11]

switched approximately half the number of times in the five-level topology and the harmonic performance is still superior compared to the NPC [14]. However, the FC inverter requires several banks of *bulky* DC capacitors, each of which needs a separate pre-charge circuit.

The DC-link voltage unbalance in NPC inverters requires sophisticated SVM techniques to resolve the problem. However, FC inverters have natural balancing of the capacitor voltages when using phase shifted-PWM techniques (discussed in next section), although for other modulation methods or for a faster DC-link balance, the state redundancies will need to be taken into account to design for better voltage control [11]. Because the DC capacitor voltages in the inverter normally vary with the inverter operating conditions, the voltages on the DC flying capacitors need to be tightly controlled, which increases the complexity of the control scheme [8].

### 2.2.6 Multilevel Inverter Modulation Principles and Techniques

With the development of multilevel inverter topologies appeared the challenge to extend existing modulation methods (switch control) to the multilevel case. The methods that have been developed had to consider the additional complexity of the inverters having more power electronics devices to control but also take into account the extra degrees of freedom provided by the additional switching states as described in section 2.2.4 [12]. A large number of modulation algorithms have been developed, and the three most suitable and practical techniques will be discussed in the remainder of this section. First, to explain the concept of PWM, a half-bridge inverter shown in Figure 2.17 will be used as an example. The DC input voltage is 200V, modulation index, $m_a$, of 0.6 and frequency modulation ratio, $m_f$, of 39.

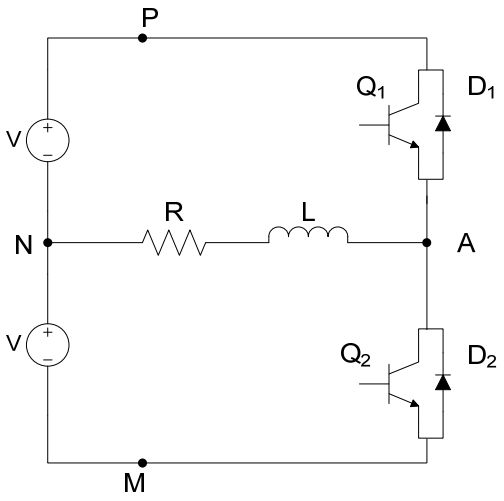



**Figure 2.17** Half-Bridge Inverter for Explaining PWM Concept

The shaping of the output voltage waveform is generally achieved by having multiple pulses in each half-period of the AC waveform. The classical method for implementing sinusoidal pulse width modulation (SPWM) is to use two waveforms as shown in Figure 2.18. Note that Figure 2.18 is roughly half a period. One signal is a sinusoid having the desired AC signal frequency (typically 60Hz) and is referred to as the "reference" signal. The triangular signal, found in Figure 2.18, is a high frequency voltage signal that is referred to as the "carrier" signal.

There are two major points that should be emphasized with regards to SPWM. The first point is that the waveforms of the carrier and the reference signal are used to obtain the timing waveform to operate switches $Q_1$ and $Q_2$ in Figure 2.17. When the carrier waveform is less than the reference signal for a period of time, $Q_1$ is ON and $Q_2$ is OFF, thus obtaining the positive pulse in Figure 2.19. When the carrier waveform is greater than the reference signal for a period of time, $Q_1$ is OFF and $Q_2$ is ON, thus obtaining the negative pulse in Figure 2.19.

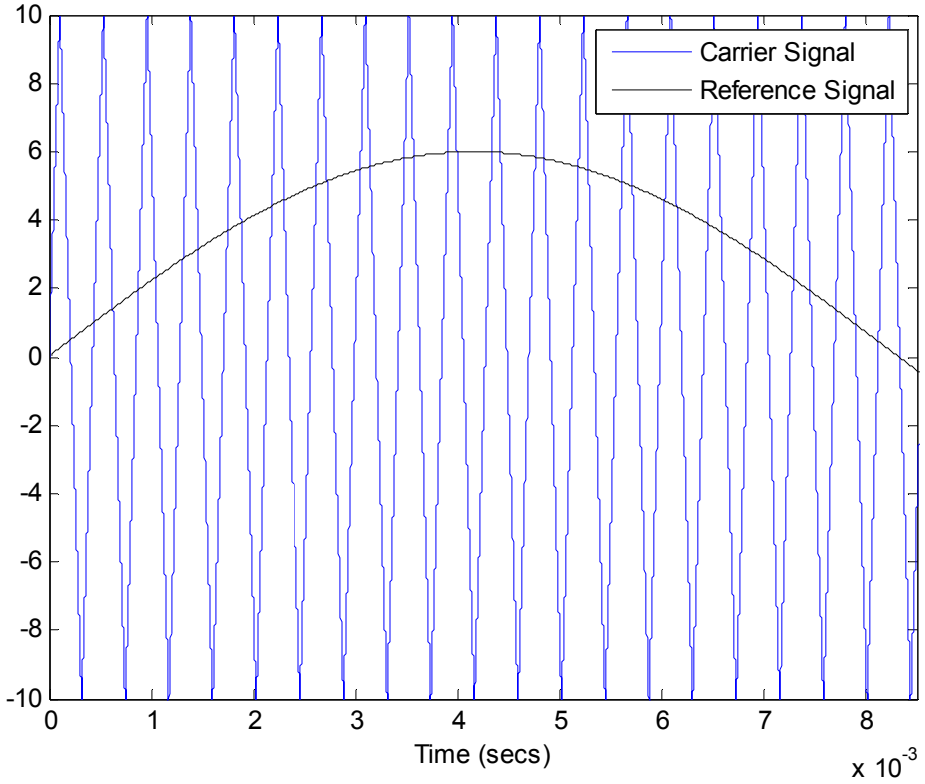



**Figure 2.18** Sinusoidal PWM Reference Sinusoid and Triangle Carrier Waveforms

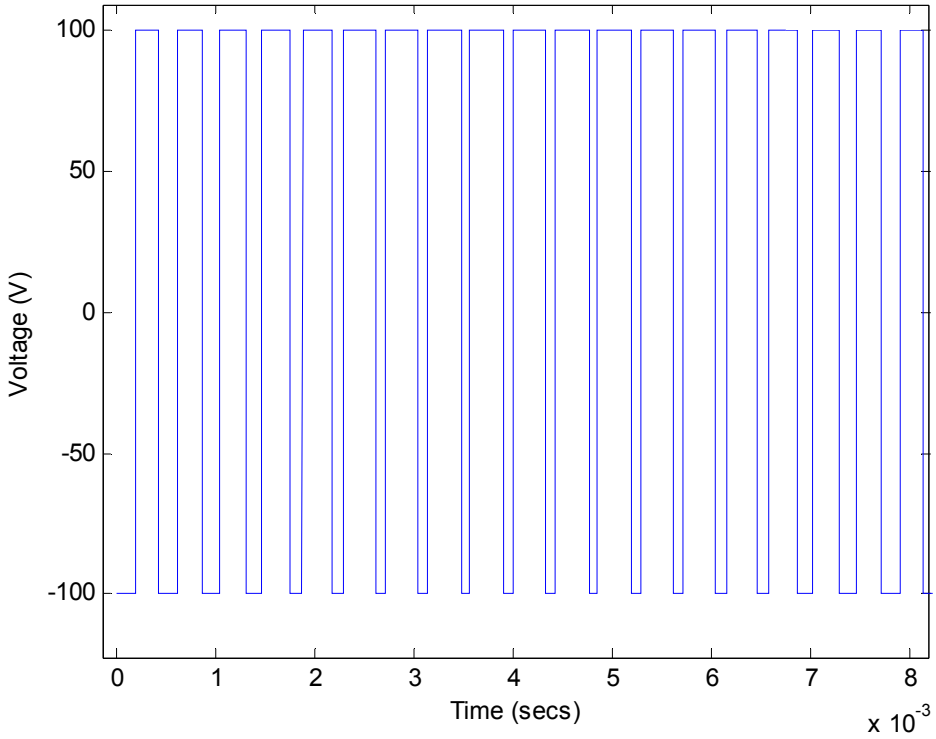



**Figure 2.19** Half-Bridge Output Voltage Waveform across RL Load

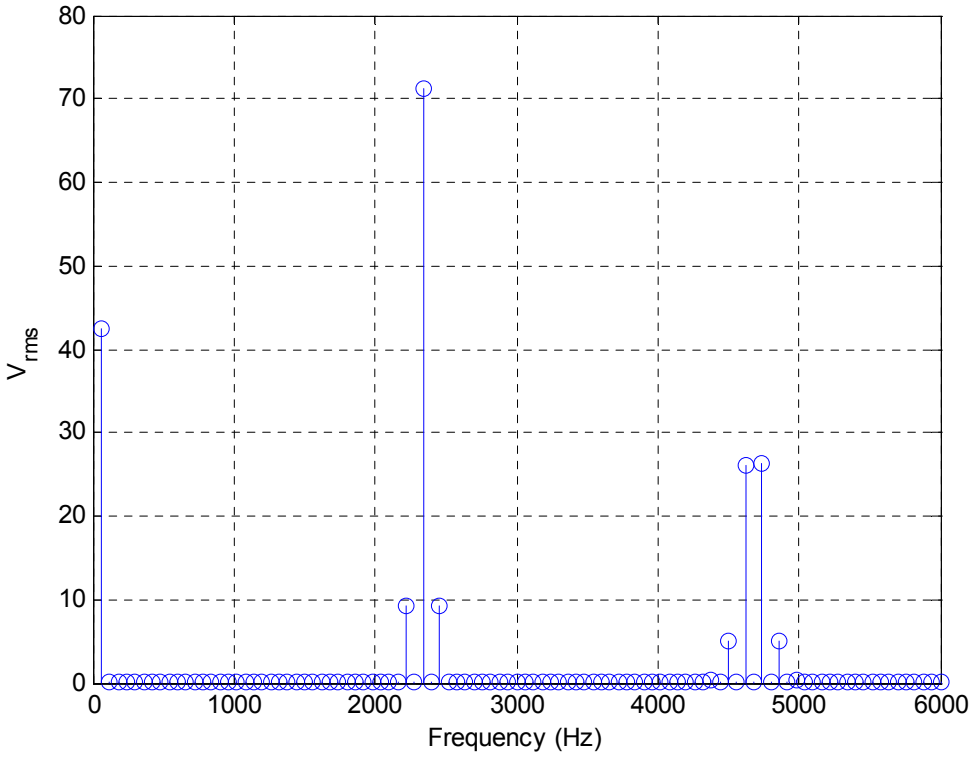



**Figure 2.20** Harmonics of Half-Bridge Output Voltage Waveform of **Figure 2.19**

The second point to mention is that by using SPWM, the harmonics of the output voltage of the inverter are shifted, with spectra shown in Figure 2.20, to frequencies far from the fundamental. The high frequency components can be removed with a low pass filter to obtain the desired fundamental component.

To conclude the PWM concept discussion, the definitions of the modulation indices previously mentioned are defined by (2.3) and (2.4), where $A$ is the amplitude and $f$ is frequency.

$$m_a = \frac{A_{reference}}{A_{carrier}} \tag{2.3}$$

$$m_f = \frac{f_{carrier}}{f_{fundamental}} \tag{2.4}$$

The three modulation schemes that were implemented in the inverters for the medium voltage DC network are the Phase Disposition (PD) technique, Phase Opposition Disposition (POD) technique, and Alternate Phase Opposition Disposition technique (APOD). All plots of these techniques have a $m_a$ value of 0.9 and $m_f$ value of 20.

A visual of the PD-PWM technique for one phase of a five-level inverter is found in Figure 2.21. There is one reference signal and four gate signals provided in this figure which span the entire amplitude range that can be generated by the inverter. There are eight switches per leg of the inverter but only four signals are required due to the complementary nature of the switch pairs. For this approach, the signals are in phase and level-shifted from each other. The POD-PWM strategy is found in Figure 2.22. This method requires that all positive carriers be in phase with each other but in opposite phase with the negative carriers. The carriers are level-shifted as was the case in the PD-PWM approach. The APOD-PWM algorithm found in Figure 2.23 is simply obtained by alternating the phase between adjacent carriers [11].

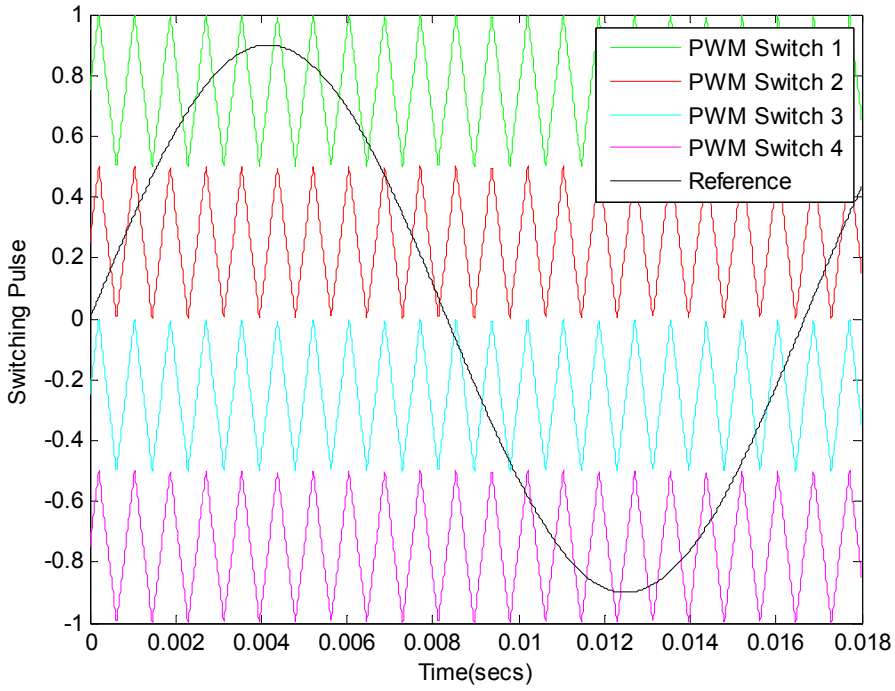



**Figure 2.21** Phase Disposition (PD) PWM Strategy

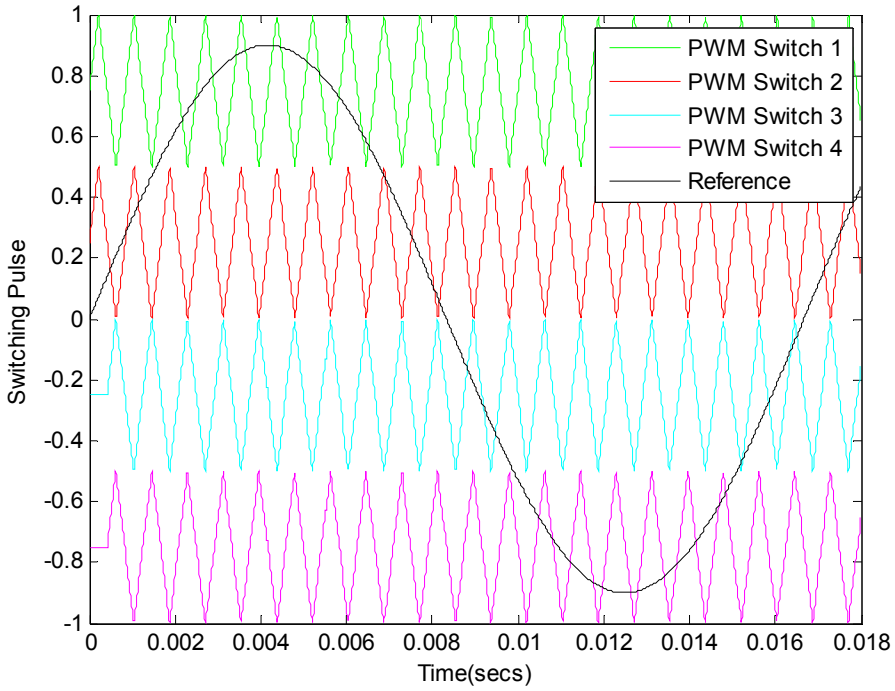



**Figure 2.22** Phase Opposition Disposition (POD) PWM Strategy

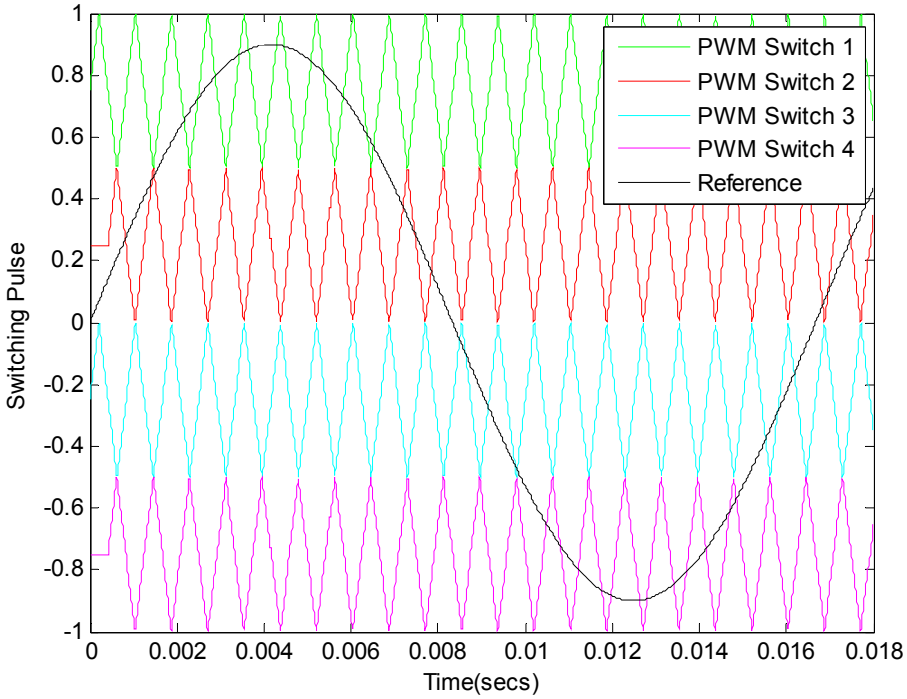



**Figure 2.23** Alternate Phase Opposition Disposition (APOD) PWM Strategy

## 2.3 MULTIPULSE RECTIFIERS

A rectifier, as opposed to an inverter, converts a waveform from AC to DC. The main feature of the multipulse rectifier lies in its ability to reduce current harmonic distortion. To comply with IEEE standard 519-1992, a standard that governs harmonic magnitudes, many drive manufacturers are increasingly using multipulse diode rectifiers which serve as the front-end to the inverter. The rectifiers on today's market can be configured as 12-, 18-, and 24 pulses per period and even 30 but 30 is seldom used in practice due to the increased transformer costs and minimum performance improvements [8]. In this thesis, a controlled, three-phase, six pulse rectifier will be described and implemented in the medium voltage DC network to provide the DC voltage used by all inverter components.

### 2.3.1 Operation of the Three-Phase, Six Pulse Bridge Rectifier

A three-phase bridge rectifier with controlled SCRs labeled $Q_1$ through $Q_6$ is found in Figure 2.24. The line-to-line output voltage waveform across the load is found in Figure 2.25 and line currents, assuming a large output inductance, in Figure 2.26. The rectifier, like all DC/DC converters, exhibits both continuous and discontinuous conduction modes depending on the inductive and capacitive values chosen. In general, two of the six semiconductor devices, whether they are diodes or thyristor based, will conduct during each interval. For this reason, the current will be zero for periods of time in the current waveforms found in Figure 2.26 [7].

If $Q_1$, for example, was uncontrollable, the device would conduct whenever the line-to-line voltage of $V_{ab}$ or $V_{ac}$ is largest in magnitude of the six line-to-line voltages possible, which are $V_{ab}$, $V_{bc}$, $V_{ca}$, $V_{ba}$, $V_{cb}$, and $V_{ca}$. This occurs for $120^o$ in each cycle [7].

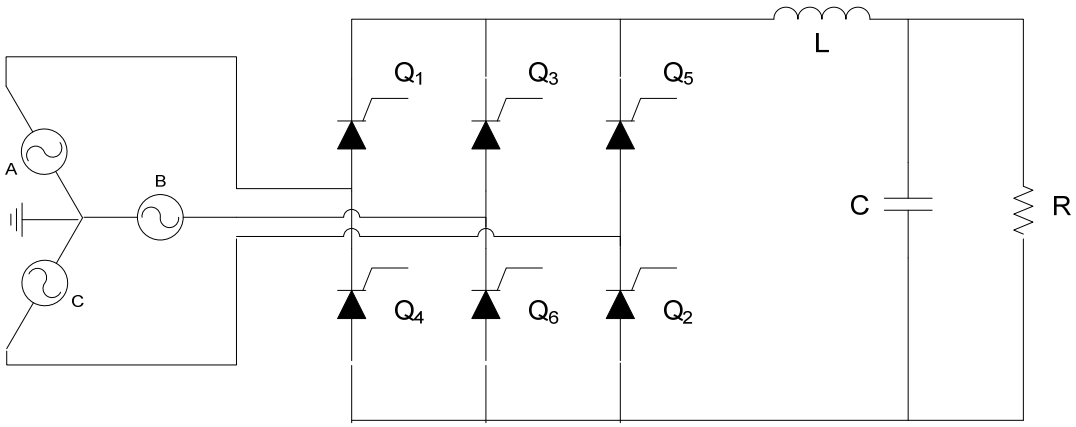



**Figure 2.24** Three-Phase Controlled, Six Pulse Rectifier Circuit [4]

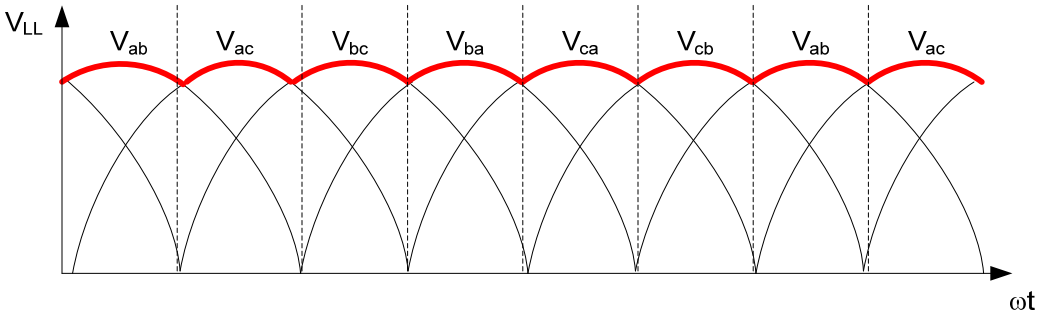



**Figure 2.25** Line-to-Line Output Voltage of Three-Phase Rectifier [4]

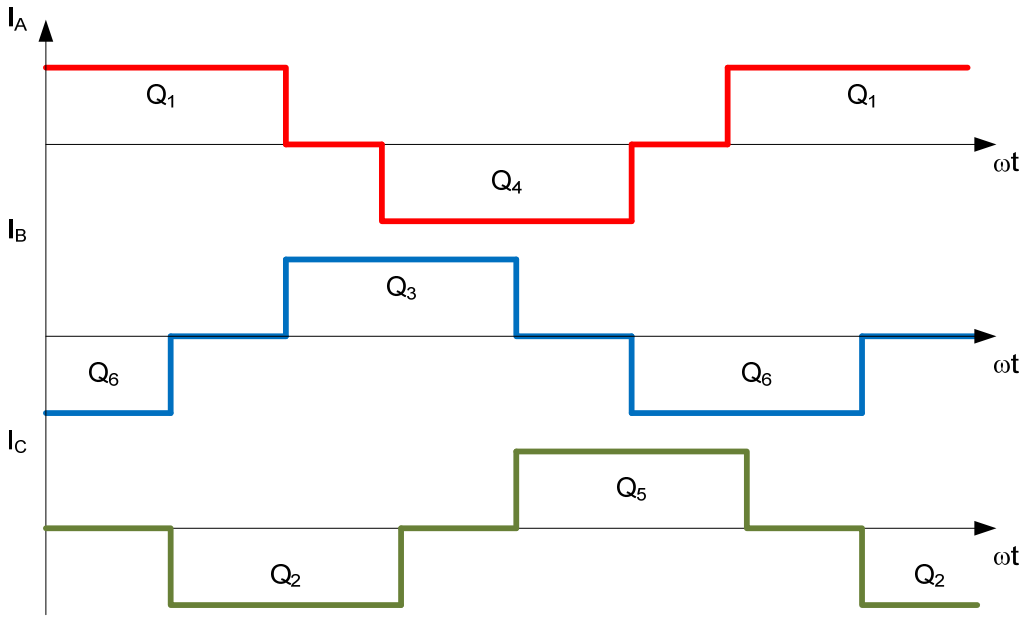



**Figure 2.26** Line Currents of Three Phase Rectifier with Active Switches [4]

The primary control variable in rectifier circuits is done through angular displacement as opposed to frequency in inverter applications. The average output voltage of the rectifier can be computed with (2.5). The parameter $\alpha$ is the firing delay, see Figure 2.27, applied to a controlled switch. In Figure 2.25, $\alpha$ is equal to zero. By varying $\alpha$, the average output DC voltage is able to shift up and down taking on a wide range of output voltages.

$$V = \frac{3\sqrt{2}}{\pi} V_{LL,rms} \cos\alpha \tag{2.5}$$

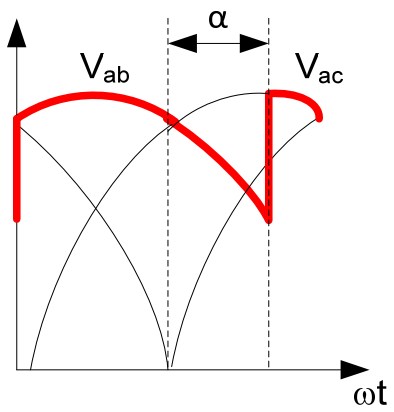



**Figure 2.27** Firing Delay in Rectifier Circuit

If the DC load is capable of supplying power, then it is possible to reverse the direction of power flow in the rectifier circuit. As shown in Figure 2.28, varying $\alpha$ beyond $90^0$ inverts the sign of the average output DC voltage, which implies that the load is delivering power, with a power factor equivalent to (2.6), to the three-phase AC system.

$$PF = 0.955\,|\cos(\alpha)\,| \tag{2.6}$$

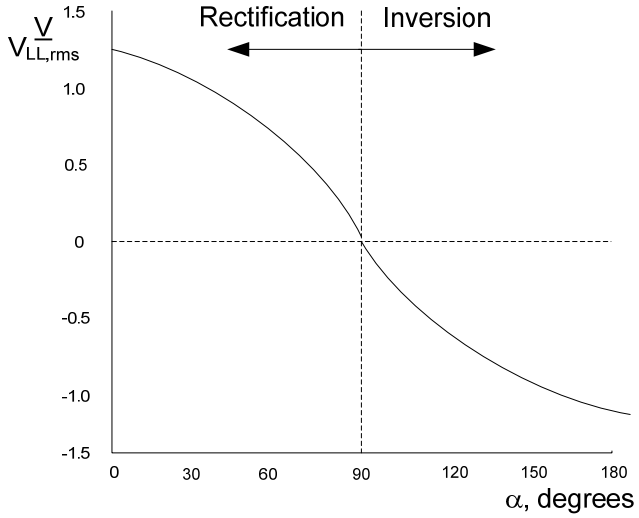



**Figure 2.28** Bidirectional Power Flow Capability in a Controlled, Three-Phase Bridge Rectifier [7]

## 2.4 BIDIRECTIONAL DC-TO-DC CONVERTER AND CONTROL

The final piece of theoretical power electronics knowledge used to establish the medium voltage DC network discussed in Chapter 4 is a discussion on the bidirectional DC-to-DC converter. The topology of the DC/DC converter, referred to as a dual active bridge (DAB) DC/DC converter, is found in Figure 2.29. The DAB topology is very attractive because of its zero-voltage switching capability, low component stresses (power dissipation), and high-power density features [15].

To help maintain the DC bus voltage of a medium voltage DC network, battery units can discharge through the bidirectional DC/DC converter and can be found in battery charging applications [16]. The topology in recent years has attracted wide interest not only for its bidirectional capability but because of its ability to serve as a DC transformer, which will be explained momentarily. The configuration has found widespread use on shipboard power

systems because of its galvanic isolation between two voltage levels through a transformer, full-bridge converters on both sides for high power applications and a current-fed converter on the low voltage side with a voltage-fed converter on the high voltage side [17].

The focus of the sections to come will be strictly on converter operation and will neglect deeper discussions on matters such as continuous conduction mode and discontinuous conduction mode (current waveform is zero for a portion of the switching interval) of DC/DC converters.

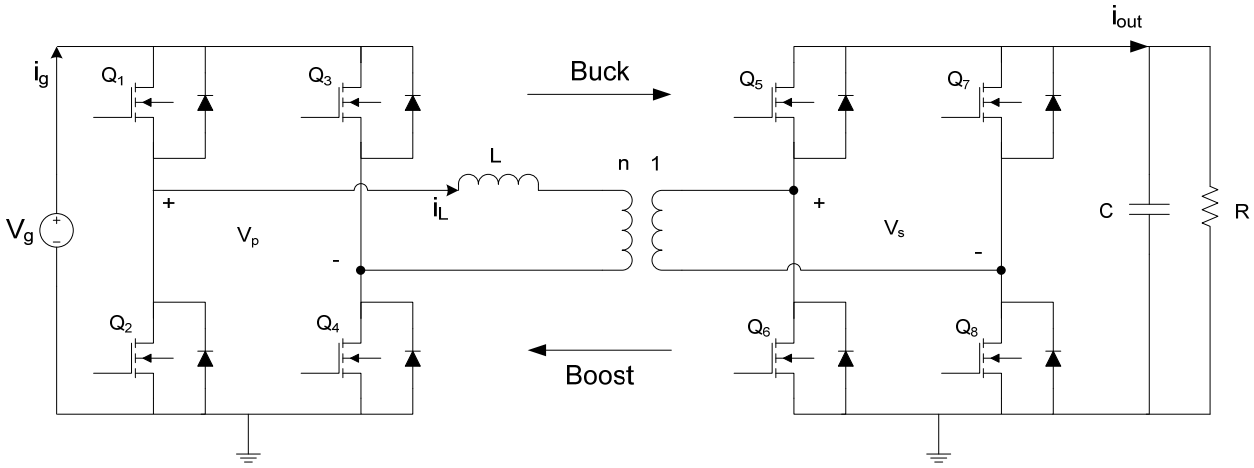



**Figure 2.29** Bidirectional DC/DC Converter [15, 16, 17]

### 2.4.1 Basic Operating Principles of the DAB DC/DC Converter

The bidirectional DC/DC converter shown in Figure 2.29 can operate as a buck converter with power flowing from the MVDC input, $V_g$, to the local load, or a boost converter with power flowing from the local load towards the MVDC bus. Based on conventional power system analysis, a rough calculation of the power flow from either bridge can be described by (2.7). Observing (2.7), net power will flow from the primary side of the converter to the secondary side if a delay exists between the primary and secondary side voltages. More specifically, if $\phi$ lies

between 0 and 90 degrees, power will flow from the primary side to the secondary side. If ϕ is between 90 and 180 degrees, power will flow from the secondary side to the primary side under the assumption that the load is a voltage source like a battery. Equation (2.7) is a normalized quantity based upon the medium voltage input, $V_g$, and appears fairly elementary. The derivation of (2.7), based on conventional methods found in [16], can be found in Appendix A of this document. For a more thorough treatment of the subject, readers are encouraged to view [15].

$$P_{out,norm} = \frac{8M}{\pi^2 X_s} \sin\phi \tag{2.7}$$

### 2.4.2 Strategies of Controlling the DAB DC/DC Converter

While performing the literature review, two techniques for controlling the switches of the DC/DC converter were found. The first approach, based on the components mentioned in the previous section, is to create a delay between the primary and secondary voltages and is illustrated in Figure 2.30. The waveforms illustrated are ideal and neglect the resonant transitions that may occur between the substrate capacitances of the semiconductors and line inductance.

Starting with the primary voltage, readers will notice numbers in each of the four intervals. These numbers are the switch numbers found in Figure 2.29. Notice that only two switches of the same full-bridge converter transition during each subinterval. When the secondary voltage lags behind the primary voltage, the converter operates in a charging (buck) mode. Similarly, when the secondary voltage leads the primary voltage, the converter operates

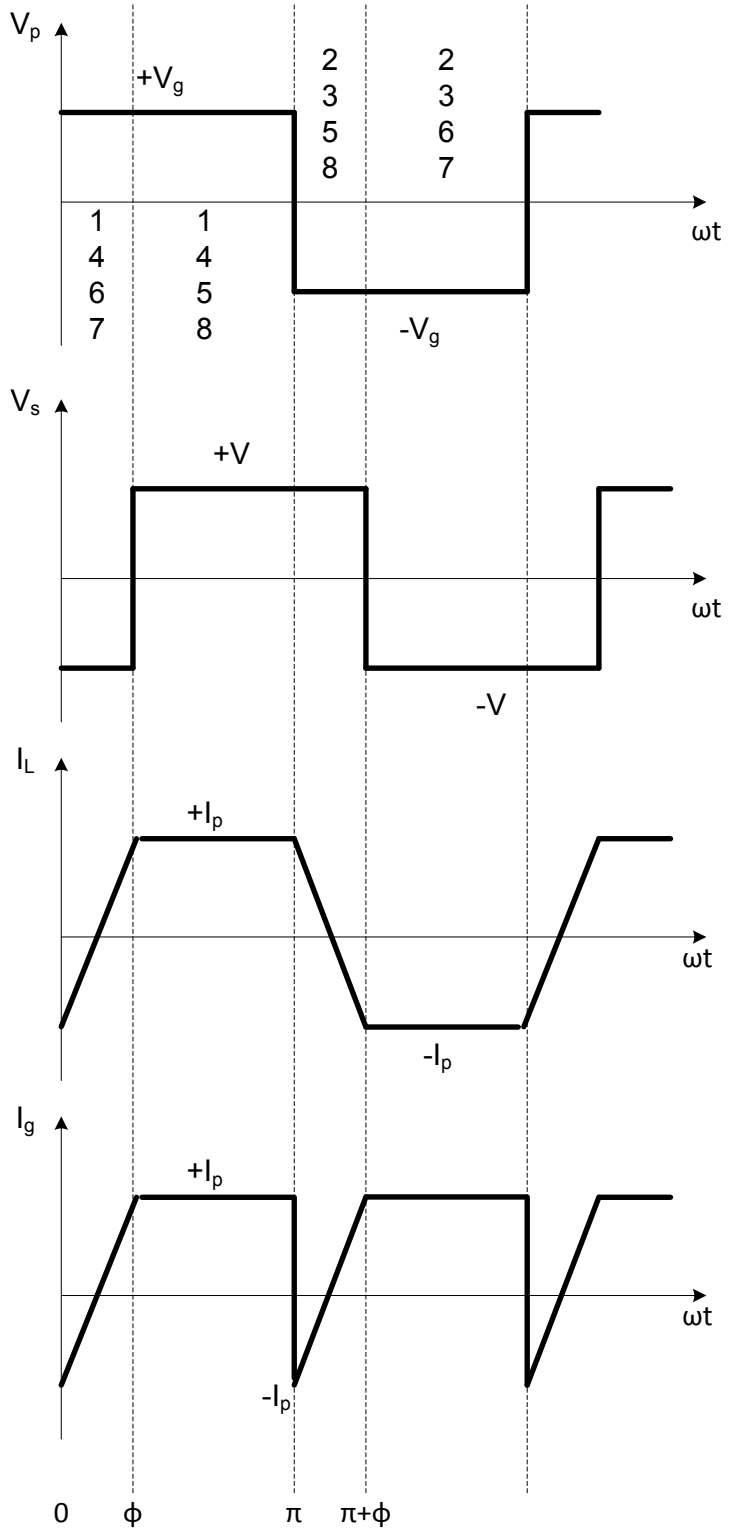



**Figure 2.30** Voltage and Current Waveforms of DAB DC/DC while Operating in Charging (Buck) Mode

in discharge (boost mode). For the remainder of this thesis, the focus will be on buck mode operation since this was the first step taken in the model development discussed in Chapter 4. The current signals shown in Figure 2.30 are the currents through the inductor, $i_L$, and gate current, $i_g$, seen by the primary side switches. The theoretical peak inductor current, $i_p$, is derived in Appendix A.

The advantage of the previously mentioned switching strategy is the control lever through the angular displacement of the primary and secondary side voltages allowing the medium voltage DC network to exchange power depending on operating conditions. The second approach found in [17] is slightly less sophisticated and minimizes controller complexity. If the converter operates in buck mode, switches $S_1$, $S_2$, $S_3$, and $S_4$ in Figure 2.29 will be switched ON and OFF in the circuit as the timing diagrams indicate in Figure 2.31. All remaining switches, $S_5$, $S_6$, $S_7$, and $S_8$, will be OFF and current will only flow through the anti-parallel diodes of these switches. Variables D and $T_s$ of Figure 2.31 represent the duty cycle and switching period of the converter, respectively.

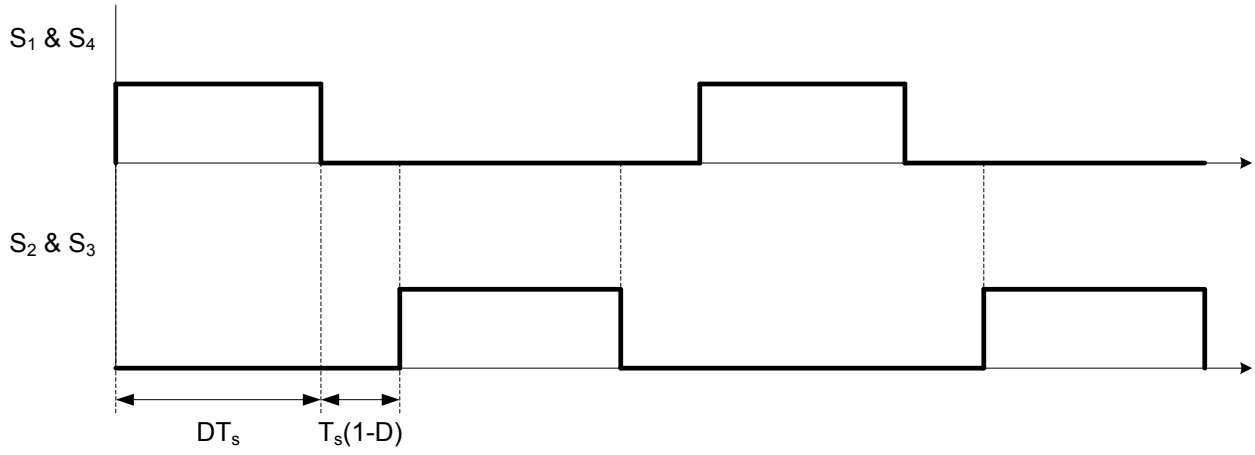



**Figure 2.31** Timing Diagrams while Operating in Charging (Buck) Mode for Second Switching Strategy

Finally, the DAB DC/DC converter, as mentioned previously, can be thought of as a modern DC transformer. The input is a DC voltage that, because of the switching action of the

semiconductor devices, becomes a square wave seen by the primary terminals of the transformer. Remember that the fundamental component of a square wave is a pure sinusoid. The signal is then bucked or boosted and goes through another series of switching events creating an output DC voltage.

# 3.0 FUNDAMENTALS OF WIND TURBINES AND ELECTRIC MACHINERY

Electric machines have been the workhorse of the past and present electric grid. Wind turbine rotors are coupled to the electric machines through a gear box providing another option in the world's portfolio for generating electrical power. The basics of analyzing these components will be presented in this chapter not only because of their importance but also because of their presence in the MVDC network.

## 3.1 INDUCTION MACHINE THEORY AND PRINCIPLES

An equivalent circuit model of a squirrel cage induction machine is found in Figure 3.1. All variables (resistance and inductance) with respect to the stator have a subscript "s" and those with respect to the rotor have a subscript "r".

It has been said that the induction machine can be thought of as a "rotating transformer". The rotor rotates with an angular frequency with respect to the stator by ($\omega_e$-$\omega_r$), where $\omega_e$ is the excitation frequency (typically based upon 50 or 60 Hz) and $\omega_r$ is the mechanical speed of the rotor. Recalling the transformer model from power system analysis theory, one will notice the coupling between the stator and rotor of the machine caused by the induced voltages, a result of Faraday's Law. Other physical parameters in the circuit include the magnetizing inductance, $L_m$, and the machine slip, s, which is defined by (3.1).

$$s = \frac{\omega_e - \omega_r}{\omega_e} \tag{3.1}$$

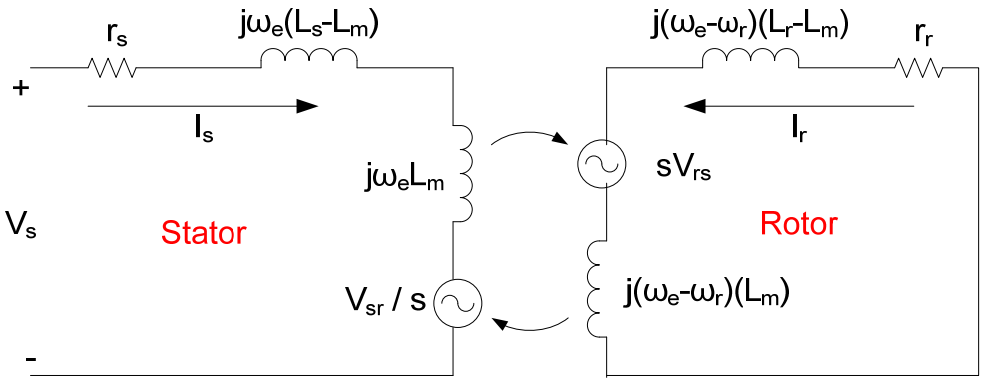



**Figure 3.1** Squirrel Cage Induction Machine Model showing Stator and Rotor Coupling [18]

The equivalent circuit model of Figure 3.1 is not convenient for determining performance parameters of the machine such as output power, electromechanical torque, and efficiency. The reason is because the stator and rotor are excited by different angular frequencies with respect to each other. Our desire is to determine a model for both the stator and rotor based on a common angular frequency.

Writing Kirchoff's voltage law (KVL) around the stator and rotor of the machine provides us with (3.2) and (3.3), respectively.

$$V_s = r_s I_s + j\omega_e L_s I_s + j(\omega_e - \omega_r)\frac{\omega_e}{(\omega_e - \omega_r)} L_m I_r \tag{3.2}$$

$$V_r = 0 = r_r I_r + j(\omega_e - \omega_r) L_r I_r + j\frac{(\omega_e - \omega_r)}{\omega_e}\omega_e L_m I_s \tag{3.3}$$

Multiplying (3.3) by 1/s changes the rotor side frequency to be based upon the excitation frequency, $\omega_e$, resulting in (3.4). Equation (3.2) for the stator and (3.4) for the rotor are brought

together to arrive at a more convenient equivalent circuit of the induction machine found in Figure 3.2.

$$V_r = 0 = \frac{r_r}{s} I_r + j\omega_e L_r I_r + j\omega_e L_m I_s \tag{3.4}$$

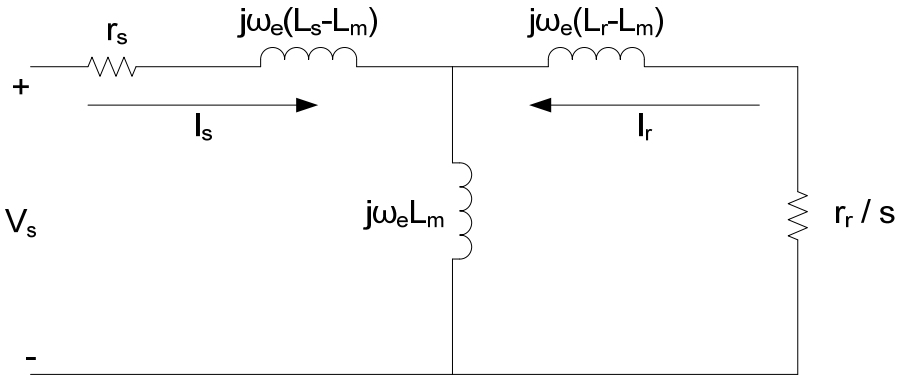



**Figure 3.2** Squirrel Cage Induction Machine Model with Respect to Stator Side of Machine

Figure 3.3 provides the labeling conventions that will be adopted throughout the remainder of this document. All stator components will be classified with one and all rotor parameters will be classified with a two. Note the direction of the rotor current in Figure 3.3 has been defined in the opposite direction compared to Figure 3.2 and is another adopted convention. A resistance, $R_m$, reflecting copper losses and eddy current losses has also been added in parallel with the magnetizing inductance.

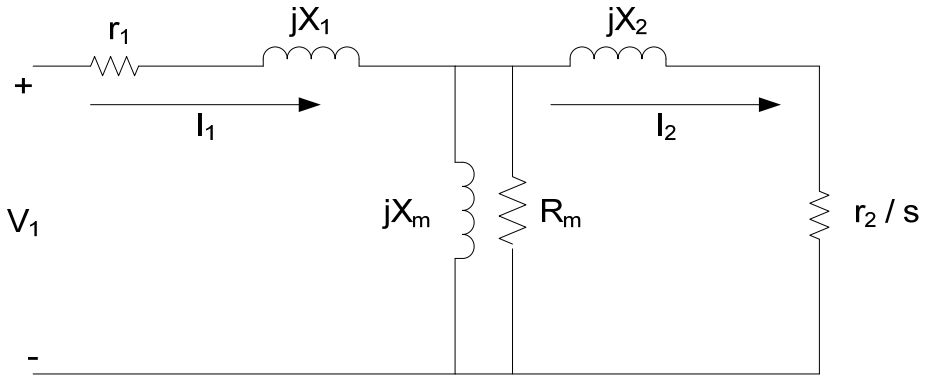



**Figure 3.3** Induction Machine Labeling Convention

### 3.1.1 Induction Machine Maximum Output Power and Torque

The mechanical output power of an induction machine is the product of the mechanical angular frequency and electromechanical torque. Mathematically, the output power and mechanical angular frequency are defined by (3.5) and (3.6), respectively. Note that *P* in (3.6) is the number of poles in the machine and should not be confused with power.

$$P_{mech} = T_e \omega_{rm} \tag{3.5}$$

$$\omega_{rm} = \frac{\omega_r}{P/2} \tag{3.6}$$

The resistance found on the rotor side of the equivalent circuit of Figure 3.3 can mathematically be divided into two terms, one reflecting the losses in the rotor and another used for calculating the output mechanical power of the machine. An alternative expression for the output mechanical power using the second term of (3.6), and more commonly used, is listed as (3.7). Equating (3.7) to (3.5) and using the definition found in (3.6), one obtains the electromechanical output torque of the machine listed as (3.8).

$$\frac{r_2}{s} = r_2 + \frac{r_2(1-s)}{s} \tag{3.6}$$

$$P_{mech} = \frac{3I_2^2 r_2(1-s)}{s} \tag{3.7}$$

$$T_e = \frac{3P}{2}\frac{I_2^2 r_2(1-s)}{s\omega_r} = \frac{3P}{2}\frac{I_2^2 r_2}{s\omega_e} \tag{3.8}$$

The objective of this subsection is to establish the theory for calculating the maximum output torque of the machine. The maximum torque of the machine is calculated by setting the load resistor of the rotor equal to the Thevenin impedance, $Z_{th}$, of the induction machine equivalent circuit and solving for the slip. Once the slip value is known, the stator and rotor currents can be determined and, hence, the maximum torque of the machine can be computed. This concept is illustrated in Figure 3.4 and the Thevenin impedance is listed as (3.9). This concept will be emphasized in more detail when the details are laid out for validating the medium voltage DC network in Chapter 4.

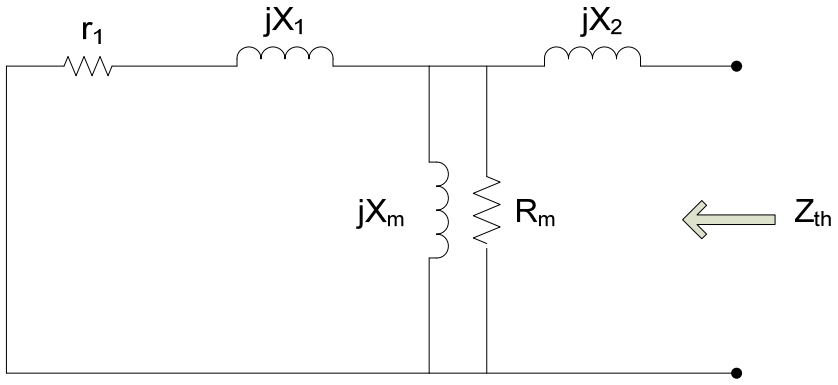



**Figure 3.4** Thevenin Impedance for Determining Maximum Output Torque of Machine

$$\frac{r_2}{s} = (r_1 + jX_1) // jX_m // R_m + jX_2 \tag{3.9}$$

## 3.2 AC DRIVES USED IN WIND TURBINE APPLICATIONS

An electric drive is a power converter interfaced with an electric machine. Due to governmental mandates for increased renewable penetration (including wind and solar), many types of drive configurations have been developed for the use in wind turbine applications. In 2007, the

WECC Modeling and Validation Working Group initiated an effort to develop and validate a series of generic dynamic models for wind turbine generators (WTG) [19].

The first WTG, referred to as a Type 1 WTG, is shown in Figure 3.5. This machine is pitch-regulated and drives a squirrel cage induction generator which is directly coupled to the grid. This configuration has been the adopted model for preliminary studies of the medium voltage DC network developed in chapter 4 due to its simplicity relative to the other types of WTGs.

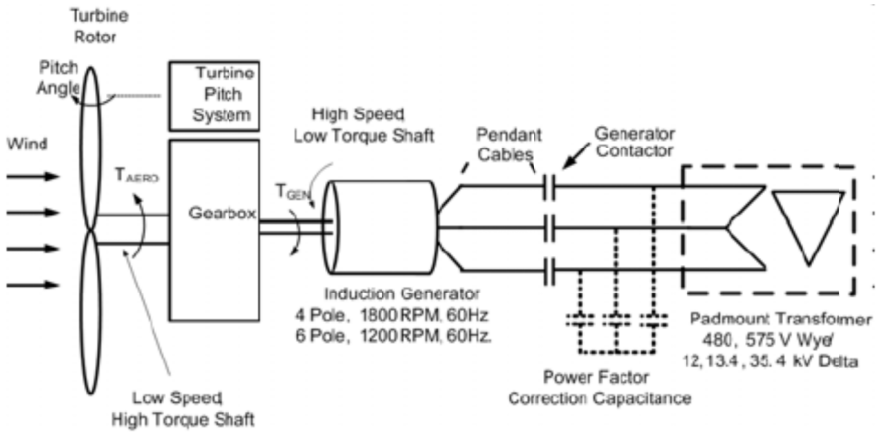



**Figure 3.5** Conceptual Block Diagram of WECC Type 1 WTG [19]

The second type of WTG is shown in Figure 3.6 and is referred to as a Type 2 WTG. The Type 2 WTG is a variation on the Type 1 WTG, operating with variable slip. The model is based upon a wound rotor induction machine, which implies that an external resistance is brought out via slip rings and brushes. The primary means of speed control for this model is done by adjusting the value of the external resistance, thus affecting the slope of the torque-speed curve and operating slip of the machine. This concept is illustrated, graphically, in Figure 3.7.

The advantage of increasing the rotor resistance results in an increase in startup torque ($s = 1$ or $\omega_r = 0$) as shown in Figure 3.7. The disadvantages to this approach are the increased losses in the system due to the addition of a resistive element. Additionally, recall that the slip of

a machine adjusts to changes in rotor speed as governed by (3.1). As the machine slip increases in value away from zero, the maximum obtainable efficiency of the machine decreases ($\eta \approx 1 - s$) The rotor speed adjustment with increasing external resistance isn't very dramatic in the range of steady-state operation ($0.90 < \omega_r < 0.98$) as Figure 3.7 indicates.

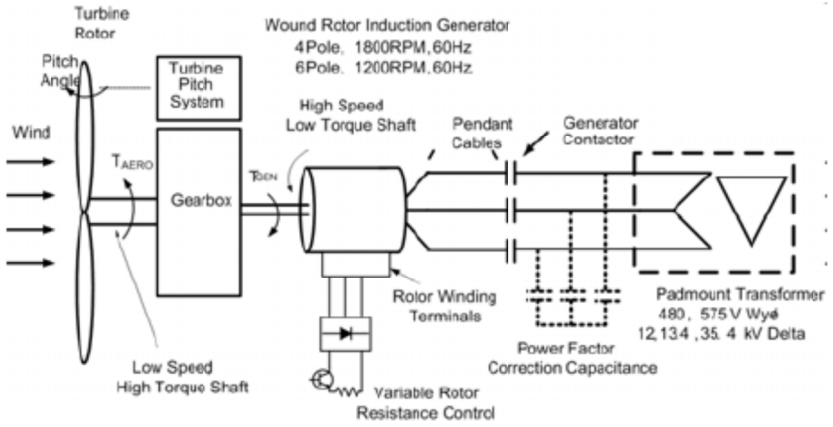



**Figure 3.6** Conceptual Block Diagram of WECC Type 2 WTG [19]

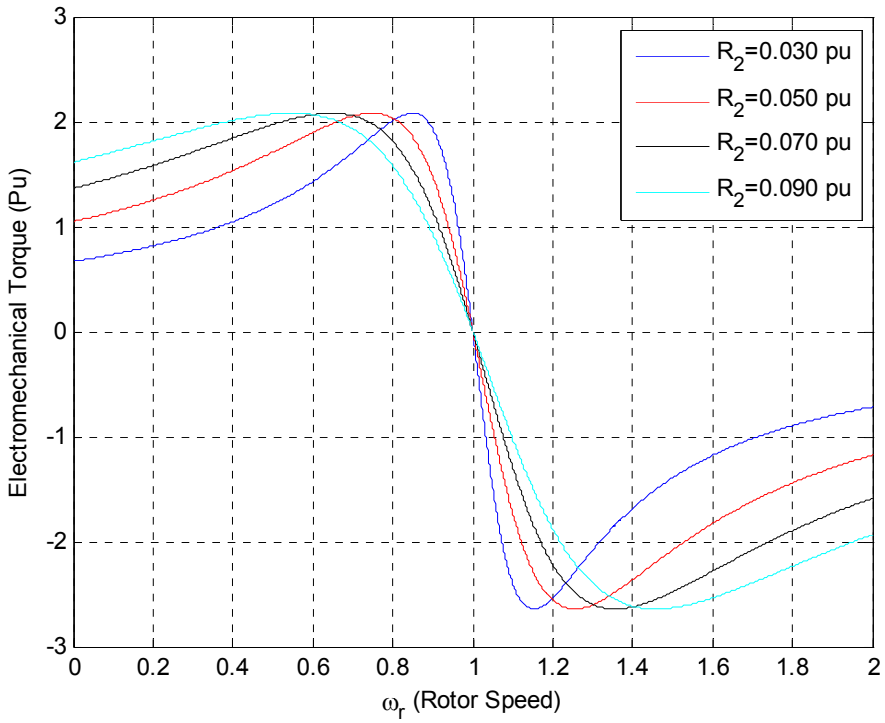



**Figure 3.7** Torque-Speed Characteristics for Varying Values of Rotor Resistance

The doubly fed induction generator (DFIG) partial topology is found in Figure 3.8 and is designated as a Type 3 WTG. The turbine is pitch-regulated and features a wound rotor induction generator with an AC/DC/AC converter connected between the rotor terminals and the grid. The power converter, which resembles a resistance to the machine, in the rotor circuit allows for the control of generator torque and flux providing quicker active and reactive power control over a wide range of generator speeds.

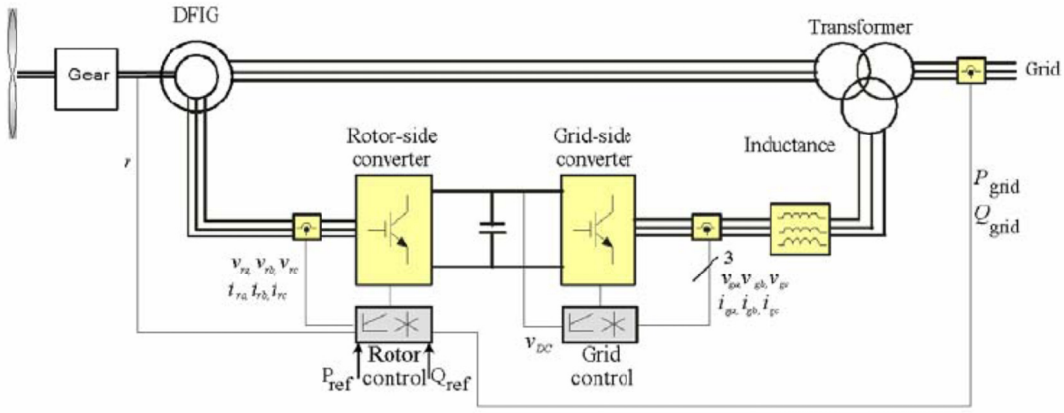



**Figure 3.8** Conceptual Block Diagram of WECC Type 3 WTG [20]

The full topology of the DFIG is found in Figure 3.9. The turbine is pitch-regulated and features the AC/DC/AC power converter through which all generator power is processed. The generator can be either an induction ($s \neq 0$) or synchronous type ($s = 0$). This configuration has the same benefits as the Type 3 WTG by providing fast active and reactive power control over a wide range of generator speeds.

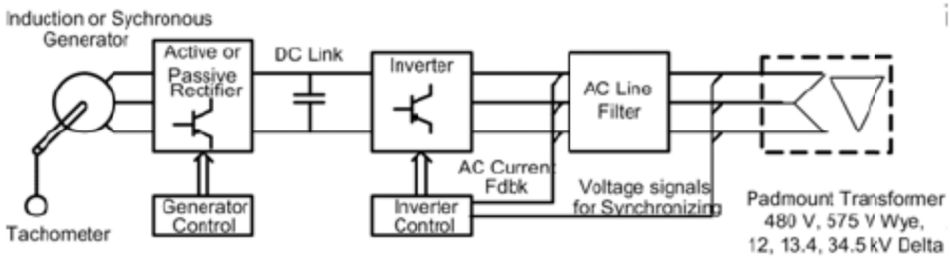



**Figure 3.9** Conceptual Block Diagram of WECC Type 4 WTG [19]

## 3.3 FUNDAMENTAL CHARACTERISTICS FOR CLASSIFYING WIND TURBINE PERFORMANCE

Before displaying the governing equations which describe wind turbine performance, a few details on wind power should be elaborated upon, hence, showing the importance of wind and why it's a part of the global generation portfolio of renewable generation resources. From elementary fluid mechanics, the mass flow rate, $\dot{m}$, of a fluid is governed by (3.10). The rate of change in the kinetic energy of this stream of air particles is governed by (3.11). Combining (3.10) and (3.11) provides a well-known relationship, listed as (3.12), describing the output power in the wind. Noting that the output power caused by the wind is proportional to the cube of the wind velocity makes wind generation quite attractive [21].

$$\dot{m} = \rho A v \tag{3.10}$$

$$\dot{K}E = \frac{1}{2}\dot{m}v^2 \tag{3.11}$$

$$P_{wind} = \frac{1}{2}\rho A v^3 \tag{3.12}$$

The model of the wind turbine system that will be presented from this point forward was developed at Purdue by P.C. Krause and gives utility engineers a handle for evaluating the transient effects of wind generators that are integrated into large scale power systems [22]. There are two wind turbine type options in PSCAD which are based upon those found in the literature. They are referred to as a MOD-2 and a MOD-5 wind turbine model. A MOD-2 wind turbine is a three blade system and a MOD-5 is a two blade system. The focus of this thesis work will be based upon the MOD-2 design.

The MOD-2 model consists of five components, which include the wind model, blade dynamics, shaft dynamics, pitch control, and machine model. Note that the first four components of this system are mechanically based. The shaft dynamics are characterized in terms of the rotation of the wind turbine blade speed, hub speed, gear box speed, and the generator mechanical speed and will not be discussed further.

The blade dynamics, governed by the non-linear equations displayed by (3.13) through (3.17), are the heart of determining the output power of the wind turbine. Equation (3.13) is a linear relationship for determining the hub speed of the wind turbine. Equation (3.14) computes the tip speed ratio of the turbine blade, which is a ratio between the wind velocity and hub speed of the turbine system. An approximate expression for the power coefficient of the MOD-2 wind turbine is listed as (3.15), which is highly non-linear and a function of blade pitch angle, β, and tip speed ratio, γ. Finally, (3.16) and (3.17) describe the output power and torque provided by the wind power as described previously with minor modifications.

$$\omega_h(\omega) = \frac{\omega}{G_R} \tag{3.13}$$

$$\gamma(\omega) = \frac{2.237 V_W}{\omega_h(\omega)} \tag{3.14}$$

$$C_p(\omega,\beta) = \frac{1}{2}\left(\gamma(\omega) - 0.022\beta^2 - 5.6\right)\exp\left(-0.17\gamma(\omega)\right) \tag{3.15}$$

$$P(\omega,\beta) = \frac{1}{2}\rho A \omega_v^3 C_p(\omega,\beta) G_\eta \tag{3.16}$$

$$T(\omega,\beta) = \frac{P(\omega,\beta)\omega_r}{\omega} \tag{3.17}$$

Plots of the power coefficient, $C_p$, and output Power and Torque as a function of mechanical speed of the turbine machine are provided in Figure 3.10 through Figure 3.12, respectively. Multiple curves are provided on these plots for varying values of blade pitch, β. As we begin our discussion in Chapter 4, where the details of the overall model development and validation of the medium voltage DC network are presented, Figure 3.10 through Figure 3.12 below will find great value as far as predicting the output power of the wind turbine induction machine used in the model.

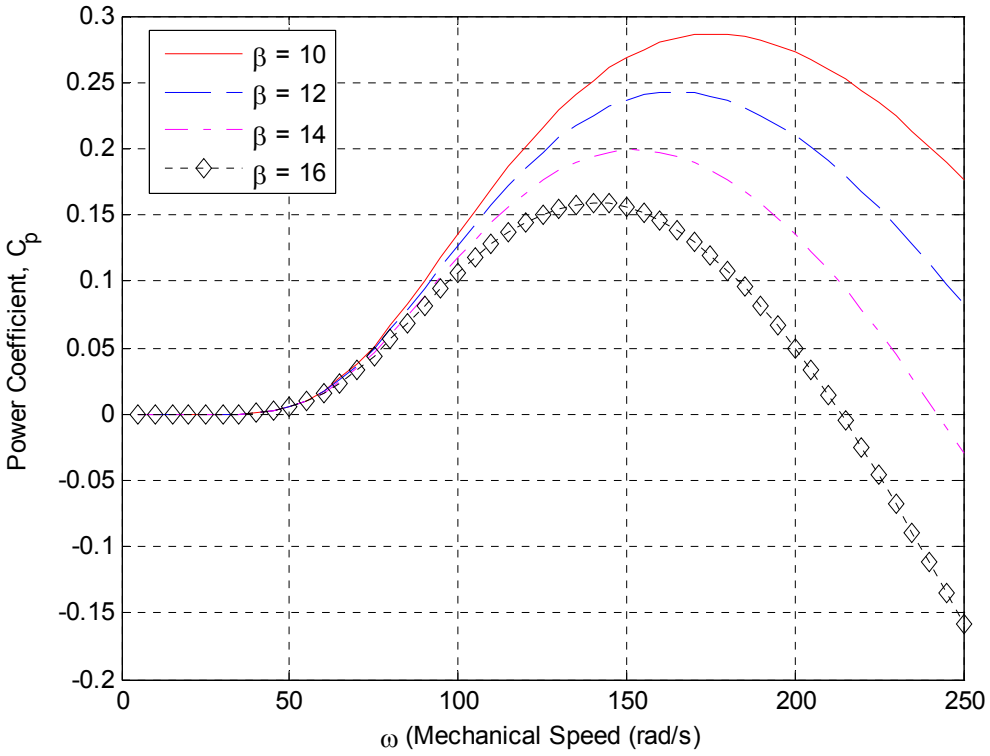



**Figure 3.10** Power Coefficient for MOD-2 Wind Turbine

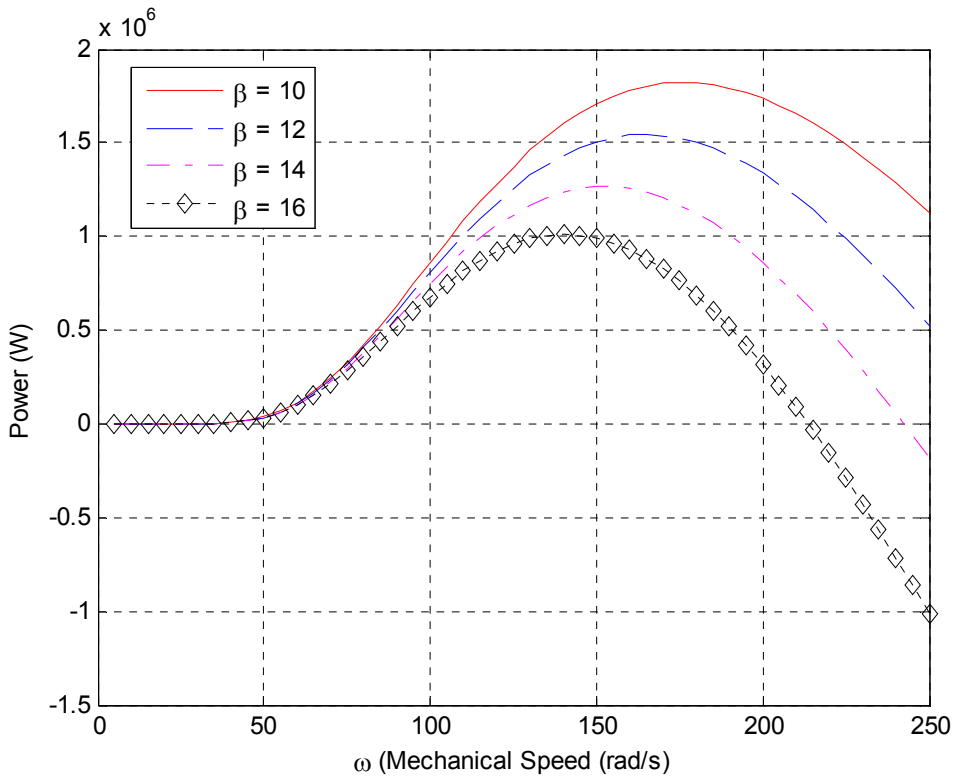



**Figure 3.11** Power Speed Curves for MOD-2 Wind Turbine

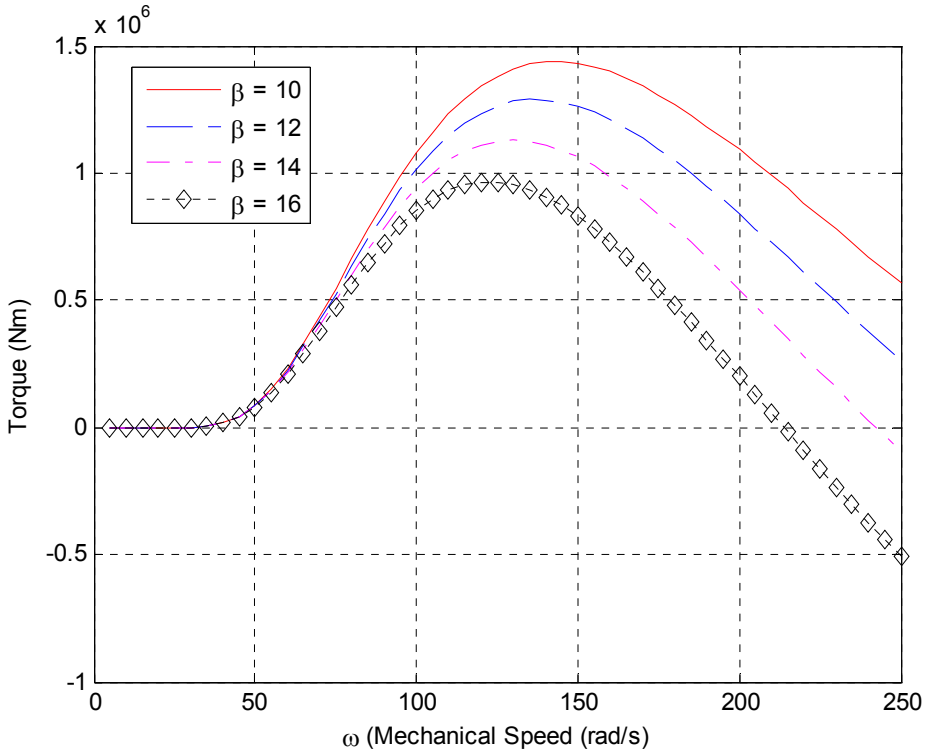



**Figure 3.12** Torque Speed Curves for MOD-2 Wind Turbine

# 4.0 MVDC MODEL DEVELOPMENT AND VALIDATION

With the minimal theoretical principles completely outlined in chapters one through three, the next task is to demonstrate their use in the development of a medium voltage DC network. A diagram of the medium voltage DC network developed that will be used as a stepping stone for the larger MVDC research project is shown in Figure 4.1.

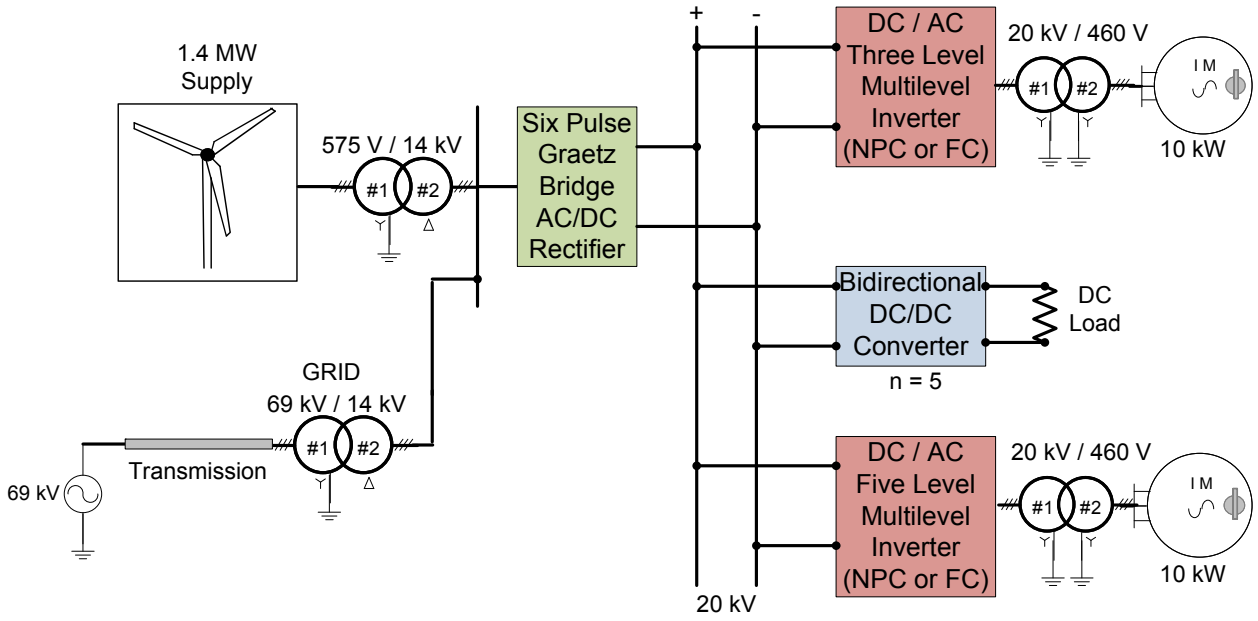



**Figure 4.1** PSCAD MVDC Network

Analyzing the figure, readers will notice that the main generation resource is wind power whose AC signals are converted to DC through a high power rectifier to establish the 20 kV DC bus voltage which serves the loads connected in parallel. Two of the loads are AC induction machines which serve to help validate the power flows on the network. NPC, as shown in Figure

4.1, or FC multilevel inverters convert the DC voltage into AC for feeding the terminals of the AC machines. The third load is a standard resistive load interfaced with a bidirectional DC-to-DC converter. All of the electronics, mechanical systems, machines, and open loop control schemes can be found in the sub-modules of Figure 4.1. The next task is to explain how the components are assembled within the sub-modules and show how the model was validated.

## 4.1 INDUCTION MACHINE MODELING AND VALIDATION

The machines serving as loads are wye-connected, 20 hp, 460 V (line-to-line rms), three-phase, 4-pole induction motors. Table 4.1 provides the parameters of the machine on a per unit basis as described by Figure 3.3 in Chapter 3. Figure 4.2 provides the PSCAD schematic for simulating the induction motor. The model has two external inputs, the steady-state mechanical speed and the load torque. The traditional procedure for simulating a motor is to start the machine using speed control and, once the simulation hovers around the expected steady-state mechanical speed, switch into torque control. This is why one will see the block representing a step change to the right of the machine in Figure 4.2 because this provides the signal to perform the latter function. Load torques, such as pumps or fans, are typically proportional to the square of the mechanical speed. The computation of the load torque is provided below the induction motor.

**Table 4.1** Induction Motor Equivalent Circuit Parameters [18]

| $r_1$ | $r_2$ | $X_1$ | $X_2$ | $X_m$ | $R_m$ |
|---|---|---|---|---|---|
| 0.025 | 0.030 | 0.10 | 0.10 | 2.4 | 20 |

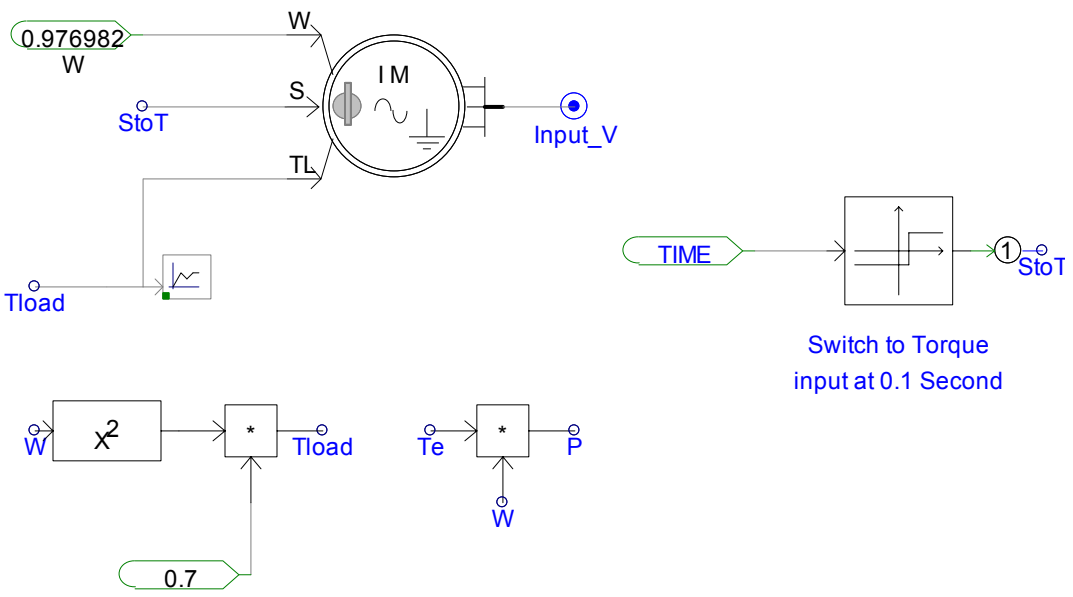



**Figure 4.2** PSCAD Simulation Model of Induction Motor

Often, the rated slip of the machine, as described by (3.1), is not given but can be computed based upon the rated mechanical speed of the machine if provided on the nameplate. As with the case of this thesis work, the nameplate of a physical machine is not provided, thus numerical techniques will be necessary for computing the rated mechanical speed based upon the parameters provided in Table 4.1. The rated mechanical speed is one of the inputs found in Figure 4.2.

Using Figure 3.3 as the basis of the discussion, the output voltage seen across the magnetizing branch of the machine can be computed with (4.1), which is obtained by using voltage divider techniques from circuit analysis. The current through the rotor of the machine can be computed with (4.2). When (4.1) is substituted into (4.2), one obtains (4.3). Equation (4.4), the per unit version of (3.7), represents the output power of the machine. To find the slip, which will allow us to determine the rated mechanical speed, (4.3) is iterated upon by choosing different values of slip to ensure that the electromechanical torque equals the load torque, a requirement for steady-state operation of the machine, and that Kirchoff's current law holds true

at the magnetizing branch node. MATLAB code which performs this operation is found in Appendix B of this document.

$$V_o = V_1 \frac{(r_2 + jX_2 s)(R_m)(jX_m)}{(r_1 + jX_1)\left[jX_m(r_2 + jX_2 s) + R_m(r_2 + jX_2 s) + jsR_m X_m\right] + jX_m R_m(r_2 + jX_2 s)} \tag{4.1}$$

$$I_2 = \frac{V_o}{\left(\frac{r_2}{s} + jX_2\right)} \tag{4.2}$$

$$I_2 = V_1 \frac{s(R_m)(jX_m)}{(r_1 + jX_1)\left[jX_m(r_2 + jX_2 s) + R_m(r_2 + jX_2 s) + jsR_m X_m\right] + jX_m R_m(r_2 + jX_2 s)} \tag{4.3}$$

Analytically, the load torque and electromagnetic torque reach a steady-state value of 0.6680 pu, which is equivalent to the output power, on a per unit basis, since we are operating at rated frequency (60 Hz). The base quantities for the output power and torque can be computed with (4.4) and (4.5), respectively, in order to transform the per unit quantity into a value containing physical units. The expected output power and torque of the machine are 9.96 kW and 52.85 Nm. The max torque of the machine, using the concept found in Figure 3.4, was determined to be 164.65 Nm, as the second MATLAB script in Appendix B indicates.

$$P_{base} = P_{Rated} = (20hp)(0.746kW) = 14.914kW \tag{4.4}$$

$$T_{base} = \frac{P}{2}\left(\frac{P_{base}}{\omega_{base}}\right) = (\frac{4}{2})(\frac{14.914kW}{2\pi(60)}) = 79.121Nm \tag{4.5}$$

A plot of the output torque of the machine, simulated with PSCAD but graphically displayed with MATLAB, is shown in Figure 4.3. The starting nature of the machine is

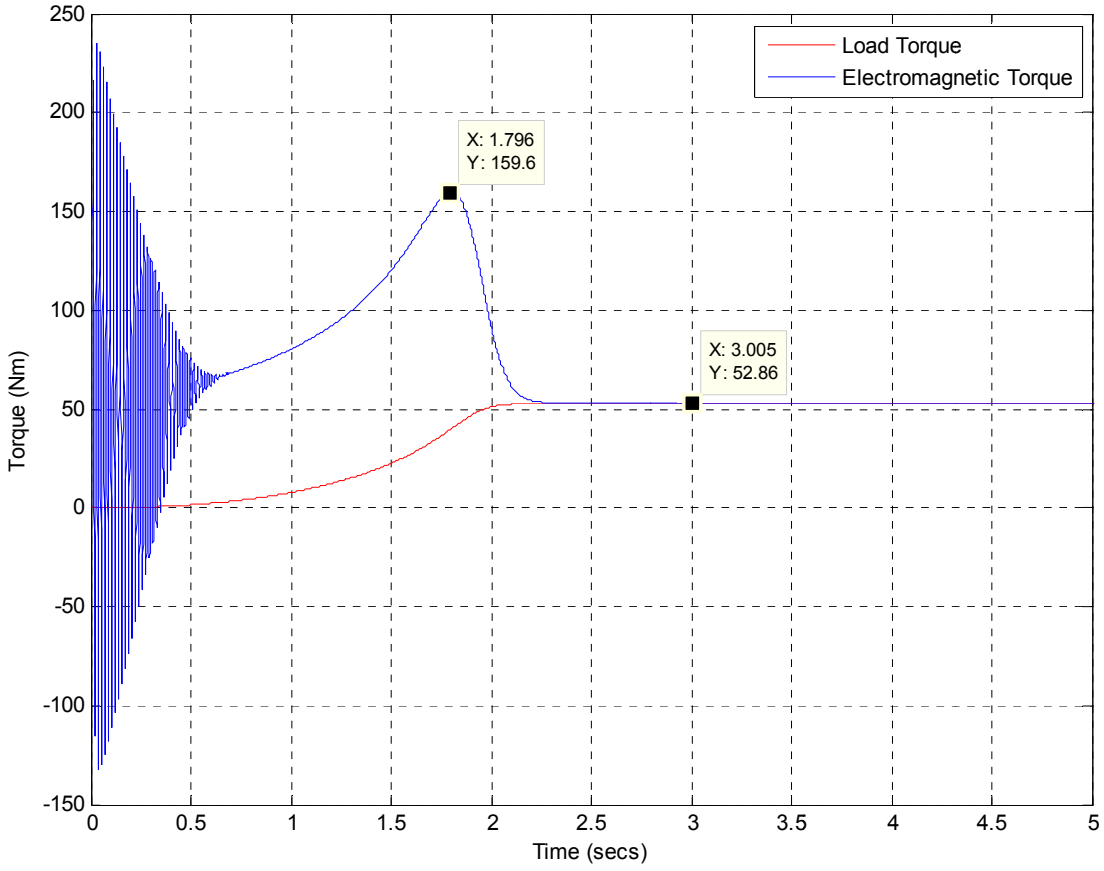



**Figure 4.3** Electromagnetic Torque and Load Torque of Induction Motors Computed through PSCAD Simulation

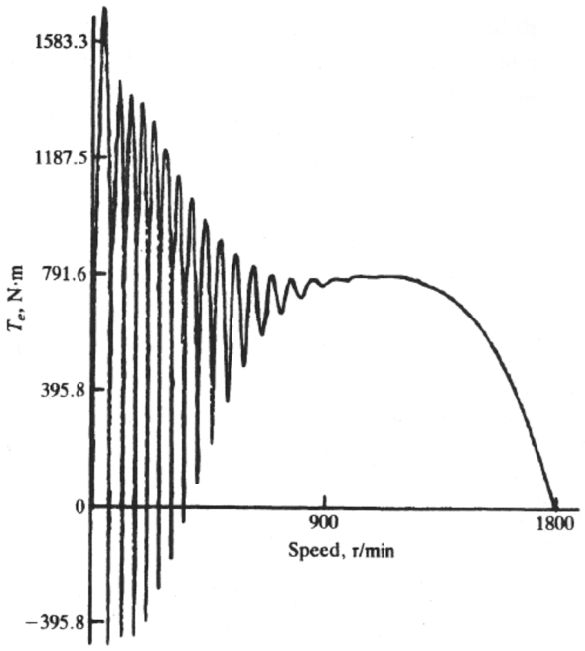



**Figure 4.4** Free Acceleration Characteristics of a 50 hp Machine [23]

validated with the results provided in Figure 4.4 and published in [23]. The output power of the machine is provided in Figure 4.5. Based upon these responses, the motor load is behaving as expected. The last point to mention is that the machines will be started from steady-state because the initial transients are not of interest for this analysis and take a lot of computational power with an interconnected system as complex as that shown in Figure 4.1.

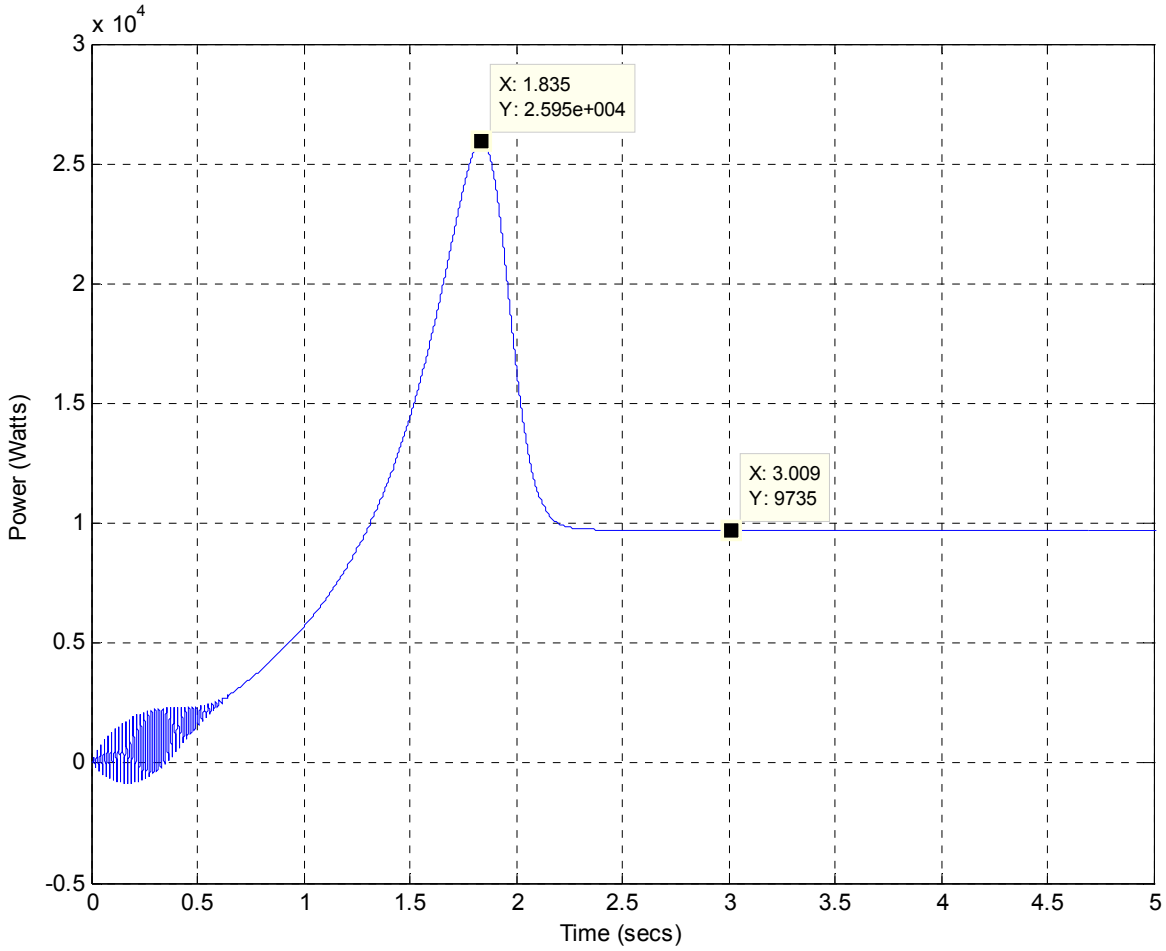



**Figure 4.5** Output Power of Induction Motors Computed through PSCAD Simulation

## 4.2 WIND TURBINE SYSTEM DEVELOPMENT AND VALIDATION

A diagram of a single wind turbine schematic is found in Figure 4.6 and will be one of two generation sources in the model. The model consists of a wind source that can be adjusted at two points in the simulation, a block representing the mechanical components of the wind turbine based on a MOD-2 design as described in Chapter 3, a wind turbine controller that controls the pitch angle, β, of the blades and another induction machine model.

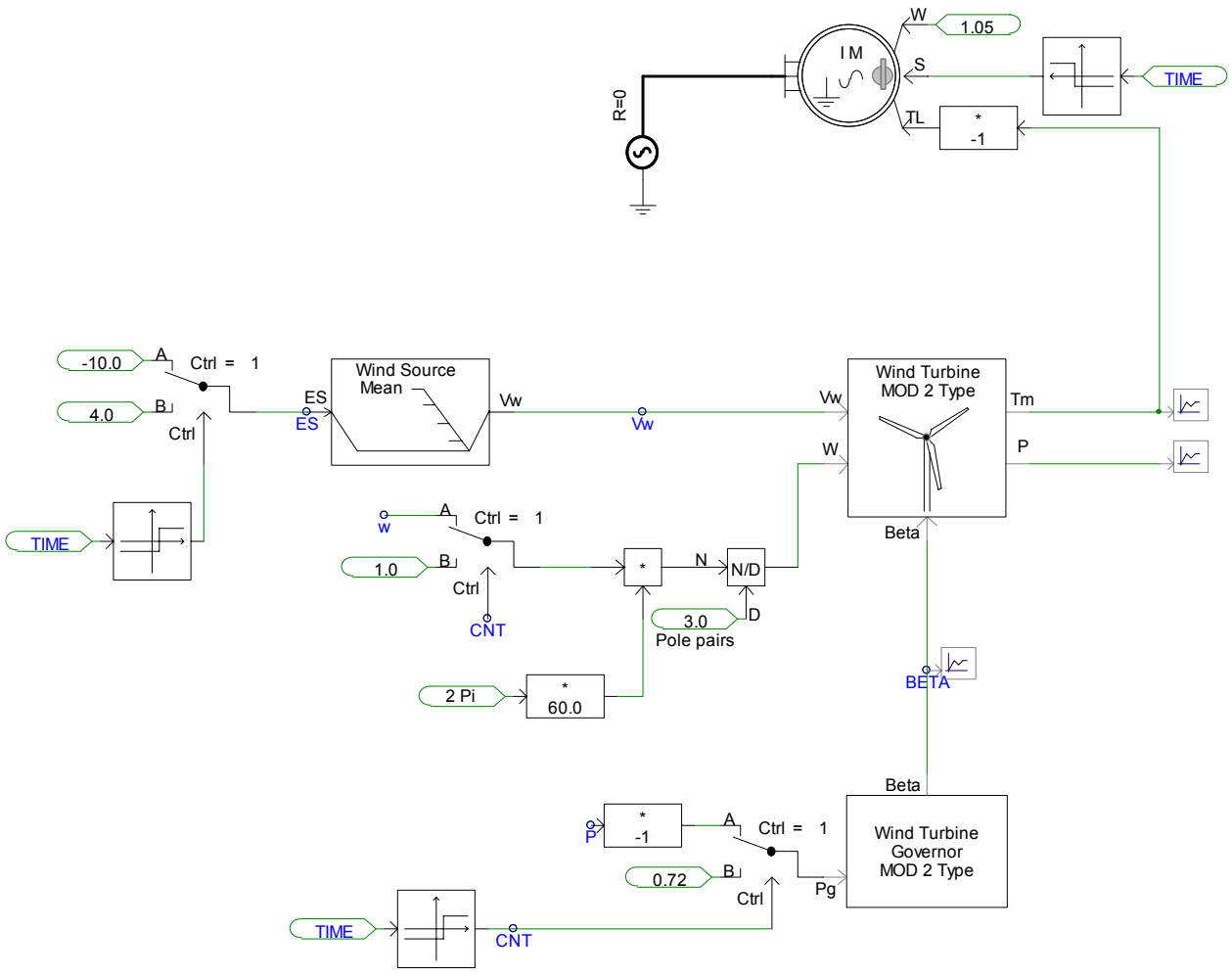



**Figure 4.6** Single Wind Turbine Model used in PSCAD Simulation of MVDC Network

As described in [22], the wind source is treated as a linear combination of a wind mean speed component, gust component, ramp component, and noise component. This is figuratively shown in Figure 4.7. For this work, a mean wind speed of 14 m/s was chosen and is the only component modeled, as indicated in Figure 4.6, to help ease the verification of the model. Throughout the simulation, the wind speed can be adjusted, through a step change, to being either 0 m/s to truly test the dynamic response of the model, or remain operating at 14 m/s. The blocks that perform this function serve as the input to the wind source in Figure 4.6.

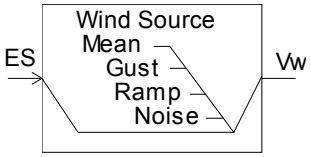



**Figure 4.7** Wind Source Components Capable of being Modeled in PSCAD

**Table 4.2** Mechanical Parameters of GE Wind Turbine [24]

| Parameter | Numerical Quantity |
|---|---|
| Generator Rated MVA | 1.667 MVA |
| Machine Rated Mechanical Speed, $\omega_r$ | 125.667 rad/s |
| Rotor Radius | 35.25 m |
| Rotor Area | 3904 $m^2$ |
| Air Density | 1.225 $kg/m^3$ |
| Gear Box Efficiency | 0.97 pu |
| Gear Ratio | 77 |

The wind turbine MOD-2 structure takes into consideration the mechanical aspects of the wind turbine. Based on the physical dimensions of a GE wind energy 1.5 sec, 60 Hz wind

turbine generator with rotor blade, the parameters found in Table 4.2 were used in the wind turbine MOD-2 block. There are three inputs requested by the wind turbine MOD-2 block, which are the mean wind speed (the source of wind power), the mechanical speed, and the pitch of the three blades that form the rotor of the turbine. The pitch of the blades is controlled through the wind turbine governor, which requires a reference speed, output power reference, and generator ratings. The control loops based upon [25] are provided in Figure 4.8. The controller is based upon classical PI control.

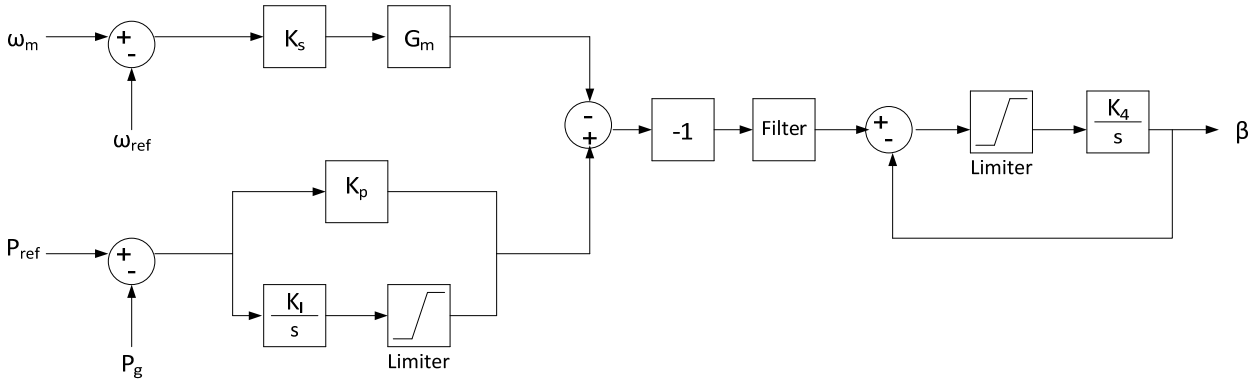



**Figure 4.8** Feedback Loops used to Regulate the Blade Pitch of a MOD-2 Wind Turbine [25]

The last component in the model is the 1.667 MVA induction generator having a voltage rating of 575 V (line-to-line rms), three pole pairs, rated for 60 Hz operation. The two inputs, like the induction motors, is a rough approximation of the rated mechanical speed, in pu, while generating, and the load torque is the torque generated by the wind source. Note that the torque and slip are negative since the machine is operating as a generator.

One of the many hurdles that needed to be overcome when developing this model was getting the output power of the machine onto the system. Induction machines always require an external source of voltage because there is no field winding associated with this type of machine. Observing the machine, there is no output terminal to directly connect to the network model. To

get around this issue, the steady-state model of the induction machine (Figure 3.3) was consulted.

The objective was to determine a way to program the software to serve the 575 V / 14 kV Y-Δ transformer with a 575 V input. Note that the rotor current of an induction machine, listed again as (4.6), is a function of the voltage seen across the terminals of the magnetizing branch of the machine. The output power, listed as (4.7), is also a function of rotor current. Eliminating the rotor current from both equations and solving for the output voltage could ideally serve as an input to a voltage controlled source. Equation (4.8) is the peak, line-to-ground output voltage, $V_o$, that is coded as an input to a voltage controlled source in PSCAD, which becomes directly connected to the primary side terminals of the 575 V / 14 kV Y-Δ transformer.

$$I_2 = \frac{V_o}{\left(\frac{r_2}{s} + jX_2\right)} \tag{4.6}$$

$$P = \frac{I_2^2 r_2 (1-s)}{s} \tag{4.7}$$

$$V_o = 575\sqrt{\frac{2}{3}P\left(\frac{r_2}{s} + jX_2\right)^2 \frac{s}{r_2(1-s)}} \tag{4.8}$$

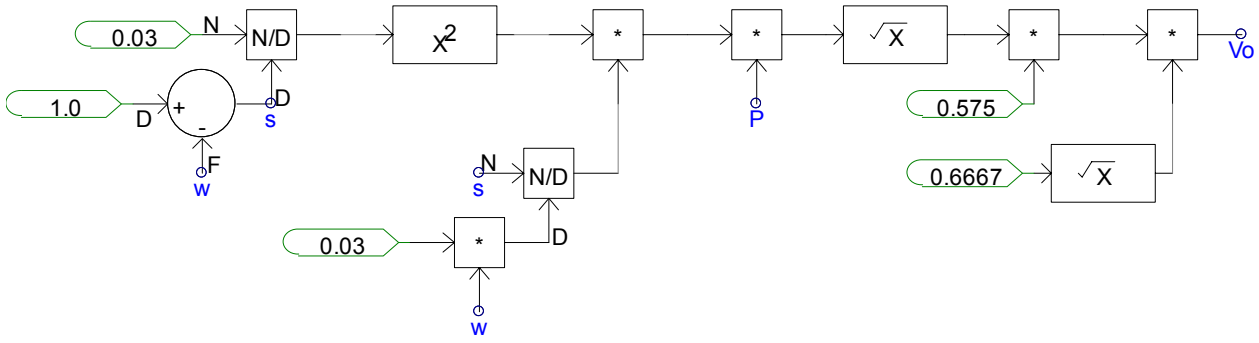



**Figure 4.9** Equation 4.8 Coded to Serve as an Input to a Controlled Voltage Source

One last comment can be made with regards to Figure 4.6. Observing the figure, one will recognize three timer blocks. One of the blocks is used to adjust the induction machine operating characteristics based upon speed control or torque control as discussed earlier regarding the induction motors. The timer block closest to the wind turbine governor control block is used to transition the controller from an arbitrarily determined constant input power of 0.72 pu to the output mechanical power of the wind turbine MOD-2 block. This aspect builds feedback control into the unit and a little intelligence. These timer blocks transition from one state to the next 0.3 seconds into the simulation. The third timer block which alters the mean wind speed is not related to the other two but, as previously mentioned, allows for dynamic adjustments to the mean wind speed during one point in the simulation.

Based upon the nonlinear equations that describe the blade dynamics of the wind turbine provided in Chapter 3, the desired output power can be determined with the aid of Figure 3.11. The initial pitch of the blade, $\beta$, is pre-programmed into the controller with a value equal to 10. The rated mechanical speed of the system is 125.67 rad/s. With these two coordinates, the expected steady-state operating point of the wind turbine system is located on Figure 4.10 with an approximate output power of -1.4 MW. Simulating the PSCAD model of Figure 4.1, the output power of the wind turbine is shown in Figure 4.11, which shows strong agreement with the analytics. Observing Figure 4.11, readers will notice a slight step change in the output waveform. This step change is a result of the machine transitioning from speed control to torque control as well as the controller intercepting the real-time wind turbine mechanical output power as described in the latter paragraph. The mechanical speed of the induction machine settles down to a value of 1.027 rad/s, hence, a value of 1.05 rad/s, chosen as an initial input estimate, was a suitable approximation.

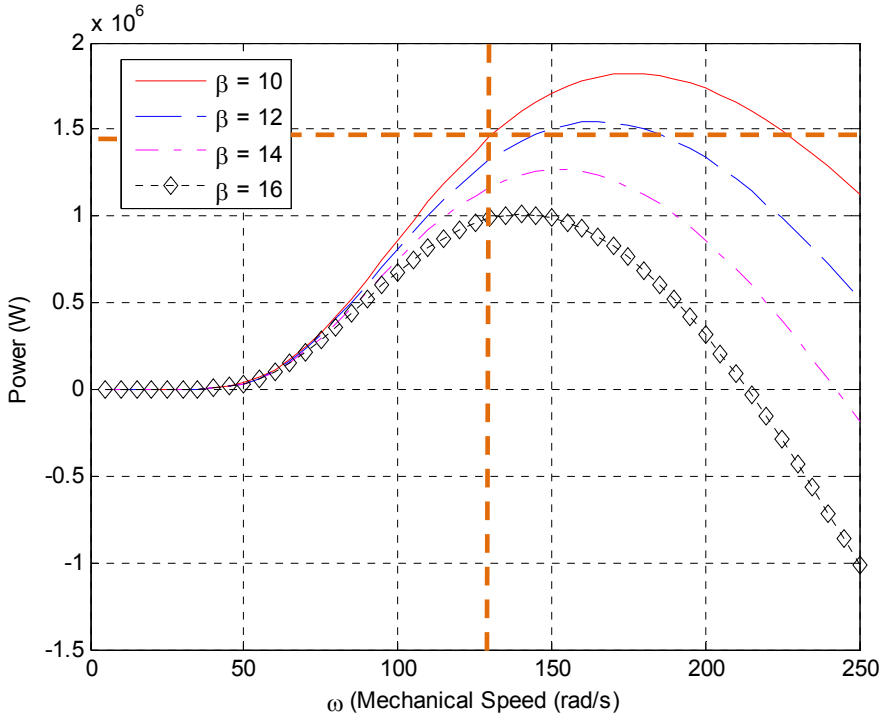



**Figure 4.10** Operating Point of Wind Turbine System under Steady-State Conditions

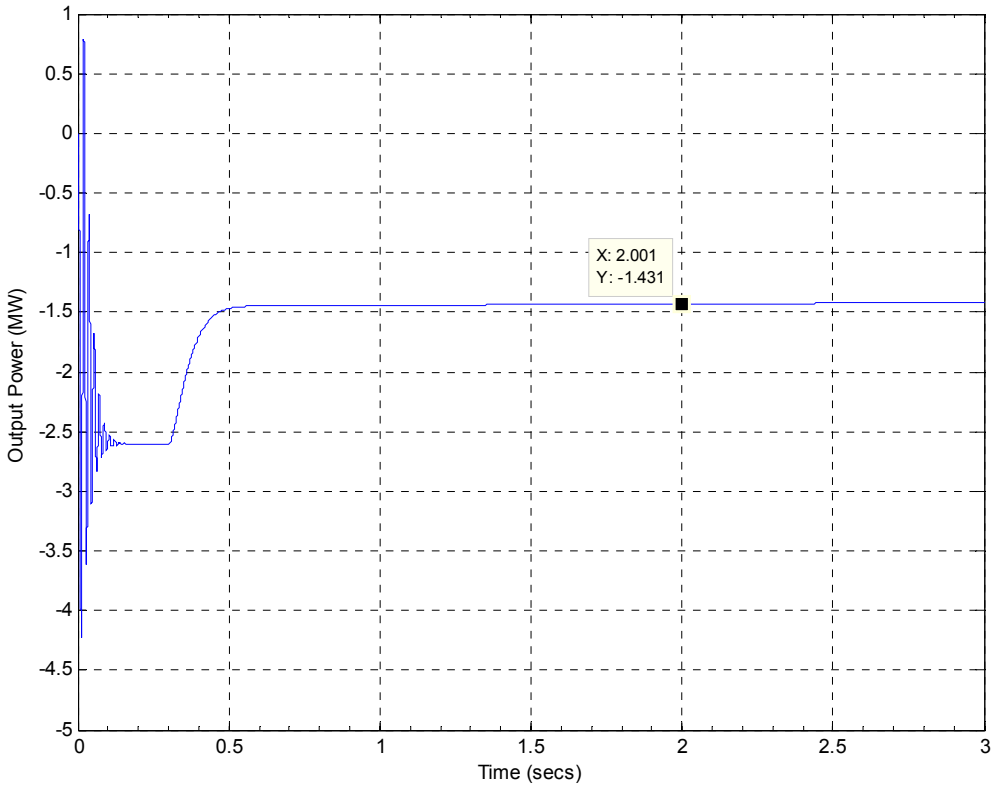



**Figure 4.11** Simulated Output Power of the Wind Turbine System under Steady-State Conditions

## 4.3 SIX PULSE RECTIFIER MODELING AND VALIDATION

A PSCAD diagram of how the six pulse rectifier was modeled is shown in Figure 4.12. The semiconductor devices are GTO's with a snubber circuit in parallel with the device. Notice the naming convention and applied gate signals applied to specific semiconductor devices are consistent with Figure 2.24. A 4000 µF capacitor was selected to provide a very stiff voltage source that will supply the 20 kV bus. The size of the capacitor is relatively big but this magnitude is typical for high power applications as demonstrated in [13, 17]. The other components in this model are either measurement signals or connections to the other sub-modules of the medium voltage DC network.

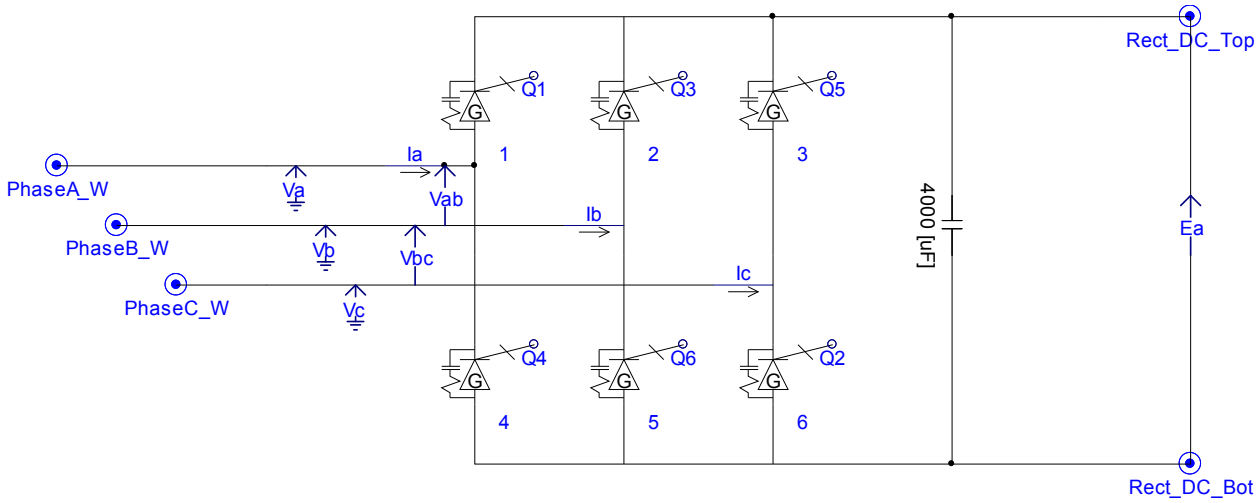



**Figure 4.12** PSCAD Model of Controllable Six Pulse Rectifier

As was mentioned in Chapter 2 and illustrated in Figure 2.25 and Figure 2.26, gate drive signals $Q_1$, $Q_3$, and $Q_5$ are delayed from each other by 120°. The same is true for the other set of remaining switches in the circuit. Figure 4.13 provides the initial steps for creating the pulse duration signals that are used as an internal input to the delay blocks found in Figure 4.14. Figure 4.13 contains a control panel giving the user access of changing the firing delay, α, and

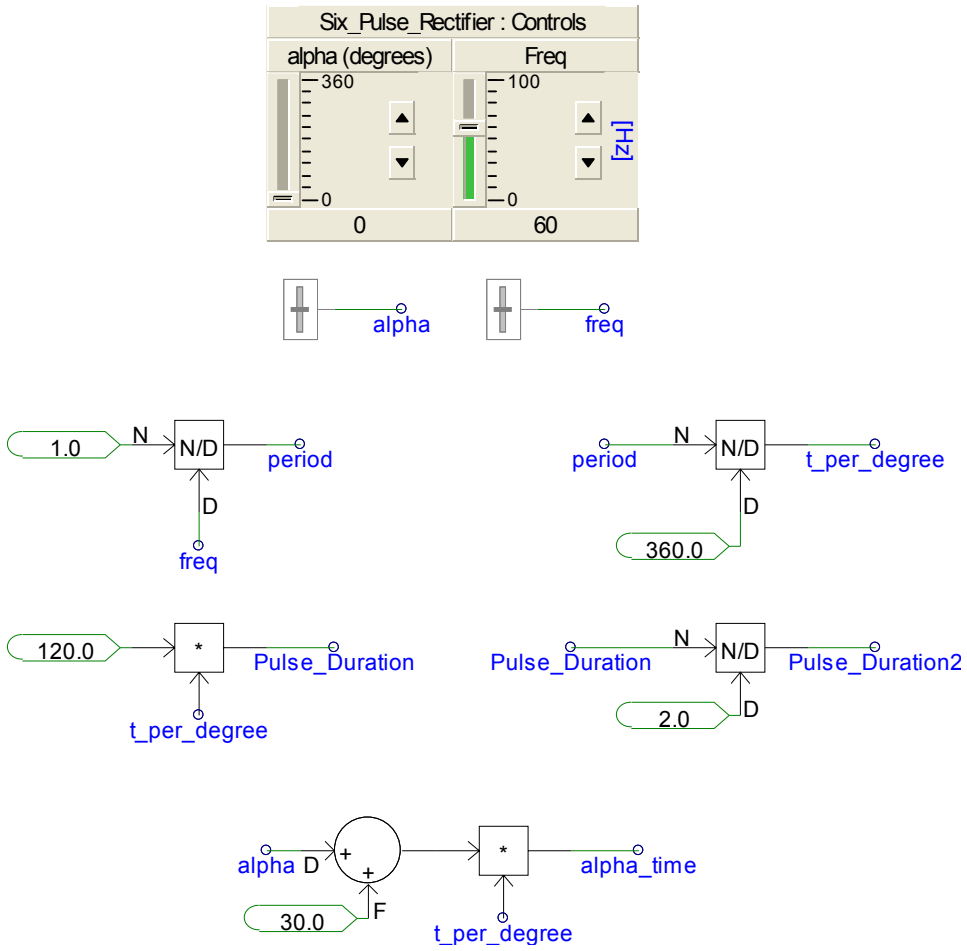



**Figure 4.13** Mathematical Relationships used to Drive the Delay Signals of **Figure 4.14**

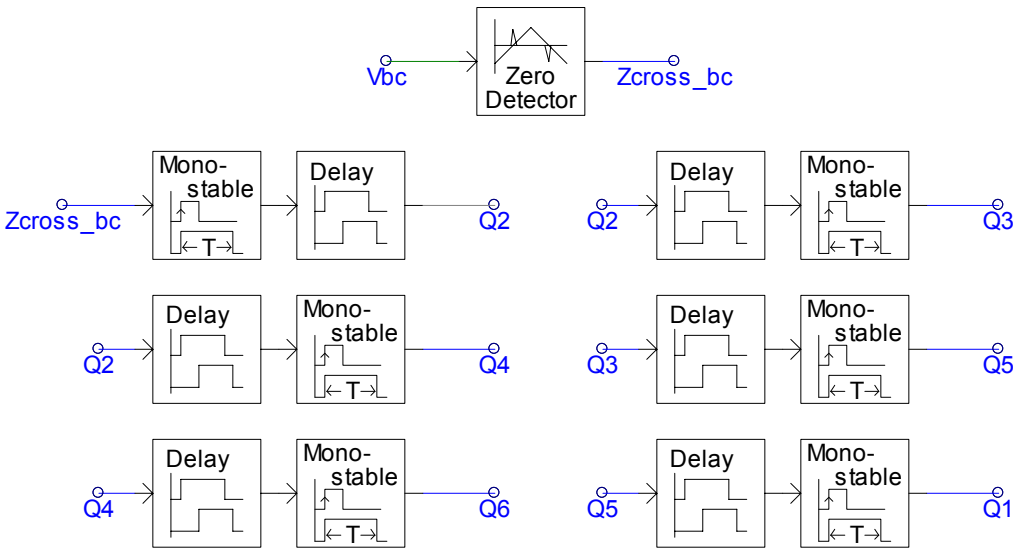



**Figure 4.14** Circuitry to Pulse Gates of Six Pulse Rectifier

the system frequency seen by the rectifier (typically 50 or 60 Hz). With the selected system frequency, the period is calculated and is used to calculate the time per electrical degree. We know that the duration of one switching sequence is $120^o$ and is multiplied by the time per electrical degree to obtain the duration time of each switch. The signal name for this duration time is called Pulse_Duration used by {$Q_1$, $Q_3$, and $Q_5$} and Pulse_Duration2 used by {$Q_2$, $Q_4$, and $Q_6$}.

In this model, switch $Q_2$ was selected as the reference switch to begin the transitions. A logical starting point to turn $Q_2$ ON would be when $V_{bc}$ crosses through zero the first time in Figure 2.26. This is the purpose of the zero-crossing detector in Figure 4.14. Once this time point in the simulation is determined by PSCAD, all the switches are delayed from $Q_2$ using the appropriate pulse duration time using the remaining block logic of Figure 4.14. Notice that the blocks on the right are for switches {$Q_1$, $Q_3$, $Q_5$} and the blocks on the left are for switches {$Q_2$, $Q_4$, $Q_6$}. Figure 4.15 provides the gate drive signals of all the switches. Note that a gate drive signal is never -1 but always 0 or 1. Figure 4.15 shows negative amplitudes for switches {$Q_2$, $Q_4$, $Q_6$} to show correlation between Figure 2.26 and Figure 4.15.

The most important aspect of a rectifier is that the unit transforms the AC signal into a DC signal. Figure 4.16 provides the line-to-line output voltage of the rectifier. Note that this output derives from simulating the entire interconnected unit of Figure 4.1. The steady-state output approaches 19.05 V, which is the expected output voltage based upon (2.5). The computation is listed as (4.9) for the reader's convenience. Although the DC voltage looks very clean of harmonics and ripple, zooming in closer around the steady-state value shows that this is

$$V = \frac{3\sqrt{2}}{\pi} V_{LL,rms} \cos\alpha = \frac{3\sqrt{2}}{\pi}(14kV)\cos(0) = 18.91kV \tag{4.9}$$

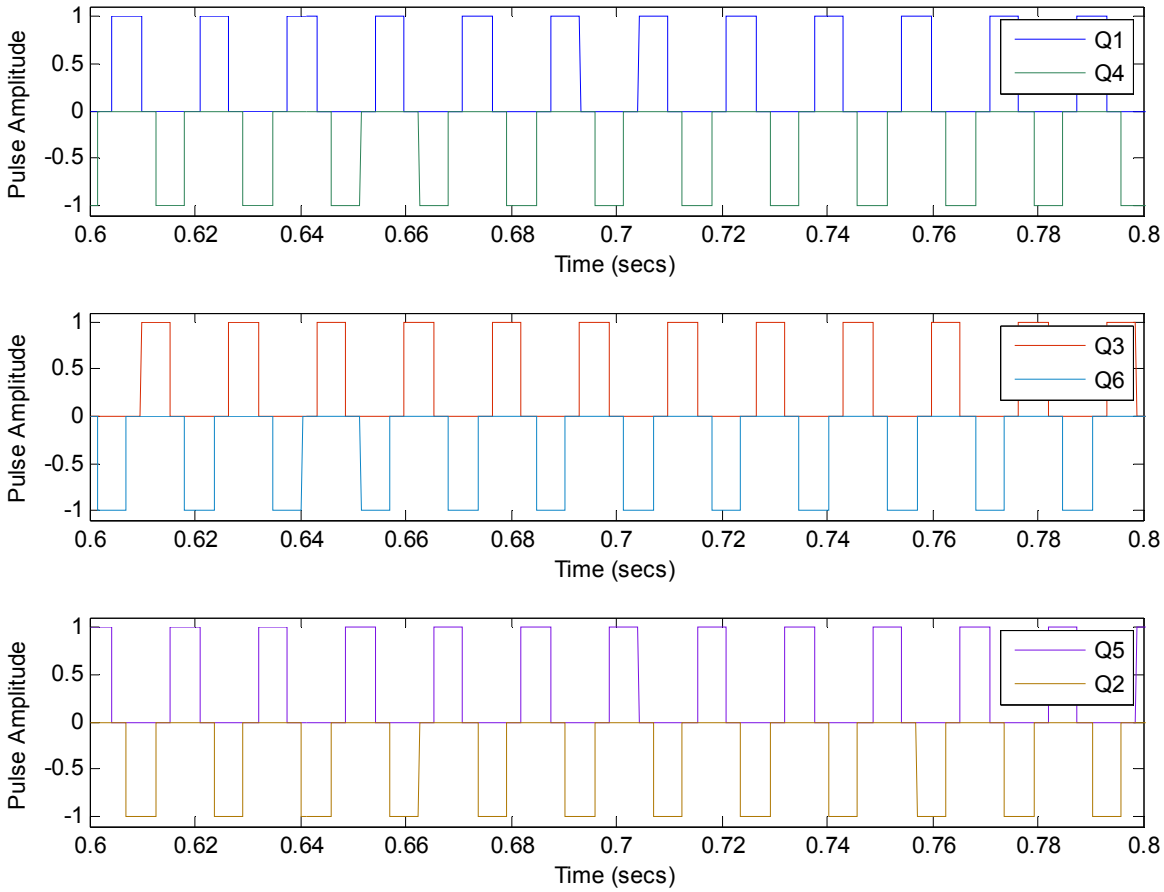



**Figure 4.15** Gate Drive Signals of Six Pulse Rectifier

not the case. In fact, a strong resemblance exists between the bottom of Figure 4.16 and Figure 2.25. The reason for the high ripple on top of the output voltage is due to the line inductance of the transformer, which is a nuisance in practical converters, or consistent charging / discharging of the output capacitor. Further details on the subject can be found in [4, 7].

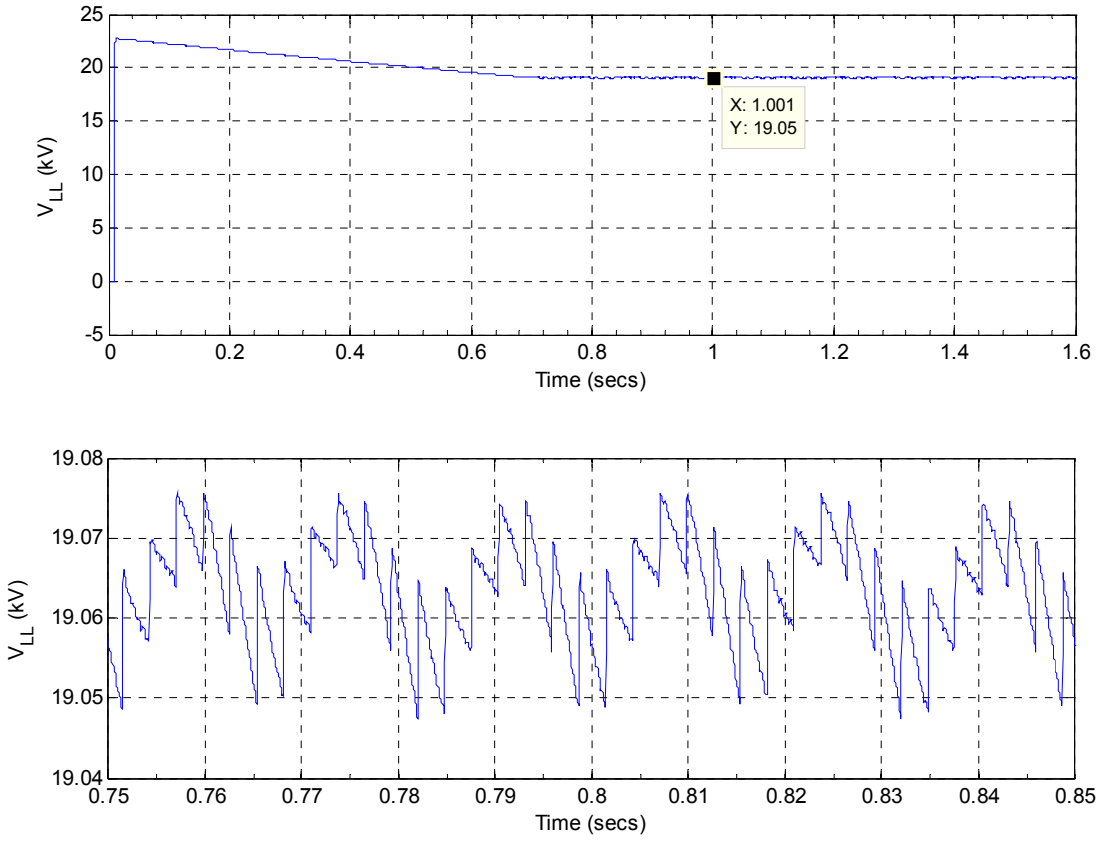



**Figure 4.16** Output Line-to-Line Voltage of Six Pulse Rectifier with $\alpha = 0^o$

Our final discussion on validating the rectifier model will be showing that by increasing the delay angle, illustrated in Figure 2.27, the output line-to-line voltage of the rectifier does drop according to (2.5). The analytics based upon (2.5) predict the output voltage to be 13.36 kV as shown in (4.10) if the firing delay angle is set to $45^o$. After tuning the alpha control of Figure 4.13 to $45^o$, the PSCAD simulation output found in Figure 4.17 shows agreement with theory.

$$V = \frac{3\sqrt{2}}{\pi} V_{LL,rms} \cos\alpha = \frac{3\sqrt{2}}{\pi}(14kV)\cos(45^o) = 13.36kV \tag{4.10}$$

For this simulation, the wind turbine system was removed and replaced with an ideal voltage source of 575 $V_{LL}$ serving as an input to the Y-Δ transformer, which is the reason for reaching steady-state rather quickly. Changing the generation source will have no impact on the control schemes of the rectifier.

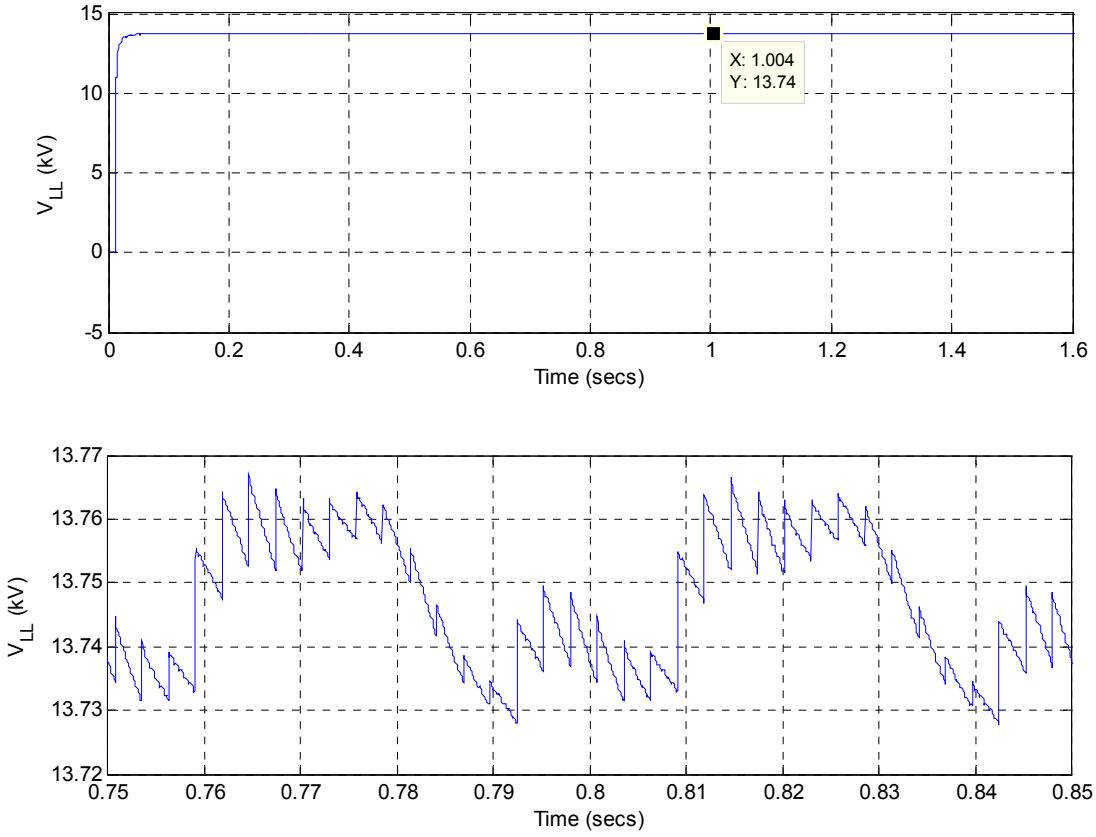



**Figure 4.17** Output Line-to-Line Voltage of Six Pulse Rectifier with α = 45°

## 4.4 DC-TO-DC CONVERTER MODELING AND VALIDATION

The bidirectional DC-to-DC converter modeled in PSCAD for the medium voltage DC network is shown in Figure 4.18. The diagram in Figure 4.18 contains an ideal voltage source at its input. The input to the DC-to-DC converter in the overall model uses the output DC voltage of the rectifier. If an ideal voltage source were not used to perform the initial model validation, the output waveforms would be questionable. The latter statement is only mentioned because, through sensitivity analysis, the parameters chosen for the converter have drastic impacts on the output waveforms that might be unrealistic. The parameters used for this converter are found in Table 4.3, which are consistent with the network model of Figure 4.1. The biggest difference between the converter used in Figure 4.18 and Figure 4.1 is the load resistance. A 18 Ω resistive load was chosen in Figure 4.1 because not enough power is generated by the wind turbine to serve the power demand of the 10 Ω resistive load in Figure 4.18.

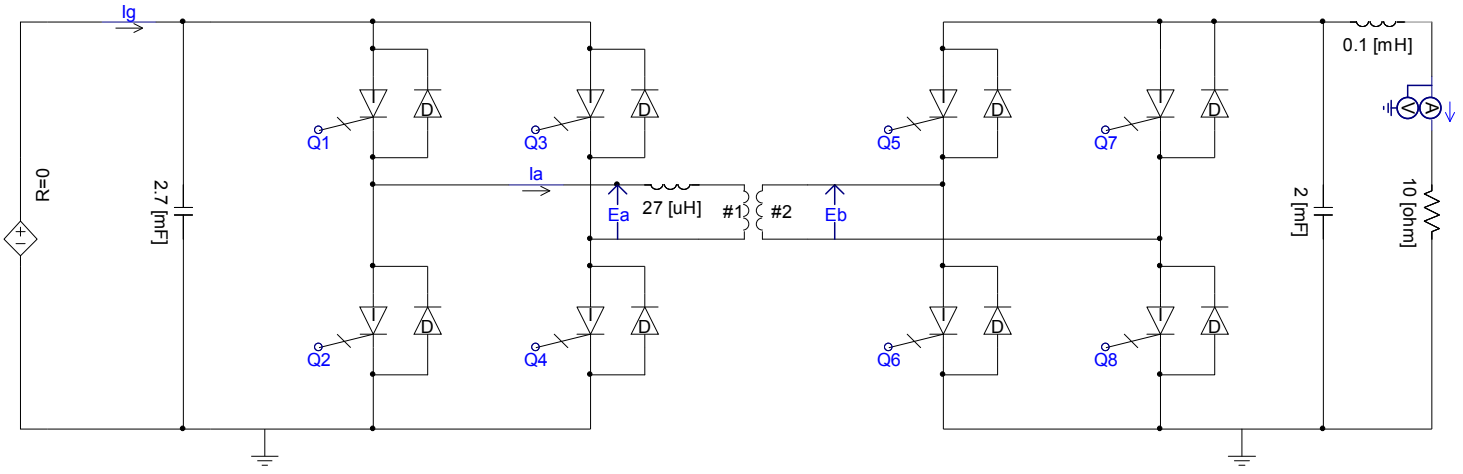



**Figure 4.18** PSCAD Model of Bidirectional DC-to-DC Converter

**Table 4.3** Bidirectional DC-to-DC Converter Parameters [17]

| Parameter | Numerical Quantity |
|---|---|
| Transformer Rated MVA | 25 MVA |
| Switching Frequency, $f_s$ | 2000 Hz |
| Input Filtering Capacitor | 2.7 mF |
| Output Filtering Capacitor | 2 mF |
| Leakage Inductance, $L_l$ | 27 μH |
| Choke Inductance | 1 mH |
| $n = n_2 / n_1$ | 5 |

A couple of different approaches can be used to validate the switch control of the converter. If the control is working appropriately, all other parameters of interest should conform to the expected theoretical values. To validate the control, the theoretical plots of Figure 2.30 should be consistent with the output waveforms of the PSCAD model. Figure 4.19 provides the primary and secondary voltage waveforms of the DAB converter of Figure 4.18. Notice that these plots are consistent with the voltage diagrams of Figure 2.30.

A 0.125 msec delay ($90^o$ phase shift) exists between the voltage waveforms, which will develop the maximum amount of power seen by the resistive load as described in Chapter 2. The primary side voltage, read from Figure 4.19, is 4 kV, which is expected since this is an internal input to the ideal voltage source. On the secondary side, 20 kV would have been *ideally* expected but, due to losses through the leakage inductance, a value slightly lower than 20 kV was achieved. Note that this diagram is enough to show that the switch control is working correctly.

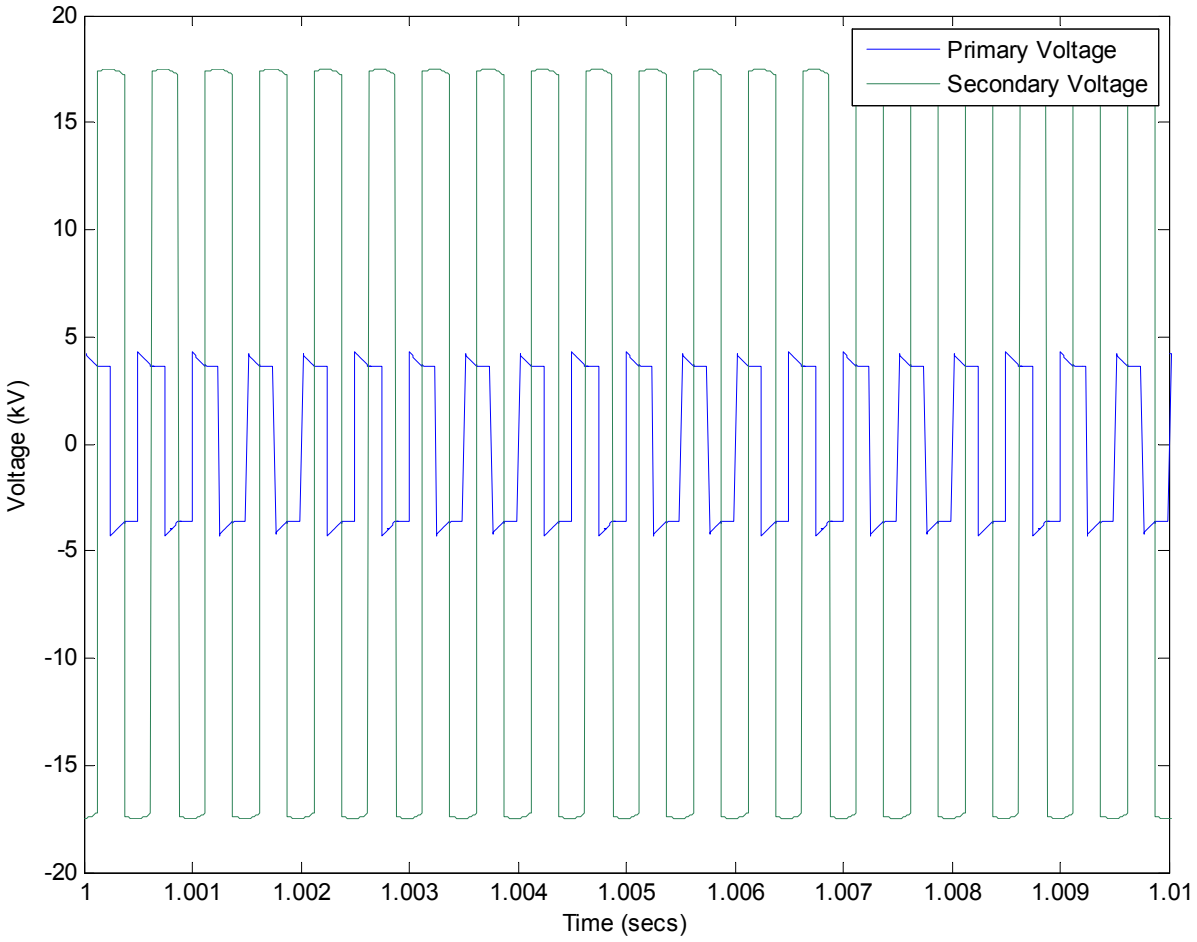



**Figure 4.19** Simulated Primary and Secondary Voltages of DAB Converter Transformer

The simulated waveforms for the input current and primary side current are found in Figure 4.20. Again, the shape of the signals can be validated with Figure 2.30 but it is not enough to validate these plots. The easiest way to validate the magnitudes of the currents is by averaging the input current signal over one period. The average DC input current, $I_g$, is mathematically written as (4.11), where D is the duty cycle and $I_p$ is the peak DC input current. Note that the triangular areas of Figure 4.21 cancel each other out leaving a rather simple integral to evaluate (an area of a rectangle), which is how (4.11) was obtained rather easily.

$$\langle I_g \rangle = I_p(1-D) \tag{4.11}$$

Equation (4.11) is in terms of the peak DC input current. Converter equations should normally be written in terms of known parameters. Recalling that the slope of the DC input current can be written from the constitutive relationship for the voltage across an inductor, (4.12), we can rewrite $I_p$ in terms of the system input parameters ($V_g$, $L_l$, $T_s$, D). This relationship is listed as (4.13). Substituting (4.13) into (4.11), we arrive at the peak DC input current, (4.14), for both the primary side current and input current of the DAB converter. If we assume that D is much less than 1, (4.14) can be reduced to (4.15). Substituting numerical quantities into (4.15), we again show strong agreement between theory and simulation with an expected peak current of 18.51 kA.

$$\frac{di_L}{dt} = \frac{v}{L} \tag{4.12}$$

$$I_p = \frac{V_g}{L_l}\left(\frac{DT_s}{2}\right) \tag{4.13}$$

$$\left\langle I_g \right\rangle = \frac{V_g}{L_l}\left(\frac{DT_s}{2}\right)(1-D) \tag{4.14}$$

$$\left\langle I_g \right\rangle = \frac{V_g}{L_l}\left(\frac{DT_s}{2}\right) \tag{4.15}$$

$$\left\langle I_g \right\rangle = \frac{4kV}{27\mu H}\left(\frac{0.5}{2}\frac{1}{2000}\right) = 18.52kA$$

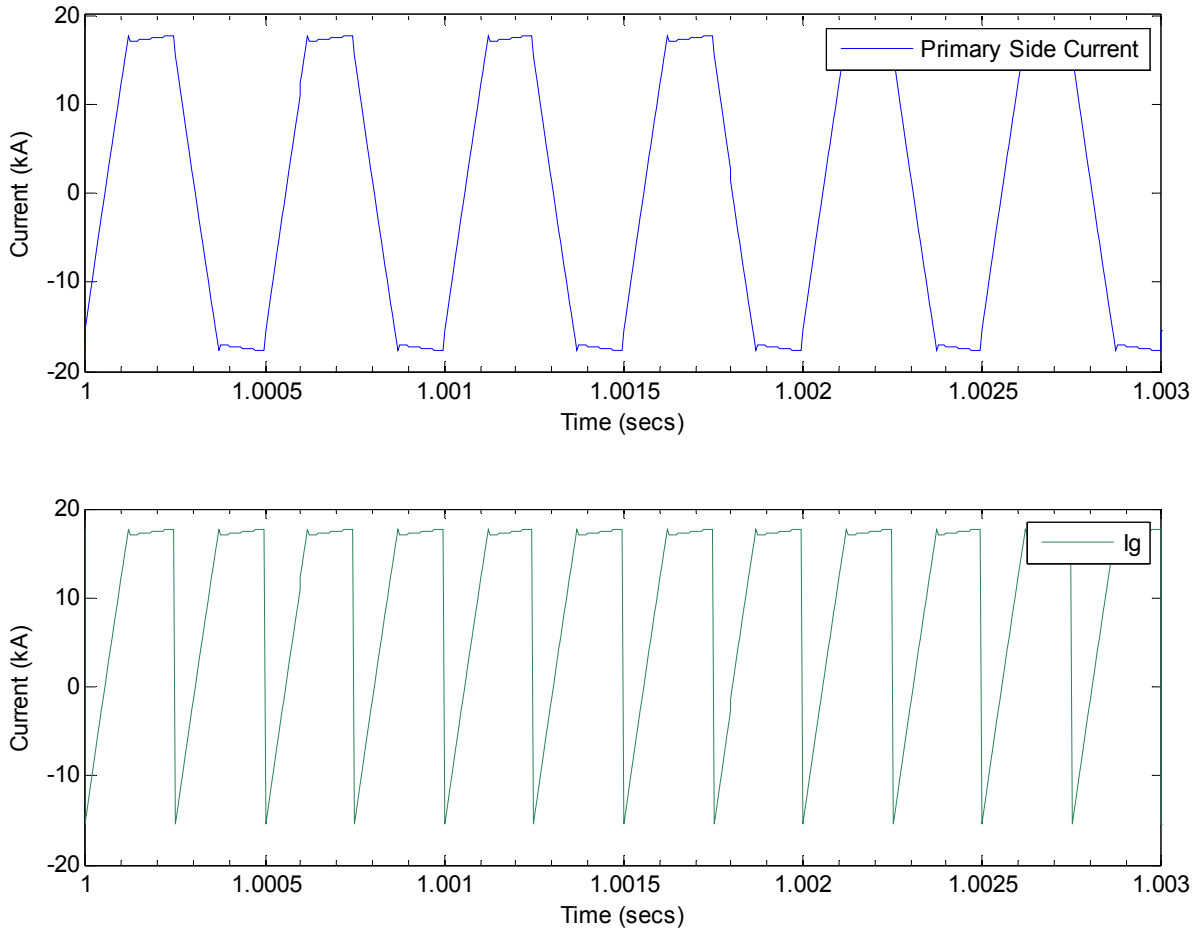



**Figure 4.20** Simulated Input Current and Primary Side Current of DAB Converter

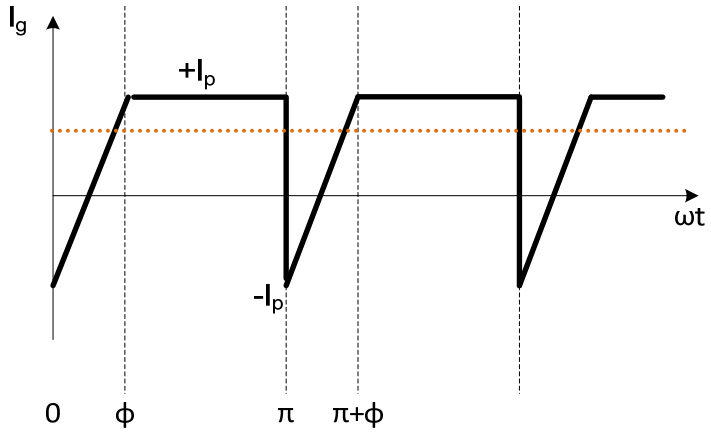



**Figure 4.21** Average Value of Input Current (Dotted Line) fed into DAB Converter

For completeness, the output DC voltage under the conditions specified is found in Figure 4.22. The beauty of this converter is that the secondary voltage of the transformer, having a square-like nature, is essentially rectified to produce a smooth, constant output voltage with appropriate switch implementation and control. The real output power of this circuit was measured and shown to be 30 MW with a 10 Ω resistive load, an expected result if one were to find the ratio between the square of the output voltage and load resistor.

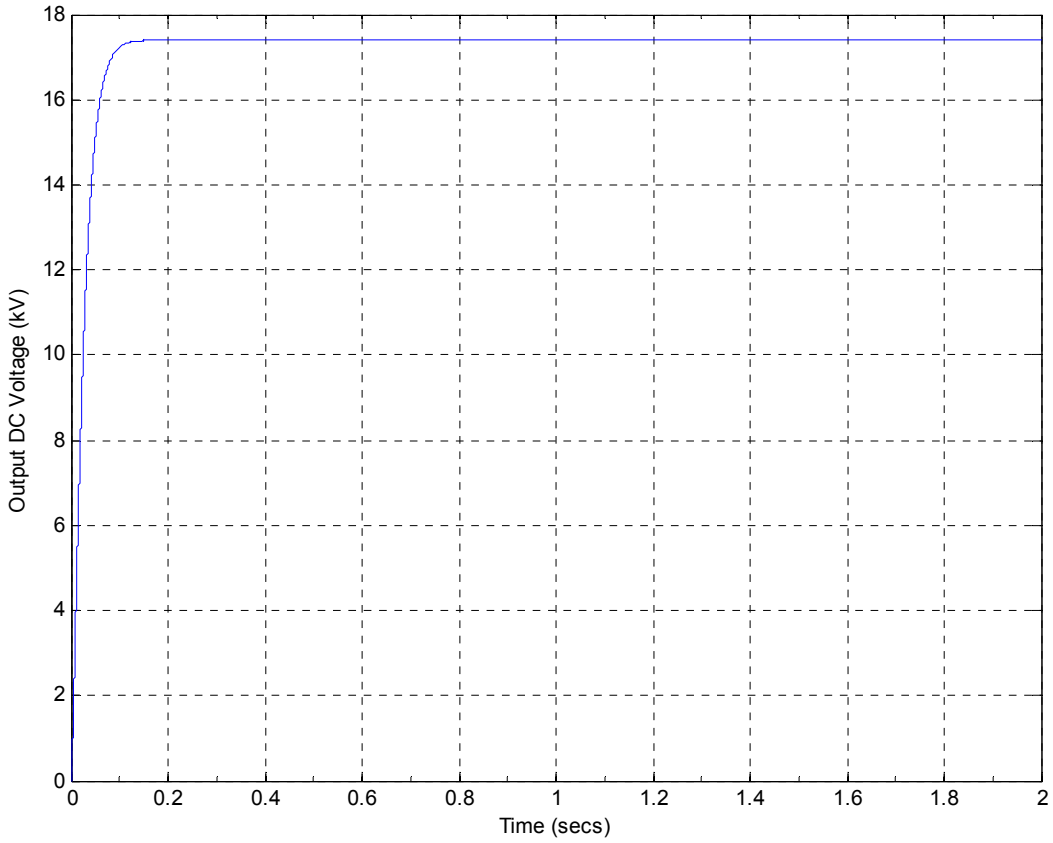



**Figure 4.22** Output DC Voltage of DAB Converter

Two methods were mentioned in Chapter 2 for switching the semiconductors, the one previously mentioned and the second with timing diagrams shown in Figure 2.31. The author feels that the method described and validated will find more wide spread use in future renewable integration applications, however, the second method was adopted throughout future simulations.

## 4.5 MULTILEVEL INVERTER MODELING AND VALIDATION

A PSCAD circuit of a five-level NPC multilevel inverter is found in Figure 4.23. The semiconductor element chosen for this model is the IGBT and is switched at a frequency of 2400 Hz. The circuit layout divides the 20 kV input DC voltage source by four resulting in 5 kV seen across each capacitor. The capacitors have a capacitance of 4000 μF, a value cited from [13].

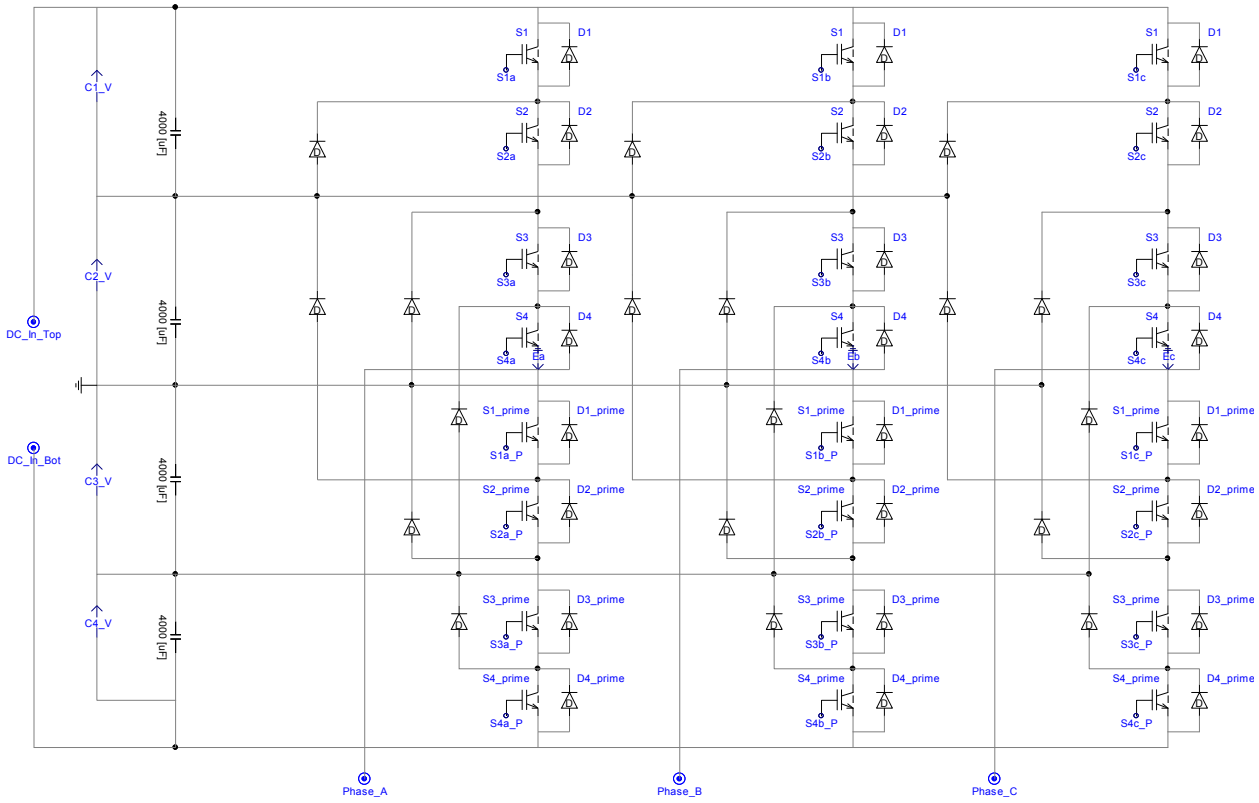



**Figure 4.23** PSCAD Model of a Five-Level Neutral Point Clamped Multilevel Inverter

For our discussions in this section, our focus will be on the five-level NPC multilevel inverter because the switching strategies are the same for any configuration of the NPC inverter as well as the five-level FC inverter. However, for completeness, the PSCAD circuit of the five-level FC inverter is found in Figure 4.24.

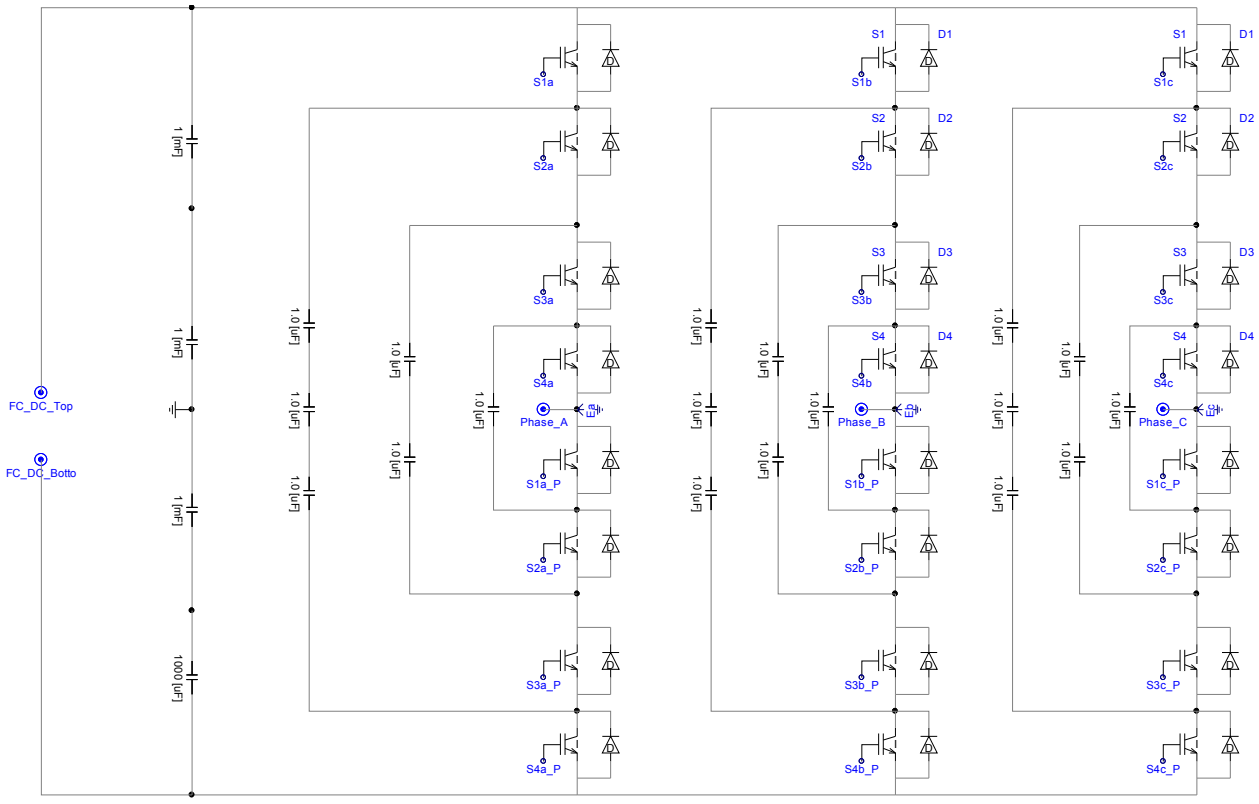



**Figure 4.24** PSCAD Model of a Five-Level Flying Capacitor Multilevel Inverter

Our discussions will begin with the control of the semiconductor switches. As was the case with the rectifier discussion, two control panels to regulate the modulation frequency and index during any point in the simulation, if desired, are coded in the model. These are graphically displayed in Figure 4.25. The reference signals for the switches of each leg are generated by the blocks found in Figure 4.26, all of which are dependent on the modulation index. There is one block set for all three phases of the power system. Finally, Figure 4.27

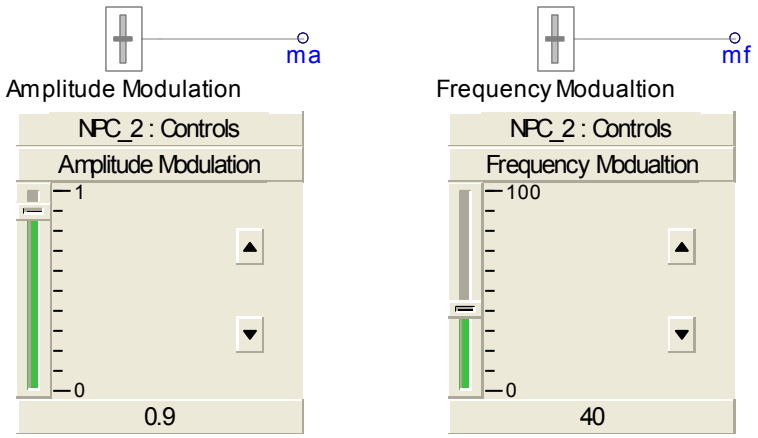



**Figure 4.25** Amplitude and Frequency Modulation Control Panels in Inverter Sub-modules

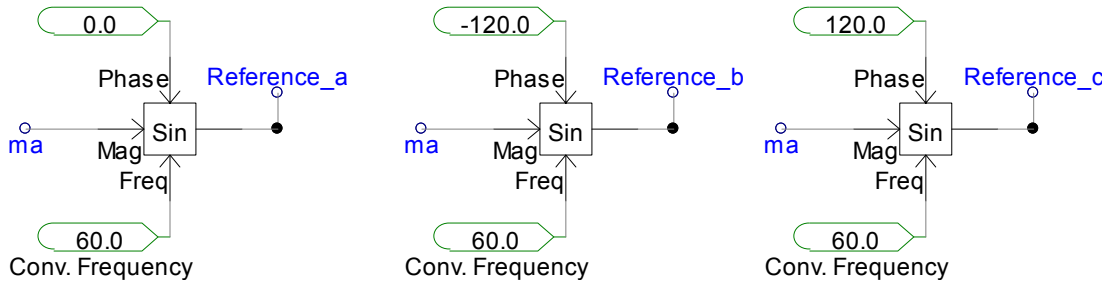



**Figure 4.26** PSCAD Blocks used to Create Reference Signals for all Three Phases of the Power System

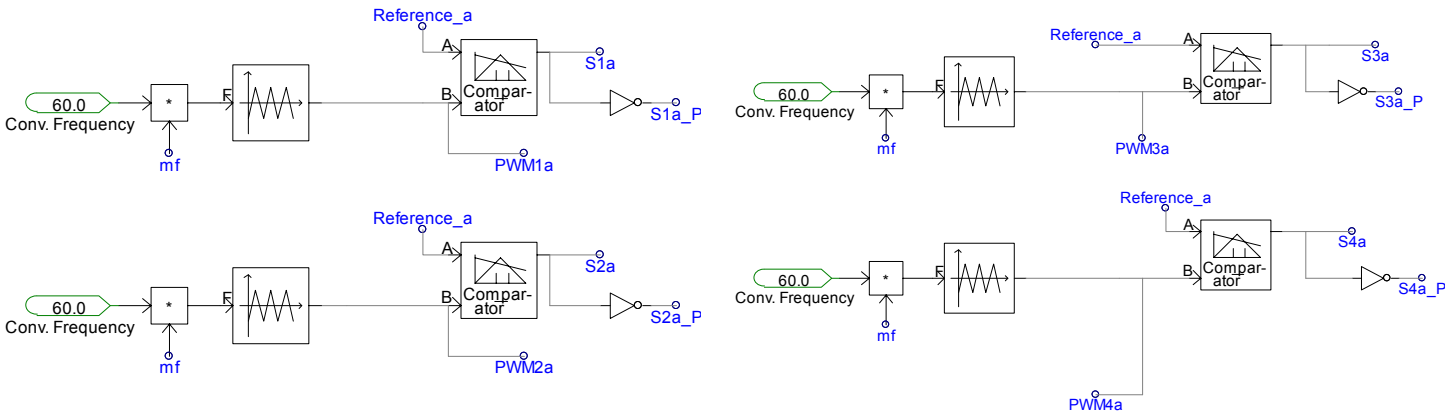



**Figure 4.27** Gate Drive Circuitry for Switching IGBT (Phase A Leg Shown Only)

shows the gate drive circuits. There are a total of 12 gate drive circuits in the model having four circuits per phase. Figure 4.27 only shows the circuitry to control the eight semiconductor devices of Phase A. As was explained in Chapter 2, the pulse width modulation theory requires two signals to control the switches, a carrier signal and reference signal. If the reference signal is higher in magnitude, at any instant of time compared to the carrier signal, then, for example, S1a will turn ON and if the reference signal is lower than the carrier signal, S1a_P turns ON. This latter point is the reason for the comparator in all the circuits of Figure 4.27 whose inputs are the reference and carrier signals. Figure 4.28 and Figure 4.29 illustrate the carrier signals and gate drive signals used to perform the DC-to-AC conversion. Note that only the signals for the top four switches of Phase A are illustrated to avoid a cumbersome and confusing plot. Based on the previous explanation and examining these figures, it makes sense why switch S4a is ON the longest of all four.

As explained in the theory of Chapter 2, a five-level multilevel inverter, in general, should have nine "steps" in its line-to-line output voltage. The line-to-line output voltage waveform of the five-level NPC inverter is found in Figure 4.30. We can observe that there are indeed nine levels in the waveform and equally spaced from each other. The target of reaching a peak of 20 kV is slightly under achieved due to losses in the medium voltage DC network. This can be fixed by altering the turns ratio on the 575 V / 14 kV Y-Δ transformer.

One of the biggest challenges with the NPC inverter topology is balancing the capacitor voltages. Figure 4.31 provides a zoomed-in shot of the voltages seen by each of the four capacitors in the model. Although the capacitors are not balanced, adverse effects on the output voltage are unnoticeable. Advanced closed loop control schemes have been investigated in [13] to solve this issue but are well beyond the scope of this work.

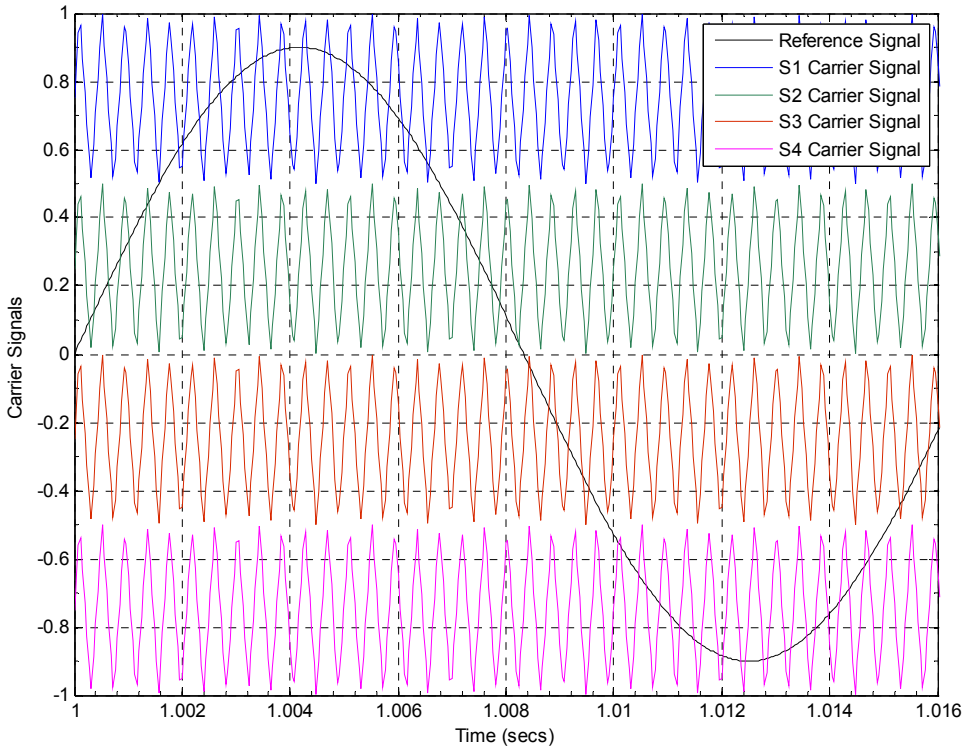



**Figure 4.28** Simulated Reference and Carrier Signals for Phase A Leg of NPC Five-Level Inverter

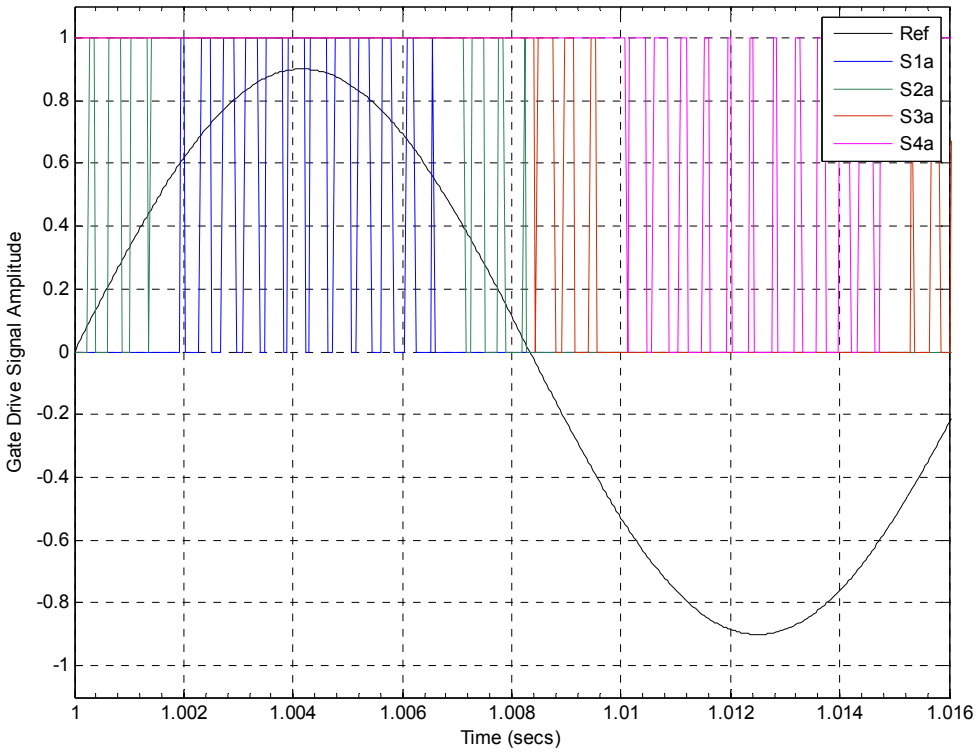



**Figure 4.29** Simulated Gate Drive Signals for Upper Half Switches of Phase A Leg

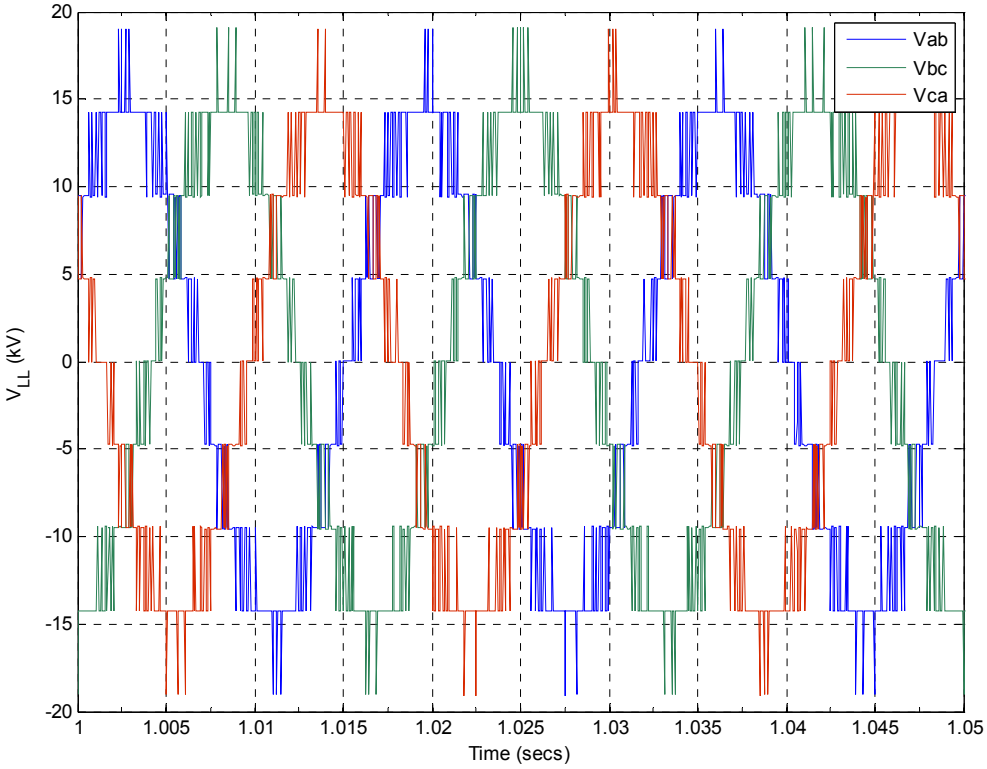



**Figure 4.30** Simulated Three-Phase Line-to-Line Output Voltage Waveform of Five-Level NPC Inverter

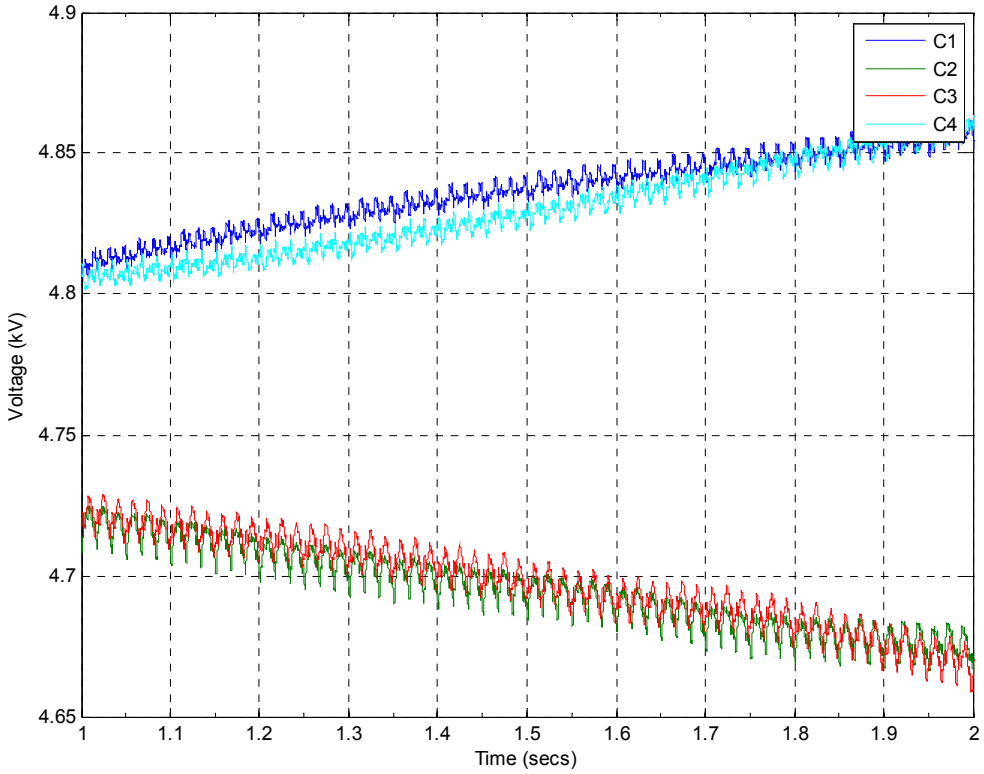



**Figure 4.31** Simulated Line-to-Line Output Voltage Waveform of Five-Level NPC Inverter

# 5.0 EVALUATING MULTILEVEL INVERTER PERFORMANCE IN A MEDIUM VOLTAGE DC NETWORK

Throughout the thesis thus far, attempts have been made to provide the underlining theory of the major components in the MVDC network model and techniques for modeling the equipment in PSCAD. The objective of Chapter 5 is to apply various types of disturbances to the validated model and evaluate their impacts on the overall system dynamic performance.

The first scenario to be evaluated is the impact on the system when the wind essentially "stops blowing". From a simulation perspective, this is when the average wind speed drops from 14 m/s to 0 m/s at a defined time in the simulation. The second scenario to be investigated is when a single phase fault is applied to the positive terminal of the DC-to-DC converter connected to the 20 kV bus. The third scenario examined is when different loads are switched in and out of the circuit and, finally, the last configuration analyzed is the impact of a line-to-ground fault at the input terminals of one of the induction machines on the network. The metric for evaluating the model's performance will be through the total harmonic distortion (THD) of the converters as well as traditional techniques, like observing overvoltages in the network, used in power system analysis.

The PSCAD model with all assembled power converters, electric machines, and wind turbine representing Figure 4.1 is found in Figure 5.1. The only components not shown are the circuit breakers. Values on metering devices should be disregarded.

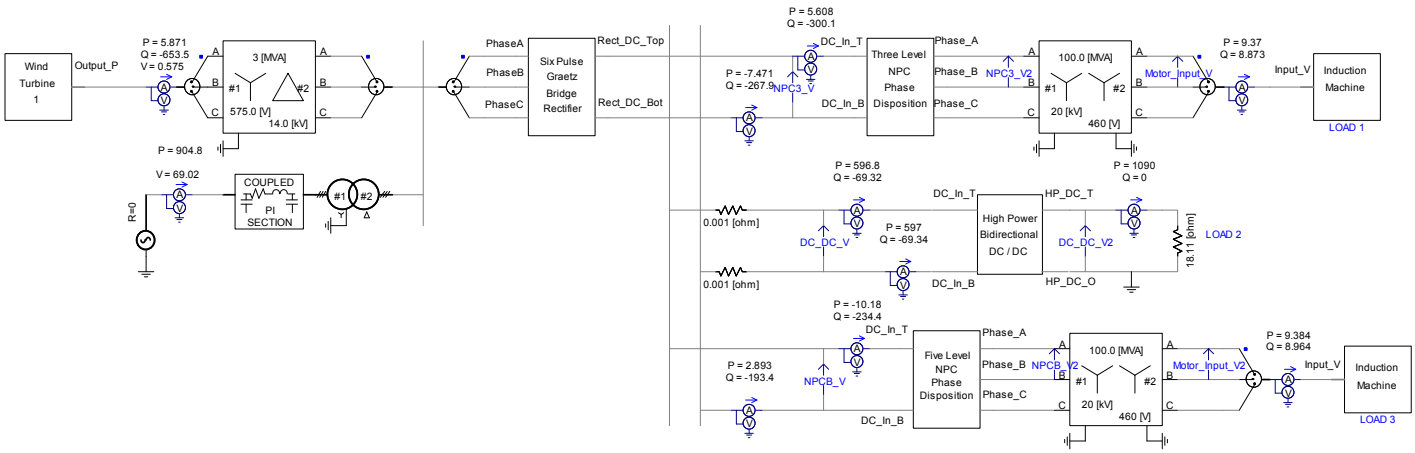



**Figure 5.1** Base Case PSCAD Model of MVDC Network

## 5.1 SYSTEM DYNAMIC RESPONSE TO CHANGES IN WIND SPEED

As described in the latter paragraphs, a test was conducted on the network which simulates the case when the wind stops blowing. The purpose of running this case is to provide a check to make sure that no matter what happens to the generation resources, the constraint of the power generated being equal to the power absorbed for any power network is appropriately maintained.

The power balancing simulation results are found in Figure 5.2. As was stated in Chapter 4, the electric machines are simulated first in speed control and switched into torque control based upon the torque supplied by the wind turbine. The transition occurs at 0.3 seconds into the simulation. The wind adjustment occurs at 1.3 seconds into the simulation, where the average wind speed drops from 14 m/s to 0 m/s in a step change fashion. The model responds as expected with the wind power delivering 1.4 MW to the system and exponentially decaying to zero. The grid, represented by an equivalent, ideal voltage source with a 69 kV transmission line whose parameters are based off of those tabulated in [27], responds to supply the demand.

The plots below the supplied generation are those of the power absorbed by the induction machine, one is only shown, and the AC load interfaced by the DC-to-DC converter. Note that the power supplied does not exactly match the demand. This is because losses exist in the 0.001 Ω resistors in series with the DC-to-DC converter and transformers, whose losses are on the order of kW.

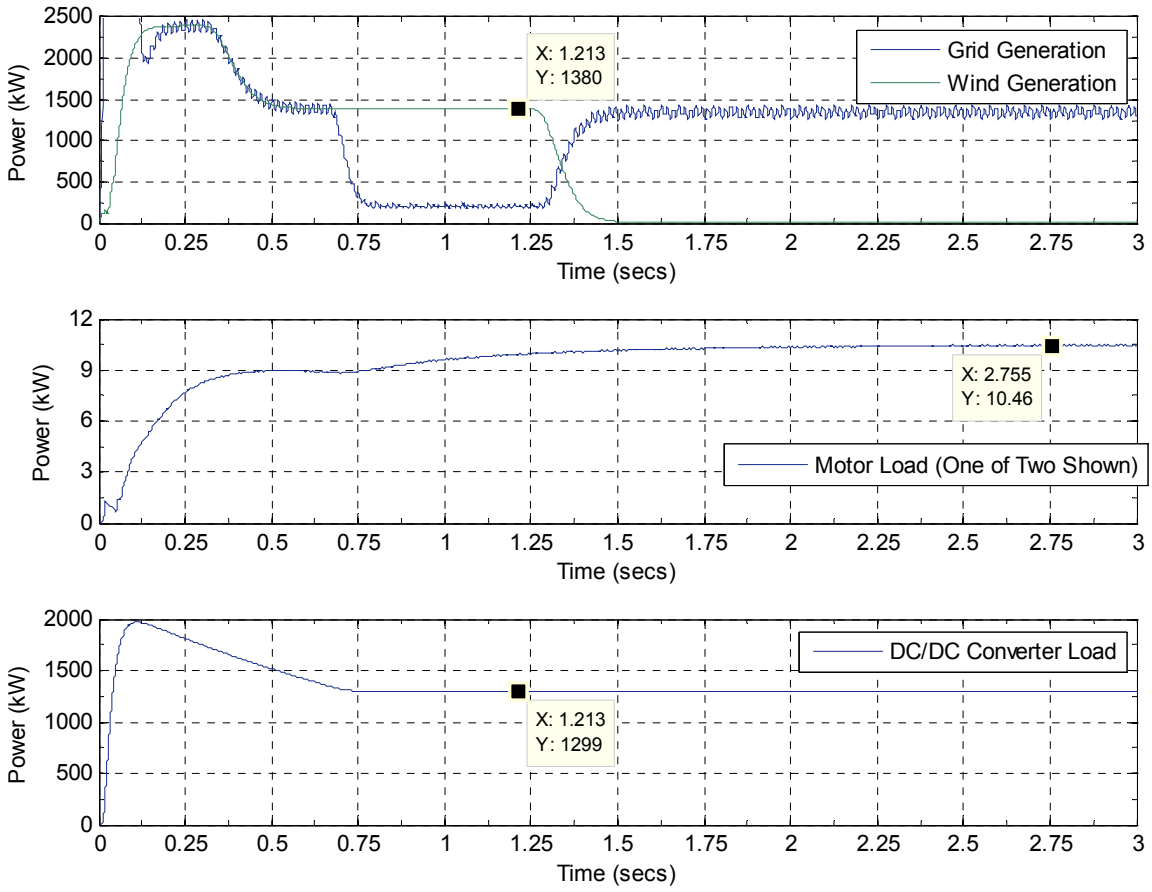



**Figure 5.2** Power Balance on MVDC Network with Change in Wind Speed

Machine parameters of interest for the induction generator interfacing the wind turbine to the MVDC network and blade pitch of the wind turbine are plotted in Figure 5.3. Notice how the mechanical speed of the induction machine drops to 1 pu. Figure 3.7 shows that when the mechanical speed is 1 pu, the output torque is zero resulting in zero output power. The most interesting response is that of the blade adjustment. The wind turbine governor in Figure 4.6

begins to respond by reducing the blade pitch angle towards zero (see Figure 3.11) to potentially increase the output power of the wind turbine.

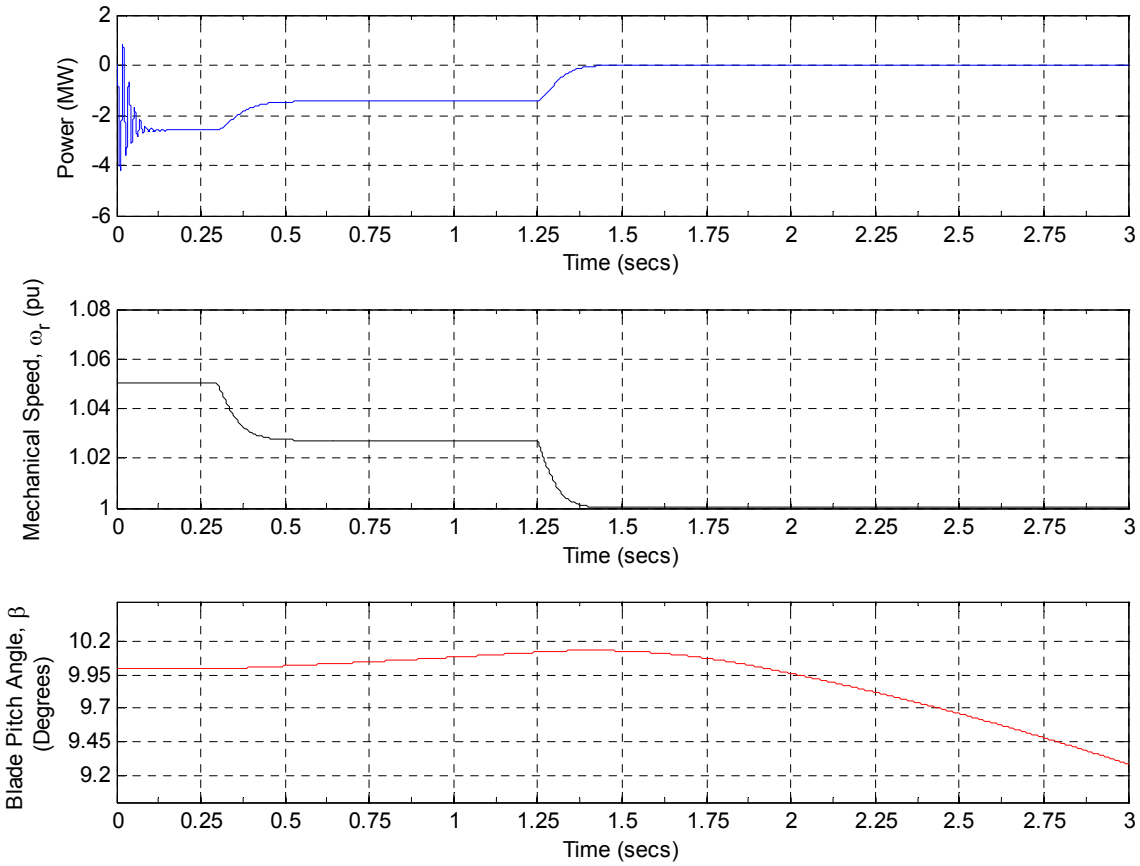



**Figure 5.3** Induction Machine Parameters with Change in Wind Speed

The total harmonic distortion of a signal is defined a number of different ways but the definition adopted by PSCAD is found in (5.1). The THD essentially provides the ratio of all the harmonics in a signal with respect to the fundamental. A low THD, a desired design goal, implies that the magnitudes of the harmonics are relatively low compared to the fundamental component of the signal resulting in less signal distortion.

$$THD = \sqrt{\sum_{h=2}^{N}\left(\frac{h_n}{h_1}\right)^2} \tag{5.1}$$

A comparison of the THD of the line-to-line output voltage of the three-level, NPC multilevel inverter and the five-level, NPC inverter models in the network is found in Figure 5.4. The pulse width modulation strategy of the inverter is based upon the phase disposition technique discussed in Chapter 2. This diagram is enough evidence to show why research and development efforts are being put forth to increase the number of voltage levels in the inverters. As the number of levels increases, the output signal closely reflects a sinusoid and the THD decreases. However, the control complexity increases.

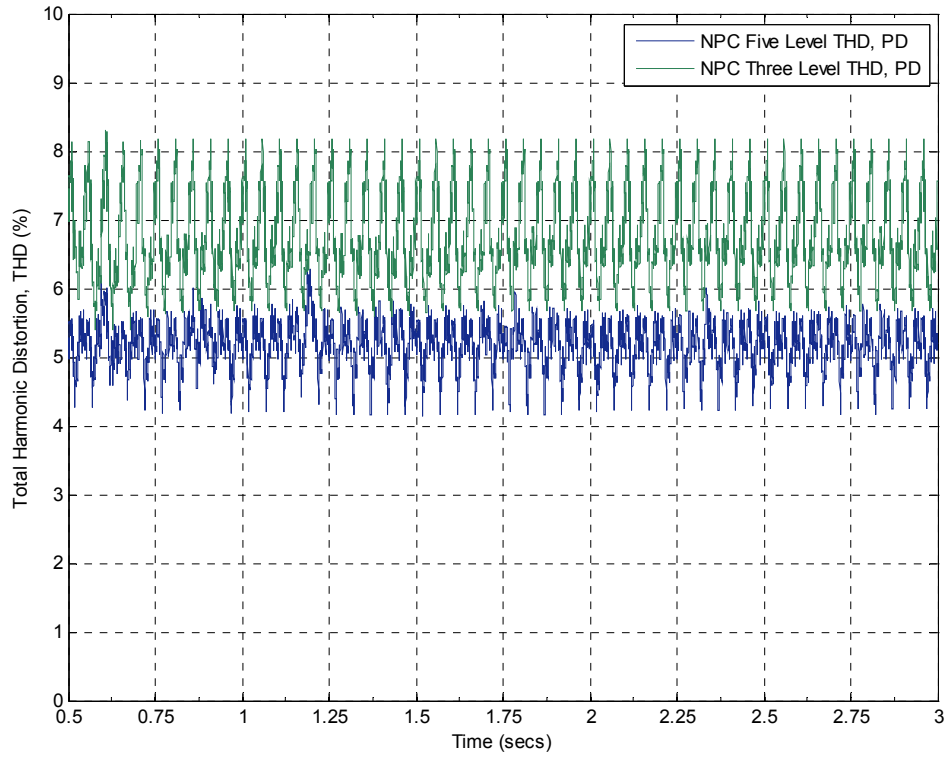



**Figure 5.4** THD Comparison of Three and Five-Level NPC Inverter Output Voltage Signal

A simulated comparison of the three different PWM techniques {PD, POD, APOD} applied to the NPC, five-level, multilevel inverter is found in Figure 5.5. One will notice that the phase disposition technique creates a lower THD compared to the other three methods and will be the selected PWM strategy for future applications; reference [28] validates this comment.

This simulation also validates the switching scheme implementation and provides another means for validating the inverter models.

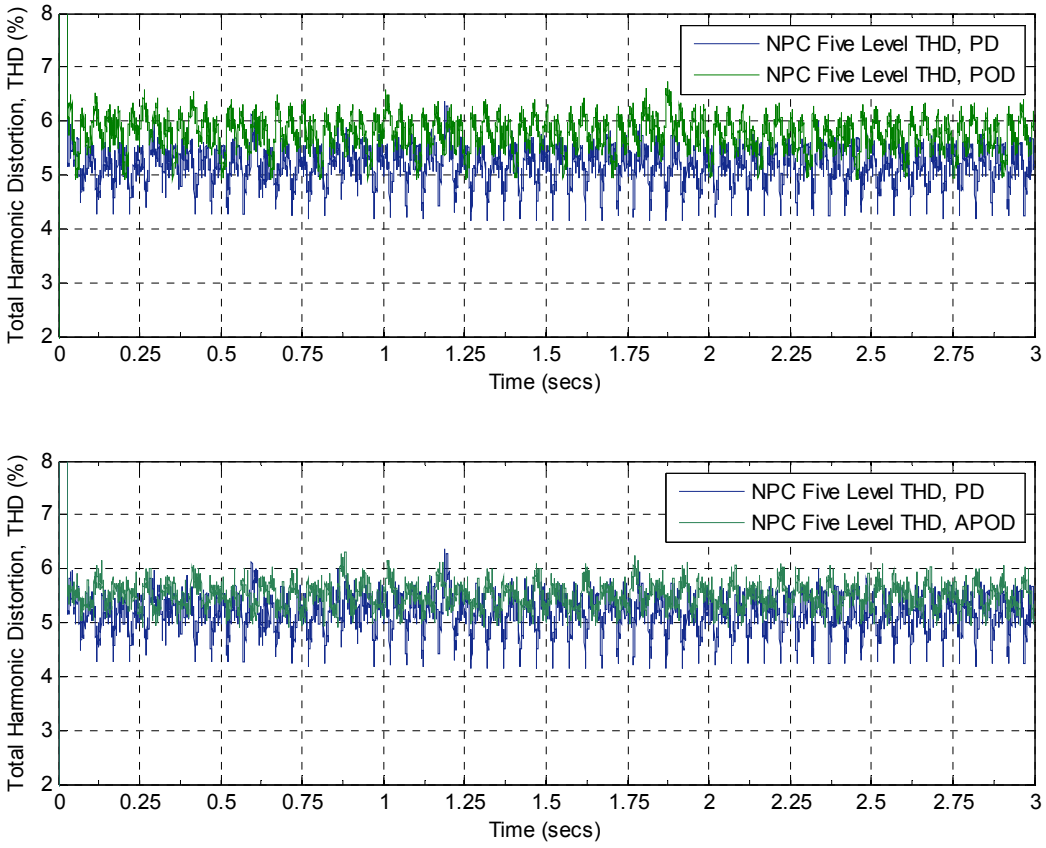



**Figure 5.5** THD Comparison between the PD, POD, & APOD PWM Methods for Five-Level, NPC Inverter

The last comment to be made on the inverters for this simulated scenario is regarding the voltages seen across the four capacitors of the NPC inverter. Simulation results of these voltages are found in Figure 5.6. Ideally, the voltages should balance with 5 kV seen across each capacitor. Capacitors $C_1$ and $C_4$ have the highest voltage across them of all four and also turn out to be the capacitors at the very top and bottom of the inverter as shown in Figure 2.16. From a practical standpoint, the capacitors will never exactly balance due to manufacturing capabilities and desired tolerances.

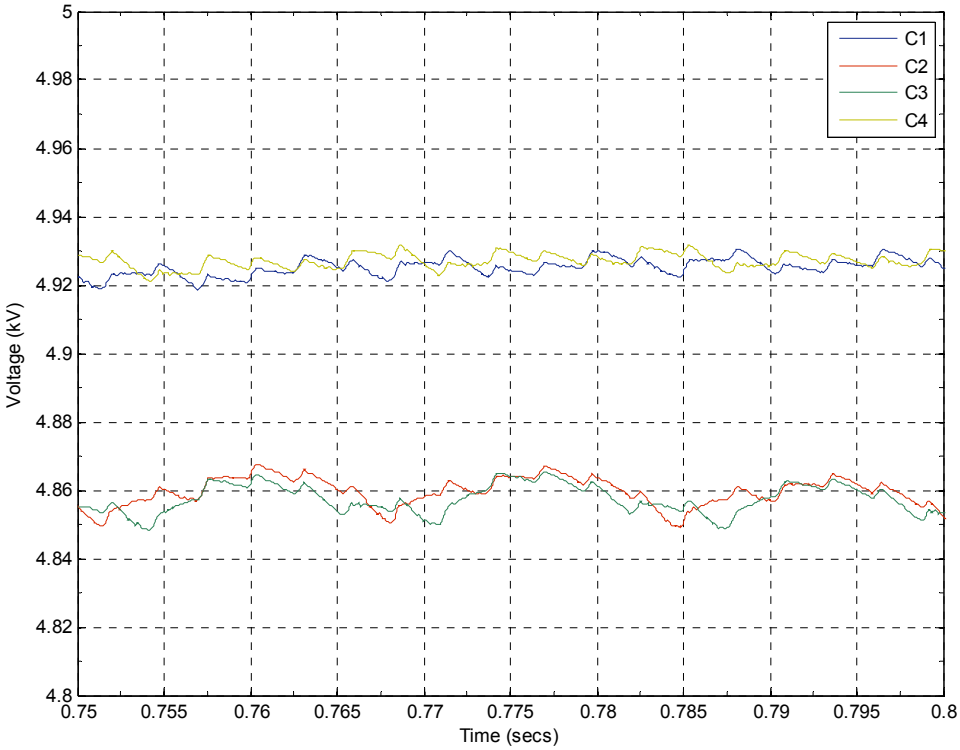



**Figure 5.6** Capacitor Voltages of NPC, Five-Level Inverter

## 5.2 FAULT APPLIED TO POSITIVE INPUT TERMINAL OF DC/DC CONVERTER

A fault (sudden occurrence of a grounding point) on a power system can potentially be the most detrimental type of disturbance because unexpected current magnitudes can be achieved and experienced by equipment not rated for such conditions. This section provides the simulation results for a single phase fault applied to the input positive terminal of the DC-to-DC converter illustrated in Figure 5.7. The fault was applied at 1.0 seconds into the simulation and lasted 0.2 seconds. The two breakers that interface the DC/DC converter with the 20 kV DC bus opened at 1.1 seconds and then closed at 1.5 seconds. In industry, this is referred to as a fault-clear scenario.

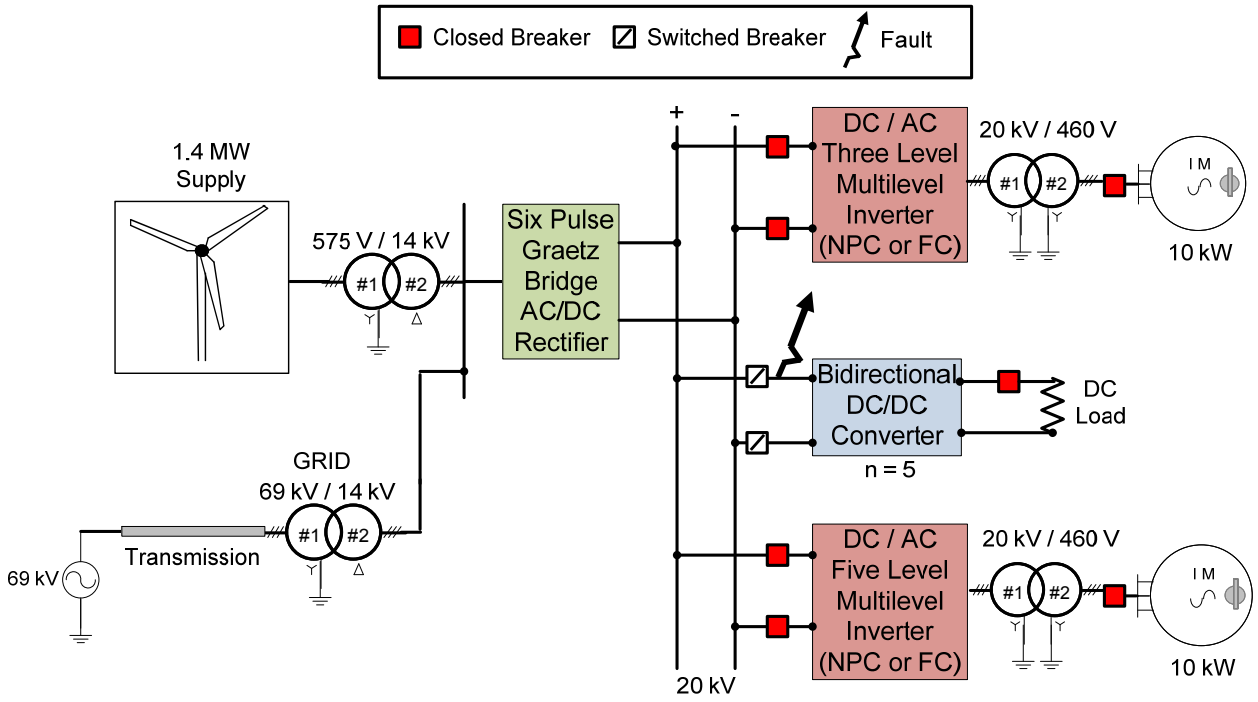



**Figure 5.7** Single Phase Fault Applied to Positive Terminal of DC/DC Converter

The first set of simulation results presented is found in Figure 5.8. The top result is the output power of the equivalent voltage source representing the utility and the bottom plot in Figure 5.8 is power generated by the wind turbine during the fault. Figure 5.9 is a plot of the line-to-ground voltage at the positive terminal of the DC-to-DC converter upon clearing the fault and closing the breaker at that connection point. The instantaneous high voltage response after closing is quite common due to the mismatch of energy initially on both sides of the breaker until an equilibrium point is reached.

Figure 5.10 and Figure 5.11 are graphics showing the output voltages of the three-level, and five-level, NPC inverters. For both cases, the capacitors are balanced up until the fault is applied but, upon clearing, the capacitors are never able to obtain a balanced state with the open

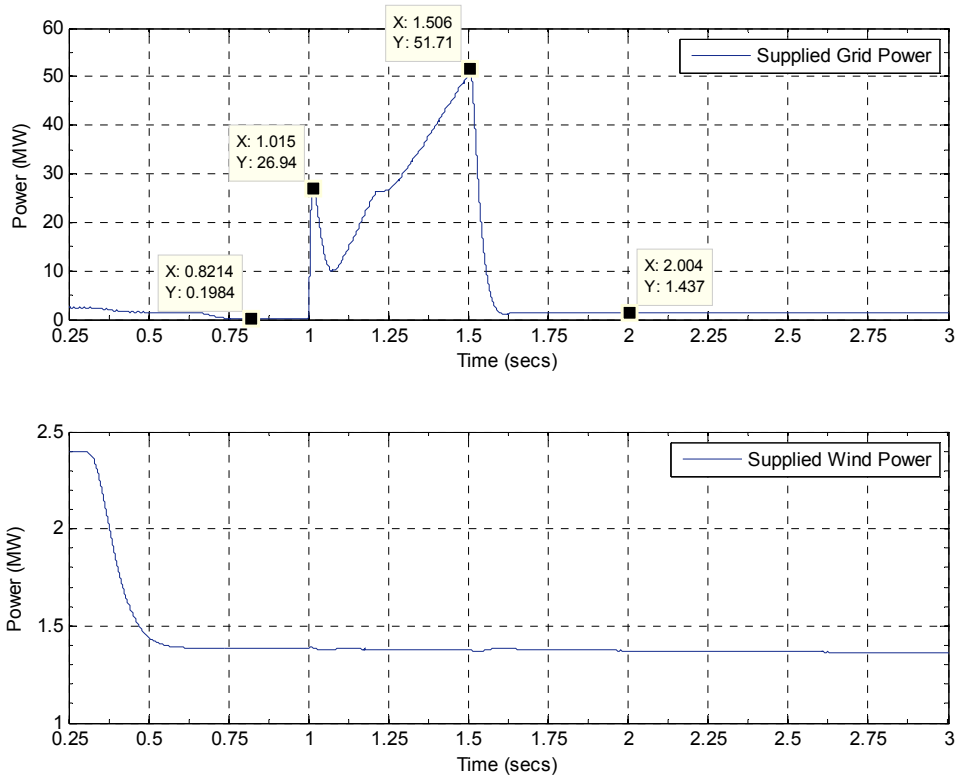



**Figure 5.8** Supplied Generation for a Single Phase Fault on DC/DC Converter Terminal

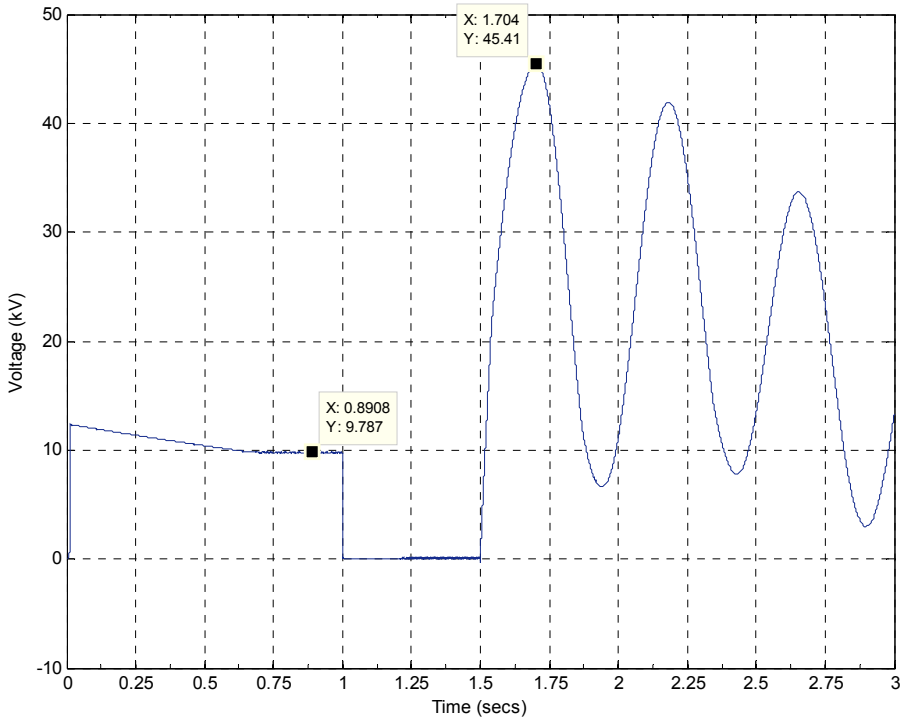



**Figure 5.9** Voltage Experienced by DC/DC Converter Breaker on System Side Upon Closing

loop control methods that have been adopted. Notice how the capacitor oscillations for the three-level, NPC inverter are sharply found in the output voltage of Figure 5.10. The THD distortion for the voltage signal of Figure 5.11 can be found in Figure 5.12. Load characteristics for the motors and DC/DC converter are found in Figure 5.13 and Figure 5.14, respectively.

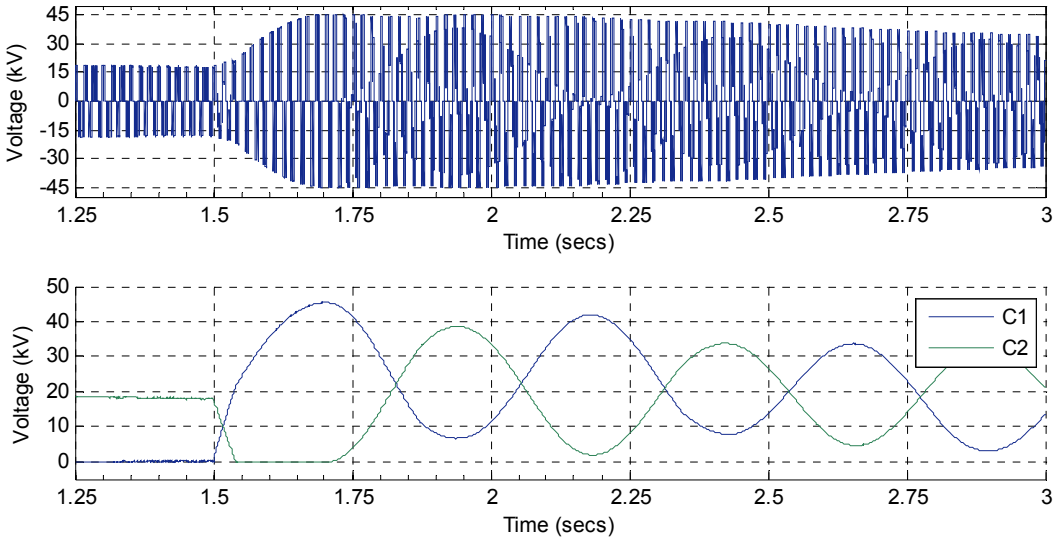



**Figure 5.10** Three-Level, NPC Inverter Output Voltage and Capacitor Voltages

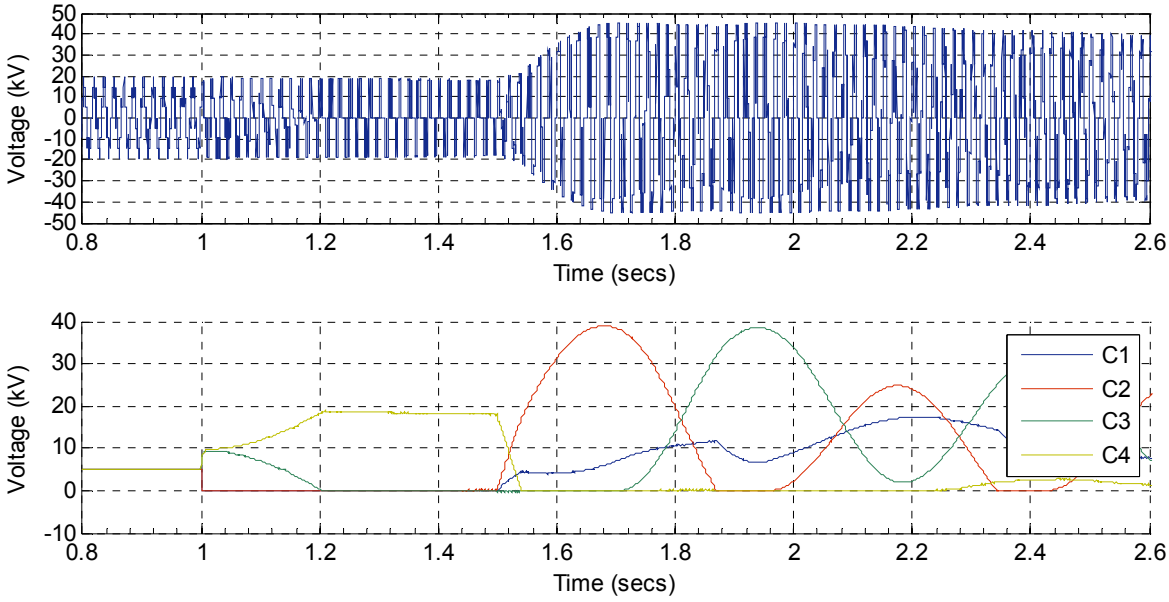



**Figure 5.11** Five-Level, NPC Inverter Output Voltage and Capacitor Voltages

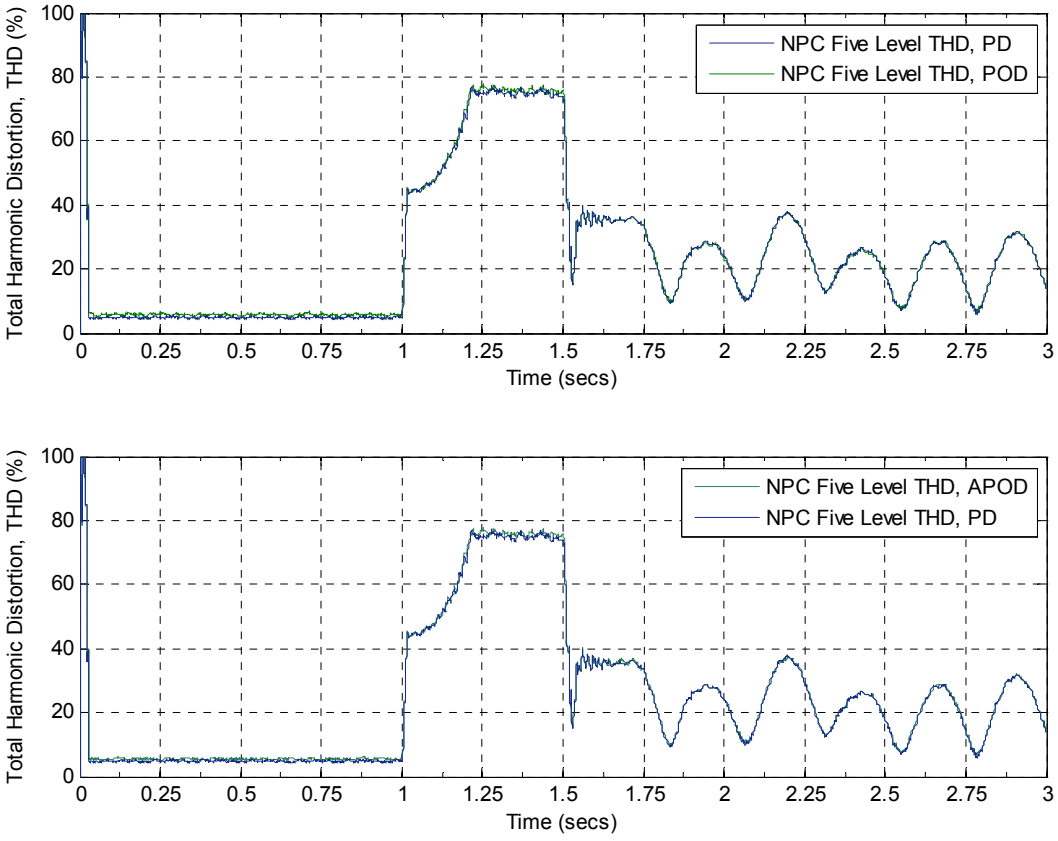



**Figure 5.12** THD for the Five-Level, NPC Inverter for Case of Fault on Positive Terminal of DC/DC Converter

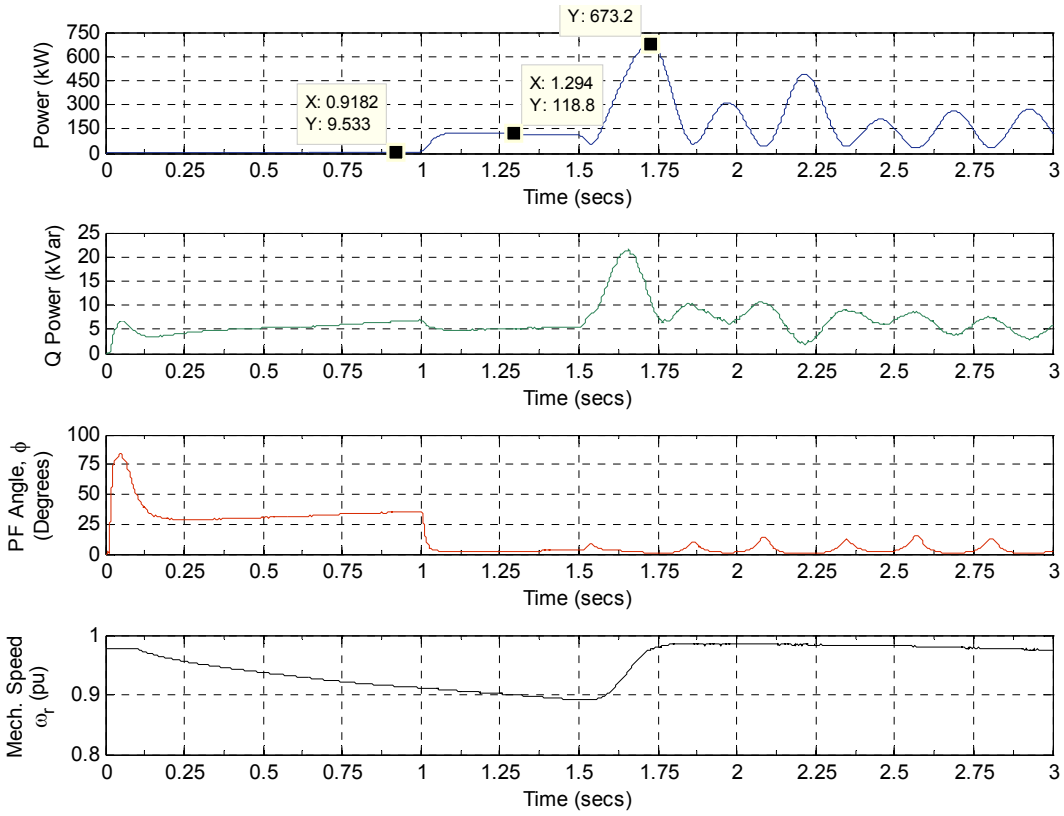



**Figure 5.13** Induction Machine Characteristics for Case with Fault on Positive Terminal of DC/DC Converter

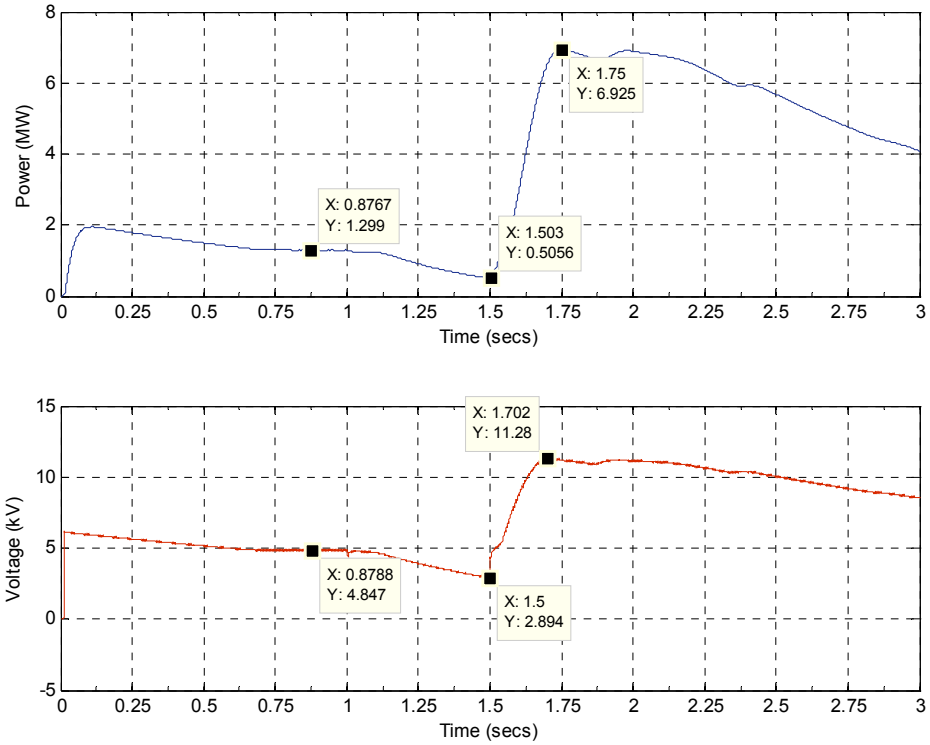



**Figure 5.14** Power and Voltage seen by DC/DC Converter Load

## 5.3 LOAD ENERGIZING AND SINGLE PHASE FAULT ON INPUT TERMINALS OF INDUCTION MOTOR

The last set of cases that will be run include a load energizing case and a single phase, line-to-ground fault applied to the input terminals of the induction motor as shown in Figure 5.15.

For the load energizing case, the top induction motor is always active in the circuit and, initially, the other two loads are not connected because the breakers interfacing the loads to the MVDC bus are open. After 1 second has passed in the simulation, the DC/DC breakers close and connect the DC/DC converter and load to the network. After 2 seconds have passed, the bottom motor is connected to the system. These simulations essentially evaluate the possibility of an overvoltage in the system because, in practice, there is a chance of the loads being connected / disconnected from the assembly.

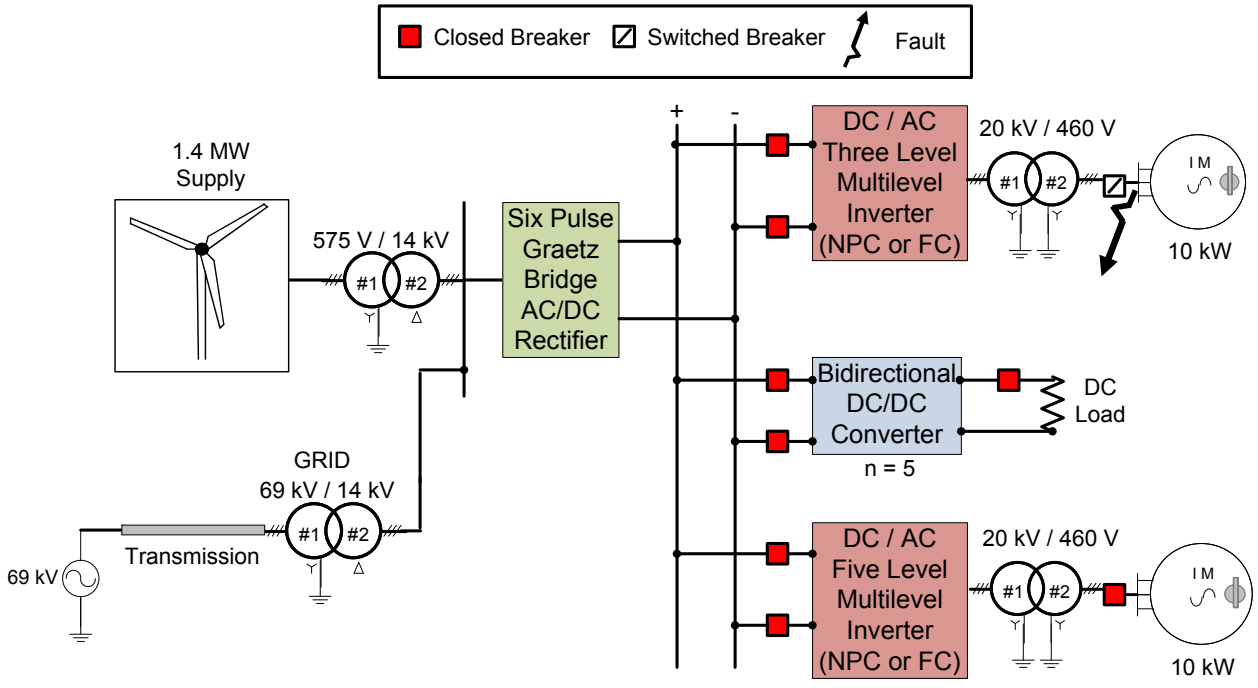



**Figure 5.15** Single Phase Fault Applied to Input Terminals of Induction Motor

Results for the load energizing case are illustrated in Figure 5.16 to Figure 5.20. Figure 5.16 provides the simulation waveforms of the supplied generation of the equivalent voltage source acting as the utility and generation provided by the wind, assuming a constant wind speed of 14 m/s. Figure 5.17 provides the output voltage of the five-level, NPC inverter and voltages seen by each of the capacitors in the inverter topology. The capacitor voltages are fairly balanced throughout the simulation cycle resulting in a clean output voltage waveform. The dip in the voltage is a result of adding the DC/DC converter load onto the MVDC bus, which is expected. The dip isn't as drastic when the bottom induction machine is added into the network because it only absorbs 10 kW in comparison to a 1.3 MW load. Figure 5.18, Figure 5.19, and Figure 5.20 provide how much real and reactive power each load absorbs throughout the simulation.

The final scenario to be presented is when a single phase fault is applied to the input terminals of the motor. The fault is applied after 1 second has passed in the simulation. The breakers, one for each phase, are opened at 1.1 seconds and then closed after 1.5 seconds. Only one illustration is provided in Figure 5.21 of the motor characteristics during the fault. The reason why there is a minimal number of graphics for this scenario is because nothing dramatically changes in the network worth reporting. In fact, HVDC systems are notorious for isolating and preventing fault effects from propagating into networks connected to the faulted network. For this case, the transformer is probably serving the role of isolating the fault in the region of the top induction motor, therefore creating no issues in other parts of the system.

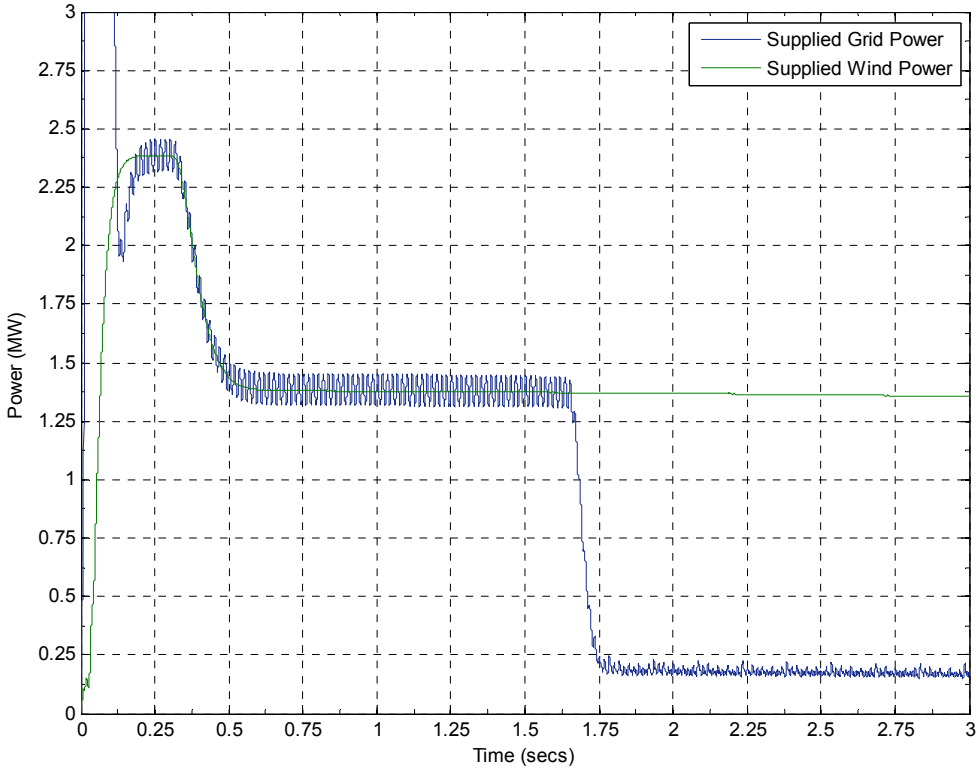



**Figure 5.16** Supplied Generation for Load Energizing Case

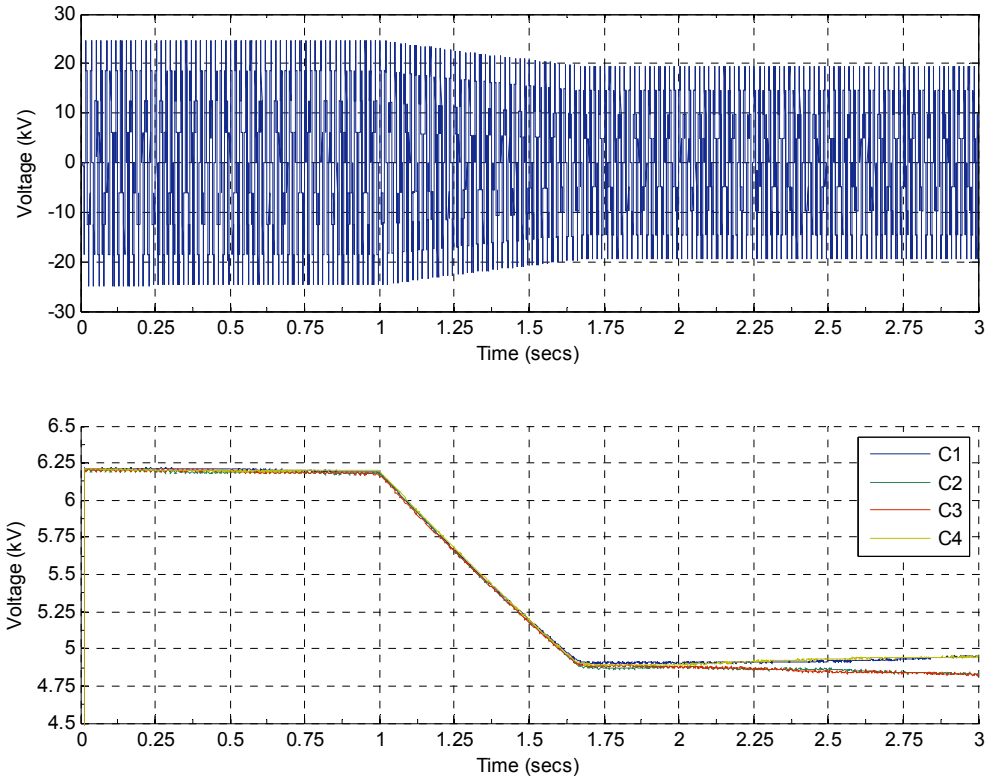



**Figure 5.17** Output Voltage and Capacitor Voltages of Five-Level, NPC Inverter for Load Energizing Case

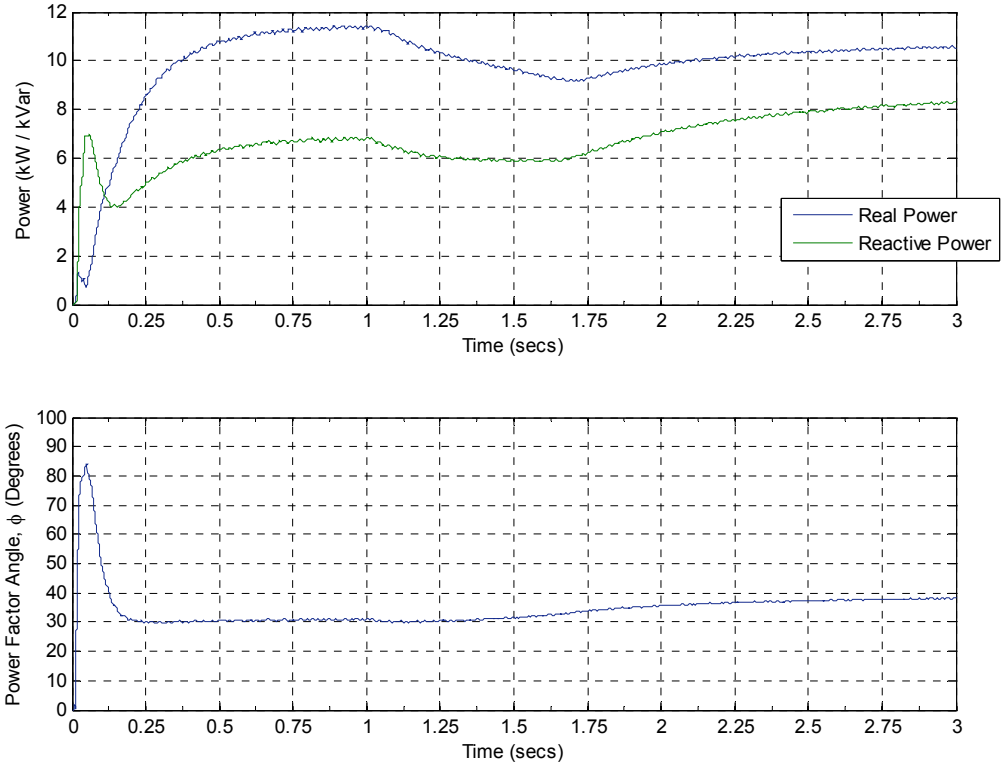



**Figure 5.18** Real and Reactive Power Absorbed by Top Motor for Load Energizing Case

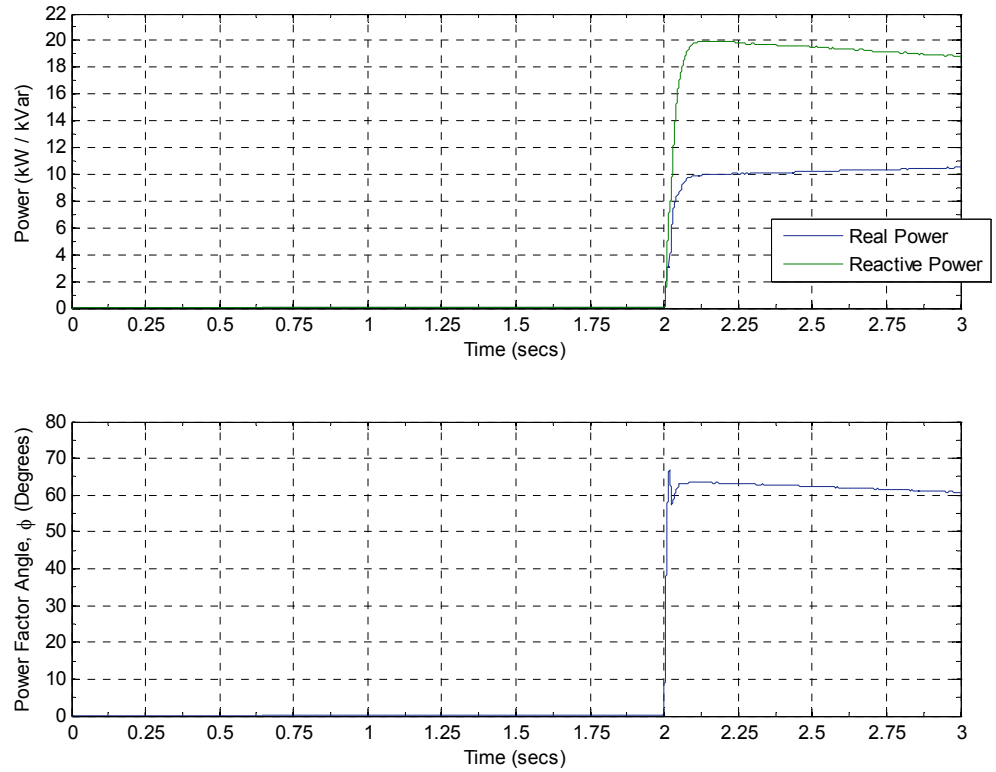



**Figure 5.19** Real and Reactive Power Aborbed by Bottom Motor for Load Energizing Case

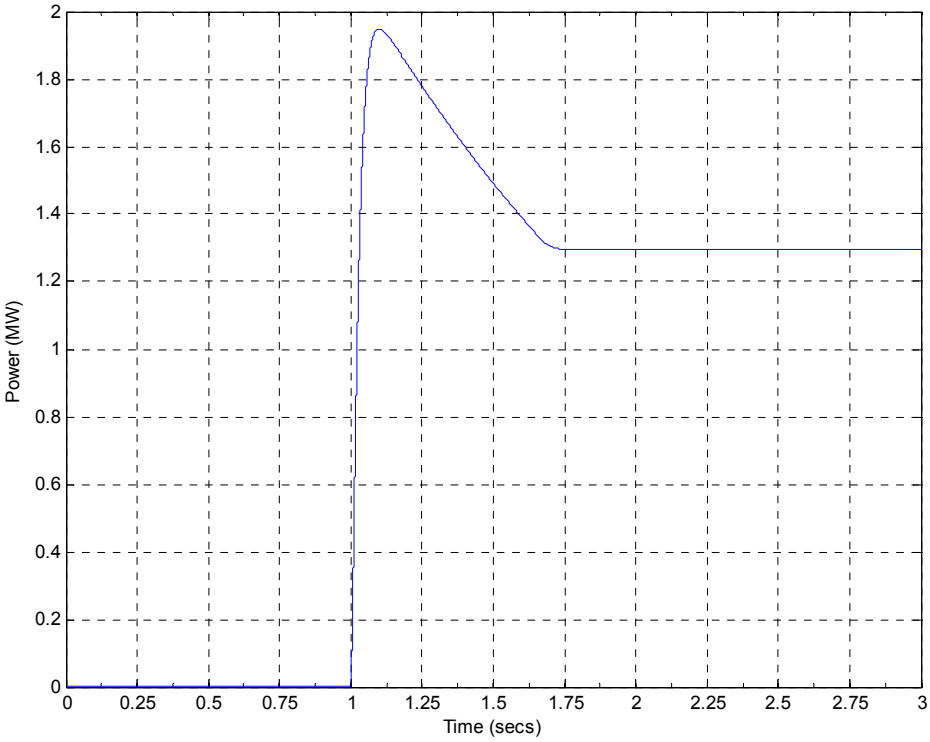



**Figure 5.20** Power Aborbed by DC/DC Converter Load for Load Energizing Case

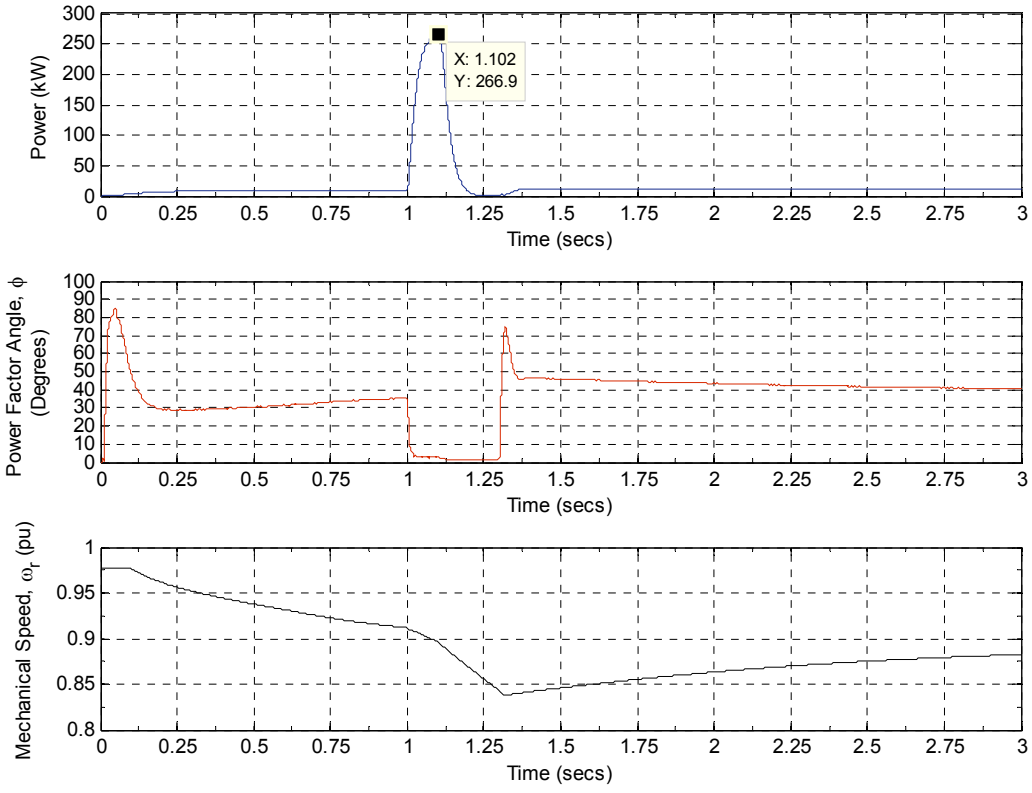



**Figure 5.21** Motor Characteristics of Concern for a Single Phase Fault on Input Terminals

# 6.0 CONCLUSIONS AND FUTURE WORK

The concept of a medium voltage DC (MVDC) network has been proposed, explained, and initially validated in the PSCAD simulation environment, an industry standard software package for modeling power system equipment. DC infrastructure development and expansion has been motivated by observing the transportation, information technology, and electronic sectors resulting in additional research needs. As the MVDC models continue to develop, predicted benefits of improved efficiencies and other concepts will begin to reveal themselves.

A literature survey of the state of the art power electronics converters and control including inverters, rectifiers, and choppers used for high power applications and renewable integration have been thoroughly investigated. The design of the various converter configurations including the Neutral-Point Clamped and Flying Capacitor, multilevel inverter topologies, dual active bridge DC-to-DC converter, and six pulse Graetz rectifier have been built in the PSCAD simulation environment. Various control techniques based upon pulse width modulation strategies including the Phase Disposition, Phase Opposition Disposition, and Alternate Phase Opposition Disposition were evaluated for the multilevel inverters with the total harmonic distortion being the chosen metric for comparison.

A 20 kV, medium voltage DC system composed of multiple generation resources including wind and equivalent voltage source representing the utility, power converters, two induction motors and one induction generator was assembled and evaluated using industry

standard analysis techniques such as fault-clear analysis and load energizing methods to help determine potential overvoltages and extreme power demands of all loads on the network. One scenario also evaluated the system performance due to sudden changes in wind speed. The outcome of this work provides a preliminary platform for future expansion of the network model that has been validated mathematically and through simulation.

A theoretical discussion was presented on the flying capacitor, multilevel topology but no simulation results have been provided. When the flying capacitor circuitry was implemented in PSCAD, the open circuit output voltage provided the expected number of levels. When the converter topology interfaced the induction motor to the medium voltage bus bar, the number of output levels was well below the expected target resulting in a highly distorted output voltage signal. The topology should not be completely abandoned because the topology might be load dependent and require separate pre-charge circuits for the capacitors, which will need evaluated in future design stages. The recommended inverter topology, under the study conditions presented interfacing the medium voltage bus with load, is the neutral point clamp inverter with the phase disposition switching strategy. The phase disposition technique resulted in a lower total harmonic distortion compared to the other switching algorithms.

Based on the discussion and results presented, future work in the MVDC development project are absolutely necessary and include the following:

- Built in feedback control structures should be implemented in the converters to control the power flow being delivered to the loads. The future application would be for consistent changes in load demand. This will also build intelligence into the network.

- Traditional generation sources composed of synchronous machines and renewable generation resources delivered from photovoltaic panels, wind turbines, fossil fuels, and storage will be interacting with each other on future grids and needs to be considered.
- Determining DC control metrics that monitor trends and changes in renewable generation supply. In AC systems, frequency and machine angular displacements are metrics for evaluating stability, as an example.
- Research initiatives in power converter technology to produce higher levels in the output voltage to minimize THD resulting in lower losses due to suppressed harmonics.
- MVDC layout and design is a critical issue that needs addressed. Will the footprint be larger or smaller compared to an existing AC infrastructure? Are the equipment costs more appealing or reduced enough to transition from AC to DC infrastructure?
- IEEE standards need initiated, developed and evaluated for DC application at the transmission and distribution level. Power converter harmonic standards and magnitudes are mentioned in [26] but determining if they are suitable for DC system operation is an area that needs an answer.

# APPENDIX A

## DERIVATION OF POWER TRANSFERRED USING A DUAL-ACTIVE BRIDGE CONVERTER [16]

### A.1.1 Instantaneous and Average Power Transferred in Dual-Active Bridge Converter

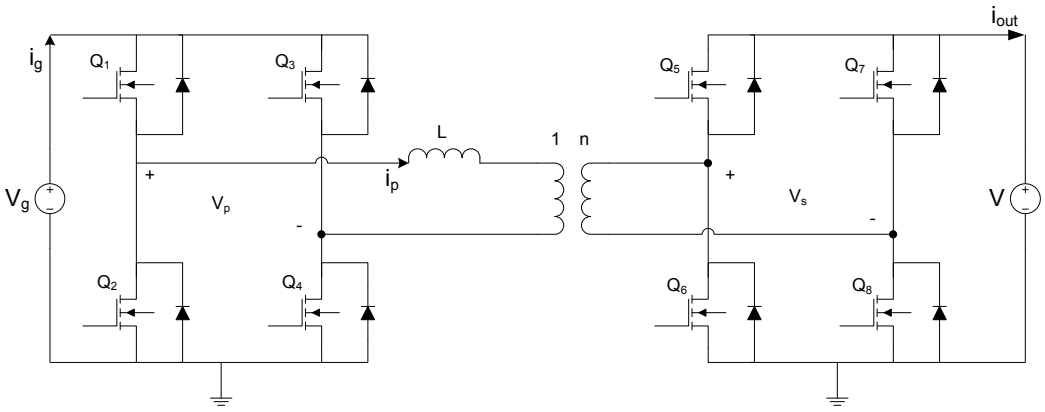



**Figure A. 1** Dual Active Bridge DC/DC Converter with Ideal Voltage Source Load

Figure A.1 has a slightly modified load compared to other models in this work. The equations derived would be suitable for a converter charging an ideal battery unit. The Fourier coefficients of a square wave are computed with (A.1), where $n$ is the harmonic and $A$ is the amplitude of the square wave.

$$a_n = 0$$
$$b_n = \frac{4n}{\pi} A \quad (Odd\ n\ Only) \tag{A.1}$$

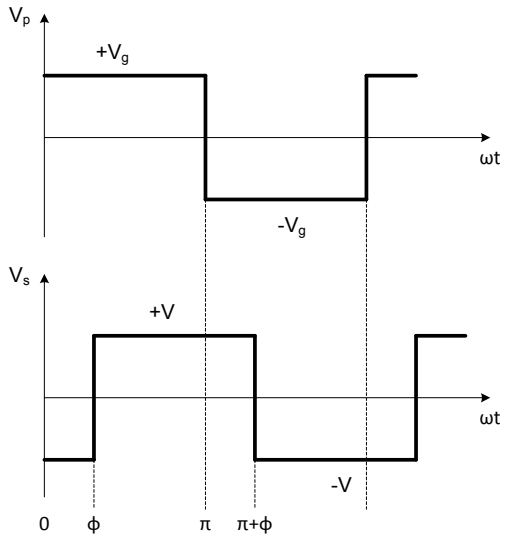



**Figure A. 2** Delays between the Primary and Secondary Voltages of the Transformer

The square waves found in Figure A.2 are approximated with the fundamental component allowing one to write the normalized primary and secondary voltages of the transformer as (A.2) and (A.3). Note that the base voltage selected is the input voltage, $V_g$.

$$V_p = \frac{4}{\pi}\sin(\omega t) \tag{A.2}$$

$$V_s = \frac{4M}{\pi}\sin(\omega t - \phi) \tag{A.3}$$

$$M = \frac{V/n}{V_g}$$

Assuming that the switches in the DC/DC converter are ideal, the converter reflects two voltage sources connected together through a reactance as shown in Figure A.3.

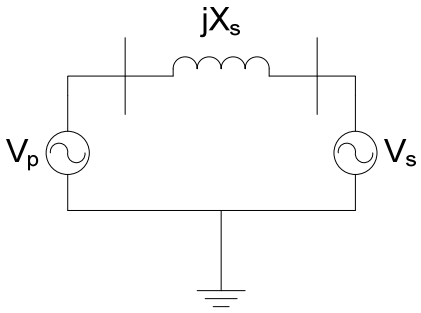



**Figure A. 3** Equivalent Circuit for Determining Power Flow in Bidirectional DC/DC Converter

Writing KVL around the circuit of Figure A.3, one obtains the current through the network given by (A.4).

$$I_{norm} = \frac{\frac{4}{\pi}\angle 0^0 - \frac{4M}{\pi}\angle -\phi}{jX_s} = \frac{4}{\pi X_s}\left[\sin(\omega t - 90^o) - M\sin(\omega t - \phi - 90^o)\right] \tag{A.4}$$

The instantaneous power and average power of Figure A.3 is given by (A.5) and (A.6), respectively.

$$P_{out,norm} = I_{norm}V_s = \frac{16M}{\pi^2 X_s}\left[-\cos(\omega t)\sin(\omega t - \phi) + \frac{M}{2}\sin 2(\omega t - \phi)\right] \tag{A.5}$$

$$\boxed{P_{out,norm} = \frac{1}{2\pi}\int_0^{2\pi}\frac{16M}{\pi^2 X_s}\left[-\cos(\omega t)\sin(\omega t - \phi) + \frac{M}{2}\sin 2(\omega t - \phi)\right]d(\omega t) = \frac{8M}{\pi^2 X_s}\sin\phi} \tag{A.6}$$

Note that when ϕ is greater than zero, the power flows from the primary side to the secondary side of the transformer. When ϕ is less than zero, the power flows from the secondary side to primary side of the transformer.

### A.1.2 Peak Current in Dual-Active Bridge Converter

Taking the derivative of (A.4) and setting this equation to zero will find the time at which the maximum peak current occurs in the current waveform. Without proof, it can be shown that the time at which this occurs is given by (A.7).

$$\omega_s t = \arctan\left(\frac{M\sin\phi}{M\cos\phi - 1}\right) \tag{A.7}$$

Substituting (A.7) into (A.4), one obtains (A.8).

$$I_{norm} = \frac{4}{\pi X_s}\left[-\cos(\arctan\left(\frac{M\sin\phi}{M\cos\phi-1}\right)) + M\cos(\arctan\left(\frac{M\sin\phi}{M\cos\phi-1}\right) - \phi)\right] \tag{A.8}$$

Each of the trigonometric expressions in (A.8) can be simplified. The first term of (A.8) can be simplified using the trigonometric identity listed as (A.9) with final result listed as (A.10).

$$\cos(\arctan(x)) = \frac{1}{\sqrt{1+x^2}} \tag{A.9}$$

$$-\cos(\arctan\left(\frac{M\sin\phi}{M\cos\phi-1}\right)) = -\sqrt{\frac{M^2\cos^2\phi - 2M\cos\phi + 1}{1 + M^2 - 2M\cos\phi}} \tag{A.10}$$

The second term of (A.8) can be simplified using the trigonometric identities listed as (A.11) with final result listed as (A.12).

$$\sin(\arctan(x)) = \frac{x}{\sqrt{1+x^2}}$$
$$\cos(\alpha - \phi) = \cos\alpha\cos\phi + \sin\alpha\sin\phi \tag{A.11}$$

$$\sqrt{\frac{M^2\cos^2\phi - 2M\cos\phi + 1}{1 + M^2 - 2M\cos\phi}}\left(M\cos\phi + \frac{M^2\sin^2\phi}{M\cos\phi - 1}\right) \tag{A.12}$$

Substituting (A.10) and (A.12) into (A.8), one obtains the normalized peak current listed as (A.13).

$$\boxed{I_{pk} = \frac{4}{\pi X_s}\sqrt{M^2 - 2M\cos\phi + 1}} \tag{A.13}$$

# APPENDIX B

## MATLAB CODES FOR COMPUTATION OF STEADY STATE PARAMETERS AND MAXIMUM TORQUE OF INDUCTION MACHINE

### B.1.1 MATLAB Code for Computing Steady-State Induction Machine Parameters

```
% Per Unit Parameters of 20Hp Induction Machine
r1=0.025;
r2=0.030;
x1=0.1;
x2=0.1;
xm=2.4;
rm=20;

% Pick Slip Value
s = 0.02309

%-------------------------------------------------------------------------
% Rated Input Voltage
V1=1

% Derivation used to Compute Rotor Current (I2)
Num = s*rm*j*xm;
Den =
(r1+j*x1)*(j*xm*(r2+j*x2*s)+rm*(r2+j*x2*s)+s*rm*j*xm)+j*xm*rm*(r2+j*x2*s);
I2 = V1*Num/Den;
AbsI2 = abs(I2)

%Does Electromagnetic Torque equal Load Torque?
Te=AbsI2^2*r2/s
TL=0.7*(1-s)^2

%Calculate Stator Current (I1)
Vout=V1*((r2+j*x2*s)*rm*j*xm)/Den;
I1=(V1-Vout)/(r1+j*x1);
AbsI1=abs(I1)

% Calculate Magnetization Current
Im=AbsI1-AbsI2;

% Calculate Im through Resistor
Im_Res=abs(Vout)/rm;

% Efficiency and Losses
nume = AbsI2^2*r2*(1-s)/s;
dene = AbsI2^2*r2/s+AbsI1^2*r1+Im_Res^2*rm;
eff=nume/dene
loss1_core=Im_Res^2*rm
loss2_stator=AbsI1^2*r1;
loss3_rotor=AbsI2^2*r2;
total_loss_rotor_stator=loss2_stator+loss3_rotor

% Rotor Speed
wr=1-s
```

```
% Steady-State Results
%--------------------------------------------------------------------------
% V1 =
%
%      1
%
% s =
%
%     0.0231
%
% AbsI2 =
%
%     0.7171
%
% Te =
%
%     0.6680
%
% TL =
%
%     0.6680
%
% AbsI1 =
%
%     0.8818
%
% eff =
%
%     0.8926
%
% loss1_core =
%
%     0.0437
%
% total_loss_rotor_stator =
%
%     0.0349
%
% wr =
%
%     0.9769
```

### B.1.2 MATLAB Code for Computing Maximum Output Torque of Induction Machine

```
% Per Unit Parameters for a 20HP Induction Machine
r1=0.025;
r2=0.090;
x1=0.1;
x2=0.1;
xm=2.4;
rm=20;
V1=1;
k=1;

% Iterative Loop for Determining Efficiency, Maximum Torque, and Slip
for s = -1: 0.001: 1
sj(k)=s;

% Calculate Rotor Current (I2)
Num = s*rm*j*xm;
Den =
(r1+j*x1)*(j*xm*(r2+j*x2*s)+rm*(r2+j*x2*s)+s*rm*j*xm)+j*xm*rm*(r2+j*x2*s);
I2 = V1*Num/Den;
AbsI2 = abs(I2);

%Calculate Stator Current (I1)
Vout=V1*((r2+j*x2*s)*rm*j*xm)/Den;
I1=(V1-Vout)/(r1+j*x1);
AbsI1=abs(I1);

% Calculate Total Im
Im=AbsI1-AbsI2;

% Calculate Im through Resistor
Im_Res=abs(Vout)/rm;

% Efficiency
nume = AbsI2^2*r2*(1-s)/s;
dene = AbsI2^2*r2/s+AbsI1^2*r1+Im_Res^2*rm;
eff(k)=nume/dene;
Te(k)=AbsI2^2*r2/s;
TL(k)=0.7*(1-s)^2;
wr(k)=(1-s);

k=k+1;

clear nume dene Im_Res Im AbsI1 I1 Vout AbsI2 I2 Num Den

end

data=[eff' Te' sj'];
x=max(eff);
[rows, cols]=find(data==x);
Results=data(29,:)
```

```
% Results (PU) for Efficiency, Torque, and Slip
%
%     0.8946    0.7962    0.0280
```

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