Numerical modelling of a high temperature power module technology with SiC devices for high density power electronics

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Abstract

This paper presents the development of a new packaging technology using silicon carbide (SiC) power devices. These devices will be used in the next power electronic converters. They will provide higher densities, switching frequencies and operating temperature than current Si technologies. Thus the new designed packaging has to take into account such new constraints. The presented work tries to demonstrate the importance of packaging designs for the performance and reliability of integrated SiC power modules. In order to increase the integrated density in power modules, packaging technologies consisting of two stacked substrates with power devices and copper bumps soldered between them were proposed into two configurations. Silver sintering technique is used as die-attach material solution. In order to assess the assembling process and robustness of these packaging designs, the thermo-mechanical behaviour is studied using FEM modelling. Finally, some recommendations are made in order to choose the suitable design for reliable power modules.

1. Introduction

The emergence of wide band gap semiconductors such as SiC enables power converters to operate at high switching frequency with better power conversion efficiencies and at temperatures beyond 200°C. The switching frequency defines primarily the size of passive components, such as inductors and transformers, used in converters for transient storage and filtering. A significant weight reduction can be expected. Moreover, the cooling requirements are much less stringent, and wide band gap semiconductors allow us to reduce the cooling system, leading to improvements in power density. This also contributes to the expected weight reduction.

To achieve the high density integration requirements for SiC power devices, classical aluminium wire bonding is replaced by copper bump interconnection in the superposition of two substrates in a sandwich. Firstly, bump interconnections have a larger diameter than the wire bonds and hence less parasitic inductance. They also offer the potential of lower resistance. The current capability is also increased. Secondly, they offer two thermal paths to dissipate the heat to the substrates. They play the role of thermal drain and stand-off elements between substrates for electrical isolation after gel filling [1]. This packaging solution improves the electrical and thermal characteristics, reduces the packaging size and present more power integration possibilities [2]. In order to realize reliable sandwich packaging, several high temperature solder alloys using low temperature processes are identified. Among these processes, there is the nano or micro-paste silver sintering technique. These processes could minimize the thermo-mechanical stresses and increase the reliability in high temperature operation [3]. In this work, the sintered silver is studied as solder joint to ensure the die-attach and also the bump interconnections. The process combines a low pressure to decrease the porosity ratio in the joint and a fixed temperature profile between 275°C and 325°C during 10 min. The temperature is chosen according to the metal powder.

The objectives of this paper are to assess the reliability of sandwich packaging technologies. Thus their thermo-mechanical behaviours were calculated and compared under thermal cycling between -40°C and +185°C. These results take into account the residual stresses induced by the sintering process at 275°C.

2. Assembly technologies

2.1. Sandwich packaging

The sandwich packaging consists in stacked substrates with semiconductor devices between them. The solder bump technique is used to realize the device top-side interconnections such as flip-chip BGA interconnects [4]. If the process is made by soldering, it usually requires three successive reflow phases and hence three different solder alloys with different melting temperatures. For the new high temperature power module, the successive reflow phases constitute an issue. For example, the range of available temperatures for the assembly process is much smaller, because the semiconductor devices have a maximum process temperature. This is of course directly linked with solder alloys allowed. To bypass the difficulty, the proposed packaging technology consists in using low temperature sintering instead of soldering, with silver paste. This assembly process is applied to minimize the thermal stresses induced by a multi-reflow process. However, particular designs are required to ensure large contact areas so as to achieve reliable assemblies, and to reduce the thermo-mechanical stresses concentration in the bump interconnections during the assembling process.

2.2. Silver sintering process

Low temperature sintering technique is an approach for high temperature lead-free solders. This technique uses silver paste as die-attach and bump solder. It can be achieved by three ways. The first way consists in using a silver micro-paste which is heated at 250°C with an applied hydrostatic pressure from 20 MPa to 40 MPa to increase the joint density [5]. The second way consists in using silver particles of a nano-scale. In such solution [6], the additional organic components such as solvent were selected so as to eliminate the applied pressure. In this case, silver nano-paste can be heated at 275°C to 325°C under standard atmospheric pressure and thus the density of sintered silver can reach 80% of bulk silver. Figure 1 shows the nano-silver sintering profile on gold (Au) and silver (Ag) metallization which is used in this study.

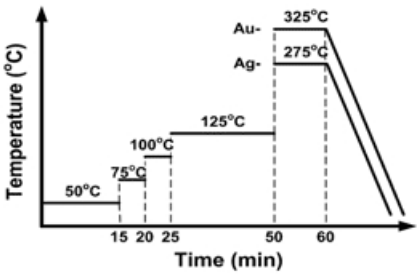


Fig. 1. Nano-paste silver sintering profile on Au and Ag final metal on devices [7]

The advantage of this technique is that once the silver nano-paste is sintered, it will have a high melting point such as bulk silver (961°C). Therefore this technique allows successive sintering operations. Consequently, the issue of using several eutectic solder alloys is removed. Another sintering technique has been newly developed by Heraeus and uses a silver micro-paste especially created for small die area less than 50 mm^2. In such case no pressure is required and the sintering process is simplified. It could be in a single step.

3. Numerical design and modelling

3.1. Packaging designs

Assembly configurations

The assembly configuration selection is defined based on the assembly technology review literature. They allow higher integration levels and double-side cooling to improve the thermal management. The copper bump may vary in shape and size as illustrated in figure 2.

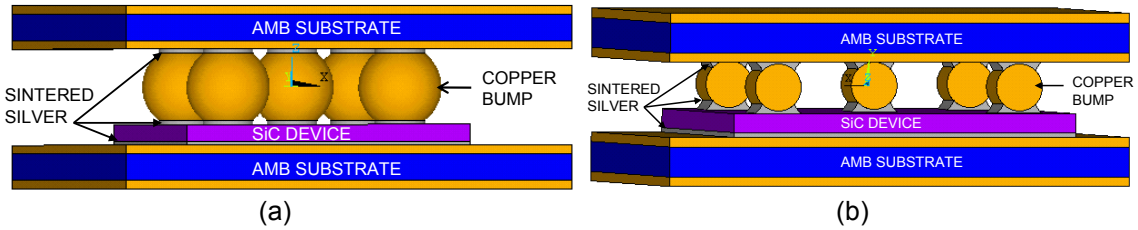


Fig. 2. Elementary packaging designs for finite element models : Spherical copper bump (a) and cylindrical copper bump (b)

The geometries of elementary packaging structures are based on standard thicknesses used also in automotive and railway power modules. The power SiC devices are 4×4×0.4 mm^3, ceramic substrates are 6×6×0.64 mm^3, the metallization is 200 µm height, the considered solder joints thickness is100 µm, truncated spherical bump is *diameter* 2 mm × *height* 1.5 mm and cylindrical bump is *diameter* 1 mm × *length* 1 mm.

Materials, thermal and mechanical parameters

The materials used in these packaging studies are SiC for power devices, silicon nitride (Si_3N_4) for ceramic substrates with copper (Cu) as metallization and silver as sintered joint.

The thermal and mechanical properties of these materials were extracted from literature regarding their thermal conductivity, coefficient of thermal expansion, Young's modulus, Poisson's ratio …etc [8, 9], as presented in table below.

Properties	Cu	SiC	Si_3N_4	Sintered Ag [9]
λ ($W.K^{-1}.m^{-1}$)	398	130	60	416
ρ ($kg.m^{-3}$)	8850	3210	3290	10^4
α ($10^{-6}.K^{-1}$)	17.3	4.8	3.3	19.6
C ($J.kg^{-1}.°C^{-1}$)	380	800	800	230
E (GPa)	128	460	310	See table below
ν	0.36	0.18	0.27	0.37
Yield Stress (MPa)	98.7	610	-	-

Temperature (°C)	-40	0	25	60	120	150
E (GPa)	9.01	7.96	6.28	4.52	2.64	1.58

3.2. Finite element modelling

Materials constitutive law and parameters

The model of the sintered silver joint is simulated with Anand's unified visco-plastic constitutive model [9]. Equations (1), (2) and (3) give the formulation of Anand's model [10]. It models the inelastic deformation behaviour of the silver joint used as die-attach and solder bump interconnection.

$$\dot{\varepsilon} = \mathrm{A}\exp\left(\frac{-Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \text{ (1)},\ s^* = \hat{s}\left[\frac{\varepsilon}{\mathrm{A}}e^{\frac{Q}{RT}}\right]^n \text{ (2)},\ h = \left|h_0\left(1-\frac{s}{s^*}\right)^a .sign\left(1-\frac{s}{s^*}\right)\right| \text{(3)}$$

Where

$\dot{\varepsilon}$ is the inelastic strain rate, ε is the inelastic strain, Q is the activation energy, A is the pre-exponential factor, ξ is the multiplier of stress, m is the strain rate sensitivity, R is the gas constant, s is the coefficient of deformation resistance, σ is the equivalent stress and T is the absolute temperature. The quantity s^* represents a saturation value of s. $\hat{s}$ is a coefficient for the saturation value of deformation resistance. h is a strain hardening function.

To complete the nine parameters of Anand's visco-plastic model (see table below) [9], there are: the initial value of deformation resistance s_0, the hardening constant h_0, the strain rate sensitivity of saturation value n and the strain rate sensitivity of hardening a. These parameters were identified between -40°C and 185°C.

s_0 (MPa)	Q (J.mol^{-1})	A (s^{-1})	ξ	m	h_0 (MPa)	$\hat{s}$ (MPa)	n	a
2.768	47442	9.81	11	0.6572	15800	67.389	0.00326	1

They have been assigned through the input for VISCO107 element in ANSYS™ software for the simulation.

Thermal cycling load

The packaging process and endurance are assessed using finite element method for two bump configurations as shown in figure 3. In order to evaluate the robustness of these packaging designs, their thermo-mechanical behaviour is studied under 3 thermal cycling loads as shown in figure 3, taking into account the validity temperature range of previous Anand's parameters. The profile begins at 25°C initial temperature, the ramp rate is 10°C/min and the dwell times are 15 min at -40°C and 185°C.

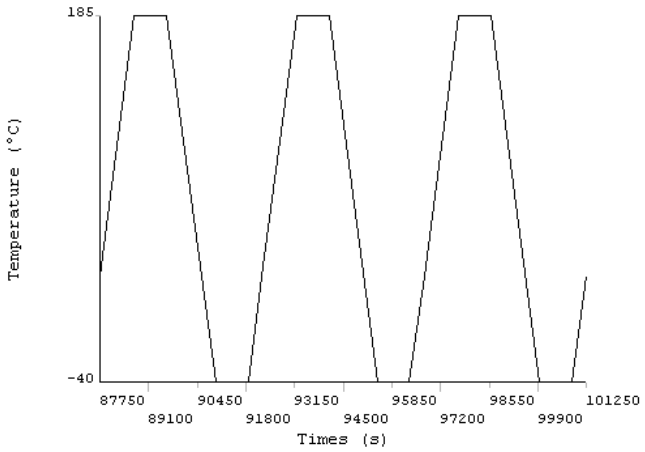
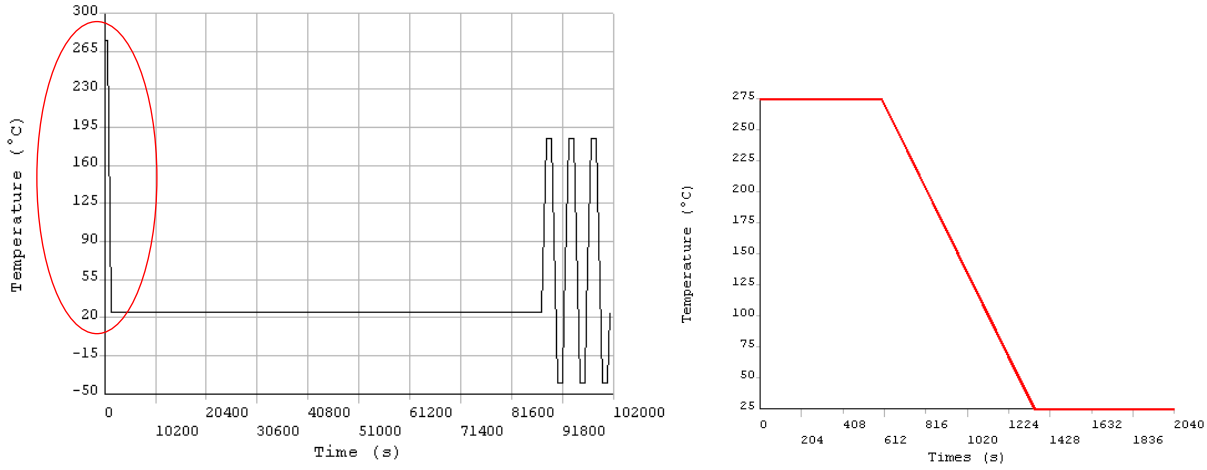


Fig. 3. Thermal cycling profiles: -40°C, +185°C

Assembling process coupled with thermal cycling load

The simulation takes into account the residual stresses induced by the assembling process. In this paper only the last step of the silver sintering process is also simulated as shown in figure 4(b). That means a dwell time of 10 min at 275°C and a ramp rate of 20°C/min before starting the 3 thermal cycles described in figure 3. Thus a stress relaxation is applied after the sintering process during 24 hours at 25°C. After what, the thermal cycling load between -40°C and 185°C is conducted (figure 4(a)).

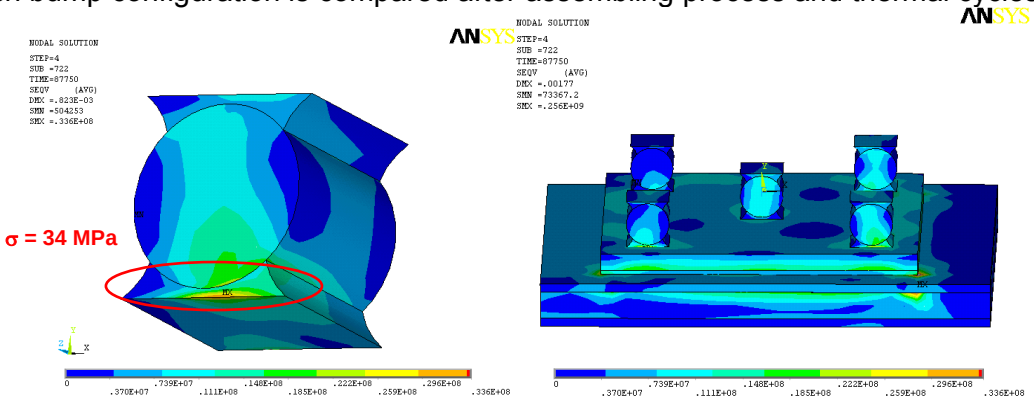


(a) (b)

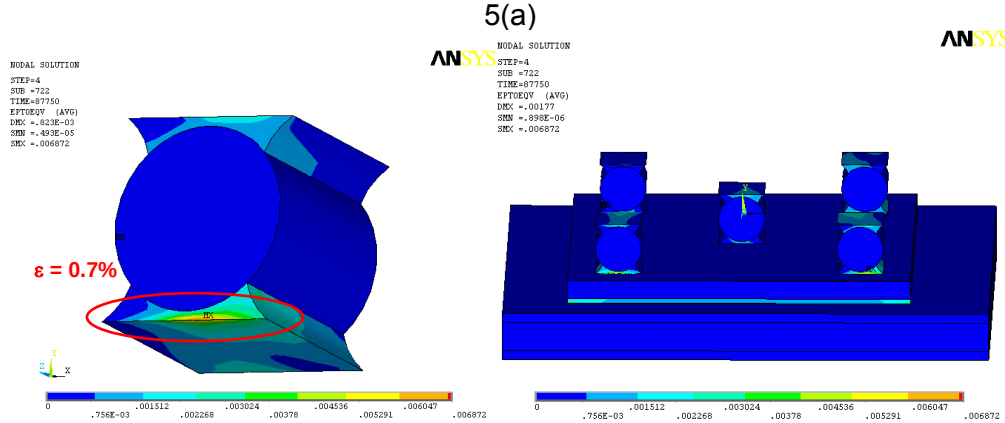
Fig. 4. Thermo-mechanical stress profile applied for simulation (a), zoom on assembling profile (b)

3.3. Simulation results

The stress distribution and the total mechanical strain are plotted after the assembling process and also at the end of the thermal cycling load. Thus the thermo-mechanical behaviour of each bump configuration is compared after assembling process and thermal cycles.



5(a)



5(b)

Fig. 5. Stress distribution [Pa] 5(a) and mechanical strain 5(b) in cylindrical bump after assembling process

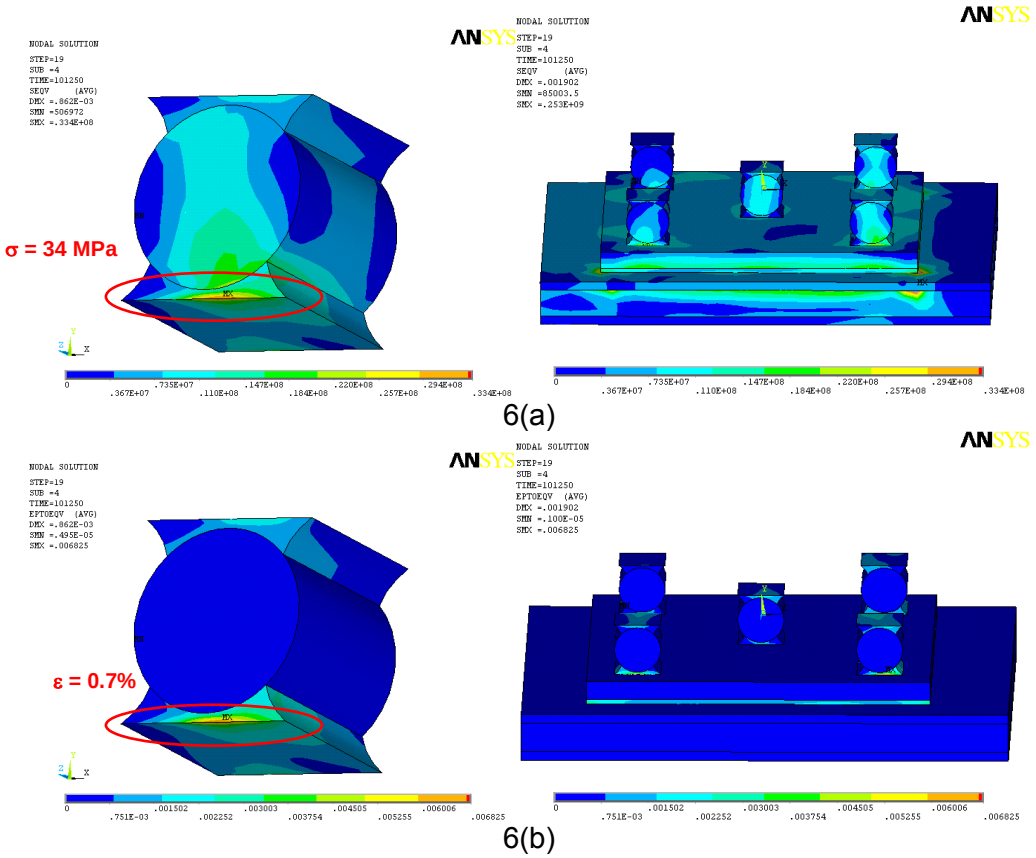


Fig. 6. Stress distribution [Pa] 6(a) and mechanical strain 6(b) in cylindrical bump at the end of 3 thermal cycles

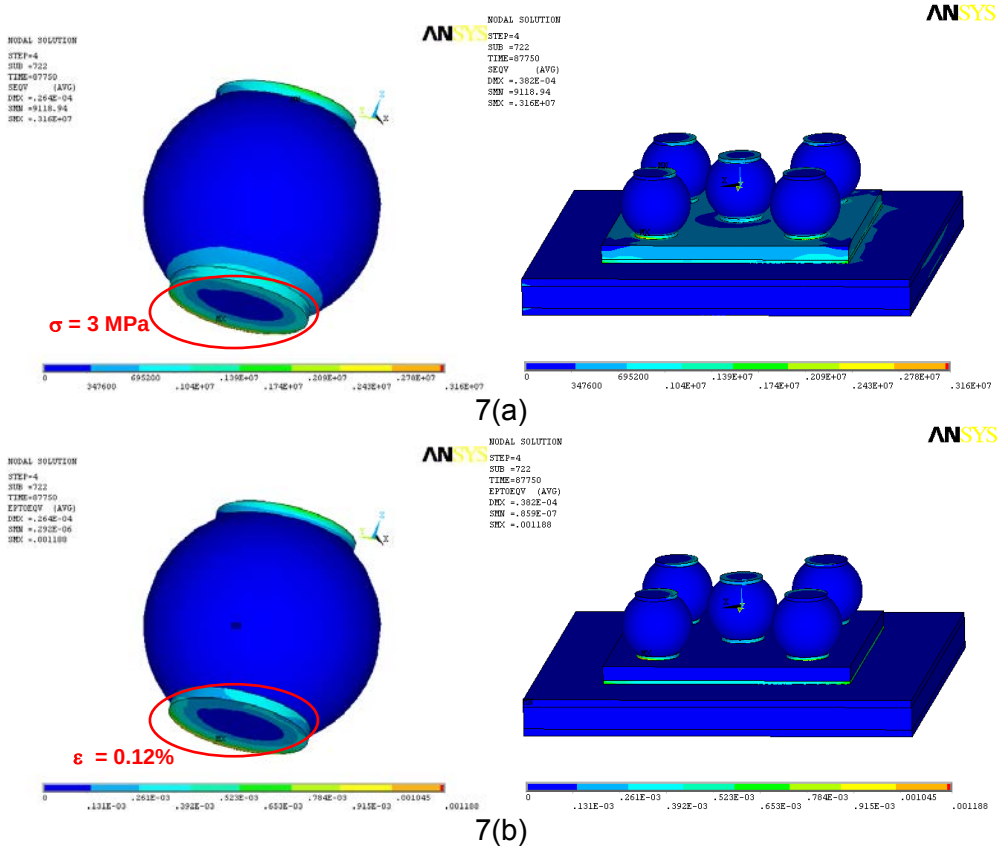


Fig. 7. Stress distribution [Pa] 7(a) and mechanical strain 7(b) in spherical bump after assembling process

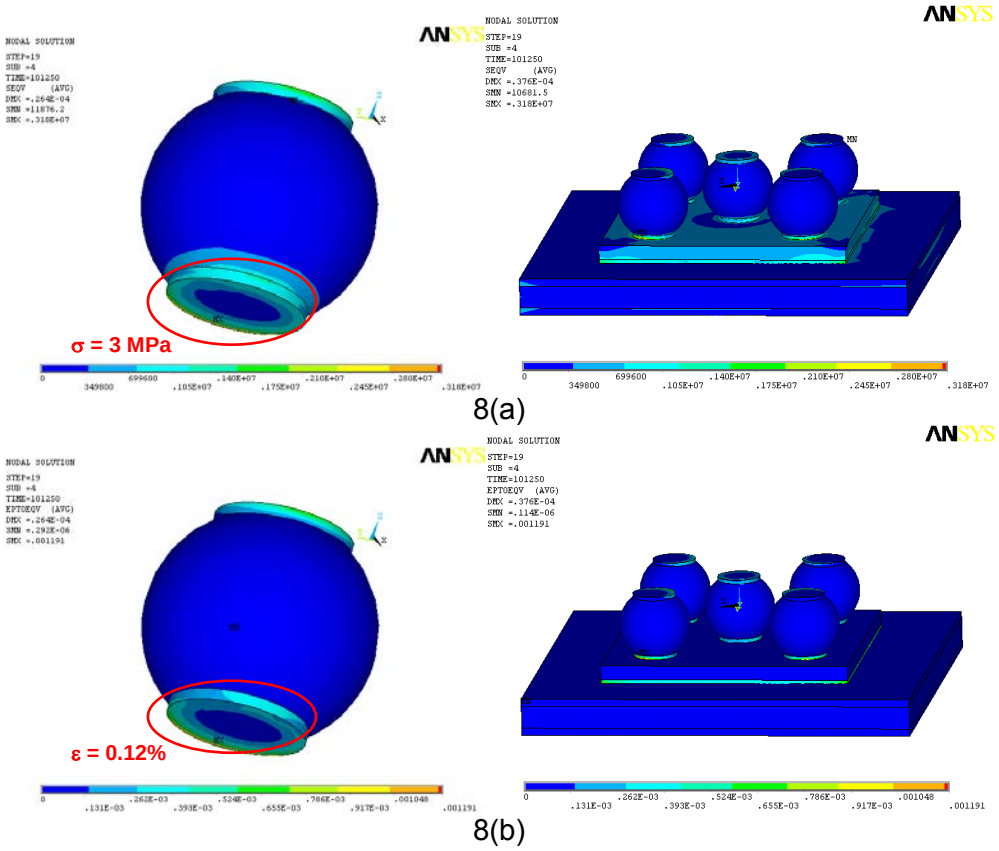


Fig. 8. Stress distribution [Pa] 8(a) and mechanical strain 8(b) in spherical bump at the end of 3 thermal cycles

3.4. Influence of Solder bump geometry on packaging behaviour

The simulation results show that the maximal strains are located in the silver sintered joints. Thus, the bump joint interface seems to be the more critical zone in the packaging. However, it can be noted that the spherical bump joint presents less strain level than a cylindrical one (ε=0.12% against ε=0.7%) after the assembling process, as shown on figures 5(b) and 7(b). At the end of thermal cycling loads, these values remain stable at respectively 0.12% and 0.7% (figures 6(b) and 8(b)).

Concerning the stress distribution, the cylindrical bump joint presents a maximal stress of about 34 MPa after the sintering process and also 34 MPa at the end of thermal loads (figures 5(a) and 6(a)). While the spherical bump joint presents a maximal stress of 3 MPa (figures 7(a) and 8(a)). These results show that the maximal stress distribution in the spherical configuration were more than 10 time lower than the cylindrical one. The results also confirm the evolution of the total mechanical strain during the thermal cycling loads. For each bump design, the stress-strain evolution is similar during the thermal-mechanical constraints.

The bump designs with large contact areas appear to be suitable for sandwich packaging using silver sintered as solder joint solution (figure 2(a)).

4. Conclusion

The objective of this study was to evaluate new packaging technologies for high temperature and high power density SiC devices. In this study, these technologies were simulated with new developed materials and assembling process. The influence of die-attach and solder bump configurations were studied in order to meet the power applications requirements.

In order to increase the power density, a technology consisting of two stacked substrates with power devices soldered between them, was proposed with good perspectives. The de-

velopment of the new silver sintering techniques allows us to remove the use of several solder alloys.

Hence, to assess reliable sandwich packaging, FEM modelling and simulation were conducted on two packaging configurations to evaluate and compare the thermo-mechanical behaviours. These calculations take into account the residual stresses induced by the assembling process.

It could be noted that the solder bump design plays a fundamental role in the packaging assembly and reliability. Then, the results point-out the use of truncated spherical solder bump as the better solution.

5. Literature

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