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Thermo-mechanical stress of bonded wires used in high power modules with Alternating and Direct Current modes

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Abstract

Today, power electronic reliability is a main subject of interest for many companies and laboratories. The main process leading to the IGBT failure is the cycling thermal stress. Indeed the current flow induce local heating and then mechanical stress. This paper deals with electro thermal stress under steady and transient current states. The main objective is to test bonded wires with active current cycle. Consequently, the thermo mechanical stress is obtained. A numerical 3D finite element model is presented and some experimental results are given. Indeed an infrared system monitors the temperature dispatching from an experimental test bench under active current cycle. The overall study is a first step before a global simulation (electrical thermal- mechanical) in order to optimize some geometric parameters of the packaging.

Keywords: Power electronic reliability, Wire bonding, Electro thermo mechanical simulation, Experimental device

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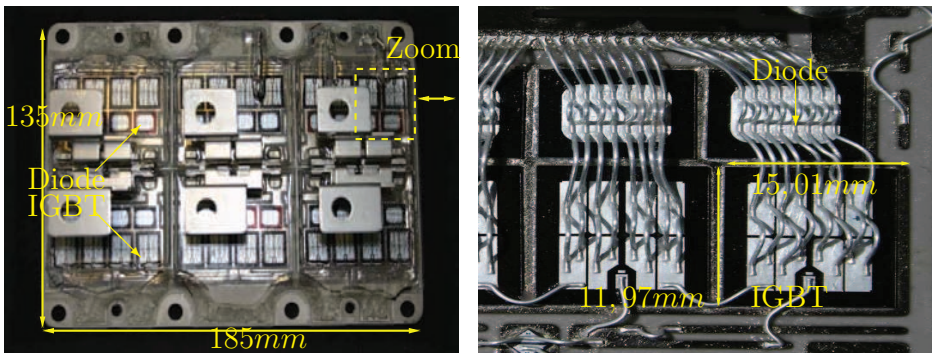
1. List of symbols

IGBT	Insulated Gate Bipolar Transistor
3D	3 Dimensions
1D	1 Dimension
FEM	Finite Element Model
CTE	Coefficient of Thermal Expansion
AC	Alternating Current
DC	Direct Current

2. Introduction

In railway applications, the power electronics components allow transferring the electrical energy between the electrical source and the electrical machine. They are used to convert the energy from alternating signals to continuous signals (or the opposite). Since many years the goal of some studies is to obtain a more integrated static converter. That is to say to have more power into less volume. Due to these stringent stresses, the power electronic lifetime has become an important field of study. In such studies, authors try to combine each aspects of the stresses experienced by the power modules.

In the field of the power electronics, the reliability of inverter architecture used in high voltage application such as railway applications is often studied. Indeed because it is mainly constituted of Insulated Gate Bipolar Transistor (IGBT). One main contributor to IGBT failure is related to wire bonds. Indeed the fatigue results is caused either by the shear stresses between the bond pad and the silicon device or by repetitive wire flexure. It is reported that the failure mainly occurs in the area where the wire is bonded with the metalization pad. The fatigue caused by thermo-mechanical stresses is a consequence of the current flow. Indeed it leads to thermal cycles that produce two different failure modes for the wire : the bond wire lift off and the heel crack mechanism, [1]. In order to study the packaged semiconductor material many sort of research has been done. Some consider simulation aspects, others experimental results. On one hand, simulations concern both 3D FEM and 1D time dependent models. Nowadays the trend is to merge the both level of simulation as started in [2], [3], [4]. On the other hand,



(a) Full module (b) Single IGBT zoom view

Figure 1: Open IGBT module - 1500A - 3300V

experimental probing mainly concerns solder alloys and mechanical shear or pull tests. For the wire bonding itself, most experimental studies emphasize the process influence on the wire bonding lifetime before failure [5], or the thermal fatigue effect as developed in [6]. Finally, others try to combine simulation and experimental results to obtain the lifetime or to improve the wire connecting layout [7].

In this paper we apply a current flow to isolated wires. Then we monitor both simulation and experimental temperature dispatching. Consequently we obtain the mechanical stress revealing specific failure modes. By this study we reveal the thermo-mechanical stresses due to the current flow in steady and transient current state. We compare both simulation and experimental results in each current mode. The main contributions of this paper are first to combine simulation and experimental investigations, then to apply a real current flow instead of an average power cycle, and finally to provide 3D numerical results. The current induces a thermal cycle conducting to mechanical stress of the bond wire. The IGBT module used for our application is a triphase 1500A 3300 V, built with 24 elementary IGBTs and their own freewheeling diodes as illustrated in Fig. 1.

3. IGBT failure modes

3.1. Overview of the main failure modes

Under normal operating conditions, power electronic modules are exposed to stringent stresses. The thermo-mechanical fatigue finally induced failure

mechanisms. The failure modes are obtained after the occurrence of electrical, thermal and mechanical phenomenon interactions. The study scope is the thermal cycling fatigue of IGBT power modules. This power cycling is known to be the main contributor of failure modes related to the IGBT module packaging. In this way, the mismatch in the Coefficient of Thermal Expansion (CTE), and the various temperature gradients within material layers are responsible of the stresses experienced by the packaging. It is noticed that the thermal cycle is obtained after exerting the real density current flux in the multilayer IGBT module. Consequently, some failure modes have been observed on the bonded wires or on the interconnection elements. Others are linked with the metalization layer, whereas some crack propagation can be found inside the ceramic layer or in the silicon chip. The solder alloy join can also be damaged. The occurrence consequence of the mentioned failure modes is IGBT device burnout or latch up.

3.2. Bond wire failure modes

Within our study scope, for power devices used in railway application, the bond wires are built with pure Aluminum hardened with some alloys in order to prevent corrosion. They are 100 - 500 μm in diameter and are connected by ultrasonic bonding. The wires that we are going to consider are bonded onto the IGBT metalization. These wires are a weak part of such an IGBT module. The two main failure modes observed are the wire bond lift off and the heel crack mechanism [1]. It is the region of the initial crack that mainly leads to one mode. Indeed the wire lift off is linked with fracture mechanic initialized within the wire tail itself [8]. During the thermal cycle, the CTE mismatch between Aluminum and Silicon induces the crack propagation that finally ends with the bond wire entirely lift-off. Some numerical studies were done to determine such strength applied onto the wire. Nowadays it is reported some process to reduce bonded wire lift off. For example, thanks to a coating layer, the wire is glue to the metalization. Another failure mode is the occurrence of crack propagation, amplified by power cycles, at the wire heel. The heel crack propagation can lead to partial wire disconnection. Thereby the electrical conductivity is not completely achieved. Effectively, when a bond wire experienced thermal cycles, the wire dilatation induces a flexure. One can find that 50 $°C$ temperature swing can produce 10 μm increase of length and then 0.05° additive angle face to the bonded region [9] (because the wire is bonded on a metalization layer). Some authors use

analytical laws that express the number of cycles to failure as a function of the plastic strain [10].

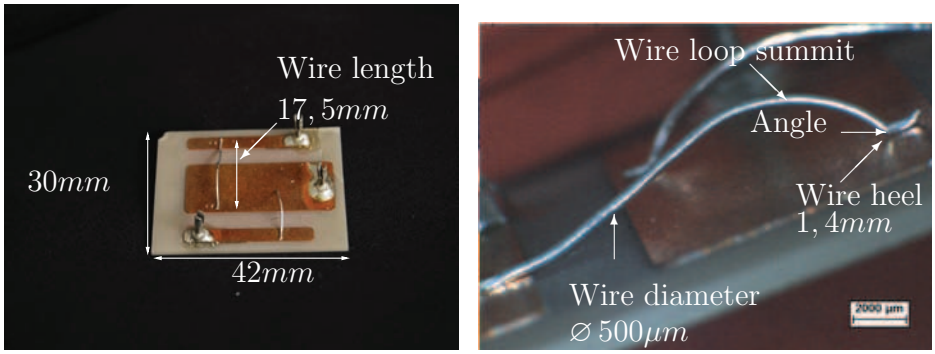
4. Experimental setup and numerical model

4.1. Experimental setup

We decided to best emphasize the main reasons on what can lead to already known failure modes of the wire bonding. More precisely, we want to reproduce the succession stress experienced by wires to point out if the same failure regions are concerned by Alternating Current (AC) or Direct Current (DC) profiles. Effectively, the high power module users engaged in PRIMES laboratory [11], experienced different wire behaviours, related to the current mode applied (DC or AC). Consequently, we design an experimental setup constituted by one (or two) isolated wire(s), bonded onto copper baseplate, Fig. 2(b). The specific region where many failure modes occur, the heel, and the angle made between the wire loop and the baseplate are pointed out. The process used is based on specific and adapted tools, under controlled atmosphere. Indeed, before connecting the wires, the substrate is cleaned thanks a plasma cleaner (O_2 followed by Ar under low pressure cycle). The wires, (Aluminium 99.99%), are 500 μm in diameter and are connected by ultrasonic bonding. The final heel shape is due to the force applied during the wire welding, which achieves a compromise between good bonding properties and prevents silicon device crack. The difficulty of measuring such experimental heat dispatching is the bonded wire thickness. Then we use an infrared camera FLIR SC 7000, which has a sensitivity of about 20 mK. A power source followed by a specific electronic card provides the direct or alternating current in bonded wires. In the case of two parallel wires we will be able to check in further studies the coupled electromagnetic effects with AC.

4.2. Numerical model

Because we are interested in bonded wire parametric optimization, we design a numerical model as close as possible of the experimental device, Fig. 3. The different properties used for each material are listed in Table 1. The finite element analyse is provided by ABAQUS, [12].



(a) Experimental setup (b) Zoom on the wire loops

Figure 2: Isolated bonded wires

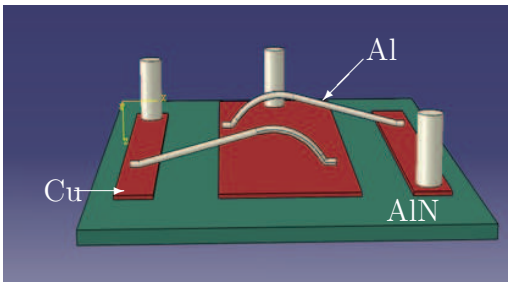


Figure 3: 3D numerical model

Properties	Al	Cu	AlN
Thermal conductivity λ $(W/m/K)$	237	401	180
Electrical conductivity σ (S/m)	$3.69 * 10^7$	$5.96 * 10^7$	10^{-14}
Volume density ρ (kg/m^3)	2700	8900	3260
Specific heat C_p $(J/kg/K)$	897	380	740
Young's modulus E (MPa)	$6.6 * 10^4$	$11 * 10^4$	$31 * 10^4$
Poisson's ratio υ	0.35	0.343	0.24
CTE α (@23 $°C$)	$2.3 * 10^{-5}$	$3 * 10^{-5}$	$4.5 * 10^{-6}$

Table 1: Material properties

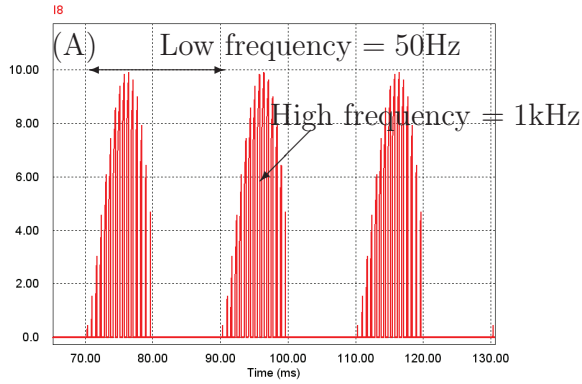


Figure 4: Alternating current profile experienced by a single bonded wire

4.3. Current flow sources

4.3.1. Direct current

The direct current applied ($I = 10\ A$) is obtained from IGBT specification related to the number of wires and from the value commonly used by authors. For example, in the case of the high power module under consideration, Fig. 1, the real current obtained is close to this value. It is computed from the maximal current value ($I_{IGBT_{max}}$) switched by the IGBT module, and divided by the number of IGBT (N_{IGBT}) and the number of power wires (N_{wires}):

$$I = \frac{I_{IGBT_{max}}}{N_{IGBT} * N_{wires}} = \frac{1500}{24 * 8} = 7.8A$$

$10A$ corresponds to a current density of $5,09 * 10^3\ A/cm^2$ flowing within the wire. It is lowest than the maximal density current value reported which is 30 to 35 A/cm^2.

4.3.2. Alternating current

Thanks to PSIM software, [13], we simulated a triphase inverter in 50 Hz steady current state, connected to resistive and inductive triphase load. We extract the current profile experienced by the bond wire, after Pulse Width Modulation strategy applied to the different IGBT gates. Then we obtained a positive period computed with a switched frequency of $1k\ Hz$ as illustrated on Fig. 4.

5. Simulation and experimental results

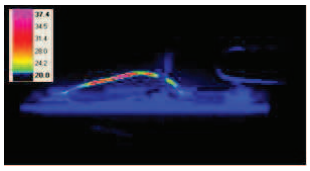
5.1. Direct Current stress

5.1.1. Thermal stress induced

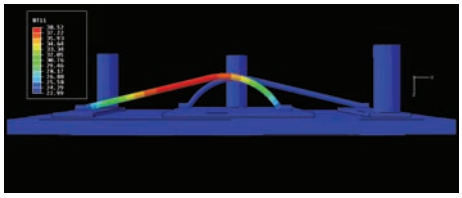
The Fig. 5(a) and 5(b) illustrate the simulation and experimental results. The temperature dispatching is due, on one hand, to the natural convection around the wire itself, and for another part to the ceramic layer situated below the wire. This good thermal conductive material plays the role of thermal cooling system. One can noticed that the maximum temperature (38 $°C$) is obtained in the middle of the bond wire. In Fig. 5(c) we compare the experimental and the simulation temperature dispatching along the wire. This result shows that we are able to take into account the thermal aspects as the far as the convection and conduction aspects are concerned. Indeed, natural convection (and his coefficient) is applied around the wire and initial temperature values are fixed. This temperature swing is also encountered by the bonded wires when they are connected to IGBT or diodes for instance. We applied this direct current to a combined diode - bonded wire prototype and we also obtain a maximal temperature on the wire itself (the temperature swing is $\Delta T = Max(T_{wire}) - Max(T_{diode}) = 33\ °C$). We can conclude that our simplified model is adapted. Added to this, when the chip will be submerged in a silicon coat (with small thermal conductive property) the heat will be more concentrated around the wire. The next section will develop what can be the mechanical stress experienced by the wire due to temperature swing.

5.1.2. Von-Mises mechanical stress

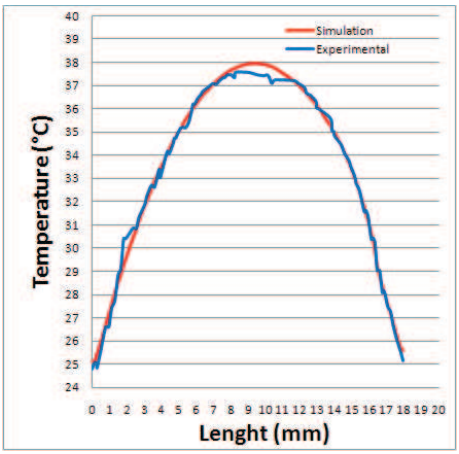
We prove the accuracy of our numerical simplified model. Indeed, the temperature dispatching experienced by the wires, leads to maximal principal stress distribution, Fig. 5(e). It is noted that the maximal value (10 MPa) is located at the tail of the wire, just in front of the heel area. This is an additional proof of why main failure modes occur close to this specific region [14]. It is noticed that the wire is considered to be bonded onto the metalization layer without residual stress. Previous works based on this geometry have shown the link between the wire bond angle and the maximal stress observed [15]. To summarize them, the table 2 shows the computed Von-Mises stress when the DC magnitude vary combined to different bonded wire angles. We can conclude that the DC magnitude and the wire angle have a huge influence with the mechanical stress. NR means non relevant,



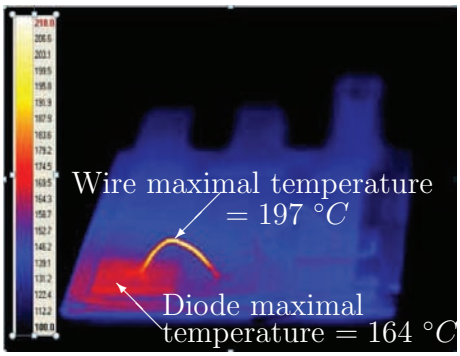
(a) Experimental temperature dispatching



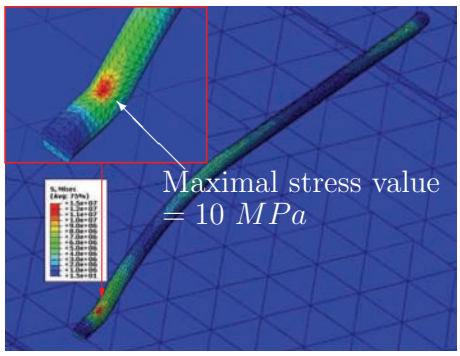
(b) Numerical temperature dispatching



(c) Comparison between simulation and experimental results



(d) Diode and single bonded wire with direct current



(e) Von-Mises stress

Figure 5: Direct Current simulation and experimental results

DC magnitude (A)	Angle (°)			
	20	40	60	80
5	2.1	2.9	2.75	3.8
10	8.3	11.5	10.9	15.7
15	18.8	26	24	NR

Table 2: Von-Mises stress (MPa) with bonded wire angle and DC magnitude swing

that is to say the value obtained is too important face to the yield strength of the aluminium used in bonded wire.

5.2. Alternating Current stress

In order to test the bond wires with real stresses, we defined an experimental setup. Consequently, the device built is able to apply the real current experienced by the bond wire. The AC profile applied is given by the simulation as illustrated in Fig. 4. It is also introduced in ABAQUS, in order to obtain the thermal heating in transient state.

5.2.1. Thermal stress induced

The temperature evolution for a middle point of the bonded wire is given in Fig.6(a). Due to the difference between the electric and temperature time constant the bond wire self-heating during AC operation increases step by step. We can clearly see the influence of the conduction terms (when the current is applied) and the influence of the specific heat capacity term (when the current is switched to 0 A). The maximal temperature value is lowest than for DC mode due to the difference between the direct current value applied and the root mean square value of the alternating current. Unless the time constants, we reveal the same behaviour between numerical model and the experimental setup. Moreover the AC applied to a combined diode - bonded wire prototype, reveals an identical behaviour, Fig. 6(b). The temperature swing experienced by the wire after 200 s cycle of AC (as shown in Fig.4), is 2.7 $°C$.

5.2.2. Von-Mises mechanical stress

The temperature dispatching and evolution during AC operation allows obtaining the maximal principal stress distribution within the bond wire. As already shown the maximal stress is induced at the heel of the bond wire. But at the opposite of what occurs with DC profile, we can conclude that

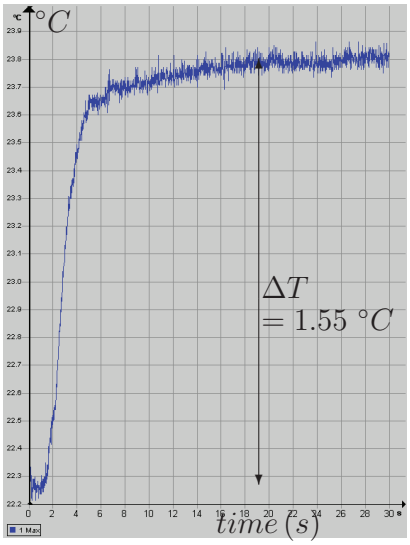
during AC operation the wire is not really stressed. Indeed the maximal value is 1 MPa, Fig. 6(c).

5.3. Discussion

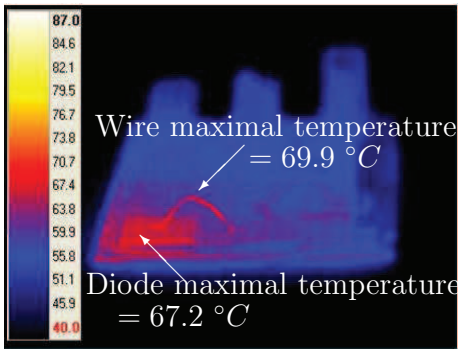
We consider a simplified model (the single wire without the chip) in order to obtain thermo mechanical numerical solutions during direct and alternating current modes. This allows us to use 3D FEM software to monitor Von-Mises stress induced by thermal dispatching, and connected to transient and steady current inputs. We first checked that the results obtained from our simplified model could be related to more realistic device. Then we can use the simplified numerical model to study a parametric or variable optimization. For instance we give some results about the influence of the direct current magnitude and the angle value. But others can be further explored, such as the optimized surface between interconnection elements and chip devices. We noted that some studies [16] [17] still use DC to stress the bonded wires or the whole packaged chip. But our study reveals that an AC do not produce exactly the same temperature dispatching and values as DC. In the future we will use this to define new stress profile. We imagine to link the current root mean square to an optimized power cycle. Indeed, we will test the high power modules with much more realistic stress.

6. Conclusions

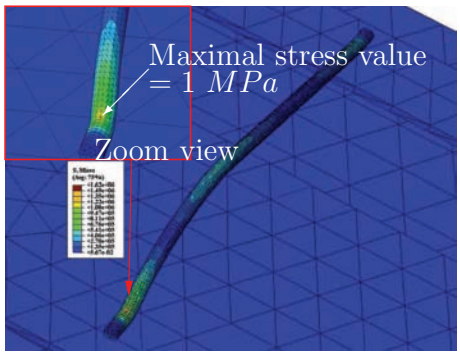
The main objective of our study is to best characterize the maximal stress experienced by bonded wires during Direct Current and Alternating Current operation modes. We realized a precise simulation which is compared to an experimental setup. The good temperature behaviour is checked between both. Thanks to the numerical study we can produce the maximal stress distribution by using the Von-Mises yield criterion. The temperature dispatching is induced after DC and AC flow within the wires. In our study the thermal cycle experienced by the bonded wire is due to the current flowing within the wire itself. It helps us to best understand the wire behaviour in such operating mode. Finally, thanks to numerical and experimental result comparison, it is noted that the maximal mechanical stress is obtained at the heel of the bond wire which is exactly where the main bond wire failure modes occur.



(a) Measured temperature swing with AC state



(b) Temperature dispatching of diode and single bonded wire with AC



(c) Von Mises stress under AC state

Figure 6: Alternating Current simulation and experimental results

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