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Radiation Effects on CMOS Image Sensors With Sub-2 μm Pinned Photodiodes

S. Place, J.-P. Carrere, S. Allegret, P. Magnan, V. Goiffon, and F. Roy

Abstract—CMOS image sensor hardness under irradiation is a key parameter for application fields such as space or medical. In this paper, four commercial sensors featuring different technological characteristics (pitch, isolation or buried oxide) have been irradiated with ^{60}Co source. Based on dark current and temporal noise analysis, we develop and propose a phenomenological model to explain pixel performance degradation.

Index Terms—Activation energy, APS, CMOS 4T image sensor, dark current, irradiation, pinned photodiode, temporal noise.

I. INTRODUCTION

THE recent evolution of mobile phone market has established CMOS Image Sensors (CIS) as the new standard for such imaging applications. These devices actually do offer the best scaling capability for pixels. Recent achievements close to micron sizes allow getting low-cost image sensors up to 10 Mega-pixels (Mpix). In order to maintain the signal-to-noise ratio while scaling the pixel size, specific care was taken to minimize noise sources. One of the most efficient ways is to use a 4T CMOS pinned photodiode pixel [1]–[4].

The use of these commercial image sensors extends in some harsh environments applications, especially for the medical, scientific or spatial imaging domains [5]. This involves new requirements, including that the CIS should become radiation tolerant. Several studies have already been dedicated to the ionizing dose induced degradation in 3T CMOS pixel ([6]–[9]), but very few are related to commercial 4T CMOS pixels with pinned photodiodes [10]–[12].

In this paper we report on the degradation induced by ^{60}Co gamma rays on some small-pitch 4T CMOS image sensors, down to 1.4 μm pixel pitch. The impact of different technological features such as Trench Isolation (TI), buried oxide (BOX) and multiple doped lateral interfaces is investigated. The pixel degradation will be first characterized by measuring the pixel dark current degradation with Total Ionizing Dose (TID). The

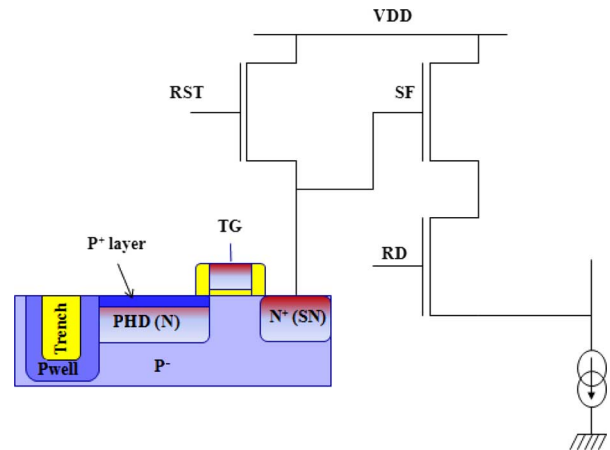


Fig. 1. Schematic representation of 4T CMOS pixel.

evolution of the dark current activation energy will also be shown to complete the discussion about the pixel degradation scheme. Finally, the pixel temporal noise evolution with TID will also be presented and discussed, assuming that the pixel dark current and the temporal noise are the major contributors of the pixel noise floor.

II. EXPERIMENTAL DETAILS

Most of the CMOS image sensors are on the so-called Active Pixel Sensor (APS) organization [13]. This means that an in-pixel charge to voltage conversion is used and associated to buffering performed by an embedded transistor called Source Follower (SF). The readout is selectively done all along the matrix with a line access transistor, the Readout transistor (RD). The sensors used in this study are 4T CMOS pixel which means that four transistors are embedded as shown in Fig. 1.

The specificity of this pixel architecture resides in the photodiode itself. It is called a pinned photodiode, which consists of a shallow buried N-type photodiode pinched by two opposite doping layers represented in Fig. 1. The Sense Node (SN) is reset at the beginning of the transfer period by activating the Reset transistor (RST), which charges the sense node to a potential of VDD. Charges integrated in the frame period are then transferred from the pinned photodiode to the sense node by activating the Transfer Gate (TG) transistor.

The four studied image sensors are based on 4T pinned photodiodes pixels manufactured in 90 nm ST microelectronics CIS processes with different isolation trenches (Shallow and deep trenches [14]), pixel pitches and buried oxide (BOX), as summarized in Table I.

The sensors have been exposed to ^{60}Co gamma rays source at the Université Catholique de Louvain (UCL). The dose rate

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TABLE I
PIXEL MAIN FEATURES

Sensor	Pixel pitch (μm)	Active area (μm^2)	Perimeter (μm)	Isolation structures	Gate oxide thickness
175STI	1.75	1.18	3.7	Shallow trench	65 Å
175DTI	1.75	1.26	5	Deep trench	50 Å
140DTI	1.4	0.55	4.15	Deep trench	50 Å
140DBOX	1.4	0.55	4.15	Deep trench + BOX	50 Å

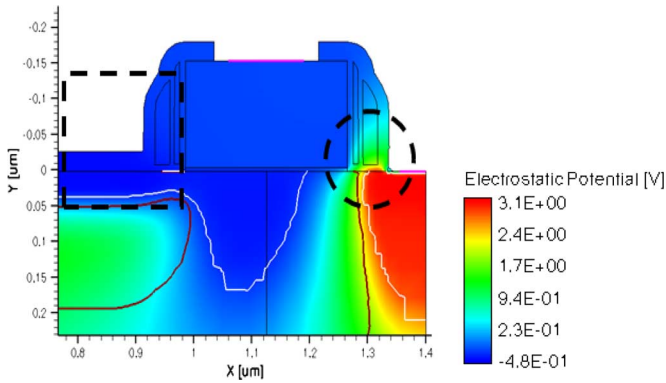


Fig. 2. Electrostatic potential mapping around pinned photodiode and transfer gate in accumulation regime.

used was 1 krad(SiO_2)/h. Each sensor was exposed without any electrical bias and at room temperature to five different TID: 3, 10, 30, 100 and 300 krad(SiO_2). Indeed, under biased irradiations, pinning layer confines potential lines at ground value ($V_{\text{sub}} = 0 \text{ V}$). As a result, insulators around pinned photodiodes are areas of weak electric field, as shown in the square on electrical TCAD simulation of Fig. 2. Values of significant fields usually encountered in degradations of MOSFETs approach the MV/cm^{-1} values. In our architecture, they are only located in the vicinity of TG as circled on Fig. 2. Dielectrics targeted are next to the SN. They are related to surrounding spacers made of silicon dioxide and nitride stacks. Fractional yield mentioned in [15] is a little more significant in these zones. However, these areas are not taking part to dark current integration in the photodiode.

Dark current mean values and histograms were evaluated on 3 Mpix arrays to a temperature of 60°C , when not specified. Note that at highest doses (30, 100 and 300 krad(SiO_2)), huge dark current values required to adjust smaller integration times to avoid dark current non linearity and distorting these measurements.

These technologies, sketched in Fig. 3, are motivated by different demands of CMOS imaging industry. The transition from STI to DTI [14] is needed to minimize electrical crosstalk which becomes more important as pixel pitch decreases. The research of enhanced QE performances lead the imaging companies to move towards backside illuminated (BSI) technologies. The integration of a buried oxide into the pixel could be one of the multiple process possibilities to achieve BSI technologies [16].

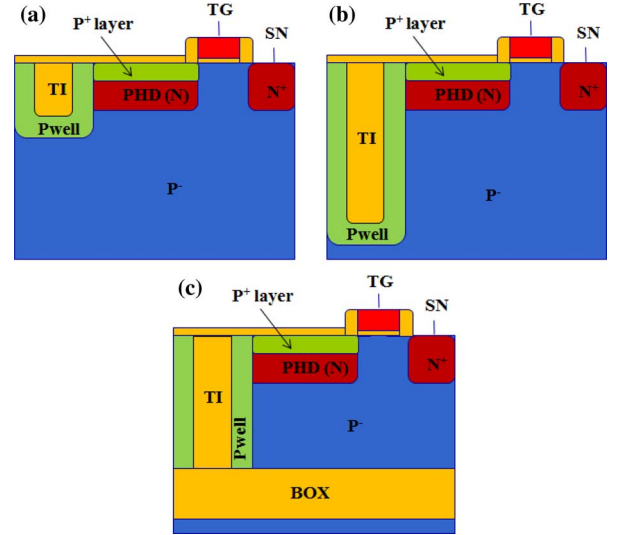


Fig. 3. Cross-sections of sensors 175STI (a), 140DTI and 175DTI (b) and 140DBOX (c).

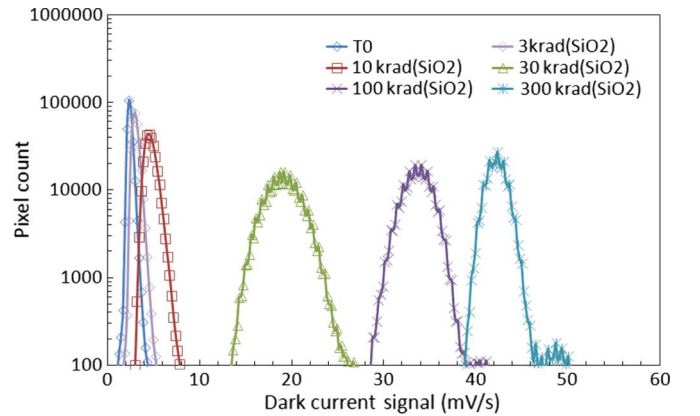


Fig. 4. Dark current signal histogram with TID for sensor 175STI.

The particular integration of sensor 140DBOX provides insight on technological issues in using BOX for BSI.

III. DARK CURRENT OBSERVATIONS

A. Degradation on Dark Current Histograms With TID

To assess the stages of endured degradation, dark current histogram evolution of sensor 175STI with ^{60}Co gamma rays dose is shown in Fig. 4.

Dark current evolution includes two phases. The curves below 30 krad(SiO_2) show slight degradation. Dark current value at the peak of the distribution slowly increases while its standard deviation rapidly increases. During the second phase (30–300 krad(SiO_2)), larger degradations are observed; peak at 30 krad(SiO_2) increases much stronger. Then, the trend alleviates for the last two doses while the standard deviation decreases all along with TID. A comparable study is made on sensor embedding deeper trenches with sensor 175DTI in Fig. 5.

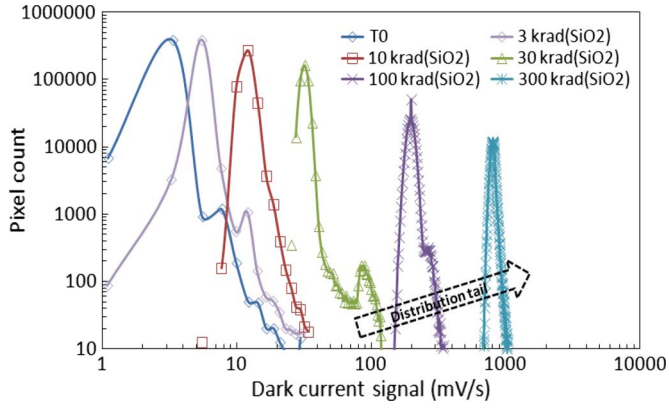


Fig. 5. Dark current signal histogram with TID for sensor 175DTI.

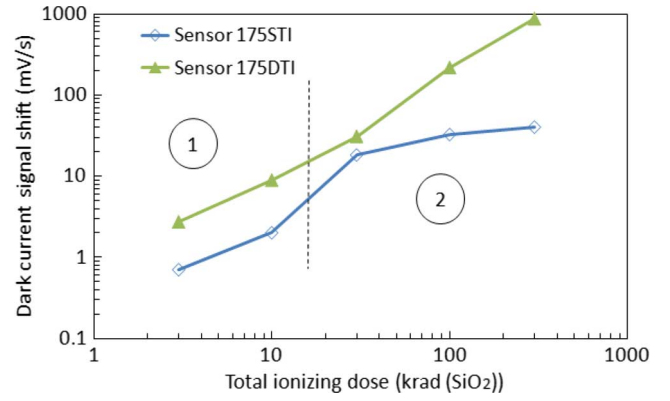


Fig. 7. Evolution of dark current signal shift with total ionizing dose between sensors 175STI and 175DTI.

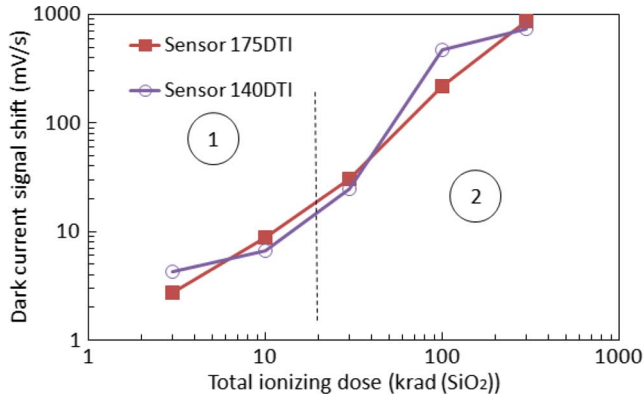


Fig. 6. Evolution of dark current signal shift with total ionizing dose on sensors 175DTI and 140DTI.

This plot shows moderate increase of dark current value at the peak up to 30 krad(SiO₂). Beyond, more important variations are observed. The standard deviation keeps increasing slowly until 30 krad(SiO₂) and faster afterwards. A secondary distribution is seen at 30 krad(SiO₂) which seems to turn into a rising distribution tail.

B. Pixel Area and Perimeter Impact

After the presentations of dark current signal histograms, a description of mean value gives a better visibility on overall radiation effects. An evaluation of the impact of pixel geometry can be performed with two different pixel pitches (sensors 175DTI and 140DTI) on a technology sharing same deep trench isolations.

Fig. 6 reveals insignificant variations with active pinned photodiode area on dark current signal shift. Since the perimeter is the same, nothing can be concluded about the perimeter contribution. However, it should be emphasized that if the perimeter was the dominant source, the observed result would be the same as what is seen in Fig. 6.

C. Technological Impact of Pixels Isolation

A second comparison is introduced in this part to confirm the impact of isolation trenches and perimeter in the pixel. Main differences between sensors 175STI and 175DTI, described in Table I, are related to trench isolation depths. The dark current degradations for both sensors with TID are plotted in Fig. 7.

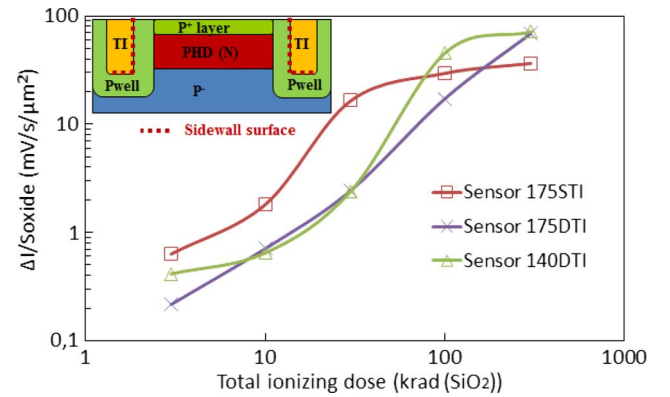


Fig. 8. Normalized contributions of dark current for the first three sensors.

At first, two different behaviors regimes are marked by a dotted line. On the area (1), at low doses (< 10 krad(SiO₂)), dark current variations exhibit the same slopes. On the area (2), beyond 10 krad(SiO₂), the variations are radically different. Indeed, shallow trench causes saturation phenomenon for the highest range of doses, whereas deep trench isolation displays a linear dark current signal shift increase on log-log scale. It suggests that trench depth have a significant influence on dark current degradation. To evaluate the impact of each isolation trench, normalization of dark current for each sensor is proposed with their respective sidewall Si/SiO₂ interface areas on Fig. 8.

When TID increases up to 30 krad(SiO₂), the contribution of deep trench is weaker compared to shallow trench. However, saturation levels presented beyond 30 krad(SiO₂) are relatively similar for sensors 175STI and 140DTI which confirms the assumption based on trench isolation degradation. A proposition of mechanism will be discussed in part IV to explain saturation phenomena observed.

D. Buried Oxide Impact

The evaluation of buried oxide impact under irradiation is evaluated with a comparison between sensors 140DTI and 140DBOX after ⁶⁰Co irradiations. Results are presented on Fig. 9.

Dark current evolution of sensor 140DBOX departs from the sensor 140DTI mainly at low doses. This can be associated to the addition of a buried oxide in sensor 140DBOX. At low

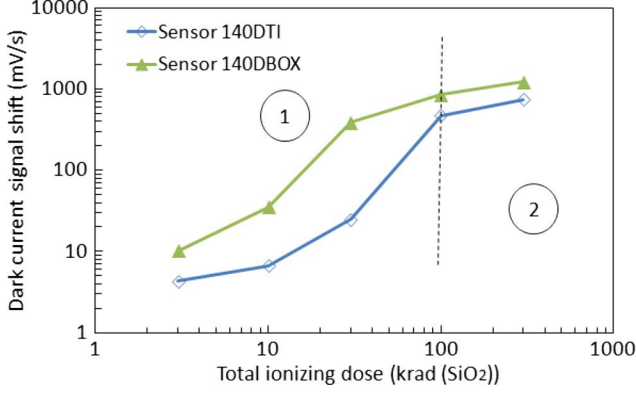


Fig. 9. Evolution of dark current signal shift with total ionizing dose for sensors 140DTI and 140DBOX.

TABLE II
SUMMARY OF DARK CURRENT IMPROVEMENT WITH PWELL DOPING BEFORE IRRADIATION

Sensor	Normalized dark current value
175STI (low doping)	1
175STI (standard)	0.68

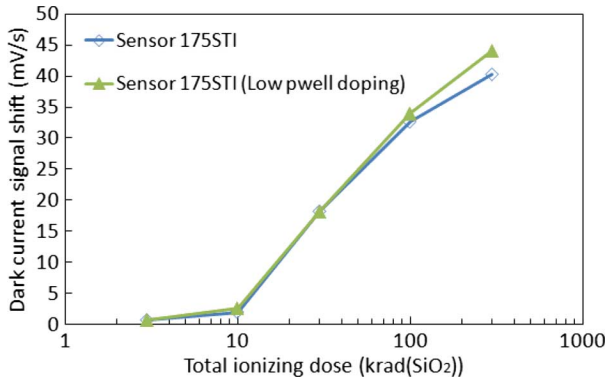


Fig. 10. Evolution of dark current signal shift with total ionizing dose for two differently doped isolation trenches on sensor 175STI.

doses, degradation is increasing faster with a buried oxide and tends to saturate in the same trend than sensor 140DTI. A proposition on physical mechanisms depending on bottom interface area is suggested in part VI.

E. Impact of Interface Doping Level

Increasing pwell doping along shallow trench isolation provides good results to lower dark current before radiation as summarized in Table II.

It is proposed here to study the impact of doping level required to improve radiation tolerance of trenches. Fig. 10 reports the behavior of two types of $1.75 \mu\text{m}$ pixel process related to the same sensor design (175STI) but with different pwell doping surrounding shallow trenches. Pixels with higher doping

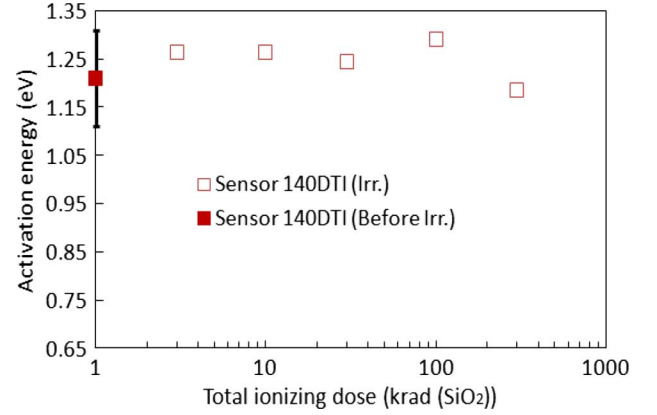


Fig. 11. Description of dark current activation energy with TID for sensor 140DTI before (Before Irr.) and after irradiation (Irr.).

on trench interfaces show a not significant dark current reduction on the range of TID observed. The results suggest that radiation hardness on sensors embedding STI cannot be modified with proposed doping levels.

IV. DISCUSSION

Dark current degradation on studied sensors is shown to depend on pixel perimeter, trench isolation depth, and the presence of a buried oxide layer. This would mean that the total area of Si/SiO₂ interfaces surrounding the photodiode mainly drives the degradation with TID. This matches well with the current understanding in radiation effects of semi-conductor devices, where the major part of damages occurs into the dielectric layers around the silicon [17]. The first parasitic effect consists in the apparition of fixed positive charges in dielectrics, due to generations of electron-hole pairs into these layers. Next, the Si/SiO₂ interface states density tends also to increase due to some holes or radiolytic hydrogen diffusion towards the interface [17].

A. Considerations on Activation Energies

To discriminate these two effects, activation energies of dark current has been measured in the range of temperature between 25 and 60°C for sensor 140DTI, as shown in Fig. 11.

Thermal signature of dark current remain relatively unchanged, around 1.25 eV, for any TID used in the range 3 to 300 krad(SiO₂). As well, this signature was extracted from each sensor. This activation energy is induced when the diffusion of minority carriers drives the dark current, which is typical on pinned photodiode architectures [18]. Values above bandgap energy can be explained by the definition of intrinsic carrier density (1), including the temperature dependence of pre-exponential term.

$$n_i = A \cdot T^{\frac{3}{2}} \cdot e^{-\frac{q \cdot E_g}{2kT}} \quad (1)$$

As diffusion current is dependent of n_i^2 term, the observed value takes into account the additional contribution of T^3 term responsible of differences with bandgap value (1.12 eV). On the contrary, activation energy around 0.65 eV (near mid-gap value) can be observed if mechanism of thermal generation dominates.

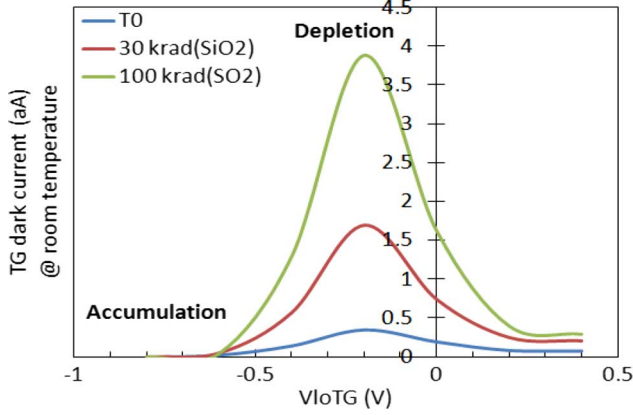


Fig. 12. Dark current evolution of TG at room temperature with irradiation and TG voltage for sensor 175STI.

This occurs when an interface area is depleted [19]. It shows at the same time a difference compared to mid-gap value (0.56 eV), also explained by the influence of pre-exponential term. As a consequence, this result means that whatever TID induced degradation, positive charge density in dielectrics remains low enough not to deplete one of the interfaces close to the photodiode. Finally, a mechanism of interface trap buildup [20] is assumed with total ionizing doses. Increasing interface state density induces an enhanced diffusion current which involves dark current evolution.

B. Electrostatic Effects of TG

During standard dark current measurement, the transfer gate contribution is assumed to be negligible compared to other contributions (perimeter and surface) because it is always biased in accumulation [21]. But this transistor can also be considered as a tool of monitoring of interface states degradation on gate oxide. A brief representation of mean dark current originated from transfer gate with TID and TG voltage is plotted in Fig. 12 at room temperature. This contribution was extracted from total dark current minus value read in accumulation. This final data represents the activity of TG.

Grove showed in [19] that the contribution at the peak on Gated Diode and, at the same time, on TG represents depletion state and is modeled by:

$$I_{genTG} = q \cdot s_0 \cdot n_i \cdot A_{dep} \quad (2)$$

With the generation velocity $s_0 = \sigma_S \cdot v_{th} \cdot N_{it}$, σ_S the mean capture cross section, v_{th} the thermal velocity, n_i the intrinsic carrier density, N_{it} the interface state density and A_{dep} the depleted interface area. From this equation, ratio of I_{genTG} extracted before and after irradiation provides us a piece of information about interface state density evolution on a fraction of TG gate oxide. The normalized values of N_{it} with dark current signal shift degradation are represented on Fig. 13 for sensor 140DTI.

Evaluation of interface states degradation reveals the same trend with dark current evolution.

Then, a statistical approach of dark current is useful to complement the mean dark current under TG. Comparison of dark cur-

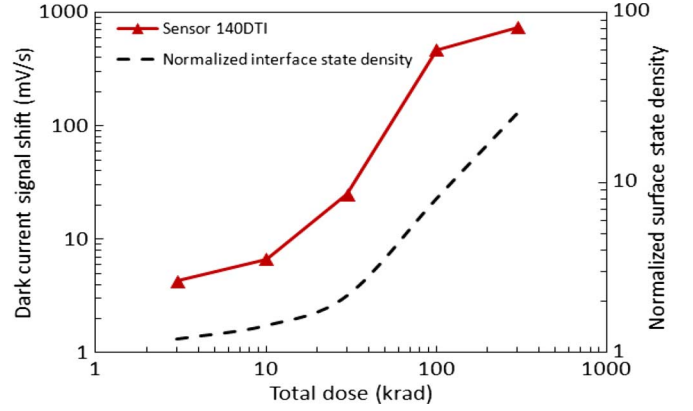


Fig. 13. Evolution of normalized Nit and dark current signal shift with TID for sensor 140DTI.

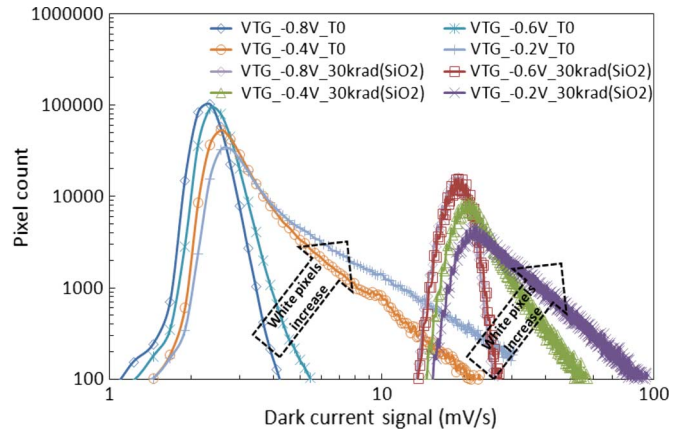


Fig. 14. Dark current signal histogram with TG OFF voltage (V_{TG}) for sensor 175STI at 30 krad(SiO_2).

rent distributions with V_{TG} before and after irradiation at 30 krad(SiO_2) is on Fig. 14.

These diagrams show that dark current value at the peak of distribution is not particularly influenced with V_{TG} . However, distributions of white pixels increase with the two highest voltages for both plotted conditions (T_0 and 30 krad(SiO_2)). The behavior of white pixels with TG bias explains the increase in mean dark current before and after irradiation. The evolution of distribution tail with TID shows that more and more pixels acquire huge dark current induced by TG interface state degradation.

C. Theoretical Analysis of Dark Current Under Irradiation

A study on the equations of dark current is proposed to provide a coherent approach on phenomena at stake along trenches.

Thus, electrons generated at the interface have to diffuse from interface to the photodiode according to diffusion equation written below:

$$\frac{\partial^2 \Delta n}{\partial x^2} - \frac{\Delta n}{\lambda_n^2} = 0 \text{ with } \lambda_n = \sqrt{D \cdot \tau_n} \quad (3)$$

With τ_n representing the minority carrier-lifetime and λ_n the diffusion length.

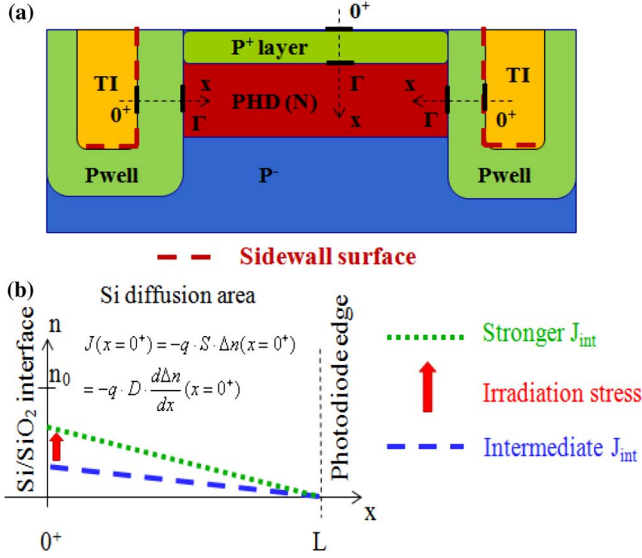


Fig. 15. Cross-section of pinned photodiode (a) and evolution of minority carrier concentration along a cut line with irradiation induced stress (b).

Also, generation current of electrons, with conventions set in Fig. 15(a), is explained in [22] with the boundary condition at the interface linking the generation/recombination current J_{int} and the diffusion current J_{diff} , as stated in (4):

$$J_{diff}(x = 0^+) = q \cdot D \cdot \frac{d\Delta n}{dx}(0^+) = J_{int}(0^+) = q \cdot S \cdot \Delta n(0^+) \quad (4)$$

With $S = \sigma_n \cdot v_{th} \cdot N_{it}$ the generation velocity of interface states, $\Delta n(x = 0^+) = n(x = 0^+) - (n_i^2/N_A)$ the variation of minority carrier density at the interface to be compared to concentration at thermal equilibrium, N_A the acceptor concentration, q the electronic charge, v_{th} the thermal velocity, σ_n capture cross-sections of electrons and D the diffusion coefficient in the diffusion area.

The desertion of minority carriers at the edge of the depletion region in Fig. 15(b) imposes (5):

$$n(x = L) = 0 \text{ and } \Delta n(x = L) = -\frac{n_i^2}{N_A} \quad (5)$$

Complete solution of dark current J_{dark} collected at the edge of depletion area ($x = L$) gives:

$$J_{dark} = J_{diff}(x = L) = -q \frac{n_i^2 \cdot D}{\lambda_n \cdot N_A} \cdot \frac{S \cdot ch\left(\frac{L}{\lambda_n}\right) + \frac{D}{\lambda_n} \cdot sh\left(\frac{L}{\lambda_n}\right)}{S \cdot sh\left(\frac{L}{\lambda_n}\right) + \frac{D}{\lambda_n} \cdot ch\left(\frac{L}{\lambda_n}\right)} \quad (6)$$

Considering (6), two realistic assumptions can be made to simplify this formula. The length L is supposed negligible compared to $\lambda_n (L \ll \lambda_n)$ and it results in:

$$J_{dark} \underset{L \ll \lambda_n}{=} -q \cdot \frac{n_i^2 \cdot D}{\lambda_n \cdot N_A} \cdot \frac{S + \frac{D}{\lambda_n} \cdot \frac{L}{\lambda_n}}{S \cdot \frac{L}{\lambda_n} + \frac{D}{\lambda_n}} \quad (7)$$

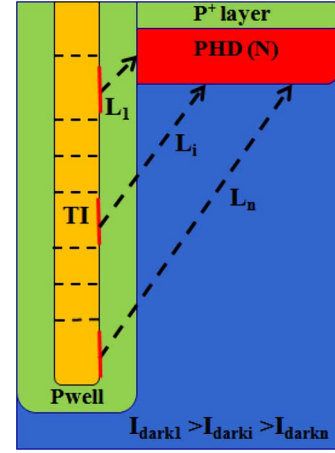


Fig. 16. Dark current reduction with different diffusion paths.

Then, it is supposed that generation processes at the interface are much more important than bulk generation ones on the length L ($S \cdot \tau_n \gg L$):

$$J_{dark} \underset{L \ll \lambda_n}{=} -q \cdot \frac{n_i^2}{N_A} \cdot \frac{\sigma_n \cdot v_{th} \cdot N_{it}}{\frac{\sigma_n \cdot v_{th} \cdot N_{it} \cdot L}{D} + 1} \quad (8)$$

This final expression shows that:

- thermal signature of dark current is characteristic of a diffusion behavior, according to n_i^2 term.
- dark current first increases linearly with N_{it} degradation.
- an important N_{it} increase induces self-limitation of minority carriers diffusion characterized by a saturation of dark current collected, as sketched and reported in Fig. 15(b) and (9):

$$J_{dark} \rightarrow -q \cdot \frac{n_i^2 \cdot D}{L \cdot N_A} \quad (9)$$

Next, (7) and (8) suppose that dark current value can be modulated with the distance L . Fig. 16 illustrates the differences on multiple paths (L_1 to L_n) from specific Si/SiO₂ interface to the photodiode.

The greater the distance, the weaker dark current value is. Overall dark current contribution along trench is represented by a sum of elementary sections. Thus, this model successfully explains at low doses why normalized contribution of deep trenches on Fig. 8. is weaker than shallow ones.

As the model is in good agreement with the saturation phenomenon at high TID, fits have been realized on each sensor in Fig. 17 on lin-lin scale.

The equation used for fitting is very similar to (8). Conclusions drawn in B) showed a strong correlation between dark current degradation and interface state density on gate oxide. Moreover, the main assumption based on a linear law between TID and N_{it} ($TID \sim N_{it} + cst$) seems reasonable from 30 krad(SiO₂). Thus, the following expression is proposed:

$$Fit(TID) = A \cdot \frac{TID - B}{C \cdot (TID - B) + 1} \quad (10)$$

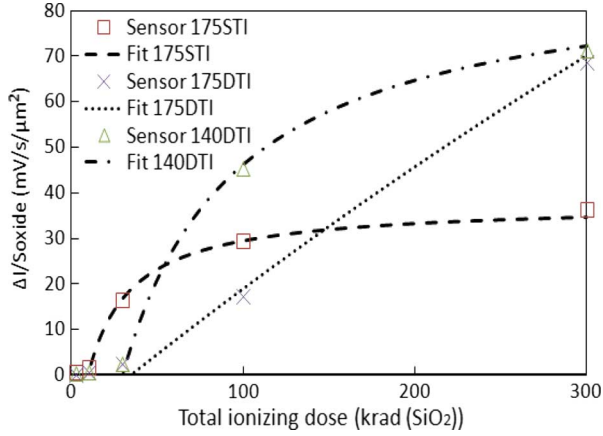


Fig. 17. Fits realized on normalized contributions of dark current.

TABLE III
SUMMARY OF SATURATION POINTS AND TRENCH VOLUME

Sensor	Saturation dose (krad(SiO ₂))	Trench volume (μm ³)
175STI	30	0.23
140DTI	100	2.1
175DTI	Not yet observed	2.5

These results well validate the saturation phenomenon described by theory in the second part of the graph.

As well, each trench presents different saturation doses, except for 175DTI where this phenomenon is not yet visible. A first assessment of saturation points with surrounding oxide's volume is made on Table III.

Unfortunately, a clear trend cannot be extracted but physical argumentation will be proposed in the overall synthesis.

V. TEMPORAL NOISE ANALYSIS

Temporal noise performance conditions image quality especially for low light level. This kind of measurement is basically made during null integration time on two snaps. Differences of these snaps suppress fixed pattern noise. Noise value is represented by standard deviation of pixels dispersion. Then, a special timing is used to discriminate the influence of respectively TG, SF and readout transistors by measuring noises of TG + SF + RD, SF + RD and RD. Operations on squared standard deviation enable identifying each contributor value.

All values of contributors are reported in Fig. 18 for sensor 175STI. The analysis of the temporal noise sources at room temperature reveals that most of the degradation comes from the SF transistor.

Another graph of relative temporal noise shift in Fig. 19 establishes the main differences between sensors 175STI, 175DTI and 140DTI. It is established that 175STI degrades faster than others. Despite gate oxide thickness on sensor 175STI departs slightly from the others (65 vs 50 Å), it reveals that oxide are too thin to explain charge effect accumulation.

Methodology of deducing normalized N_{it} established in part IV B is useful here to assess gate oxide degradation on each

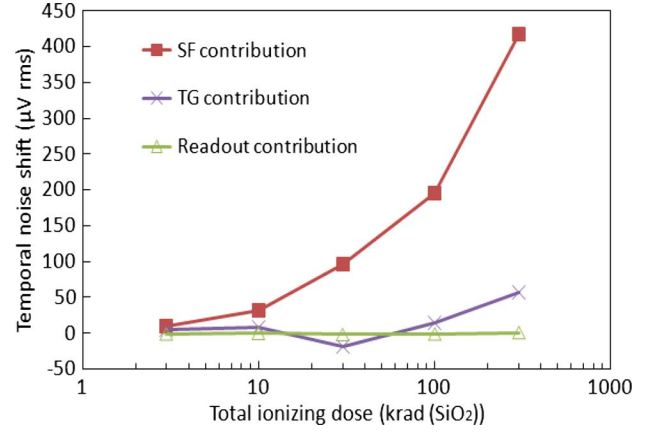


Fig. 18. Different contributors of temporal noise for sensor 175STI.

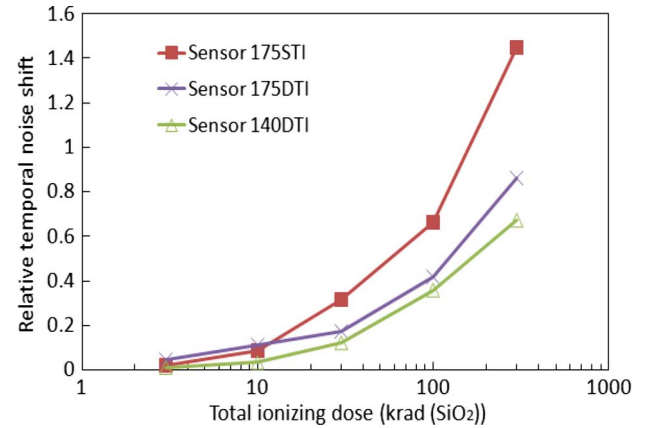


Fig. 19. Evolution of relative temporal noise shift with total ionizing dose on three different sensors.

TABLE IV
SUMMARY OF NORMALIZED N_{SS} EVOLUTION UNDER TG

Sensor	N_{SS} T_0	N_{SS} 100 krad(SiO ₂)
175STI	1	x12
140DTI	1	x4.8
175DTI	1	x6

sensor. Table IV below resumes normalized N_{it} for three sensors at 100 krad(SiO₂).

Values of interface state density on gate oxides reveal that dielectrics materials used for 175STI exhibit a twice more important degradation at 100 krad(SiO₂). As TG and SF share the same gate oxide, properties at the interface are identical. Processes for gate oxide growth of sensor 175STI are first suspected. But the configuration of trench isolation needs also to be discussed. On sensor 175STI, any method has been used to dope isolation sidewalls. Interfaces and traps in the vicinity of STI are free to interact with SF channel as depicted in Fig. 20(a). On the contrary, DTI are systematically doped on sidewalls which quenches or at least minimize noise sources, as sketched on Fig. 20(b).

To enrich data set about temporal noise, SF distributions of sensors 175DTI and 175STI are respectively in Fig. 21 and Fig. 22. Peak variations in Fig. 21 are not significant

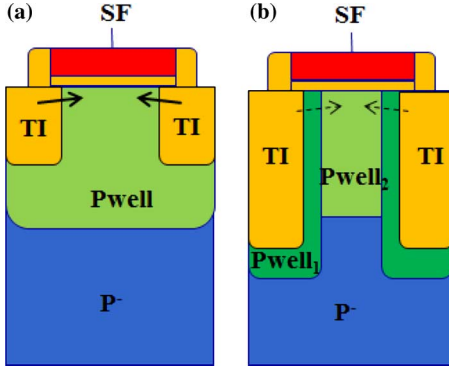


Fig. 20. Comparison of SF channel cross-sections in sensor 175STI (a) and in sensors 140DTI and 175DTI (b).

VI. DISCUSSION

Though every oxide (gate oxide, dielectric gapfill, buried oxide) have different process conditions (RTO, LPCVD, . . .), it has been evidenced that interface state degradation is strongly correlated with dark current saturation phenomena induced by trenches. Moreover, cross conclusions can be drawn between dark current and temporal noise results. Thus, the contribution of lateral trenches beyond 30 krad(SiO₂) was considered to explain SF noise degradation. An evolution with oxide volume is proposed to explain the origin of saturation threshold and how it differs from a trench to another. Indeed, the physics and especially the diffusion mechanisms of radiolytic hydrogen released after irradiation, and discussed at the beginning of part IV, could be different, depending on aspect ratios of trenches and dielectrics volume inside. The properties of hydrogen diffusion in dielectrics, ruled by Fick's law, would then condition the ability of interfaces to degrade during irradiation, inducing a different saturation threshold. This general assumption could be applied on all extended oxide parts and especially buried oxide. This additional oxide volume, releasing even more hydrogen, would explain the early saturation at 30 krad(SiO₂) on 140DBOX sensor.

VII. CONCLUSION

Commercial advanced CMOS image sensors have been irradiated with a ⁶⁰Co gamma-ray source. Despite these pixels with pinned photodiodes have not initially been developed to be radiation tolerant, it was observed on these devices a pretty good radiation hardness, with a sensor functionality preserved up to 300 krad(SiO₂). The exposition to the ionizing environment has mainly impacted the dark current signal and temporal noise of the sensor. Indeed, it was shown that some technological characteristics like the pixel isolation or the buried oxide can modulate the degradation of dark current, respectively at high and low TID. Even if the nature of every oxide introduced is radically different and complex, an Arrhenius analysis of dark current highlights that TID induced damages were not due to a depleted interface, as previously observed on 3T CMOS image sensors. A mathematical model based on N_{it} degradation along trench isolations is in good agreement with experimental data. In the future, it would be interesting to investigate the contribution of positive charges generated in oxides and compare them with the saturation effect induced by interface state density degradation. As well, the evolution of temporal noise has been mainly attributed to TID induced damages in the SF of the pixel. It is correlated with interface state density of MOS gate oxide and/or isolation trenches.

Finally, the Si/SiO₂ interface on top of the pinned photodiode did not appear to be the main degradation source after irradiation according to data measured on sensors embedding deep trench isolations. For further radiation hardness improvement, perimeter effects will have to be mitigated by new process conditions on trench isolations or by design variation.

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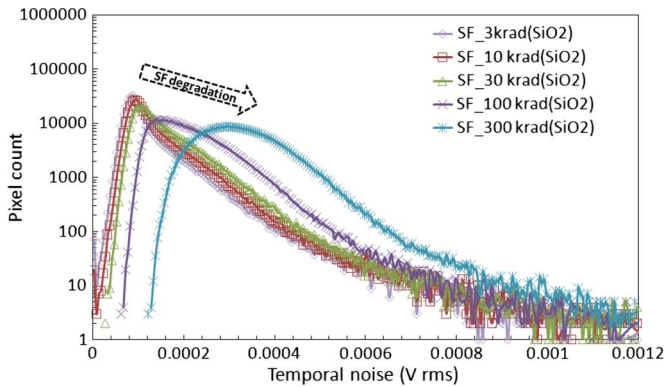


Fig. 21. Evolution of temporal noise distribution with TID for SF in sensor 175DTI.

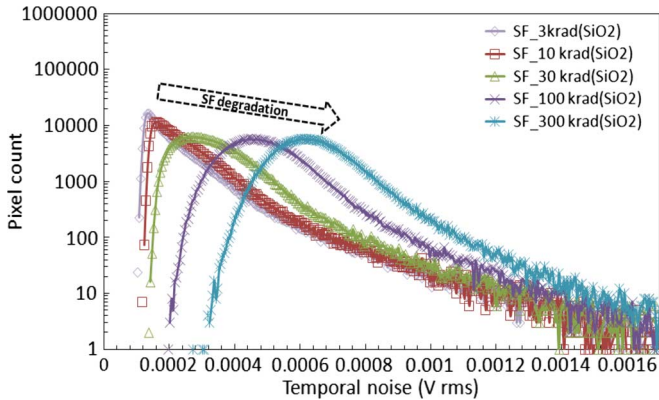


Fig. 22. Evolution of temporal noise distribution with TID for SF in sensor 175STI.

until 30 krad(SiO₂) with a slight transfer of population from peak to distribution tail. Major differences occur beyond 100 krad(SiO₂) with a shift of temporal noise on values at the peak and on standard deviations. The same behavior is observed on sensor 175STI in Fig. 22 with significant variations above 30 krad(SiO₂).

At the moment, it seems difficult from results reported to point out the main contributor of the temporal noise degradation. Two phenomena are here targeted between gate oxide and lateral trench degradation.

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REFERENCES

- [1] R. M. Guidash *et al.*, "A 0.6 μm CMOS pinned photodiode color imager technology," in *Proc. Int. Electron Device Meeting*, 1997, pp. 927–929.
- [2] E. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.
- [3] I. Inoue *et al.*, "New LV-BPD (Low Voltage Buried Photo-Diode) for CMOS imager," in *Proc. Int. Electron Device Meeting*, 1999, pp. 883–886.
- [4] A. El Gamal and E. Eltoukhy, "CMOS image sensors," *IEEE Circuits Des. Mag.*, vol. 21, no. 3, pp. 6–20, May–Jun. 2005.
- [5] J. Leijtens *et al.*, "Active pixel sensors: The sensor of choice for future space applications," in *Proc. SPIE*, 2007, vol. 6744.
- [6] G. R. Hopkinson *et al.*, "Radiation effects in a CMOS active pixel sensor," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2480–2484, Dec. 2000.
- [7] B. Pain *et al.*, "Hardening CMOS imagers: Radhard-by-design or radhard-by-foundry," in *Proc. SPIE*, 2004, vol. 5167, pp. 101–110.
- [8] V. Goiffon *et al.*, "Analysis of total dose-induced dark current in CMOS image sensors from interface state and trapped charge density measurements," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3087–3094, Dec. 2010.
- [9] J. Bogaerts *et al.*, "Total dose and displacement damage effects in a radiation-hardened CMOS APS," *IEEE Trans. Electron. Devices*, vol. 50, no. 1, pp. 84–90, Jan. 2003.
- [10] P. Rao *et al.*, "Degradation of CMOS image sensors in deep-submicron technology due to γ -irradiation," *Solid-State Electron.*, vol. 52, no. 9, pp. 1407–1413, Sep. 2008.
- [11] J. Tan and A. Theuwissen, "Total ionizing dose effects on 4-transistor CMOS image sensor pixels," in *Proc. IEEE Int. Conf. Electron Devices and Solid-State Circuits*, Dec. 2010, pp. 1–4.
- [12] J. Tan *et al.*, "4T CMOS image sensor pixel degradation due to x-ray radiation," in *Proc. Int. Image Sensor Workshop*, Hokkaido, Japan, 2011.
- [13] A. Theuwissen, "CMOS image sensors: State-of-the-art and future perspectives," in *Proc. Eur. Solid-State Device Research Conf.*, 2007, pp. 21–27.
- [14] A. Tournier *et al.*, "Pixel-to-pixel isolation by deep trench technology: Application to CMOS image sensor," in *Proc. Int. Image Sensor Workshop*, Hokkaido, Japan, 2011.
- [15] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 483–499, Jun. 2003.
- [16] J. Prima *et al.*, "Improved color separation for a backside illuminated image sensor with 1.4 μm pixel pitch," in *Proc. Int. Image Sensor Workshop*, Bergen, Norway, 2009.
- [17] H. L. Hugues and J. M. Benedetto, "Radiations effects and hardening of MOS technology: Devices and circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 500–521, Jun. 2003.
- [18] H. I. Kwon *et al.*, "The analysis of dark signals in the CMOS APS imagers from the characterization of test structures," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 178–184, Feb. 2004.
- [19] A. S. Grove and D. J. Fitzgerald, "Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions," *Solid-State Electron.*, vol. 9, pp. 783–806, 1966.
- [20] D. M. Fleetwood *et al.*, "Effects of hydrogen transport and reactions on microelectronics radiation response and reliability," *J. Microelectron. Reliab.*, vol. 42, pp. 523–541, 2002.
- [21] H. Han *et al.*, "Evaluation of a small negative transfer gate bias on the performance of 4T CMOS image sensor pixels," in *Proc. Int. Image Sensor Workshop*, Ogunquit, ME, 2007, Session 12.
- [22] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. Hoboken, NJ: Wiley, 1981, p. 56.