Radiation Effects in Pinned Photodiode CMOS Image Sensors: Pixel Performance Degradation Due to Total Ionizing Dose

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***Abstract*—Several Pinned Photodiode (PPD) CMOS Image Sensors (CIS) are designed, manufactured, characterized and exposed biased to ionizing radiation up to 10 kGy(SiO_2). In addition to the usually reported dark current increase and quantum efficiency drop at short wavelengths, several original radiation effects are shown: an increase of the pinning voltage, a decrease of the buried photodiode full well capacity, a large change in charge transfer efficiency, the creation of a large number of Total Ionizing Dose (TID) induced Dark Current Random Telegraph Signal (DC-RTS) centers active in the photodiode (even when the Transfer Gate (TG) is accumulated) and the complete depletion of the Pre-Metal Dielectric (PMD) interface at the highest TID leading to a large dark current and the loss of control of the TG on the dark current. The proposed mechanisms at the origin of these degradations are discussed. It is also demonstrated that biasing (i.e., operating) the PPD CIS during irradiation does not enhance the degradations compared to sensors grounded during irradiation.**

***Index Terms*—4T pixel, active pixel sensor, APS, buried photodiode, charge transfer, CMOS image sensor (CIS), dark current, deep submicron process, DSM, interface states, ionizing radiation, MAPS, monolithic active pixel sensor, photon transfer curve (PTC), pinned photodiode (PPD), pinning voltage, pre-metal dielectrics (PMD), quantum efficiency, radiation hardening, RHBD, shallow trench isolation (STI), total ionizing dose (TID), trapped charge.**

I. Introduction

PINNED photodiode (PPD) CMOS Image Sensors (CIS) [1] are the most promising photodetectors for a growing number of high performance imaging applications where ionizing radiation can be an issue (such as space, scientific, nuclear, medical and military instruments). However, whereas some radiation-hardening-by-design initiatives can be found in the literature [2], [3], the behavior of the pinned photodiode and its associated Transfer Gate (TG) after exposure to ionizing radiation is not fully understood today. Indeed, the physical process at the origin of radiation induced dark current in pinned photodiode has not been completely clarified and only a few other parameters or characteristics have been studied on irradiated PPD CIS (e.g., External Quantum Efficiency (EQE) in [4] and noise in [5]–[7]). Moreover, most of the previous work has been performed on devices grounded during irradiation, which may hide some effects that could be enhanced by the local electric field during exposure.

The aim of this work is to provide an overview of the Total Ionizing Dose (TID) effects that may occur in PPD CIS operated during irradiation (not to evaluate precisely the radiation hardness of the tested sensors at a given TID for a specific environment). To do so, we study the main parameters and characteristics of six 4T-PPD-CIS manufactured in two widely used commercially available CIS foundries. Several original radiation effects on PPD CIS are reported, and all these results seem to indicate that the electrostatic structure of the buried photodiode (i.e., the space charge region thickness and location) is changed, even at low TID, leading to complex degradation mechanisms.

After the description of the experimental details, the results of the measurements performed on the irradiated PPD CIS are presented and discussed in Section III. More detailed discussions on the overall degradation mechanism and the effect of biasing during irradiation are finally presented in Section IV.

II. Experimental Details

Two unhardened CIS designs based on PPD pixels (see Fig. 1 for a cross sectional view and Fig. 2 for a simplified layout illustration), with four transistors (the most simple PPD pixel architecture) and without micro-lens or color filter, were manufactured using two different CMOS foundries. Both processes are widely used commercially available 0.18 μm CIS technologies. The image sensor details are summarized in Table I. As discussed in detail in [8], V_{LOTG} represents the voltage applied on the TG when it is turned off. The value shown in the table is the optimal value selected for this study.

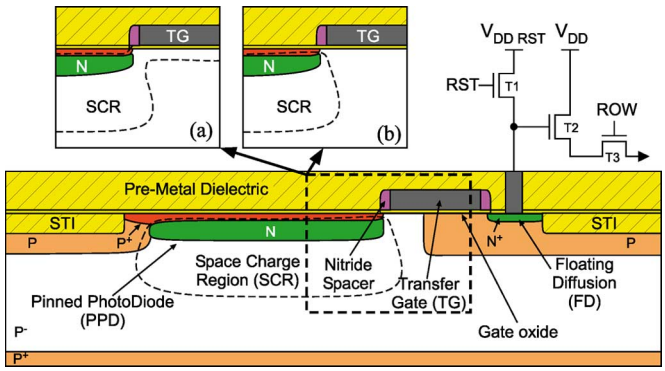

Fig. 1. Cross sectional view (not to scale) of a 4T Pinned PhotoDiode (PPD) pixel. Insets show the TG depletion region for two bias cases: (a) $V_{LOTG} = 0$ V: the TG depletion region merges with the photodiode depletion region. (b) $V_{LOTG} < 0$ V: the gate is accumulated and the photodiode depletion region does not touch any oxide interface anymore. The typical depth of Shallow Trench Isolation (STI) in the studied technology is about 400 nm.

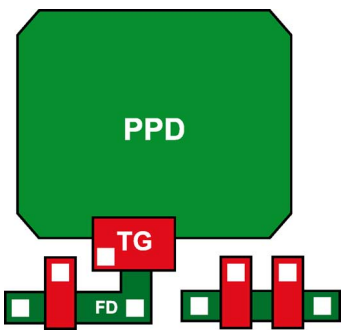

Fig. 2. Simplified top-view illustration of the studied 4T pinned photodiode pixels.

TABLE I
KEY FEATURES OF THE STUDIED CMOS IMAGE SENSORS

Features	Sensor A	Sensor B
Array size	256 × 256	256 × 256
Pitch (µm)	7	4.5
PPD area (µm^2)	6.25	2.2
PPD perimeter (µm)	10	7.7
CVF (µV/ e$^-$)	57	38
V_{LOTG} (V)	− 0.65	− 0.5
MOVS (mV)	885	345
Full Well (ke$^-$)	15.5	9.1
Technology	CIS PPD 0.18 µm	CIS PPD 0.18 µm
Foundry	Foundry A	Foundry B

The pixels have been designed for testing purpose. It means that the pixel layout has been kept simple (e.g., rectangular photodiode) to ease the interpretation and that these sensors are not optimized (e.g., fill factor, TG shape, Maximum Output Voltage Swing (MOVS), dynamic range. . .) for a dedicated high performance application. It is worth mentioning that only the functions necessary to the imagers are on-chip for easier analysis: the pixels, the address decoders and the analog sampling/ readout chains. The sequencer and the analog-to-digital conversion chain are located on the test boards (and were not exposed to ionizing radiation) to ensure that the observed degradations come only from the sensor.

All the measurements were performed using the timing diagram illustrated in Fig. 3, but without the optional dump/injection phase (if not stated otherwise). During this phase, if the RST

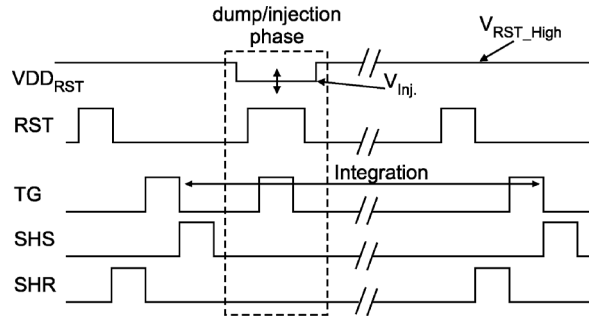

Fig. 3. 4T PPD timing diagram showing the optional injection or dump phase.

MOSFET supply voltage V_{DDRST} is kept at its nominal value $V_{RSTHigh}$, the buried photodiode is emptied a second time by activating the TG and the RST MOSFET simultaneously. This dump phase is used in most of commercial products since it reduces the image lag (but without improving the charge transfer efficiency) and provides additional benefits such as a better behavior in case of blooming. It is interesting to notice that if V_{DDRST} is lowered during this phase, charges can be injected into the photodiode (this is discussed in detail in Section III.D).

We have voluntarily decided not to use this dump/injection phase (except for pinning voltage estimation). We use the most elementary 4T-PPD timing diagram with no dump/injection phase for two main reasons: 1) the dump phase artificially improves the charge transfer efficiency and so, hides its degradation and 2) a simpler timing diagram is supposed to ease the radiation effects analysis.

For each tested CIS foundry, two devices were exposed biased—or more precisely biased and sequenced continuously thanks to an FPGA board as in standard operating conditions—and one was exposed grounded (for a total of six studied pixel arrays) to $10keV$ X-rays at CEA-DIF with no lid or cover glass on top of the sensors. The absorbed TID ranges from 0.5 kGy(SiO_2) to 10 kGy(SiO_2) and the dose rate was about 1 Gy(SiO_2)/s.

III. RESULTS

A. Unchanged Parameters

Before discussing the main results, it is necessary to verify that the sensors are still working well after the highest TID. Fig. 4 shows four raw frames taken by two irradiated sensors after 3 and 10 kGy(SiO_2). It can be seen that both sensors are still functional after 10 kGy(SiO_2), confirming once again [9] that the integrated digital circuits (address decoders and switches) are not significantly degraded. Indeed, in order to get an image, the logic gates of the row and column decoders must operate properly to activate, in the right order, every pixel. If a single digital MOSFET was not working after irradiation, it would lead to image artifacts and the original pattern would not be reconstituted properly. Supply current and electrical transfer function (from the Floating Diffusion (FD) to the sensor output) were measured after each step and no change was observed, even after the highest TID. The mean-variance characteristics (i.e., output voltage variance as a function of mean output voltage) after each TID did not show any significant conversion factor (CVF) degradation. These results

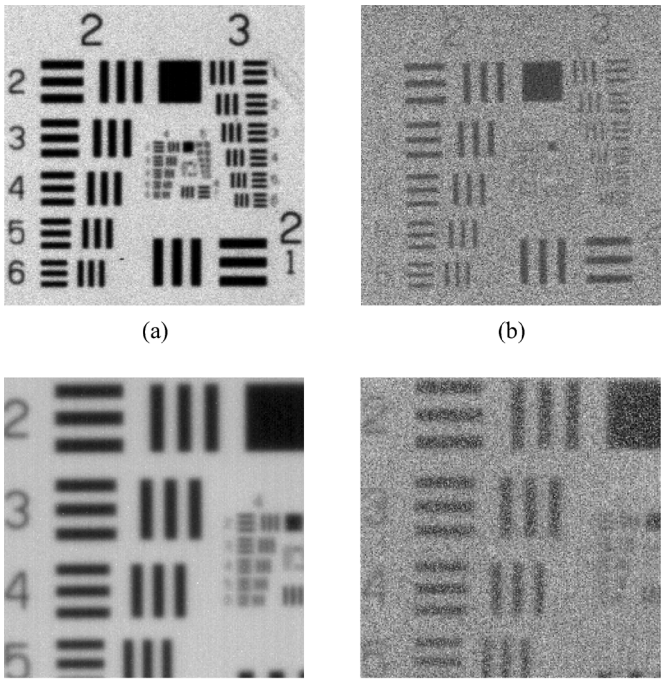

Fig. 4. Raw images of the 1951 USAF resolution test chart captured with sensor A (a) after 3 kGy and (b) after 10 kGy. Same test chart captured with sensor B (c) after 3 kGy and (d) after 10 kGy.

correspond well to previous study results [9]: they have shown that the digital circuits and the analog readout chains (including T1, T2 and T3 in Fig. 1) are not degraded in this TID range and that radiation-hardened-by-design transistors are not necessary. Therefore, all the radiation effects presented in the following can be attributed to the PDD, the TG or both.

B. Photon Transfer Curve and Sensitivity

Fig. 5 presents the Photon Transfer Curve (PTC) of sensor A and sensor B respectively, measured using a bandpass filter centered on 650 nm. Several TID induced effects appear on both sensors PTC: a drop of the saturation voltage (and thus of MOVS), a slight change in the PTC slope and, only for sensor A, the appearance of a low-level non-linearity for TID higher than 0.5 kGy(SiO_2). The change in the PTC slope, which seems to become smaller when the TID is increased, can only be due to a change in the EQE (since no degradation of the analog readout chain or the CVF was observed). This factor can be defined as the ratio between the number of collected electrons and the number of incoming photons on the entire pixel surface. Concerning the saturation voltage drop, both sensors exhibit a comparable behavior. Same measurements previously performed on 3T pixels with conventional photodiode showed the exact opposite, i.e., a rise of the saturation voltage induced by the TID [10] attributed to a modification of the reset transistor threshold voltage. To exclude this cause, direct analog voltage measurements have been performed directly on the sensor output. The reference voltage measured in these conditions did not change significantly with TID showing that the RST MOSFET (T1 in Fig. 1) is not involved here. Furthermore, these direct output voltage measurements showed that the minimum and maximum FD voltages stay in the linear range of the electrical transfer

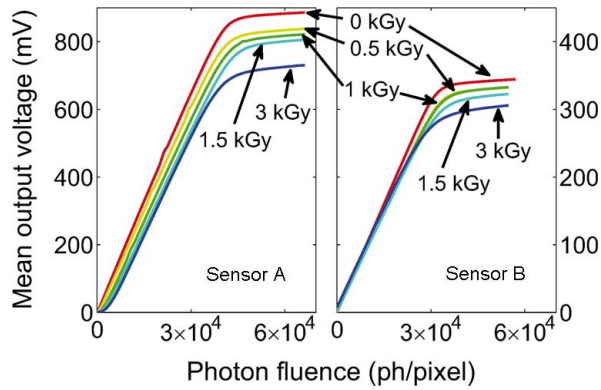

Fig. 5. Sensor A (left) and B (right) PTC before and after irradiation.

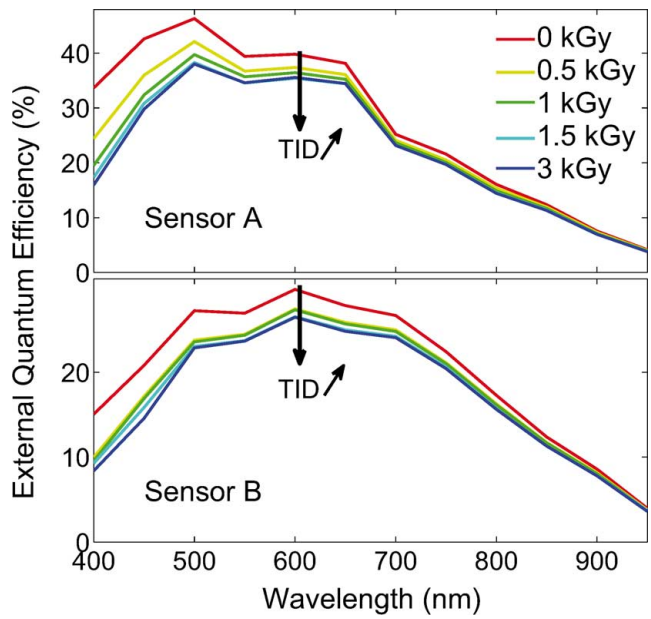

Fig. 6. Sensor A (top) and B (bottom) EQE before and after irradiation.

function. Hence, a pixel element located before the FD must be involved in this MOVS decrease: the photodiode itself, the TG or both.

We have seen previously on the PTC that the TID induces noticeable changes on the sensitivity. This is confirmed by the EQE measurements presented in Figs. 6 and 7. The EQE is clearly lower after irradiation, especially for short wavelengths.

This wavelength-dependent effect strongly suggests a change in the surface recombination velocity directly related to an interface state density increase[1] at the PMD or STI interfaces (see Fig. 1) as concluded in [4], [10].

Fig. 7 compares the drop of saturation voltage and EQE for devices grounded and biased during irradiation. One can see that there is no effect of this biasing condition on the TID induced PTC and EQE degradations.

[1]Carriers generated by short wavelength photons are mainly located near the surface of the pixel. In frontside illuminated sensors it means that short wavelength photons mainly generate carriers near the dielectric/silicon interfaces such as the interfaces between the Pre-Metal Dielectric (PMD) (or the Shallow Trench Isolation (STI)) and the silicon. The effective diffusion length in this region is mainly limited by the recombination lifetime at the dielectric/Si interfaces. Hence, a drop of collection efficiency at the shortest wavelengths can be explained by an interface state density increase leading to an interface recombination lifetime reduction.

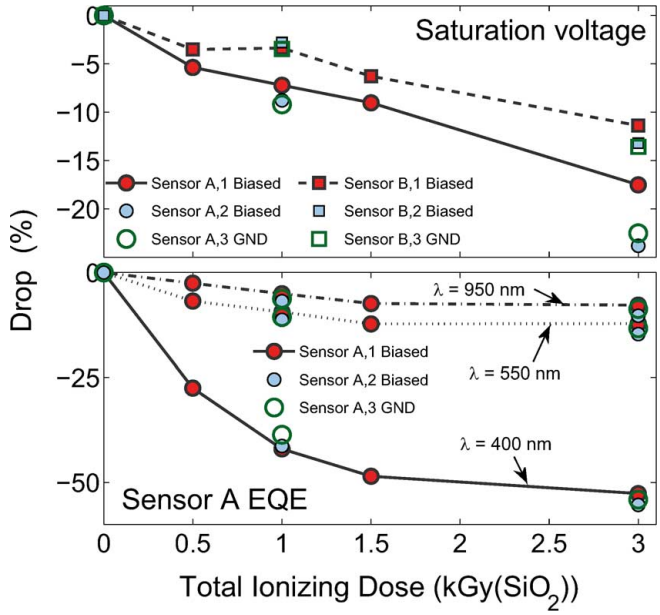

Fig. 7. Sensor A and B saturation voltage drops measured at 650 nm with a photon fluence of $6.5 \cdot 10^4$ ph/pixel (top) and sensor A EQE drop with TID at three wavelengths (bottom).

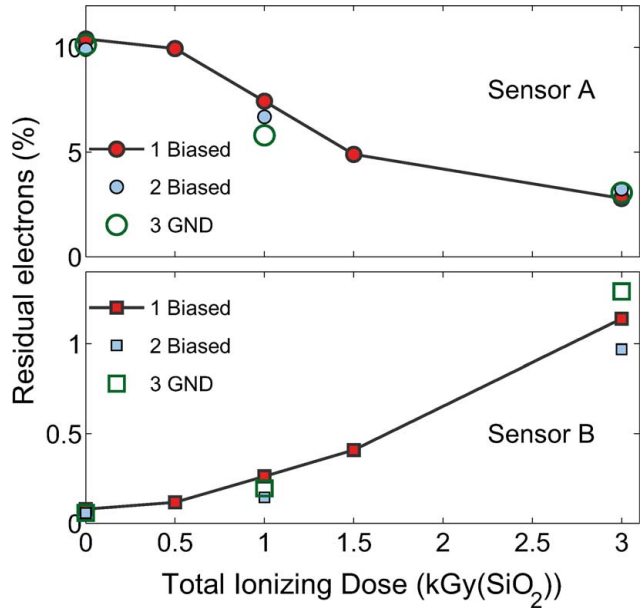

Fig. 8. Percentage of residual electrons (in the dark frame that follows the pulse frame), for sensors A and B, with regard to the TID. Number of electrons in the frame integrating the pulse is around 4000 for each sensor and each TID step.

C. Charge Transfer Efficiency

The TG Charge Transfer Efficiency (CTE) can be estimated by illuminating uniformly the pixel array during one frame and by measuring the number of deferred charges in the following non-illuminated frames. In an ideal sensor with perfect transfer efficiency, there should not be any deferred charge in the dark frame that follows the illuminated frame. In a real device, some electrons generated during the illuminated frame may stay in the pixel, due to an incomplete transfer. Then, these residual electrons will be transferred during the following readout phases (corresponding to the following dark frames), leading to a non-zero signal in one or more successive dark frames. Hence, the number of residual electrons in the dark frame that follows the illuminated frame is a good factor to evaluate the efficiency of the transfer (the higher is the percentage of deferred electrons, the worse the CTE is). Such transfer efficiency evaluation has been performed using a pulsed LED. The light pulse is synchronized in such a way that it is entirely temporally localized in a single frame. The results presented in Fig. 8 represent the number of deferred electrons in the frame that follows the frame illuminated by the LED pulse.

One can see in Fig. 8 that, before irradiation, the sensor A CTE seems very poor (more than 10% of residual electrons in the frame following the pulse frame) compared to values usually reported on state-of-the-art micron size pixels (a few electrons or even less than one residual electron). However, as mentioned in Section II, the dump phase is not used for this study and the real CTE of the TG is measured. This poor lag performance could be artificially improved by one or two orders of magnitude simply by using the dump phase. In this case, the remaining lag charges are evacuated during this optional phase, and these charges do not appear in the following frame (but these useful charges are lost), leading to an apparent very efficient charge transfer. For a radiation effect study, this dump phase would hide the main part of the CTE degradation and complicate the analysis.

Sensor B CTE would also be better if a dump phase was used, but its CTE is already pretty good, especially when compared to sensor A. Each CIS foundry has its own TG doping profile, and it may play a role in this observed discrepancy by leading to different potential distributions. However, it cannot be simply attributed to this cause here since as good CTE as sensor B CTE was observed in the laboratory on other pixel designs manufactured with foundry A, and very poor CTE was achieved with foundry B on larger pixels. A part of this difference might be attributed to the difference in photodiode area (Table I), since smaller buried photodiodes are easier to drain and have a lower pinning voltage [11], which helps the transfer. Finally, as detailed previously, the photodiode layout used for this study is a simple rectangle, which may not be the best shape for an optimized transfer [12] in the 7-μm-pitch sensor A, whereas it may not be of importance for the very small diode of sensor B.

After exposure to ionizing radiation (Fig. 8), both CTE change significantly. To our knowledge, such radiation effect has never been reported before in PPD CIS. However, the results obtained on sensors A and B disagree : in the first case, TID seems to improve the transfer (the percentage of residual electrons decreases) and in the second case, the transfer is degraded when the TID is increased. The main cause of image lag in PPD CIS is: a potential barrier or pocket between the photodiode and the TG [13], [14] and they are illustrated in Fig. 9. A potential barrier is created when the overlap between the TG and the photodiode is not sufficient (or if the local P doping concentration in this overlap region is too high) whereas a potential pocket may exist if the TG overlaps too much the photodiode. At the end of the transfer, a barrier can prevent charges from being drained out of the photodiode whereas a potential pocket can trap signal charges, leading to incomplete transfer. Radiation induced positive charges trapped in the

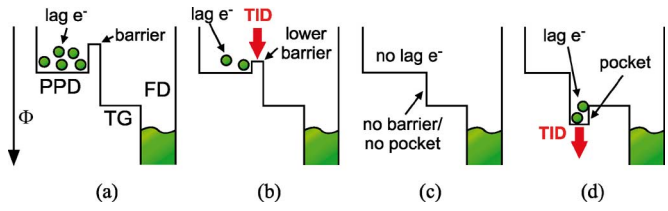

Fig. 9. Proposed mechanism for the observed CTE variations with TID illustrated by simplified electrostatic potential diagrams at the end of the transfer phase (TG still ON). Potential diagrams of the sensor A pixel (a) before and (b) after irradiation. Potential diagrams of the sensor B pixel (c) before and (d) after irradiation.

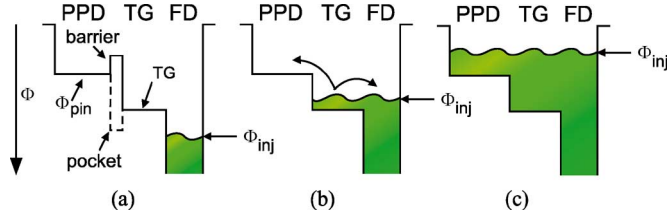

Fig. 10. Simplified electrostatic potential (Φ) diagram of the PPD, the TG and the FD for three cases of interest: (a) when $\Phi_{\rm inj} > \Phi_{\rm TG}$, (b) when $\Phi_{\rm pin} < \Phi_{\rm inj} < \Phi_{\rm TG}$ and (c) when $\Phi_{\rm inj} < \Phi_{\rm pin}$. A potential barrier and a potential pocket are also shown in (a) for illustration.

dielectrics around this overlap region (e.g., the PMD and the nitride spacers) lead to an additional electric field that tends to lower potential barriers and increase the depth of potential pockets as illustrated in Fig. 9.

Since sensor B CTE is very good before irradiation, we assume that nothing limits the transfer, and so that there is no major potential barrier (Fig. 9(c)). In this case, the accumulation of trapped positive charges in this overlap region degrades the CTE by creating a potential pocket that keeps some electrons at the end of the transfer phase (Fig. 9(d)). In the case of sensor A, the poor CTE might be due to a high potential barrier or a deep pocket. Since the irradiation improves the CTE of sensor A, it strongly suggests that sensor A CTE is limited, before irradiation, by a large barrier that leads to an incomplete transfer as shown in Fig. 9(a). In this hypothesis, this high barrier is lowered after irradiation by the positive oxide trapped charge (Fig. 9(b)), explaining the difference with sensor B. It is important to notice in Fig. 8 that the differences between biased and grounded sensors during irradiation are within the device mismatches.

D. Pinning Voltage

The pinning voltage $V_{\rm pin}$ (or pinch-off voltage) of a pinned photodiode, is the maximum deviation, from its equilibrium value, of the electron quasi-Fermi potential in the N doped region of the buried photodiode [15]. This value is reached when the photodiode is fully depleted. In other words, when all the electrons have been transferred out the photodiode (this should be the case at the beginning of each integration phase). Measuring the absolute pinning voltage is tricky. There is one well established technique to measure it on test structures [15]. This technique was recently transposed to the measure of the pinning voltage inside a pixel array [16]. It relies on the use of the injection phase presented in Fig. 3. During the injection phase, $\rm V_{DDRST}$ is lowered to $\rm V_{inj}$ in order to inject charges in the photodiode that will be readout during the next readout phase. This principle is illustrated in Fig. 10. When $\rm V_{inj}$ is higher than the pinning voltage (Fig. 10(a)), no charge is injected into the photodiode and the measured output voltage at the end of the integration time is almost zero. When $\rm V_{inj}$ is lower than the pinning potential (Fig. 10(c)), charges are injected into the photodiode and this number of injected carriers increases with further decrease of $\rm V_{inj}$. Therefore, the $\rm V_{inj}$ voltage at which the output voltage starts to increase with decreasing $\rm V_{inj}$ should correspond to the pinning voltage. Nevertheless, due to the non-ideality of charge transfer, and especially the fact that the photodiode and TG structures are optimized for a transfer from the photodiode to the FD, the accuracy of this method for determining the absolute pinning voltage may not be good. It should be, however, a good tool to characterize pinning voltage changes, for example in irradiated devices.

The result of this technique on sensor A is shown in Fig. 11. The observed behavior corresponds to the expected trend for $\rm V_{inj} > 2$ V and for $\rm V_{inj}<0.4$ V, but an unexpected plateau appears between these two $\rm V_{inj}$ values. This increase of output signal that starts for $\rm V_{inj}\approx 2$ V is attributed to the phenomenon illustrated in Fig. 10(b). When the injection potential becomes lower than the TG surface potential $\Phi_{\rm TG}$, electrons are accumulated under the TG. When the TG is suddenly switched off, some of the channel charges go back to the FD, but some are injected into the photodiode. These injected charges generate an output signal in the next readout phase. For the following analysis, one should keep in mind that: the beginning of the plateau corresponds to the condition $\Phi_{\rm inj}\approx\Phi_{\rm TG}$, the height of the plateau should be proportional to the number of charges injected into the photodiode when the TG is switched-off, and the $\rm V_{inj}$ value at which the output starts to increase with decreasing $\rm V_{inj}$ is related to the pinning voltage. Based on these hypotheses, one can see in Fig. 11 that TID clearly increases the pinning voltage of the irradiated A sensors, with a huge increase after 10 kGy. On the other hand, the TG threshold voltage does not seem degraded, since the beginning of the plateau does not change with TID. It indicates that TG gate oxide degradation is not significant here and that the trapped charge in the lateral STI is not sufficient to have a visible impact on the TG channel potential in this wide transistor.

The same radiation effects can be observed on the other technology (clear shift of $\Phi_{\rm pin}$ and no change of $\Phi_{\rm TG}$), as presented in Fig. 11. In addition, the plateau height increases with TID. This effect agrees with the previous conclusion suggesting the radiation induced creation of a potential pocket. Indeed, the higher the TID, the deeper the potential pocket, and the more electrons are trapped in the pocket and released in the next readout phase. It should be emphasized that, on both tested technologies, there is no difference between the sensor biased and grounded during irradiation. To our knowledge, these results presented in this section are the first evidences of TID effect on pinning voltage in PPD CIS.

E. Dark Current

Dark current measurements were performed in a dark temperature test chamber at a regulated temperature (295 K, except

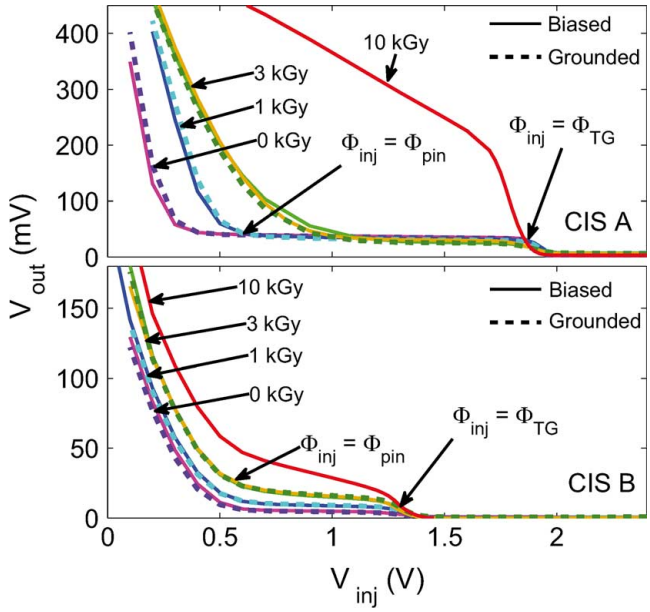

Fig. 11. Pinning voltage measurements of sensor A (top) and sensor B (bottom), for several TID.

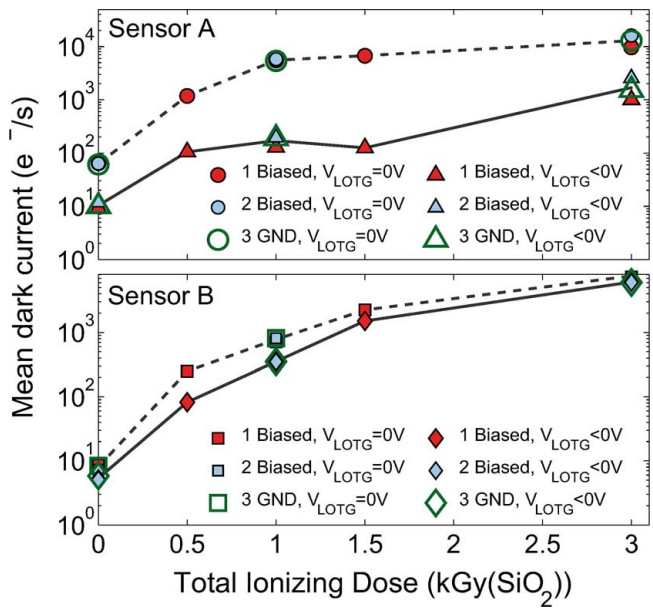

Fig. 12. Mean dark current increase with TID for the six studied sensors and for two $\mathrm{V_{LOTG}}$ values (accumulation $\mathrm{V_{LOTG}} < 0$ V and depletion $\mathrm{V_{LOTG}} = 0$ V). $T = 295$ K.

for activation energy determination). The evolution of dark current with TID is presented in Fig. 12 for both CIS technologies, for two TG bias configurations during integration, and for the two biasing conditions during irradiation (biased and grounded). The observed increase on both technologies is very similar to what has been previously seen on the same PPD CIS technology node [8]. The most original result presented in this figure is the absence of effect of biasing during irradiation on the dark current increase with TID.

As regards the influence of the TG OFF voltage ($\mathrm{V_{LOTG}}$), Fig. 13 provides a little more information. It can clearly be seen in Figs. 12 and 13 that the use of negative $\mathrm{V_{LOTG}}$ leads to a major reduction in dark current in sensor A, both before and after irradiation. Since the general shape of the characteristics is

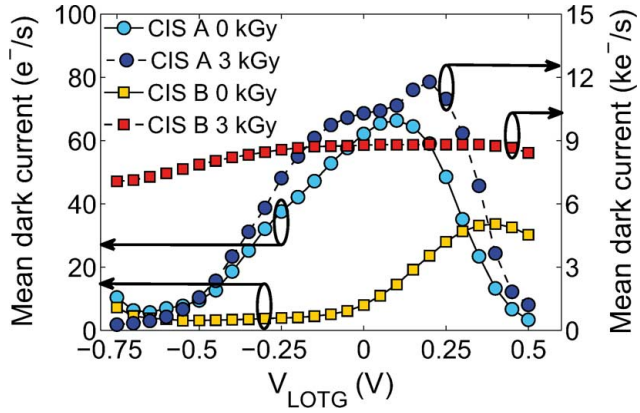

Fig. 13. Sensor A and B mean dark current as a function of $\mathrm{V_{LOTG}}$ before irradiation and after 3 kGy(SiO_2). $T = 295$ K.

not changed much (no obvious shift), the TG threshold voltage does not seem degraded by the TID. It is in good agreement with the pinning voltage measurement presented previously. On the other hand, in sensor B (Fig. 13), negative $\mathrm{V_{LOTG}}$ only reduces the dark current by a few percent after 3 kGy(SiO_2), whereas it has a strong influence before irradiation. The transfer gate oxide is not supposed to be significantly degraded since previous work has shown that gate oxide trapped charge and interface density changes are not observed in this TID range (10 kGy(SiO_2) in a similar technology [17]). Moreover, pinning voltage measurement on B sensors also shows no change of TG threshold voltage with TID.

The Arrhenius plots of the average dark currents presented in Fig. 14 provide further insight into this phenomenon. In addition to the evolution of dark current with temperature, the typical variation of the diffusion current with temperature ($\propto T^3 n_i^2$, [18], represented by a dashed line in Fig. 14) and of the interface state generation current with temperature ($\propto T n_i$, [18], represented by a solid line) are also plotted for comparison. By comparing the evolution of dark current with temperature to these two typical sources of leakage current[2], one can estimate what the main contribution is at room temperature (the vertical dashed line represents the 295 K temperature).

For both sensors, when the TG is depleted ($V_{\mathrm{LOTG}} = 0$ V), the dark current is always dominated by the interface state generation current. This behavior was expected since the buried photodiode depletion is in direct contact with the dielectrics surrounding the TG (PMD, STI, nitride spacer and gate oxide). When the TG is in accumulation ($\mathrm{V_{LOTG}}$<0 V), the behaviors of the two sensors differ once again. Sensor A dark current is dominated by the diffusion contribution up to 3 kGy. It indicates

[2]If the slope of the measured dark current evolution with temperature is close to the slope of the diffusion dark current (i.e., if the measured data are almost parallel to the dashed lines), it can be inferred that the diffusion contribution is the main one. On the other hand, if the slope of the measured data is closer to the theoretical slope of the generation current (i.e., if the data are almost parallel to the solid lines), the generation contribution is most likely the most important source of dark current. Since the diffusion contribution rises more rapidly with temperature than the generation contribution, the dark current source that dominates can change with temperature, leading to different slopes at different temperatures. That is the reason why, in some cases in Fig. 14, at the same TID, the generation current seems to dominate at low temperature and is hidden by the diffusion current at higher temperature (leading to a GEN arrow and a DIFF arrow, both pointing toward the same set of data in Fig. 14, but not in the same temperature range).

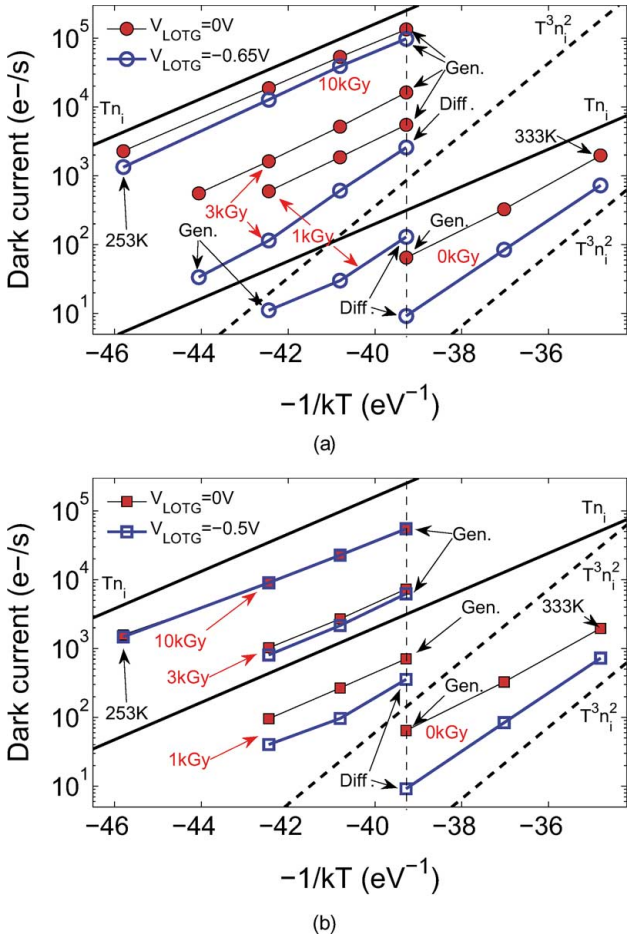

Fig. 14. Dark current Arrhenius plot of (a) sensor A and (b) sensor B. The ideal diffusion and generation contribution evolutions are represented by $T^3 n_i^2$ and $T n_i$ respectively. "Gen." stands for "Generation contribution" and "Diff." for "Diffusion contribution". The vertical dashed line represents the regulated temperature used for this study: 295 K. The dark current values given after 10 kGy at 295 K are extrapolated from measurements performed at lower temperature (and same TID).

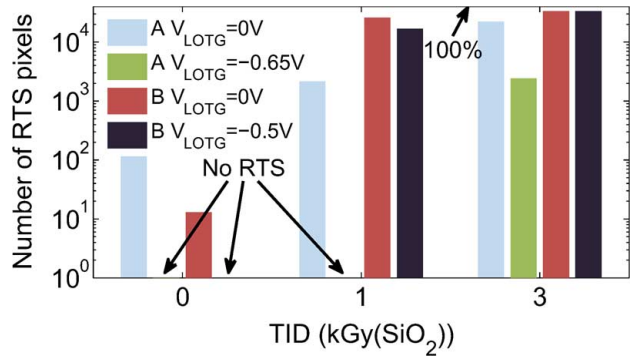

Fig. 15. Number of detected RTS pixels for each TID and for two transfer gate biasing conditions during integration.

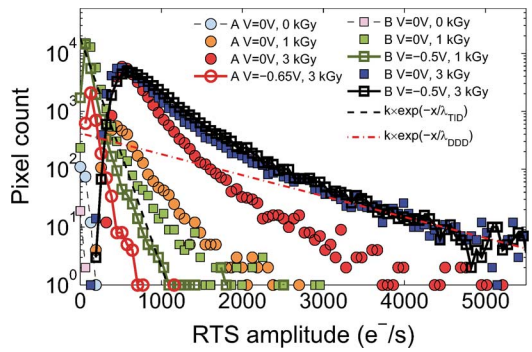

Fig. 16. Dark current RTS transition maximum amplitude distributions. Maximum values go up to 13 ke^-/s. $T = 295\mathrm{K}$.

that the TG is well accumulated, and that the photodiode depletion region is kept away from the oxides in most of the pixels. It also confirms that the TID can enhance the diffusion contribution coming from the surrounding interfaces through the generation of interface states as discussed in [6], [8]. At 10 kGy, the generation current is the main contribution, even in accumulation. It shows that the photodiode depletion region reaches the surrounding oxides.

As regards sensor B, when the TG is accumulated, the generation contribution is eliminated before irradiation, reduced at 1 kGy and no more controlled after 3 kGy. This observation suggests a reduced P doping in the overlap region (or a larger extension of the PPD N doping below the transfer gate), compared to sensor A. It would explain why the transfer efficiency is better for sensor B (lower or even no barrier), and why the TG, when negatively biased, does not manage to prevent the photodiode depletion region to reach the oxides for TID above 1 kGy.

F. Dark Current Random Telegraph Signal

Interface state induced Dark Current Random Telegraph Signal (DC-RTS) has been recently observed in CIS with conventional photodiodes in 3T pixels before irradiation and after exposure to ionizing radiation [19]. DC-RTS has also been reported on unirradiated PPD [20], but only if the TG is not accumulated (and thus, if the photodiode depletion region reaches the TG channel). We therefore wanted to see if TID could also generate DC-RTS centers in PPD, and if accumulating the TG mitigates this parasitic dark current variation.

DC-RTS measurement, detection and parameter extraction are realized accordingly to the technique described in [21]. A narrow temporal detection window (i.e., two hour measurements with one sample every second) was used to speed up the measurements for this first study. It means that many other RTS may be missed (the ones faster than one second and the ones slower than two hours).

The resulting number of detected DC-RTS pixels is presented in Fig. 15. As in conventional photodiodes, TID is clearly able to massively generate DC-RTS centers in PPD when the TG is depleted (on both technologies): almost all the pixels exhibit such RTS behavior after 3 kGy(SiO_2), and the ones that do not are most likely simply not detected by the algorithm. Most of the active RTS centers in this case are most likely located in the TG channel (STI sidewalls or gate oxide). The effect of TG accumulation is confirmed before irradiation, but also after 1 kGy(SiO_2) on sensor A (no RTS pixel detected). However, after 1 kGy(SiO_2) on sensor B and after 3 kGy(SiO_2) on sensor A, a large number of RTS pixels are also detected in accumulation mode, showing that the photodiode depletion region of some pixels starts to reach the dielectric interfaces. The fact that this degradation appears at a lower TID on sensor B than on sensor A agrees well with the previous conclusion on the TG-photodiode overlap region.

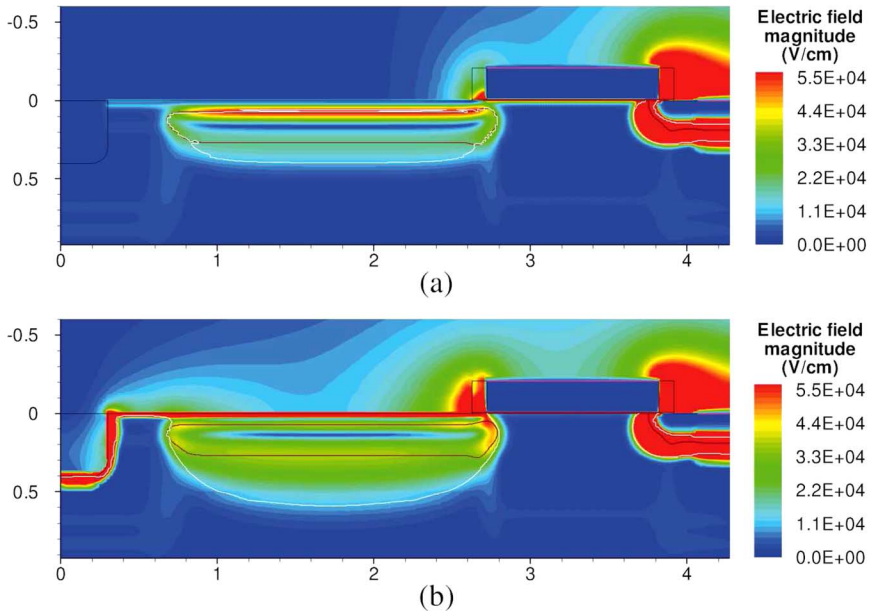

Fig. 17. Transient TCAD simulations, realized right after the reset of the photodiode and illustrating: (a) the distribution of electric field around the unirradiated PPD during integration (b) the degradation mechanism that appears at high TID. This latter simulation has been performed with a trapped charge density $N_{\rm ot} = 1.4 \times 10^{12}$ cm^{-2}. The maximum value on the electric field magnitude scale has been manually fixed to the maximum magnitude in the unirradiated pinned photodiode: 55 kV/cm to reveal the electric field magnitude in the PMD. The photodiode has been emptied in the previous TCAD transient step, and the TG is biased in accumulation (negative gate voltage), as in a real integration phase.

The DC-RTS transition maximum amplitude distributions shown in Fig. 16 exhibit the classical exponential behavior, but with a little change of slope on some of the curves. Moreover contrary to what has been observed in 3T CIS exposed to ionizing and non-ionizing radiation sources [19], [21], there is not a unique exponential slope for all the distributions (it depends on TID, TG bias, and technology). The exponential slope values are between the one reported on 3T CIS exposed to ionizing radiation [19]($\lambda_{\rm TID} \approx 110{\rm e}^-/{\rm s}$) and the one attributed to displacement damages [21] ($\lambda_{\rm DDD} \approx 1200{\rm e}^-/{\rm s}$). It suggests that TID induced DC-RTS in PPD CIS can be as intense as displacement damage induced DC-RTS.

IV. Discussions

A. PPD Degradation Mechanisms

Except for the EQE drop at short wavelengths and the dark current increase that have been discussed previously [4], [6], [8], [10], the other reported degradations require further analysis. TID is known to generate trapped positive charges in dielectrics [22], and this trapped charge density increase has been previously measured in the typical dielectrics that surround the buried photodiode on a similar process [17], [23] (the PMD, the STI, and the gate oxide of "high voltage" (i.e., 3.3V) MOSFET). The PMD trapped charge reduces the effective P doping concentration in the pinning layer (the P+ layer between the PMD and the photodiode in Fig. 1). Thus, the photodiode depletion region extends further toward the PMD interface when the absorbed TID rises leading to an increase of the pinning voltage, as observed in Section III.D.

The PTC clearly shows that the saturation voltage decreases with TID on both technologies, and according to the analysis of Section III.B, this full well variation can only be due to the photodiode or the TG. As mentioned previously, the results presented here strongly suggest that the TG threshold voltage is not modified in the studied TID range, and thus that the channel doping profile and the gate oxide are not degraded. It also shows that the lateral STI do not lead to a Radiation Induced Narrow Channel [17], [24] (RINCE) in these wide MOSFET (≈ 2 μm wide). Hence, the observed full well capacity drop is caused by a degradation of the buried photodiode itself. The amount of charge that can be stored in a PPD can be roughly approximated by $Q = V_{\rm pin} \times C_{\rm PPD}$. We have just seen that $V_{\rm pin}$ increases with TID whereas the full well charge Q decreases. Hence, it can be inferred that the photodiode capacitance $C_{\rm PPD}$ decreases with TID, and more rapidly than the $V_{\rm pin}$ increase. This hypothesis agrees with the suspected vertical depletion width increase. Indeed, as in a classical PN-junction, the $C_{\rm PPD}$ drops when the depletion width increases. Such effect can be explained in the PPD by a two plate capacitor model [15] in which the distance between the two plates would be increased by the TID (once again, due to the reduction of the pinning layer effective doping concentration).

At the highest TID used for this study, the photodiode depletion region reaches the PMD interface and the photodiode is no longer buried as illustrated by the TCAD simulation presented in Fig. 17. This effect was already reported for process induced degradation in PPD [25]. It corresponds to the point where the dark current is dominated by a generation contribution, even with the TG accumulated, and to the point at which a large number of DC-RTS are detected despite the accumulation of the TG. This proposed mechanism is also in good agreement with the CTE evolution with TID on both sensors, as discussed in Section III.C.

B. Effect of Biasing During Irradiation

The other important result is the fact that biasing or not the sensors during irradiation does not influence the TID induced degradation whereas it is well known that CMOS integrated circuits are much more degraded by TID when biased during irradiation [22]. First, it has been shown several times previously in this CIS technology node [9], [26] that the TID induced degradation in 3.3 V MOSFET is negligible and that there is almost no radiation effect on the digital or analog circuits in CIS exposed to ionizing radiation, even after 10 kGy. It corresponds to what is observed on the sensors tested here (on both technologies). Therefore, all the degradations are coming from the photodiode, and from the overlap region of the TG and the photodiode.

One can see in Fig. 17(a) that when the sensor is biased the photodiode electric field does not penetrate the surrounding oxides and that the electric field in the surrounding dielectrics is very low (i.e., well below 1 MV/cm). When the photodiode is not biased, the electric field in the photodiode is lowered, but the electric field in the surrounding oxide is not significantly changed. The transient state simulated corresponds to the beginning of the integration phase when the photodiode is empty (worst case for PPD electric field) and when the TG is accumulated (slightly negatively biased). It should be noticed that if the TG is biased to 0 V during integration, the electric field in the oxide is even lower.

The other case that should be considered is the case when the TG is turned on to transfer the charges. This state lasts about 1 μs to be compared to the time required to readout the pixel array which is longer than 10 ms. It means that the TG is positively biased only 0.01% of the time (this ratio is much lower if an additional integration time is added). Therefore, the sensor is at least 99.99% of the time in a state where there is no significant electric field in the oxides surrounding the photodiode. This is most likely the reason why no effect of biasing during irradiation is seen on these 4T PPD CIS.

V. Summary and Conclusion

Six PPD CIS manufactured in two widely used commercial CIS foundries have been exposed to ionizing radiation and characterized. Several key performances appear to be degraded by the TID. As reported in previous studies, interface state buildup leads to the reduction of the quantum efficiency at short wavelengths and to the increase of dark current (also enhanced by the trapped charge for the highest TID). The dark current degradation is partially mitigated if the transfer gate is placed into accumulation during the integration phase. Despite the fact that no MOSFET was hardened by design, no sign of MOSFET degradation was observed up to 10 kGy. Several original results have also been presented:

- an increase of the pinning voltage with TID,
- a decrease of the photodiode full well capacity, attributed to a drop in photodiode capacitance,
- a large change in charge transfer efficiency attributed to the lowering of potential barrier and the creation of potential pocket in the photodiode/TG overlap region,
- the creation of a large number (almost in all the pixels after 3 kGy) of TID induced dark current RTS centers active in the photodiode, even when the TG is accumulated, and with maximum amplitudes that can reach the typical values of displacement damage induced RTS,
- at the highest TID, the complete depletion of the PMD interface, above the photodiode, leading to large dark current values and the loss of control of the TG on the dark current,
- and the fact that biasing (i.e., operating) the sensor during irradiation does not enhance the degradation compared to sensors grounded during irradiation.

These results have been achieved using a 10 keV X-ray source with a high dose rate, and recent work [27] suggests that CMOS thick oxides such as STI may be degraded up to four times more rapidly if exposed to ^{60}Co with a low dose rate. If this hypothesis is confirmed, it will mean that in these irradiation conditions, the observed degradations could appear at very low TID (possibly below 0.1 kGy and the full depletion of the PMD interface for a few kGy).

The reported results have the following implications:

- it appears necessary to monitor all the PPD characteristics for the accurate evaluation of the radiation hardness of a PPD CIS (i.e., not only the dark current),
- most of the reported degradations come from trapped charges in the PMD and are not likely to be easily mitigated by design techniques,
- biasing PPD CIS during radiation test is preferable, but it does not appear to be strictly necessary since it does not change significantly the electric field magnitude distribution in the dielectrics surrounding the photodiode (and thus the magnitude of the radiation effects),
- since the photodiode electrostatic structure is significantly altered at the highest TID, N-channel PPD CIS may not be suitable for very high TID environment (but P-channel PPD CIS may be [28]),
- TID induced dark current RTS could possibly become a serious limitation for low light level PPD CIS applications in ionizing environment.

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