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Enhanced Radiation-Induced Narrow Channel Effects in Commercial 0.18 μm Bulk Technology

Marc Gaillardin, *Member, IEEE*, Vincent Goiffon, *Member, IEEE*, Sylvain Girard, *Member, IEEE*, Martial Martinez, Pierre Magnan, *Member, IEEE*, and Philippe Paillet, *Senior Member, IEEE*

***Abstract*—Total ionizing dose effects are investigated in input/output transistors that are fabricated by using a commercial 0.18 μm bulk process. An enhanced radiation-induced narrow channel effect is demonstrated in N-type metal–oxide semiconductor (NMOS) and P-type metal–oxide semiconductor (PMOS) transistors, leading to a significant threshold voltage shift which may compromise circuit operations. Calculations using a code dedicated to radiation-induced charge trapping in oxides show that the radiation-induced positive charge trapping in trench oxides leads to the modifications of the electrical characteristics experimentally evidenced. Radiation hardening issues are finally discussed as a function of the device geometry and design.**

***Index Terms*—Deep submicron (DSM) bulk technology, metal–oxide semiconductor (MOS) transistors, radiation-induced narrow channel effect (RINCE), total ionizing dose.**

I. Introduction

INTEGRATED circuits (ICs) for space, scientific, and medical applications must be tolerant of a wide range of total ionizing dose (TID). During the past five years, most TID effects studies were focused on new technologies, such as fully depleted SOI [1]; FinFETs [2]–[4]; FinFlash memories [5], [6]; or metastable dip random-access memory [7]. On the other hand, TID effects are generally not considered a major issue for design hardening in deep submicron (DSM) complementary metal–oxide semiconductor (CMOS) bulk transistors [8], [9]. However, the continuous shrinking of integrated device dimensions leads to an enhanced susceptibility of transistors due to radiation-induced charge trapping in shallow trench isolation (STI) [10], such as STI sidewall leakage currents and radiation-induced narrow channel effects (RINCE), which was demonstrated for high TID ($>$10 Mrad) [11]. Whereas several studies have been dedicated to STI-induced leakage currents in DSM metal–oxide semiconductor field-effect transistors (MOSFETs) [10], [12], [13], few papers have been published on RINCE and on the behavior of irradiated STIs [14], [15]. Moreover, most of the available results have been achieved on core transistors and only few data are available on I/O transistors. This is especially true for PMOS transistors, which are commonly assumed as less sensitive to TID. There are two reasons for this as follows.

1) PMOS transistors are not susceptible to sidewall leakage current.
2) The main TID effect on PMOS transistors is thus related to the radiation-induced charge trapping in the gate oxide, which is strongly limited in low-voltage operation DSM transistors due to the continuous thinning down of the gate oxide with the technology integration.

Even so, it was demonstrated that applications for which narrow transistors are needed, such as CMOS image sensors, based on a bulk DSM technology may be sensitive to a much lower TID ($>$100 krad) [16]. Since such transistors are widely used for I/Os or analog applications, studying their TID behaviors as a function of their geometry and design is thus needed to manage mitigation techniques.

This paper investigates the TID effects in NMOS and PMOS I/O transistors related to the STI. We report NMOS transistor leakage current increase, as usually observed, and unexpected very large RINCE in NMOS and PMOS transistors related to radiation-induced positive charge trapping in STI. The effect of biasing on their degradations is also studied for both MOS transistors types. First, the TID response of the gate oxide is separated to the one of the trench oxide by studying enclosed and open layout transistors, respectively. Then, charge-trapping properties of the STI are analyzed with electrical characteristics measured on field-oxide FETs (FOXFET) along with dedicated self-consistent calculations of charge trapping in the STI on a FOXFET structure. Finally, we discuss the enhanced RINCE sensitivity observed on NMOS and PMOS transistors related to the device geometry and its implications on the radiation hardening of modern CMOS ICs.

II. Experimental Details

A. Test Structures

Elementary transistors were fabricated by using a commercial bulk 0.18 μm process optimized for mixed-signal applications and CMOS image sensors. The I/O transistor manufacturing process involves a gate stack made of a 7-nm-thick SiO_2 gate dielectric (processed using a double gate–oxide growth which is named GO2 in the following text), topped by a highly doped polysilicon gate. Adjacent devices are dielectrically isolated by shallow trench isolations (STI) with a thickness T_{STI} of about 400 nm. NMOS and PMOS transistors with various geometries have been achieved: the device widths W vary between 0.24 and 10 μm and the gate lengths L_G vary between 0.34 and 10 μm.

TABLE I
BIAS CONFIGURATIONS DURING IRRADIATION

NMOS	ON	OFF	NON
V_S	0	0	0
V_D	0	V_{DD}	0
V_G	V_{DD}	0	- V_{DD}
PMOS	**ON**	**OFF**	**NON**
V_S	V_{DD}	V_{DD}	0
V_D	V_{DD}	0	0
V_G	0	V_{DD}	V_{DD}
V_{NWELL}	V_{DD}	V_{DD}	0

All transistors are designed with a standard open layout where the STI circles the entire active silicon area. Additional NMOS transistor designs are also available including one annular enclosed layout transistor (ELT) drawn with the minimum geometric rules and one FOXFET. In the FOXFET, a polysilicon gate is deposited directly on the STI which acts as a thick gate dielectric between two Nwell-doped regions making the source and the drain areas of a large transistor. All devices are mounted in standard pin grid-array packages.

B. Experiments

Each transistor was irradiated at room temperature using 10-keV X-rays at a constant dose rate of 100 $\mathrm{rad(SiO_2)/s}$ to reach a maximum total dose of 1 $\mathrm{Mrad(SiO_2)}$. The total dose was deposited in several irradiation steps which were immediately followed by static electrical measurements performed by using a HP 4145 parametric analyzer. Three different bias configurations were applied to the devices during irradiation: ON, OFF AND NON. They are detailed in Table I where bias applied to source, drain, gate, and Nwell terminals are referenced as V_S, V_D, V_G, and V_{NWELL}, respectively. The substrate is always grounded during irradiation. The nominal bias voltage V_{DD} for I/O transistors is $V_{DD} = 3.3$ V for the studied technology. The NON-bias configuration does not correspond to a conventional circuit case. Above all, it was performed to study the effect of the radiation-induced positive charge-trapping location on the electrical characteristics of MOS transistors. The additional NULL (all terminals grounded) bias configuration during irradiation was also performed on FOXFETs.

III. EXPERIMENTAL RESULTS

Since the mechanisms of radiation-induced charge buildup occur in most oxides [17], we thus must consider the TID response of the gate oxide and of the field oxide of the tested bulk transistors.

A. Contribution of the Gate Oxide to the TID Response of MOS Transistors

Enclosed layout transistors are first characterized under irradiation to infer the sole TID effect on gate–oxide properties. Modification of the electrical characteristics will be only be attributed to the charge buildup in the 7-nm-thick gate oxide. This is justified by the absence of interface between the source-to-drain conduction channel and the trench oxide in the enclosed layout design.

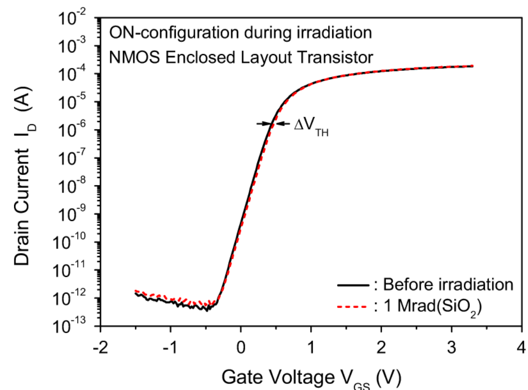

Fig. 1. Drain current I_D versus gate voltage V_{GS} characteristics of an enclosed layout transistor before irradiation (black line) and after 1 $\mathrm{Mrad(SiO_2)}$ (red dashed line).

Fig. 1 exhibits the $I_D - V_{GS}$ curves of the NMOS ELT before irradiation (black line) and after a total dose of 1 $\mathrm{Mrad(SiO_2)}$ (red dashed line). In that case, the device was biased in the ON-state configuration during irradiation. This type of configuration should maximize the positive-charge trapping at the gate–oxide/active silicon interface (only the gate is biased at V_{DD}; the other terminals are grounded). Fig. 1 shows no sufficient radiation-induced change of the electrical characteristics to extract any electrical parameter shift. The radiation-induced charge buildup in the gate oxide can thus be neglected even at a total dose of 1 $\mathrm{Mrad(SiO_2)}$. No significant discrepancy to this behavior was observed under irradiation for the other tested bias configurations. Results obtained on the ELT highlight the weak influence of charge buildup in the 7-nm-thick gate oxide on the electrical characteristics of the tested bulk transistor.

B. Total Ionizing Dose Effects in NMOS Transistors Designed With an Open Layout

Fig. 2 illustrates a series of subthreshold I-V curves measured on a wide [W = 10 μm, Fig. 2(a)] and a narrow [W = 0.24 μm, Fig. 2(b)] open-layout NMOS transistors. These results show that increasing TID leads to the buildup of positive–oxide trapped charges at the Si/STI interfaces. These charges decrease the threshold voltage of the parasitic lateral transistor. This clearly appears as a shoulder on the I-V curves of both transistors of Fig. 2 at a total dose of about 70 krad$(\mathrm{SiO_2})$. This parasitic lateral transistor induces excessive drain leakage current I_{OFF} defined at a gate voltage $V_{GS} = 0$ V. Fig. 3 shows the I_{OFF} variations versus the total dose for 10 μm wide (filled symbols) and 0.24 μm narrow (open symbols) transistors irradiated in the three different bias configurations described in Table I. This figure is evidence that the ON-state corresponds to the worst bias configuration during irradiation considering the occurrence of the parasitic sidewall transistor. This parasitic conduction channel increases the leakage current by about three orders of magnitude after 100 krad$(\mathrm{SiO_2})$. On wide transistors [Figs. 2(a) and 3, black squares], the leakage current reaches a maximum at 500 krad$(\mathrm{SiO_2})$ before decreasing. This phenomenon may be explained by the following mechanisms: the radiation response of the transistor is first dominated by the radiation-induced positive trapped charge in the STI, causing

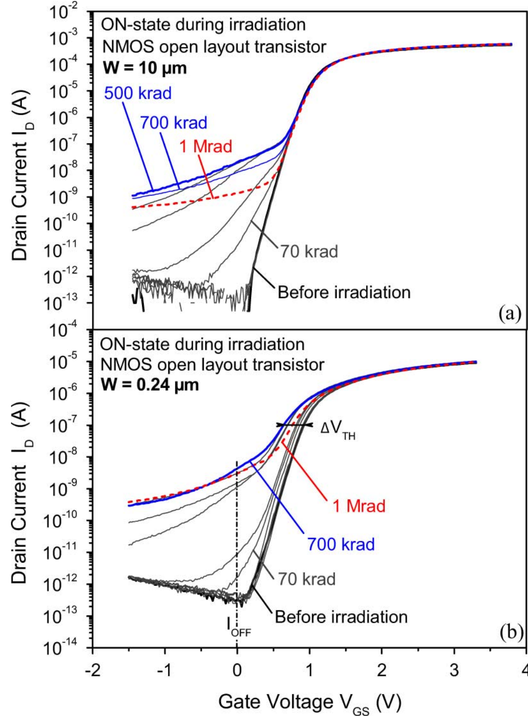

Fig. 2. Drain current versus gate voltage characteristics of NMOS open layout transistors at several total dose steps from before irradiation (bold black line) to 1 $\mathrm{Mrad}(\mathrm{SiO_2})$ (red dashed line). $\mathrm{I_D} - \mathrm{V_{GS}}$ curves are presented for wide transistor with $\mathrm{W} = 10\ \mu\mathrm{m}$ (a) and for a narrow transistor with $\mathrm{W} = 0.24\ \mu\mathrm{m}$. (b). Both transistors have a gate length of $\mathrm{L_G} = 0.34\ \mu\mathrm{m}$.

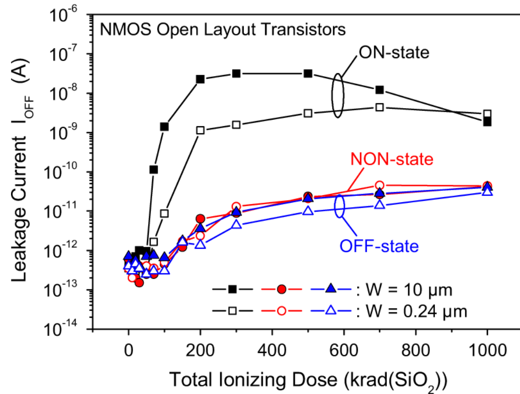

Fig. 3. Leakage current $\mathrm{I_{OFF}}$ as a function of the total ionizing dose for wide ($\mathrm{W} = 10\ \mu\mathrm{m}$, filled symbols) and narrow ($\mathrm{W} = 0.24\ \mu\mathrm{m}$, open symbols) open layout NMOS transistors. The results are displayed for devices irradiated in the ON-state (black squares), the NON-state (red circles), and the OFF-state (blue triangles) bias configurations. All transistors have a gate length $\mathrm{L_G} = 0.34\ \mu\mathrm{m}$.

the occurrence of the parasitic sidewall conduction. For higher TID, this may be counterbalanced by the contribution of the negatively charged interface traps at the silicon/STI interfaces slightly decreasing the leakage current.

Moreover, for a chosen bias configuration, the shapes of the $\mathrm{I_{OFF}}$ versus TID curves exhibit a TID threshold at which the leakage current increases sharply. This suggests that the triggering of the parasitic lateral transistor does not depend on the width of the device but only on the bias configuration used during irradiation. This was previously observed by [11] since

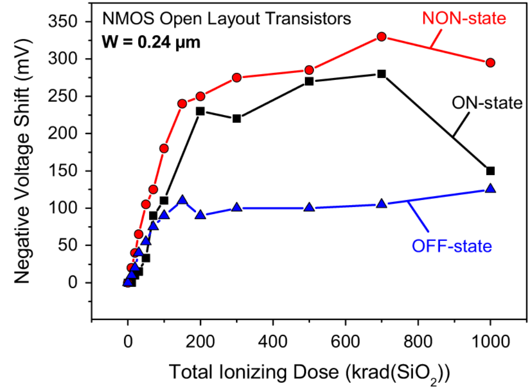

Fig. 4. Negative voltage shift versus total ionizing dose for a narrow ($\mathrm{W} = 0.24\ \mu\mathrm{m}$) open layout NMOS transistors. The results are displayed for the three bias configurations during irradiation described in Table I. All transistors have a gate length of $\mathrm{L_G} = 0.34\ \mu\mathrm{m}$. Results for wide transistors ($\mathrm{W} = 10\ \mu\mathrm{m}$ are not displayed because the variations are negligible.

the parasitic sidewall transistor should be similar to whatever the width of the transistor is.

The negative voltage shifts extracted by using a constant current approach (at low $\mathrm{V_{DS}}$) on narrow NMOS transistors as a function of TID are illustrated in Fig. 4. The results are only presented for narrow transistors ($\mathrm{W} = 0.24\ \mu\mathrm{m}$) since the ones related to the wide transistors ($\mathrm{W} = 10\ \mu\mathrm{m}$) stay within the measurement uncertainties. Here, the response of narrow transistors strongly depends on the bias configuration during irradiation as the location of the positive trapped charges is defined by the shape of the electric-field lines in the trench oxide during irradiation. So, the NON-state and the ON-state appear as the worst cases from the voltage-shift standpoint. In those cases, most of the positive charges generated during irradiation, which have escaped initial recombination, may be trapped at the STI/active-silicon boundaries. Positive charges may be trapped in the entire depth of the trench evenly distributed along the source-to-drain conduction channel. This lowers the source-to-body and body-to-drain potential barriers and then the threshold voltage. This phenomenon is known as RINCE [11]. In our case, this RINCE is very intense with a $\mathrm{V_{TH}}$ shift reaching about 200 mV at a dose of 100 krad$(\mathrm{SiO_2})$ and exceeding 300 mV at larger doses. The gate oxide is not involved in the degradation since wide transistors do not exhibit the RINCE and since no $\Delta\mathrm{V_{TH}}$ is observed in ELT (Fig. 1).

Each characteristic displayed in Fig. 4 shows two major regions. At low dose, below 150 $\mathrm{krad}(\mathrm{SiO_2})$, the negative voltage shift quickly rises, corresponding to an efficient positive charge trapping in the trench oxide which corresponds to the enhanced RINCE. The slopes vary between each bias case during irradiation. This may be due to the various locations and densities of the positive trapped charges in the STI which will be further investigated in Section IV using dedicated self-consistent TCAD calculations of charge trapping. This will provide valuable insights to explain the behavior of open layout transistors.

At higher total ionizing doses, above 150 $\mathrm{krad}(\mathrm{SiO_2})$, each characteristic saturates. This may be due to the buildup of interface traps which are negatively charged in NMOS transistors. This competing mechanism is partly screened at low dose but

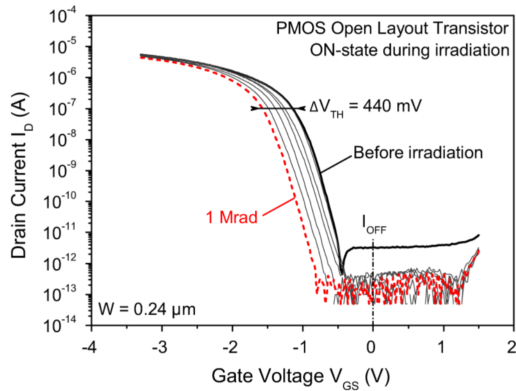

Fig. 5. Drain current versus gate voltage characteristics of the PMOS open layout transistors at several total dose steps from before irradiation (bold black line) up to $1\ \mathrm{Mrad(SiO_2)}$ (red dashed line). $\mathrm{I_D - V_{GS}}$ curves are presented for a narrow transistor with $\mathrm{W} = 0.24\ \mu\mathrm{m}$ biased in the ON-state during irradiation. The gate length is $\mathrm{L_G} = 0.34\ \mu\mathrm{m}$.

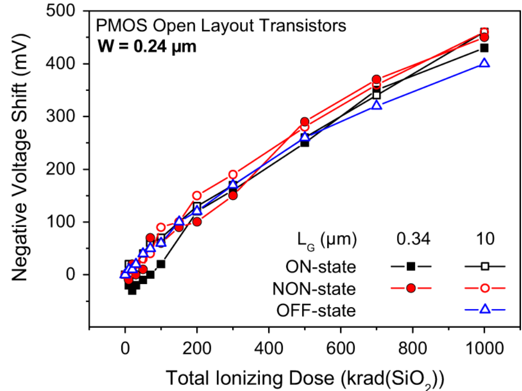

Fig. 6. Negative threshold voltage shift versus total ionizing dose for narrow ($\mathrm{W} = 0.24\ \mu$m) open layout PMOS transistors. Results obtained with two gate lengths are represented: $\mathrm{L_G} = 0.34\ \mu$m (filled symbols) and $\mathrm{L_G} = 10\ \mu$m (open symbols). The results are displayed for the three bias configurations during irradiation described in Table I.

it may counterbalance the positive charge trapping at high total dose. It may also be due to saturation of the hole traps in this part of the STI. Here again, Section IV, which is dedicated to the radiation-induced charge trapping and interface traps in the trench oxide, will provide additional data to obtain new insights on the charge-trapping properties of the STI.

C. Electrical Performance Degradation of Bulk PMOS Transistors

Most studies on the total dose effects on MOS devices focus on NMOS transistors because they are usually the most sensitive device to ionizing radiation, especially for bulk transistors with a thin gate oxide.

Based on the results presented in the previous part, the positive charge trapping in the trench dielectrics should change the electrostatic potential in the PMOS transistor as well as in the NMOS one. This corresponds to what can be inferred from Fig. 5 where the I-V curves obtained on a narrow ($\mathrm{W} = 0.24\ \mu$m) PMOS transistor before irradiation (black line) and after $1\ \mathrm{Mrad(SiO_2)}$ (red dashed line) biased in the ON state are drawn.

A large threshold voltage shift is observed ($\Delta\mathrm{V_{TH}} \approx 440$ mV). To our knowledge, such a threshold voltage variation at $1\ \mathrm{Mrad(SiO_2)}$ on a PMOS transistor with a thin gate oxide has never been reported before. In [11], more than $100\ \mathrm{Mrad(SiO_2)}$ were needed to attain such a threshold voltage shift on PMOS transistors designed with a similar geometry ($\Delta\mathrm{V_{TH}}$, which is limited to 30-40 mV at $1\ \mathrm{Mrad(SiO_2)}$ in [11]).

The threshold voltage shift has been extracted on a narrow PMOS transistor with a gate length $\mathrm{L_G} = 10\ \mu$m (open symbols) and a gate length $\mathrm{L_G} = 0.34\ \mu$m (filled symbols) as a function of total ionizing dose in Fig. 6. All voltage shift versus TID curves follow a similar trend. It clearly does not depend on the gate length and on the bias configuration during irradiation. With radiation-induced charges being positive as well as the interface traps in PMOS transistors, this could explain the overall trend drawn in Fig. 6 in comparison to the behavior observed in Fig. 4.

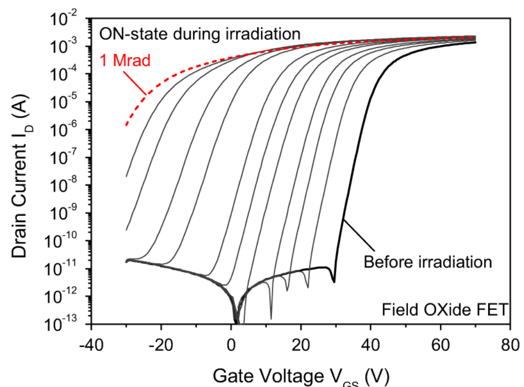

Fig. 7. Drain current $\mathrm{I_D}$ versus gate voltage $\mathrm{V_{GS}}$ characteristics of a FOXFET at several total dose steps from before irradiation (bold black line) to $1\ \mathrm{Mrad(SiO_2)}$ (red dashed line). The FOXFET was irradiated in the ON-state bias configuration during irradiation ($\mathrm{V_G} = \mathrm{V_{DD}}$, other terminals were grounded).

IV. Discussion on the Ionizing Radiation-Induced Effects in Trench Oxides

A. Insights on the Radiation-Induced Charge Trapping in Trench Oxides: FOXFET Characterization

The FOXFET is a convenient tool to characterize the sole radiation-induced charge trapping and interface traps buildup in the field oxide. As described in Section II-A, the FOXFET is a MOS transistor where the STI acts as a gate oxide in which large radiation-induced positive charge trapping should occur. This leads to a large threshold voltage shift in its I-V characteristics (Fig. 7).

The threshold voltage shift observed in Fig. 7 exceeds 50 V after $1\ \mathrm{Mrad(SiO_2)}$. In that case, the electric-field lines start from the gate to reach the STI-silicon interface where most of the radiation-induced positive charges are trapped efficiently, modifying the device response. Using other bias configurations during irradiation should modify the radiation-induced charge-trapping location in the STI. This is illustrated in Fig. 8 where negative threshold voltage shifts observed on the FOXFET are

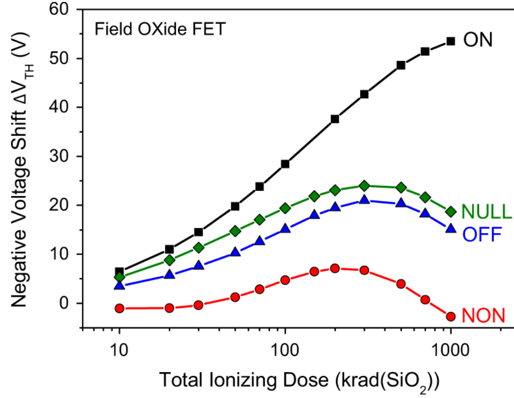

Fig. 8. Negative threshold voltage shift versus total ionizing dose for the FOXFET. Results are displayed for the three bias configurations during irradiation described in Table I: the ON-state (black squares), the OFF-state (blue triangles), and the NON-state (red circles). The additional NULL-state bias configuration (all terminals grounded) performed only on FOXFET is added (green diamonds).

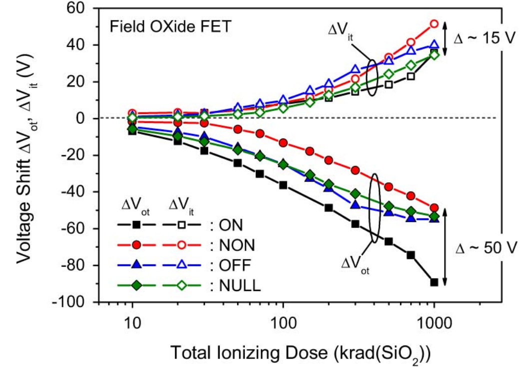

Fig. 9. Voltage shifts versus total ionizing dose associated with the oxide-trapped charges ΔV_{ot} and to the interface traps ΔV_{it} for the FOXFET. Results are displayed for several state bias configurations during irradiation: the ON-state (black squares), the OFF-state (blue triangles), the NON-state (red circles), and the NULL-state.

displayed as a function of total ionizing dose and of the bias configuration during irradiation.

The radiation-induced positive charge-trapping location and density mostly depend on the shape of the electric-field lines in the oxide. The bias configuration during irradiation thus plays a major role in the behavior exhibited in Fig. 8. Results gathered by using the ON-state bias configuration do not exhibit a clear saturation of the radiation-induced voltage shift. By contrast, results obtained using the other bias configurations during irradiation all reach a maximum at about 200 $\mathrm{krad(SiO_2)}$. This classical balance effect between trapped-oxide charges and interface traps is maximized in the NON-state (red circles) for which the net influence of each contribution leads to an apparent threshold voltage shift around zero at 1 $\mathrm{Mrad(SiO_2)}$. This parameter extraction may screen a large increase of the subthreshold slope that degrades the I-V characteristics.

Thus, the contributions related to the oxide trapped charge ΔV_{ot} and to the interface traps ΔV_{it} are now separated [18] in Fig. 9 to weigh up their respective impact on the curves exhibited in Fig. 8. The first interesting feature is that the interface traps contribution ΔV_{it} (in the upper part of Fig. 9) seems less sensitive to the bias state configuration during irradiation than the contribution related to the oxide trapped charge ΔV_{ot} (lower part of Fig. 9). The maximum difference between ΔV_{it} reaches 15 V at 1 $\mathrm{Mrad(SiO_2)}$ between the ON-state (black squares) and the NON-state (red circles) when this difference between ΔV_{ot} values exceeds 50 V at 1 $\mathrm{Mrad(SiO_2)}$. If the large discrepancies measured between ΔV_{ot} would have been expected as a function of the bias configuration during irradiation, it is not straightforward concerning those related to ΔV_{it}. It is especially true for voltage shift observed using the NON-state for which a negative bias is applied on the gate electrode. In that case, one could expect that no buildup of an interface trap should occur.

The TID effects on MOS structures were widely studied in the literature [19]–[26], including the mechanisms responsible for the generation of interface traps under irradiation [27]–[31]. Even if the details of the interface traps generation still need to be investigated, especially in thick oxides, a consensus was reached on the overall physical mechanisms which govern the buildup of interface traps at silicon/oxide interfaces under irradiation. First, it is not directly caused by ionizing radiations themselves but that they follow successive phenomena [17]. In some manner, protons are first liberated during hole transport. Then, the protons drift to the silicon/oxide interface where they may react with hydrogen atoms of passivated silicon dangling bonds. The reaction results in one $\mathrm{Si^+}$ defect, the interface trap, in addition to a $\mathrm{H_2}$ molecule. This formalism assumes that the interface traps buildup is bias dependent and that no (or few) interface traps may be created at the silicon/oxide interface under negative bias.

However, [32] has demonstrated a buildup of the interface traps under low negative electric fields across an oxide. In such a case, it is assumed that the $\mathrm{H^+}$ transport across the oxide is no longer driven by the externally applied electric field on the electrodes but by the electric field induced by the nonuniform radiation-induced positive charge trapping in the oxide itself. In other words, the field due to the oxide-trap charge exceeds the one related to the external bias. Extractions of ΔV_{it} displayed in Fig. 9 seem to point out such a behavior. Data gathered using the NON-state bias during irradiation (red circles, $-V_{DD}$ on the gate electrode) clearly exhibit a significant voltage shift due to the buildup of interface traps at the silicon/oxide interface. It is even the largest ΔV_{it} extracted for the highest total ionizing doses.

The bias applied across the 400-nm-thick oxide corresponds to an electric field just below 0.1 MV/cm ($hbox 8.25 \times 10^{-2}$ MV/cm). It thus seems reasonable to consider that the generation, transport, and trapping of positive charges in the oxide bulk due to ionizing radiation induce a more intense electric field than the one related to the external bias. Calculations of charge trapping using a dedicated self consistent code are thus necessary to investigate the radiation-induced oxide charge trapping more deeply as well as the interface traps buildup in thick oxides.

B. Investigations on the Oxide Charge Trapping in FOXFETS Using Dedicated Self-Consistent Calculations

Dedicated TCAD simulations were performed to calculate the nonuniform radiation-induced positive charge trapping in

the oxide of the FOXFET. These simulations will help to understand the mechanisms governing the experimentally observed (Fig. 9) dependence of ΔV_{ot} with the bias configuration during irradiation.

The simulated structure is representative of the $0.18\ \mu$m bulk technology in terms of geometry and doping levels. The gate oxide made of a traditional trench oxide has a thickness of 400 nm. The effective gate length of the FOXFET is about 700 nm. Highly doped regions are formed using standard diffusion processes, and an n-type polysilicon gate is deposited on the thick oxide to conclude the FOXFET fabrication process.

Numerical simulations were performed using Sentaurus Device Radiation [33], a self-consistent code dedicated to TID effects. This code is used here to calculate the radiation-induced hole trapping in the FOXFET's gate oxide. Poisson and carrier continuity equations are involved in the modeling of the transport of radiation-generated charges in the oxide. A set of parameters validated for thermal SiO_2 is used here as well on the trench oxide. Simulation parameters include a uniform trap density $N_{tp} = 10^{18}$ cm^{-3} and a hole capture cross-section $\sigma_{pt} = 6.8 \times 10^{-14}$ cm^{-2}. The effective hole mobility is set at $\mu_p = 10^{-5}$ cm^2/V.s, and the one related to the electrons is set at $\mu_n = hbox20$ cm^2/V.s in the oxide. The cross-section for electron recombination on the trapped holes is $\sigma_{pr} = 10^{-12}$ cm^2.

Using this set of parameters, we assume that the simulated oxide charge-trapping properties of the trench oxide, notably in terms of trapping cross sections, are close to those of a thermal SiO_2. Obviously, these parameters may differ because of the nature of the dielectric. However, the simulations performed here will give insights on the oxide charge-trapping profiles which remain governed by the shapes of the electric-field lines and of the current flows in the oxide. Thus, the electron-hole pairs generated in the insulator during irradiation are separated by the local electric field. Electrons are rapidly evacuated because of their highly effective mobility. Holes follow the local electric-field lines in the oxide and get trapped close to the silicon/oxide interfaces.

The shape of the electric-field lines is first calculated as a function of the bias configuration before irradiation. The result of this simulation is displayed in Fig. 10 where the isopotential lines are drawn for the ON-state [Fig. 10(a)], the NULL-state [Fig. 10(b)], the OFF-state [Fig. 10(c)], and the NON-state [Fig. 10(d)]. The white arrows perpendicular to the isopotential curves depict the electric field. Fig. 11 shows the resulting radiation-induced hole trapping after a $1\ \mathrm{Mrad(SiO_2)}$ total ionizing dose exposure following the same bias conditions during irradiation, respectively.

In the ON-state [Fig. 10(a)], the electric-field lines originating from the gate reach directly to the silicon channel/oxide interface where the radiation-induced charges can be mostly trapped [Fig. 11(a)]. The electrostatic potential in the silicon is thus efficiently modified inducing the threshold voltage shift ΔV_{ot} observed in Fig. 9 (over 50 V after $1\ \mathrm{Mrad(SiO_2)}$).

In the OFF state [Fig. 10(b)], the electric-field lines leave the drain to mainly reach either the gate/oxide interface of the silicon/oxide interface. This leads to a high concentration of trapped holes in these areas [Fig. 11(b)], which locally exceeds the one obtained in the ON-state. However, despite the high

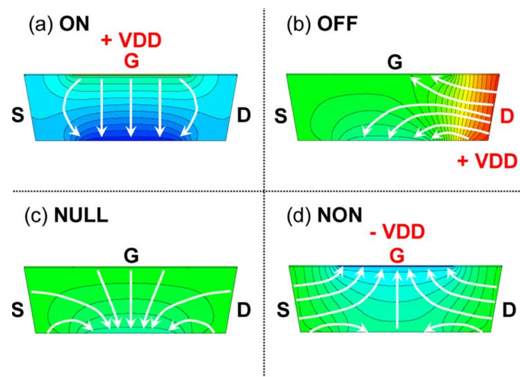

Fig. 10. Simulated electrostatic potential in the oxide of the FOXFET in the (a)ON-state, (b) the OFF-state, (c) the NULL-state, and (d) NON-state before irradiation. The arrows correspond to the shape of the electric-field lines.

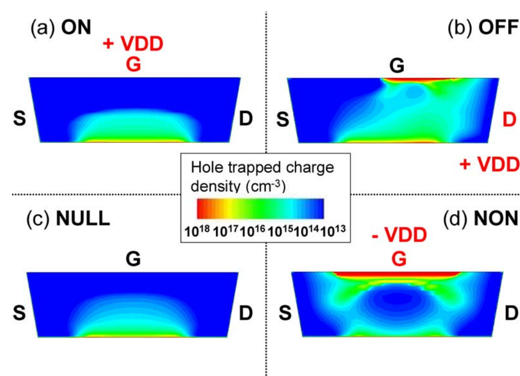

Fig. 11. Simulated radiation-induced hole trapped charge in the 400-nm-thick gate oxide of the FOXFET. Hole-trapped charge profiles are calculated according to the same bias configurations as in Fig. 10.

concentration, the radiation-induced hole trapped charge is not enough evenly distributed along the conduction channel. The surface potential in the silicon is not sufficiently modified to imply a similar voltage shift ΔV_{ot} than the one observed in the ON-state.

In the NULL-state [Fig. 10(c)], all terminals are grounded during irradiation. Electrostatic potential drops are thus only due to doping gradients. This leads to similar shapes of electric field lines as the one observed in the OFF-state. Only the maximum value of the electric field is lowered. The radiation-induced hole trapped charges are consequently mainly located at the silicon/oxide interface but with lower densities [Fig. 11(c)].

Finally, the NON-state [Fig. 10(d)] corresponds to the exact opposite bias case to the ON-state. The electric-field lines point directly to the gate electrode where most of the radiation-induced charges are trapped. At the source/bulk and drain/bulk junctions, some electric-field lines also leave the source and drain to reach the bulk silicon due to the potential drops at PN junctions (such as in the NULL-state). This may explain the more complex hole trapped charge profile obtained in this bias case during irradiation [Fig. 11(d)]. Most of the radiation-induced trapped holes are located directly at the gate/oxide interface far from the silicon/oxide interface. At the beginning of the irradiation, the holes trapped at the silicon/oxide interface are only due to the few electric-field lines originating from the source and drain. For higher total ionizing doses, the effect of

the gate bias is gradually weakened. This is due to the strong buildup of the positive oxide trap charge directly at the gate/oxide interface supporting the reversal of the electric field in this region. To summarize, most of the radiation-induced trapped holes are far from the silicon/oxide interface, impacting the surface potential in the silicon less and then the device electrical characteristics.

C. Discussion on the Effect of Bias on the Buildup of Interface Traps in Trench Oxides

Assuming the hole-trapped charge profiles calculated in Fig. 11, the low external electric field due to the external bias applied on the electrodes during irradiation may be much lower than the one induced by the positive charge buildup in the oxide bulk. The shape of the electric field in the oxide can be sufficiently modified to induce the transport of protons liberated during hole transport to silicon/oxide interfaces where they may generate interface traps, even in negative bias conditions during irradiation (NON-state [Fig. 11(d)]. TCAD calculations performed in the NON-state show such an electric field reversal through the STI at high TID. So, as already proposed in [32], this electric-field modification may support the increase of the contribution related to the interface traps ΔV_{it}, cancelling the oxide-trapped charges contribution ΔV_{ot} on the apparent threshold voltage shift ΔV_{TH} observed in Fig. 8 (red circles). This point needs to be further investigated to be completely clarified. To do so, experiments using various negative biases should be carried on in addition to postirradiation anneals in order to maximize the relative contribution of the interface traps over the one related to the oxide-trapped charges.

V. Trends on the RINCE in I/O Transistors

After discussing the properties of the trench oxide via the characterization and modelling of a dedicated structure, the FOXFET, this section now focuses on the effect of the oxide traps in shallow trench isolations on the electrical characteristics of typical I/O transistors (using the GO2 option) based on a bulk 0.18 μm CMOS process.

A. Trends on the Radiation-Induced Narrow Channel Effects in I/O Transistors

3-D TCAD simulations were performed on an NMOS I/O transistor structure encapsulated in STI with various device widths. Simulations were carried on in the ON-state bias configuration during irradiation. Based on the results of Section IV-B on the FOXFET and on the shape of the electric-field lines in the STI under a positive bias on the gate electrode, the hole-trapped charge is distributed at the STI/silicon interface along the conduction channel. Furthermore, trapped charges are spread in the entire thickness of the STI down to the bottom of the source and drain regions. The same simulation would have been performed in the NON-state using a trapped charge distribution always evenly distributed along the conduction channel but mainly located in the upper part of the STI (e.g., at the gate-STI-silicon corner). Since the hole-trapped charge in the STI does not depend on the width of the transistor, the same amount of charge is applied at the STI/silicon interfaces whatever the width of the simulated transistor is.

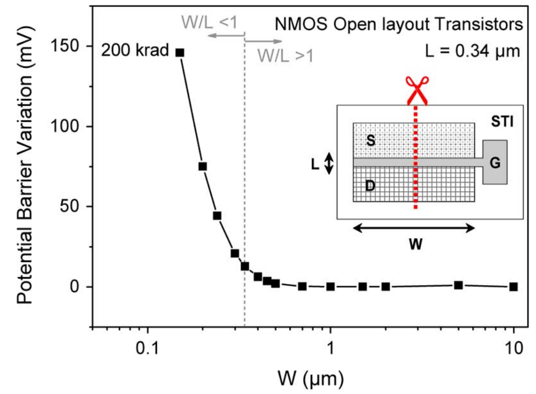

Fig. 12. Simulated source-channel potential barrier variation in the silicon, at the silicon/gate–oxide interface, in the source-drain axis. The curves are probed in the middle of the transistor width which varies from 0.15 μm ($W/L \approx 0.44$) to 10 μm ($W/L \approx 30$). The gate length is fixed at 0.34 μm. A sheet density of charges corresponding to a 200 krad(SiO_2) irradiation is applied at the STI/silicon interface in each case.

Fig. 12 exhibits the simulated source-to-channel potential barrier drop in the middle of the transistor width. This parameter is extracted for several transistors' width giving a picture of the RINCE. Potential barriers are probed at the exact same distance of both lateral STIs. This corresponds to the minimum electrostatic potential variation in the conduction channel area induced by the trapped charges in the STI. The potential barrier drop will be larger when probing it closer to the silicon/STI interface.

In wide transistors ($W/L \gg 1$), trapped holes at the STI/silicon interfaces can efficiently modify the electrostatic potential only in the area where they are trapped, inducing the STI sidewall leakage current in NMOS transistors. However, they do not have a sufficient "range of action" to degrade the potential well in the whole width of the transistor. The source-to-drain potential barrier height in the middle of the transistor width remains sufficiently high to avoid any threshold voltage shift of the main transistor as observed in Fig. 2(a). However, the parasitic conduction at the edges of the transistor remains active with increasing TID (not shown here).

In narrow transistors ($W/L \leq 1$), the radiation-induced positive trapped charges in the STI strongly lower the source-to-drain potential barrier in the active silicon even in the middle of the transistor's width. The STI trapped charges induce a lowering of the potential barrier in the entire width of the transistor. In other words, the narrow transistor may be modelled as a series of only few discrete elementary transistors in parallel across the gate width (by contrast, the wide transistor may be modelled using a series of a large number of such discrete elementary transistors). Thus, the trapped charge in the STI is sufficient to induce an efficient potential drop in all of these elementary transistors. So the main transistor which is modelled by the sum of each discrete elementary transistor is thus strongly affected by this potential drop which results in the threshold voltage shift observed in Figs. 2(b) and 4. Conversely, for the wide channel case, the potential drop does not extend across the entire gate width, less impacting the device response. Similar interpretations can be made for PMOS transistors. They only play a role on parasitic sidewall conduction. Here, however, it is shifted far

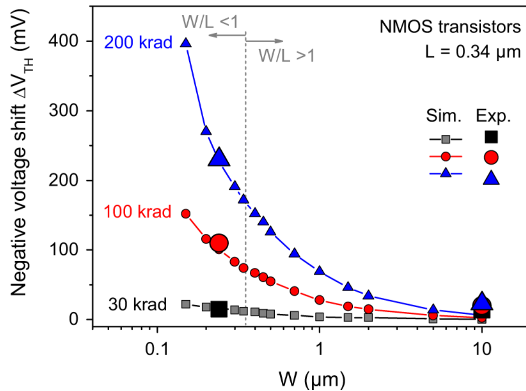

Fig. 13. Simulated threshold voltage shift ΔV_{TH} on NMOS transistors as a function of the transistor geometry expressed as the transistor's width. Results are shown for three levels of total ionizing dose: 30 krad(SiO_2) (black squares), 100 krad(SiO_2) (red circles), and 200 krad(SiO_2) (blue triangles). Experimental data are added by using large symbols.

from the main PMOS transistor without significantly changing its electrical characteristic.

In contrast, as already observed in NMOS transistors, the reduction of the transistor width enhances the effect of the trapped charge in the STI on the electrostatic potential in the entire width of the transistor. Furthermore, the contribution of the positively charged interface traps strengthens the threshold voltage shift instead of limiting it in NMOS transistors explaining the large RINCE depicted in Figs. 5 and 6.

B. Implications for Circuit Design for Radiation Hardening of ICs Based on COTS Technology

For each simulated transistor, the threshold voltage shifts induced by the positive charges trapped at the STI/silicon interface were extracted to gain additional insights on the ionizing radiation sensitivity of such transistors related to their geometries. Calculated ΔV_{TH} results are summarized in Fig. 13 as a function of the transistor's width W at various levels of positive charge densities (e.g., total ionizing dose) Simulations are compared to experimental results (added using large symbols). Fig. 13 reveals good agreement between simulations and experiments.

In Fig. 13, the gate length is fixed at the nominal value for I/O transistors of this technology $L = 0.34\ \mu m$. The transistor width W is thus the sole variable parameter. We choose to indicate the corresponding W/L ratio in order to keep in mind that analog circuit designers generally avoid using the W/L ratio smaller than one. However, specific applications, such as CMOS image sensors, need smaller W/L ratios to improve the integration of the electronic part close to the photodetection part.

This graph exhibits a clear trend on the radiation-induced narrow channel effect as a function of the transistor geometry. The smaller the transistor's width, the higher the transistor sensitivity to ionizing radiation is. Such a trend is very close for PMOS transistors. Core transistors (GO1) from the same technology are most probably not as sensitive as transistors designed using the GO2 option of the technology. Since core transistors use an extremely thin gate oxide, the gate electrode has a much stronger capacitive control of the electrical potential over the conduction channel. But depending on the doping concentration in the channel region and on the transistor's design, a RINCE may also be observed and it needs further investigation to be extensively quantified. However, GO2 transistors are widely used for analog applications, I/Os, and optoelectronic devices, such as CMOS image sensors. In the worst case, this set of data shows that the RINCE may imply significant threshold voltage shifts for relatively low TID (about 150 mV at 100 krad, and about 400 mV at 200 krad), both on NMOS and PMOS transistors. This should be taken into account to manage a hardening strategy to design radiation-tolerant circuits based on COTS technology within the requirements of the intended radiative environment. Furthermore, these values of threshold voltage shifts may be easily introduced in circuit simulations to predict the sensitivity to ionizing radiation of elementary cells. This approach would help one to adjust the mitigation strategies for the radiation hardening by the design of ICs.

VI. Conclusion

We demonstrate that charge trapping in trench oxides induces an unexpected enhanced radiation-induced narrow channel effect in bulk transistors used in I/O and analog circuits. A weaker RINCE was already observed in NMOS transistors by [11]. However, strong unexpected modifications of PMOS transistors' characteristics are exhibited. They may compromise circuit hardening if this phenomenon is neglected in the radiation hardening by design strategy. Investigations on the charge-trapping properties of shallow trench isolations using the FOXFET are discussed by using experiments along with dedicated self-consistent calculations of charge trapping in oxides. The dependence of the voltage shifts with the bias configuration used during irradiation is discussed related to the oxide-trapped charge and to the interface traps. Insights into the effect of the charge-trapping location on the electrostatic potential modifications induced inside the active silicon are reported. From these data obtained on the trench oxide, 3-D TCAD simulations were then performed on nominal transistors to understand the physical mechanisms leading to the enhanced radiation-induced narrow channel effect as evidenced on experiments. Finally, calculations were conducted to draw trends on the radiation sensitivity of elementary devices as a function of their geometries to discuss the radiation hardening by design issues on GO2 transistors optimized for analog, I/O, and optoelectronic applications.

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