URL: http://dx.doi.org/10.1109/TNS.2011.2171502

Generic Radiation Hardened Photodiode Layouts for Deep Submicron CMOS Image Sensor Processes

V. Goiffon, *Member, IEEE,* P. Cervantes, C. Virmontois, *Student Member, IEEE,* F. Corbière, P. Magnan, *Member, IEEE,* M. Estribeau, *Member, IEEE*

***Abstract*—Selected radiation hardened photodiode layouts, manufactured in a deep submicron CMOS Image Sensor technology, are irradiated by ^{60}Co γ-rays up to 2.2 Mrad(SiO_2) and studied in order to identify the most efficient structures and the guidelines (recess distance, bias voltage) to follow to make them work efficiently in such technology. To do so, both photodiode arrays and active pixel sensors are used. After 2.2 Mrad(SiO_2), the studied sensors are fully functional and most of the radiation hardened photodiodes exhibit radiation induced dark current values more than one order of magnitude lower than the standard photodiode.**

***Index Terms*—CMOS Image Sensors, CIS, Active Pixel Sensors, APS, Monolithic Active Pixel Sensor, MAPS, Ionizing Radiation, Total Ionizing Dose, TID, Dark current, Radiation Hardening By Design, RHBD, Interface states, Trapped charge, Shallow Trench Isolation, STI, Deep Submicron Processes, DSM.**

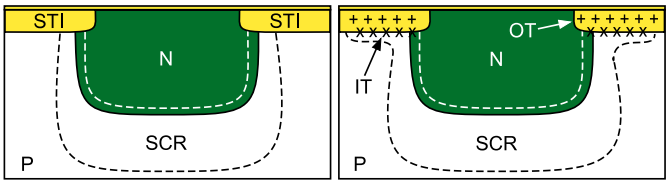
I. Introduction

MOST of the early developments of Active Pixel Sensor (APS) technology, also called CMOS Image Sensor (CIS) technology, have been realized in the frame of space applications [1]. The ionizing radiation hardness of CMOS imagers soon became an important topic and the first radiation hardened pixel layouts were proposed in the late 90's [2]. Whereas transistor related issues can be mitigated by the use of classical hardening techniques [3] (i.e. Enclosed Layout Transistor (ELT) or P-channel transistors instead of N-channel transistors), photodiode radiation hardening has always been a major challenge, especially to reduce the ionizing radiation induced dark current increase. Hancock *et al.* first improved the photodiode radiation hardness of APS by using Enclosed Layout N+ photoDiode (ELD) in 1997 [2] in a 1.2 μm process. In 2001 they proposed the surround gate (or gated), implant setback (or recessed field oxide) and silicide bounded N+ photodiode layouts [4] and tested them in a 0.5 μm process. At that time, they pointed out the need to apply a negative bias on the surround gate to reach the accumulation regime and prevent the depletion region from reaching the field oxide. However, no data were given about the influence of gate bias on the dark current evolution. A few years later [5], they evaluated the radiation hardness of the surround gate N_{well} photodiode in a standard Deep SubMicron (DSM) CMOS process (0.25 μm) which used Shallow Trench Isolation (STI) instead of a LOCOS field oxide. They also tested with good results the use of a P+ guard ring to stop field oxide inversion induced leakage. In 2002, the idea of surrounding the N_{well} photodiode by a P+ implant (surround P+ diode) was introduced [6] but with no reported supporting data. Bogaerts *et al.* [7] achieved very good photodiode radiation hardness in 0.7, 0.5 and 0.35 μm CMOS processes, but with the use of a surface P+ implant resulting from a custom process modification that is not available in standard CMOS processes. In the late 2000's, dark current increase improvements achieved by the use of N_{well} gated photodiodes (grounded in [8], [9] but terminated by a P+ ring, and with no bias information in [10]) were briefly reported in LOCOS based 0.35 μm technology. At the same time, the radiation responses of gated, recessed field oxide and P+ surround photodiodes (with no recess distance) were studied [11] in a DSM (0.18 μm) CMOS process dedicated to CIS (also called CIS process).

CIS are used in a growing number of applications requiring radiation hardness (space, scientific, medical, industrial and military applications). Nevertheless, despite the previously mentioned efforts, there is no clearly identified photodiode layout today, compatible with any DSM CMOS process (dedicated to CIS or not and with no additional custom step), that will lead for sure to an improved radiation hardness for a large Total Ionizing Dose (TID) range. Indeed, most of the work cited previously has been performed on LOCOS based technology, and most often on N+ diodes. Moreover, the best structure is not the same from one technology to another (and also from one work to another mainly because the tested structures are usually not the same) and these discrepancies are very rarely discussed. Worse, in the case of DSM CMOS technologies, there are several ways to implement all these structures, such as the distance between the STI, or the gate, and the junction or the choice of gate bias. To our knowledge, the effects of such parameters have not been studied before.

In this work we propose to study selected TID radiation hardened photodiode layouts, manufactured in a DSM CMOS image sensor technology, in order to identify the best structures and the guidelines to follow (recess distance, bias voltage) to make them work efficiently in such technology. To do so, and to improve our understanding of hardened photodiode behaviors, we use both photodiode arrays (i.e. isolated photodiodes connected in parallel) and APSs. The former are used to analyze in detail the behavior of each diode by performing I-V measurements whereas the latter provide statistical dark current characteristics and allow the evaluation of in-pixel gain variations. The selected TID range (up to a

V. Goiffon, P. Cervantes, C. Virmontois, F. Corbière, P. Magnan and M. Estribeau are with Université de Toulouse, ISAE, Image Sensor Research Team, Toulouse, 31055, France (Phone: +33 5 6133 8093, Fax: +33 4 6133 8345, e-mail: vincent.goiffon@isae.fr).



(a) (b)

Fig. 1. Illustration of TID effects on conventional CIS photodiodes: photodiode cross-section (a) before and (b) after exposure to ionizing radiation. The radiation induced positive trapped charges (OT) and interface states (IT) that play a role in the degradation are indicated in (b). SCR = Space Charge Region.

few Mrad(SiO_2) covers space and medical applications but also many scientific (e.g. nuclear and particle physics) and industrial (e.g. nuclear power plant monitoring, electron microscopy, etc.) applications. Despite the fact this work focuses on TID effects only, it should be emphasized that displacement damage effects [12] can add to the TID degradation in several radiation environments (e.g. in space where particles such as protons induce displacement damage) generally leading to hot pixel generation.

II. Radiation Hardened Designs

A. TID effects in CIS: starting hypothesis

Previous studies on TID effects on 3T CIS manufactured using DMS CIS processes [11], [13]–[15] have shown that the main TID induced degradation is an increase of the average level of dark current, whatever the considered particle (X-rays, ^{60}Co γ-rays or protons[1]). Based upon the circuit level analyses presented in [11], [14], it has been demonstrated that the photodiode was the dominant contributor to this TID induced average dark current increase. The corresponding model for the effects of photodiode dark current is shown in Fig. 2. The current source representing dark current acts to discharge the photodiode capacitance (leading to a reduction of the sensor dynamic range). The remaining part of the circuit exhibits little degradation up to 500 krad(SiO_2) (although there is variation of the maximum output voltage swing and the gain) that can easily be mitigated by using ELTs in the pixel [3], [14]. The first step to improve the radiation hardness of CIS against TID is therefore to mitigate the TID induced dark current increase of the photodiode.

The photodiode junction perimeter P_j has been clearly identified as the main source of ionizing radiation induced dark current increase in conventional CIS photodiodes [2], [4], [5], [11]. The role of trapped charge density ($N_{\rm ot}$) and interface state density ($N_{\rm it}$) in this degradation has been recently discriminated [15] and can be summarized by the following equation when the dominant mechanism is the Shockley-Read-Hall (SRH) Recombination-Generation (R-G) mechanism (i.e. for magnitudes of electric field lower than a few 10^4 V/cm):

$$I_{\rm SRH} = K P_j W_{\rm ox} N_{\rm it} \exp\left(\frac{-E_g}{2kT}\right), \qquad (1)$$

[1]As mentioned in the introduction, proton irradiation also induces displacement damage effects (such as the creation of hot pixels) that are not considered in this paper.

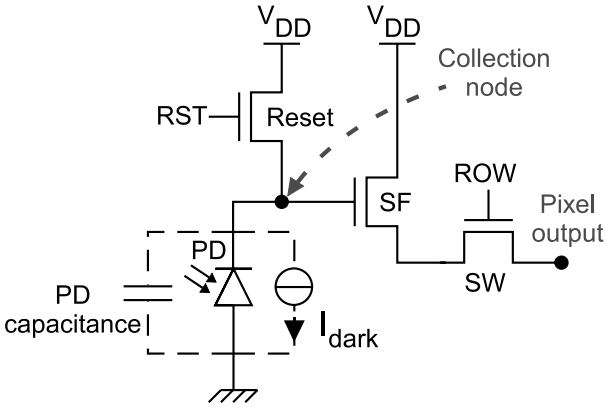


Fig. 2. 3T pixel schematic showing the parasitic dark current ($I_{\rm dark}$) path that discharges the photodiode capacitance during integration. PD = PhotoDiode, SF = Source Follower, SW = row selection SWitch, RST = ReSeT.

with $W_{\rm ox}$ the depletion width at the oxide interface and K a proportionality factor weakly dependent on temperature in comparison to the exponential factor. This radiation induced dark current increase is directly proportional to the number of active interface states, acting as SRH R-G centers, in the photodiode depletion region. Hence, CIS dark current rises with the radiation induced interface state density increase, $\Delta N_{\rm it}$. In addition to this phenomenon, radiation induced trapped charge density increases, $\Delta N_{\rm ot}$, can enhance the degradation by extending the depletion width at the STI interface, $W_{\rm ox}$, as illustrated in Fig. 1. This results in a larger number of active interface states in the photodiode depletion region.

B. TID hardened design selection

With this degradation process in mind, two effects have to be mitigated: the interface state density increase in the depletion region and the trapped charge induced depletion region extension. The interface state density increase can possibly be reduced by changing the oxide located on the photodiode perimeter. Gate oxides are supposed to exhibit a much lower $\Delta N_{\rm it}$ than the STI oxides, and the silicon/oxide interface located below the Pre-Metal Dielectric (PMD) oxide layer (most likely an HPCVD silicide block oxide layer) appears to induce less $\Delta N_{\rm it}$ with TID than the STI oxide [15]. Therefore, in all the selected radiation hardened structures the STI has been recessed away from the photodiode junction (as shown in Fig. 3). Standard CMOS manufacturing processes offer more efficient ways to deal with the depletion region extension at the oxide interface by controlling the surface potential: surface shallow implants and polysilicon gate. According to these possibilities, three types of radiation hardened photodiode layout have been selected: Recessed STI (RSTI), Surround P+ implant (SP+) and Gated photodiodes. In contrast to most of the radiation hardened gated photodiodes studied previously (N+ photodiode with the polysilicon gate self-aligned to the N+ implant), the STI, the polysilicon gate and the surface P+

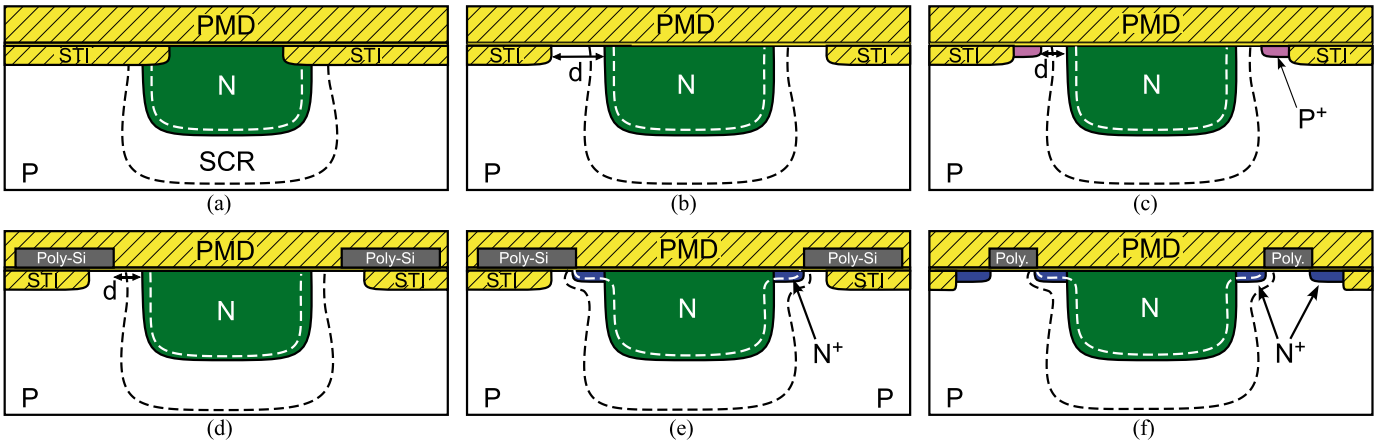


Fig. 3. Simplified cross sections of the manufactured photodiodes. (a) Standard photodiode (STD). (b) Recessed STI (RSTI) photodiode. (c) Surround P+ (SP+) photodiode. The distance d is defined between the junction and the STI (and the P+ diffusion respectively). (d) and (e): Gated photodiodes. In (d), d is defined between the junction and the beginning of the polysilicon gate. In (e), an N+ diffusion is used to separate the gate and the photodiode (Gated N+ diode). (f) Enclosed layout photodiode (ELD).

implants are not self-aligned to the photodiode sensor N_{well} in CIS processes. Therefore several distances d have been drawn between the as-drawn photodiode layer and the as-drawn STI (or gate or P+ implant) layer. Minimum recess distances have been used in previous work [11], [14] and lead to poor results due to high electric field effects. RSTI photodiodes (Fig. 3b) are expected to lead to improved radiation hardness only because the PMD layer is supposed to exhibit lower ΔN_{it} and ΔN_{ot} with TID. SP+ (Fig. 3c) and Gated (Fig. 3d, e and f) photodiodes are supposed to prevent the surface depletion width extension. In the Gated photodiode set of structures, two self-aligned versions are drawn: the Gated-N+ (Fig. 3e) and the Enclosed Layout Diode (ELD) (Fig. 3f). In both cases the sensor N_{well} is extended by an N+ implant which is self-aligned to the polysilicon gate. In the case of the ELD, the gate itself is surrounded by another N+ shallow implant as in an ELT. The studied structures are summarized in Table I. It should be emphasized that P+ guard rings are not used to prevent field oxide inversion, since the proposed structures (except the RSTI ones) are supposed to prevent the inversion layer from reaching the field oxide.

TABLE I
SUMMARY OF THE STUDIED PHOTODIODE LAYOUTS. SA STANDS FOR SELF-ALIGNED.

Name	Type	d (µm)
STD	Standard	-
RSTI 0.5	Recessed STI FOX	0.5
RSTI 1.0	Recessed STI FOX	1.0
RSTI 2.0	Recessed STI FOX	2.0
SP+ 0.1	Surround P+ implant	0.1
SP+ 0.2	Surround P+ implant	0.2
SP+ 0.3	Surround P+ implant	0.3
SP+ 0.5	Surround P+ implant	0.5
Gated 0.1	Gated photodiode	0.1
Gated 0.2	Gated photodiode	0.2
Gated 0.3	Gated photodiode	0.3
Gated 0.5	Gated photodiode	0.5
Gated N+	Gated photodiode	SA
ELD	Enclosed Layout Diode	SA

III. EXPERIMENTAL DETAILS

Two APSs, constituted by 128x128 10-μm-pitch 3T-pixels, have been designed and manufactured using a commercial $0.18\ \mu m$ CMOS process dedicated to imaging applications. The active pixel arrays are divided into 32x32 pixel areas which only differ by their photodiode layout (summarized in Table I). Conversion factors (CVF) were determined using the classical Mean-Variance method [16]. Pre-irradiation CVFs are around $16\ \mu V/e^-$ for STD photodiodes, $9\ \mu V/e^-$ for Gated N+ and ELD photodiodes and $12\ \mu V/e^-$ for all the other pixels. The CVF is related to the collection node capacitance through:

$$\mathrm{CVF} = \frac{q}{C_{\mathrm{CN}}} \times G_{\mathrm{RD}}\ , \qquad (2)$$

where q is the elementary charge, G_{RD} the gain of the readout chain from the in-pixel source follower to the output PMOS stage (further description of the readout chain can be found in [14]) and $C_{\mathrm{CN}} = C_{\mathrm{PD}} + C_{\mathrm{P}}$. The parameter C_{PD} is the photodiode capacitance (mainly due to the depletion volume around the junction), and C_{P} is the parasitic collection node capacitance without the photodiode capacitance (mainly the addition of the source follower MOSFET gate capacitance, the reset MOSFET source capacitance and the interconnection capacitance). Since all the pixels have the same readout chain (including the same in-pixel transistor designs), it is important to notice that the only parameter that can vary from one design to another is the photodiode capacitance. Therefore, it can be seen that recessing the oxide increases the photodiode capacitance. This is due to the sidewall junction height which is greater when the STI is recessed. In this case the sidewall capacitance is significantly increased leading to the observed

effect. In addition to this effect, the Gated N+ and ELD pixels exhibit an even lower CVF due to the additional capacitance brought by the N+/P junction. If necessary for the application, this change of capacitance between the standard photodiodes and the radiation hardened ones can be compensated by slightly changing the dimension of the diodes (e.g. reducing the dimensions of the radiation hardened photodiodes would compensate the loss of CVF at the cost of a possible lower collection efficiency but with a possible improved geometric modulation transfer function). However, depending on the application, a drop of CVF can be an advantage since it is correlated to a full well increase (the larger the capacitance, the larger the full well in charge). Another consequence of this increase of capacitance is the increase of input referred reset noise. Indeed, the input referred reset noise in 3T-APS is usually expressed (in electrons):

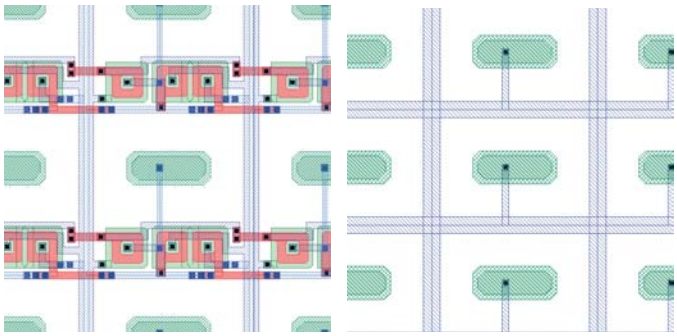
$$\sigma_{n\mathrm{RST}} = \frac{C_{\mathrm{CN}}}{q}\sqrt{\frac{kT}{n \times C_{\mathrm{CN}}}} = \frac{1}{q}\sqrt{\frac{kTC_{\mathrm{CN}}}{n}}, \qquad (3)$$

with k the Boltzmann constant, T the temperature and n a factor varying between 1 and 2 as discussed in [17]. Such reset noise rise leads to a reduction of the signal to noise ratio if this noise is the limiting noise and if the signal is not increased accordingly to the full well extension.

As regards the MOSFETs, the three in-pixel NMOSFETs have been designed using an enclosed layout (as can be seen on the layout presented in Fig. 4a) whereas the remaining part of the sensor is unhardened. The pixel layout has not been optimized for high performance but to allow the direct comparison of the studied photodiode layouts by keeping exactly the same junction perimeter regardless of which layout variation is used. That is the reason why the STD photodiode is so small and why the fill factor is low in Fig. 4a. All these photodiode layouts have also been placed outside the active pixel sensor for direct I-V measurements. For each photodiode layout of Table I, 300 photodiodes were connected in parallel in a metallic array to allow direct dark current measurements. All the I-V results presented in this paper on the photodiode arrays are divided by 300 to retrieve the dark current of a single photodiode. All the studied in-pixel and isolated photodiodes (even the radiation hardened layouts) are based on a CIS $\mathrm{N_{well}}$ doping profile and have the same junction dimensions ($2 \times 5\ \mu\mathrm{m}$), as illustrated in Fig. 4.

All the measurements presented have been performed at $22°\mathrm{C}$ except activation energy measurements that were performed between $-20°\mathrm{C}$ and $22°\mathrm{C}$. Since the dark current in such conventional diode is proportional to the photodiode perimeter (as discussed previously), the given dark current values can be extrapolated to any design simply by multiplying the presented value by the ratio of the targeted photodiode perimeter by the photodiode perimeter used here ($14\,\mu\mathrm{m}$).

In order to study TID effects only (and not displacement damage effects) a ^{60}Co γ-ray source has been chosen since it induces a high charge yield [18] leading to the worst case degradation. Room temperature ^{60}Co irradiations took place at UCL, Belgium, at a dose rate close to 1 krad(SiO_2)/h and up to a TID of 2.2 Mrad(SiO_2). Two irradiation conditions have been used: biased and grounded. For the APS, biased means



(a) (b)

Fig. 4. STD photodiode active pixel layout (a) and isolated STD photodiode array layout (b).

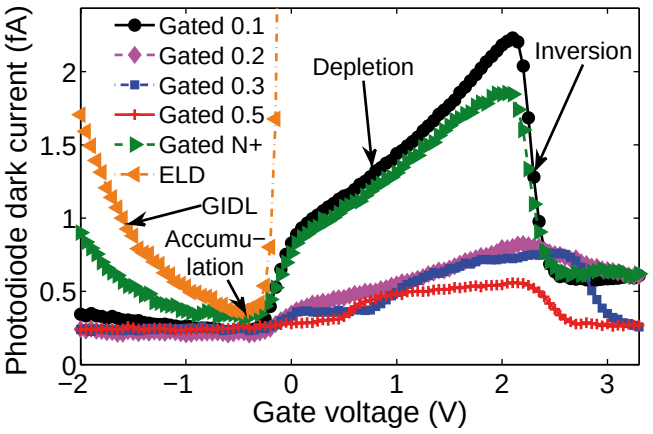


Fig. 5. Gated diode measurements performed before irradiation on the Gated photodiodes for $V_D = 1.8V$.

that the devices were operated with dynamic bias, using a regular rolling shutter operation, to ensure regular photodiode resets and realistic biasing conditions for the APS transistors. A 2 V bias was applied to the isolated photodiode cathodes to represent the in-pixel photodiode voltage after reset. The gates were biased in accumulation (-0.4 V).

IV. Pre-irradiation results

Before comparing the unirradiated photodiode behaviors, an optimal bias voltage must be chosen for the gate of the Gated photodiodes. Fig. 5 presents the gated diode measurements [19] performed on selected structures. The chosen diode voltage $V_D = 1.8$ V corresponds to the estimated in-pixel Gated photodiode voltage after reset. The accumulation, depletion, and inversion regimes can be clearly recognized. In depletion mode, the leakage currents are very high since the depletion region extends below the gate until reaching the STI. In inversion mode, only the interface states below the gate are screened by the inversion channel but the STI interface states generate additional dark current. As mentioned in [4], accumulation appears to be the best regime to select since the depletion region does not extend below the gate in this case. Nevertheless, placing the gated diodes too far in the accumulation regime leads to so called Gate Induced Drain Leakages (GIDL) [20]. This GIDL is due to the overlapping

of the gate with the N region. That is the reason why placing the gate away from the junction (as in the Gated 0.3 and Gated 0.5 photodiodes) mitigates the GIDL effect. The Gated N+ and ELD photodiodes exhibit a very large GIDL in accumulation because, as in a standard transistor channel, the N+ diffusion extends below the gate. Based on these characteristics, -0.4 V was chosen as the optimal gate voltage used during measurements [2]

Fig. 6 presents the I-V characteristics of most of the studied photodiodes before irradiation. The exponential behavior that can be seen on some I-V characteristics (e.g. SP+0.2, SP+0.3, ELD structures) indicates the presence of high electric fields [21]. Such electric field magnitudes can lead to enhanced leakage current through the Poole-Frenkel (PF) and the Trap Assisted Tunneling (TAT) effects [22]. The influence of PF and TAT mechanisms on dark current temperature dependence can be summarized by a decrease ΔE of apparent activation energy [21]:

$$I_{\text{dark}} \propto \exp\left(\frac{-(E_g/2-\Delta E)}{kT}\right) . \quad (4)$$

Hence, if the apparent activation energy is significantly lower than $E_g/2$, it indicates that PF and TAT are the dominant dark current generation processes.

Another leakage current mechanism can occur in heavily doped junctions: Band-to-Band Tunneling (BBT) [23]. SP+ I-V characteristics with the smallest recess distance d (SP+0.1 and SP+0.2) appeared clearly dominated by an intense tunneling effect (as illustrated by the I-V characteristics of the SP+0.2 diode in Fig. 6), most likely BBT (the reverse leakage current at 1.8 V was about 100 nA for SP+0.1 and about 100 pA for SP+0.2), and will not be studied further. BBT is not supposed to play a role in the other structures where the doping density at the junction is much lower.

As mentioned previously, the in-pixel photodiode operating voltage in the dark, after reset is around $1.8-2$ V in this circuit. One can see in Fig. 6 that at this reverse bias, all the proposed structures exhibit a larger dark current than the standard photodiode. This is often the case in radiation hardened structures [4], [5], [11]. For several photodiodes (SP+0.3, ELD and Gated N+, which is not shown in Fig. 6 but exhibited the same behavior as the ELD photodiode) this can be attributed to electric field magnitude dependent effects (PF or TAT) due to either the gate overlap (TAT GIDL [20]) in the case of gated diodes or to the high doping density in the case of SP+ photodiodes. For the other structures, the increase does not look exponential up to the operating voltage (≈ 2 V), and it is most likely due to the depletion width extension W_{ox} with reverse voltage, as in the standard photodiode. Thus, the discrepancies between these structures and the standard photodiode are most likely due to a higher interface state density at the PMD/Si interface than at the STI/Si interface before irradiation. However, electric field enhancement seems to occur in almost all the radiation hardened structure for voltages above 2 V.

[2]It should be emphasized that no significant change in conversion factor has been observed when the gate voltage was swept. Thus, the slight change of surface depletion region around the photodiode with gate bias was not sufficient to induce measurable change in the overall photodiode capacitance, and hence the collection node capacitance.

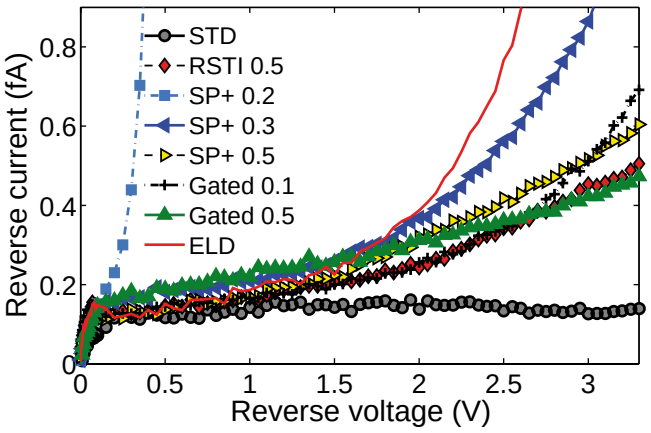


Fig. 6. Current-voltage characteristics of the studied photodiodes before irradiation. For clarity, some photodiode results are not shown.

The photodiode sensitivity to visible light is evaluated using External Quantum Efficiency (EQE) measurements, as shown in Fig. 7. Such characterization consists of determining for an APS, the number of electrons collected for an incoming number of photons per pixel for several wavelengths. No dramatic sensitivity drop is observed on the radiation hardened devices, except for the ELD diode in the case where the "drain" is biased. Indeed, in this case, the ELD "drain" is able to collect photo-generated electrons, and thus reduces the number of photo-electrons collected by the main photodiode. When the ELD drain is floating, the drain does not collect photo-generated charges, and the ELD photodiode EQE becomes similar to the other gated photodiode EQEs. The drain bias condition is not given for the dark current measurements, since in accumulation mode, the drain bias has no effect on the photodiode leakage (it was confirmed experimentally). It is also observed that the short wavelength sensitivity is reduced in the case of the gated photodiode (due to the poor transmission coefficient of the polysilicon gate) whereas it appears to be enhanced in RSTI and SP+ photodiodes. In these latter structures, photo-electrons generated at the surface (in the N region) have less distance to diffuse before being collected by the surface depleted region, which most likely explains the sensitivity enhancement at short wavelengths.

V. Post Irradiation Results

A. Functionality

Before discussing the dark current results, the sensor functionality and its performances must be verified for the selected TID range. Fig. 8 presents the images taken by one of the sensors after irradiation. The image taken before irradiation is not shown since no change was observed up to 100 krad(SiO_2) (Fig. 8a). The two middle-top white zones are the SP+ 0.1 and SP+ 0.2 regions which exhibit extremely high leakage currents (resulting in saturated images).

It should be emphasized that the 1951 USAF resolution test chart can be well recognized, even after 2 Mrad(SiO_2). Hence, the image sensor readout chain and digital circuits (mainly

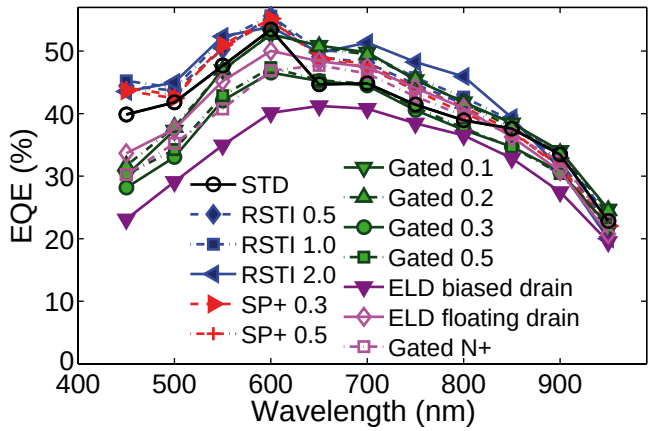
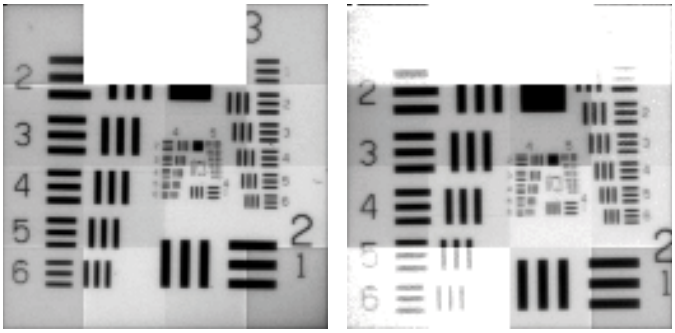


Fig. 7. External quantum efficiency characteristics of the studied photodiodes.



(a) (b)

Fig. 8. Raw images, in electronic charge, of the 1951 USAF resolution test chart taken with APS1 after (a) 100 krad(SiO_2) and (b) 2.2 Mrad(SiO_2) with similar illumination condition and fixed integration time (8 ms). The sensor was operated during irradiation. It can clearly be seen that the sensor functionality is preserved up to the maximum TID. Zone distribution, from top left to bottom right, first line: STD, SP+ 0.2, SP+ 0.3, STD; second line: Gated 0.1, Gated 0.2, Gated 0.2, SP+ 0.3; third line: Gated 0.3, Gated 0.5, RSTI 2.0, SP+ 0.5; fourth line: STD, RSTI 0.5, RSTI 1.0, RSTI 1.0.

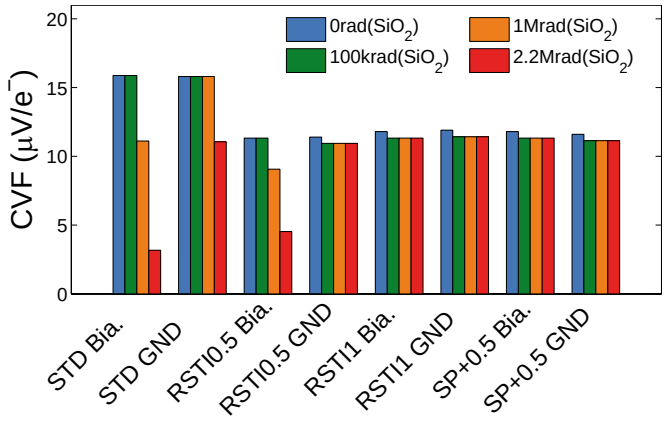


Fig. 9. Conversion factor evolution with TID of several pixel types. No change of CVF was seen in the structures not shown in the figure.

command and addressing circuits) are still fully functional after this TID despite the fact that no precaution has been taken to make them radiation tolerant.

Fig. 9 shows the evolution of the CVF with TID for representative photodiodes. STD and RSTI 0.5 pixel CVFs clearly drop after 1 Mrad(SiO_2) when biased (operated) during irradiation. The effect is weaker when the devices are not biased during irradiation. Regarding the other pixels, no change in CVF can be seen (same results for the pixels not shown in this figure). The dark current results presented hereafter take into account this gain degradation. The possible origin of this degradation is discussed in section VI-A.

B. Dark current evolution with TID

Irradiated sensor and isolated dark current evolutions with TID are presented in Fig. 10 and Fig. 11 for devices biased (or operated) during irradiation. The dark current values measured on the APS and isolated photodiodes grounded during irradiation were very close (30% standard deviation between the biased and grounded devices) to the values of Fig. 10 and Fig. 11 except for the RSTI diodes. This latter discrepancy is discussed in section VI-A. The relatively small effect of biasing during irradiation on photodiode dark current increase can be explained by the pretty weak change of electric field magnitude in the STI between the grounded and biased conditions in comparison to the changes observed in a classical MOSFET gate oxide.

Most of the photodiodes appear to behave the same in the sensor pixel array and in the isolated test structure with comparable measured dark current values, despite the different measurement techniques. This good agreement between the APS and the isolated photodiodes shows that isolated photodiodes are well representative of the in-pixel photodiode behavior. It also shows that the in-pixel dark current evolution is only due to the photodiode (as concluded in [11]) and neither to the surrounding transistors nor to the readout chain.

After the first irradiation step (3 krad(SiO_2)) the standard photodiode dark current has increased more than most of the selected radiation hardened photodiodes. The improvement factor of the best structures ranges from 2 to more than 40 as compared to the standard photodiode over the entire TID range. The best structures are the ones that exhibited the weaker dependence on bias voltage before irradiation. These structures are also the ones with the largest recess distance d (RSTI 1.0, RSTI 2.0, Gated 0.5, SP+ 0.5). In contrast, the worst responses (at least up to 1 Mrad(SiO_2)) are obtained with the smallest d (SP+ 0.3, ELD, Gated N+ and Gated 0.1) and it is most likely due to electric field related effects (PF and TAT) accordingly to the pre-irradiation results. There is one exception to this overall trend: a sudden change of behavior can be seen on the APS RSTI 0.5 plot: after 100 krad(SiO_2), RSTI 0.5 dark current rises quickly until almost reaching the standard photodiode dark current value whereas there is no obvious sign of electric field enhancement in their I-V characteristics and activation energies (Fig. 12). The same effect can be observed on all the RSTI isolated photodiodes but not on the RSTI 1.0 and 2.0 embedded in the sensor pixel array. This effect is discussed more in detail in section VI-A.

The previous assumptions about the role of electric field in the observed degradation can be validated by extracting the dark current activation energy (i.e. by extracting the exponential factor of the dark current temperature dependence).

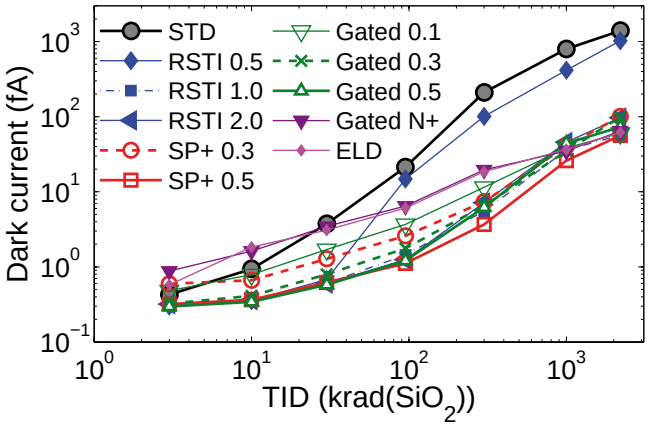


Fig. 10. CIS dark current evolution with TID (operated with dynamic bias during irradiation).

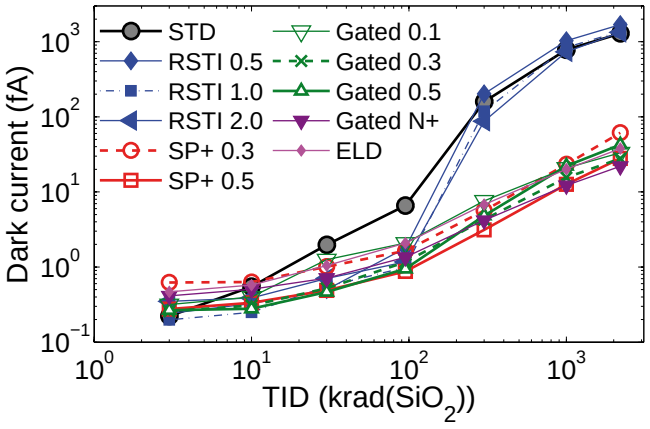


Fig. 11. Isolated photodiode dark current evolution with TID (biased during irradiation).

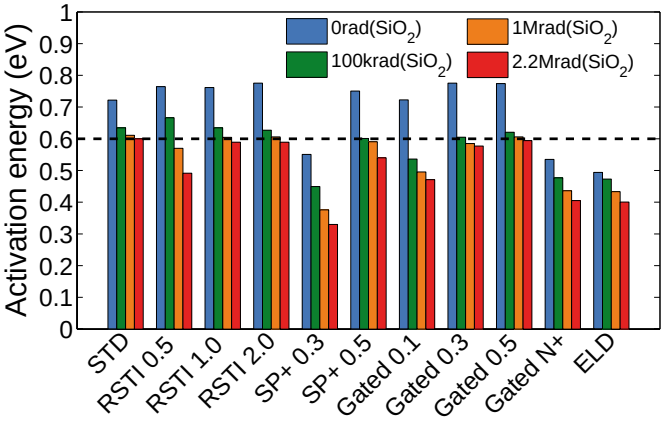


Fig. 12. Dark current activation energy evolution with TID of several pixel types. The TID levels are expressed in rad(SiO_2).

Fig. 12 summarizes the extracted dark current activation energies. Before irradiation, a number of pixels exhibit a dark current activation energy above the expected value for mid-gap centers (≈ 0.6 eV). This suggests the dominance of non-mid-gap centers before irradiation[3]. After exposure to γ-rays, the activation energy of almost all the photodiodes aligns well on the expected ≈ 0.6 eV for mid-gap center dominated SRH current (see (1)). The only exceptions are the photodiodes suspected to be dominated by electric field dependent process (Gated N+, ELD, SP+0.3, Gated 0.1). These devices clearly exhibit dark current activation energies much lower than the expected value for mid-gap centers, validating the PF or TAT hypothesis accordingly to (4). Fig. 13 shows APS dark current distributions of selected number of pixels after 100 krad(SiO_2). Despite the fact that most of the studied structures have not been manufactured with self-aligned implantations, all the distributions look pretty uniform (i.e. almost Gaussian-shaped). It is interesting to notice that the photodiode structures with no electric field effect exhibit a Gaussian-shaped distribution, with no hot pixel, whereas the structures where high electric fields exist have a more pronounced hot pixel distribution tail. As regards the RSTI 0.5 photodiodes, it can clearly be seen that the whole pixel population has shifted uniformly toward the standard photodiode population but with no clear sign of electric field enhancement. Finally, after 2.2 Mrad(SiO_2), one can see in the I-V characteristics (Fig. 14) that the best structures (SP+ 0.5 and Gated 0.5) exhibit a small increase with reverse voltage as expected for an SRH dominated reverse current. The STD and RSTI isolated photodiodes behave the same but with a weaker rise than the SP+ 0.5 and Gated 0.5 above 1 V. It suggests that increasing the voltage beyond 1 V does not induce an increase in the number of R-G centers in the depleted region. As regards the SP+ 0.2, SP+ 0.3, ELD, Gated N+ and Gated 0.1, a very clear exponential dependence on reverse voltage can be seen, indicating that these diode dark currents are still dominated by electric field dependent processes after the highest TID exposure levels (as confirmed in Fig. 12).

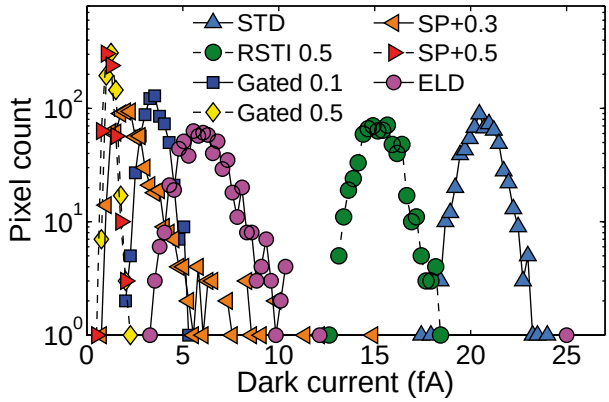


Fig. 13. Dark current distribution after 100 krad(SiO_2) of several types of pixel.

[3]As a first approximation, for a point defect in a reverse biased PN junction depletion region, the generation rate is proportional to [24] $n_i / \left(2\cosh\left\{\left|E_i - E_t\right| / kT\right\}\right)$. When the trap energy level E_t is more than a few kT away from E_i, the generation rate becomes proportional to $n_i \times \exp\left\{\left|E_t - E_i\right| / kT\right\}$ leading to an apparent activation energy around $|E_t - E_i| + E_g/2 > E_g/2$ whereas mid-gap centers will exhibit a generation rate activation energy closer to $E_g/2$.

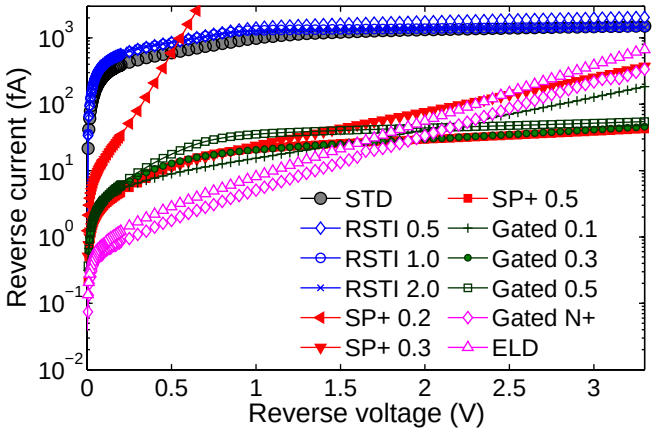


Fig. 14. Current-voltage characteristics of the studied photodiodes after 2.2 Mrad(SiO_2).

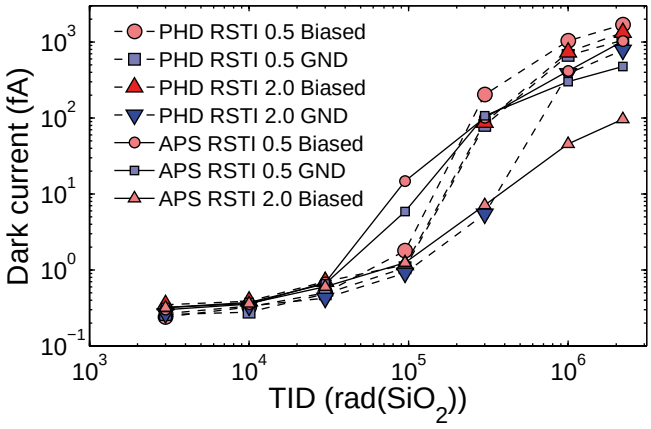


Fig. 15. RSTI photodiode dark current evolutions with TID for two biasing conditions during irradiation: biased and grounded.

It should also be mentioned that no shift in the optimal accumulation voltage was seen in the gated diode characteristics after irradiation, indicating no significant charge trapping in the gate oxide.

VI. Discussions

A. Depletion width extension

As mentioned previously, some RSTI photodiodes exhibit a sudden change in dark current increase with TID and others do not. Fig. 15 summarizes the observed behavior in APS and isolated photodiodes for the two biasing conditions during irradiation (grounded and biased). A sudden rise of dark current can be seen in most of the RSTI photodiode plots but it appears at a higher TID: 1) when the device is not biased, 2) in the isolated photodiodes when compared to the APS pixels and 3) when the recess distance is larger. These observations strongly suggest a depletion width ($W_{\rm ox}$) extension due to the trapped charge density increase as concluded in [15] and as illustrated in Fig.1b. In the case of the RSTI 0.5 photodiodes, in the 100 krad(SiO_2)-300 krad(SiO_2) TID range, $W_{\rm ox}$ becomes large enough to reach the STI inducing a sudden rise of dark current (due to an instantaneous increase of the number of R-G centers in the depletion region). After 2 Mrad(SiO_2) (Fig. 14), there is almost no more noticeable increase with reverse voltage above 1 V in STD and RSTI characteristics because the STI (and PMD oxide for the RSTI diodes) is fully depleted. In this case, a further increase in the reverse voltage does not lead to a depletion width extension at the oxide interface, thus the dark current stays constant in this voltage range.

The phenomenon is delayed when the recess distance is greater (RSTI 1.0 and RSTI 2.0) since the distance to deplete is larger. It seems also delayed when the device is not biased during irradiation, this effect mainly related to $\Delta N_{\rm ot}$ might be more dependent on electric field than the main cause of dark current increase ($\Delta N_{\rm it}$). The depletion width extension with TID cannot be seen in the other structures since the surface potential is controlled by a gate or by a surround P+ implant.

The discrepancies between the RSTI photodiodes integrated in sensor pixels and the isolated ones are not understood. It cannot be attributed to the differences between the dynamic bias used in the operated APS during irradiation and the static bias used for isolated photodiode since the same differences were observed in devices grounded during irradiation. Since the photodiode layout is the same, it might be due to the in-pixel photodiode environment. Indeed, in the pixel, the photodiode is surrounded in two directions by the three in-pixel transistors as shown in Fig. 4. Another difference is the fact that the in-pixel photodiode is connected in parallel to the source of the in-pixel reset MOSFET. Whatever the reasons for these discrepancies, the in-pixel RSTI 1.0 and RSTI 2.0 photodiodes are expected to suffer from the same oxide full depletion effect for TID levels above 2.2 Mrad(SiO_2).

It is also interesting to notice that this dark current rise in the APS is correlated with the CVF reduction shown in Fig. 9, at least in the device biased during irradiation. The readout chain electrical transfer function cannot be the cause of this drop since the other pixels, with the same readout chain, do not exhibit this degradation. It can then be inferred that the CVF drop comes from the photodiode itself, and that it is due to a change of capacitance related to the depletion of the isolation oxide. One possibility is that after the isolation oxide interface have been depleted, higher TID leads to weak then strong inversion as illustrated in Fig. 16. Hence, adjacent photodiodes become connected by this inversion channel. In this case, the total photodiode capacitance of one pixel would be the sum of the photodiode junction capacitance ($C_a + C_p$), the channel inversion capacitance $C_{\rm inv}$ and possibly the adjacent photodiodes and so on. For a quantitative evaluation, the channel resistance would have to be taken into account to carefully determine the resulting capacitance. However, such evaluation would require a three dimensional analysis, taking into account the pixel layout, the quantity of charge in the STI and the interaction with in-pixel transistors depletion regions. To validate this hypothesis would also require performing direct capacitance measurements and additional sensitivity measurements. Such analysis goes beyond the scope of this study. However, without a quantitative evaluation, it can at least be said that such possible field inversion would most likely result in a capacitance increase and thus, to a CVF

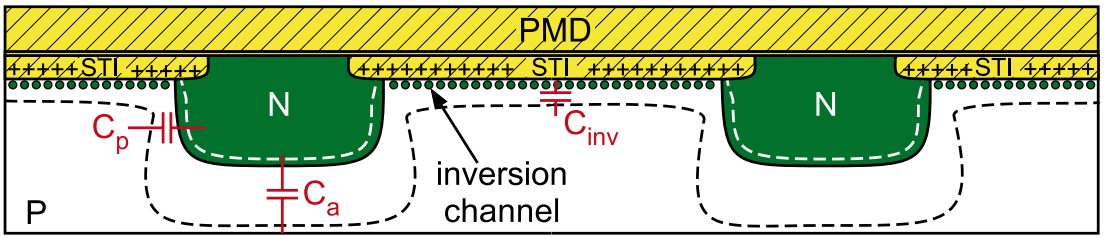


Fig. 16. Illustration of field oxide inversion on two adjacent photodiodes (i.e. pixels). C_a and C_p represent respectively the area and peripheral (sidewall) photodiode junction capacitances. $C_{\rm inv}$ the inversion channel capacitance.

decrease. More complex mechanisms would also appear with significant current flowing from one pixel to another leading to a strong electrical cross-talk. This effect might contribute to the loss of contrast observed in the standard photodiode and RTSI 0.5 areas of Fig. 8. As mentioned previously, all these hypothetical effects are mitigated in the radiation hardened structures surrounded by a gate or a surround P+ implant.

B. Conclusions on radiation hardness

The main results from a radiation hardness point of view are: 1) no noticeable degradation of the digital circuit and the readout chain have been observed despite the fact that no radiation tolerant layout has been used except in the pixel; 2) the best structures at TID below 100 krad(SiO_2) are the RSTI, SP+ 0.5 and the Gated 0.5; 3) above 100 krad(SiO_2), a structure with surface potential control is necessary to mitigate the large dark current increase and CVF drop of STD diodes and the SP+ 0.5 and Gated 0.5 photodiodes appear to be the best candidates.

Therefore, for TID levels up to about 2 Mrad(SiO_2), the use of radiation hardening by design techniques is only necessary in the pixel. P+ rings are not necessary in surface potential controlled devices (SP+ and Gated) but may be efficient above 100 krad(SiO_2) to mitigate the CVF drop and to reduce slightly the dark current increase of STD and RSTI photodiodes. Taking into account fill factor constraints and the fact that a polysilicon gate reduces the sensitivity at short wavelengths (e.g. see Fig. 7), the best structure for applications below 30 krad(SiO_2) appears to be the RSTI photodiode with a 0.5 μm recess distance (shorter recess distances lead to bad results in this range [14]). From 100 krad(SiO_2) and above, the SP+ structures with a 0.5 μm recess distance appears to be the best choice. This latter structure also leads to good performance below 100 krad(SiO_2) but with a reduced fill factor compared to the RSTI 0.5.

To go beyond 2.2 Mrad(SiO_2), ELT might be necessary in the whole sensor to insure the functionality. It is also interesting to notice in Fig. 14 that if the sensor readout chain is adapted to allow a shift of photodiode reset supply voltage from 2 V to 1 V, a further one order of magnitude reduction in dark current could be achieved by using the Gated structures where the dark current is dominated by electric field dependent process (Gated N+ and ELD). However, the following limitations must be taken into account. Reducing the photodiode reset supply voltage without changing the readout chain would reduce the maximum output voltage swing and operating the photodiode below zero volt would reduce the collection efficiency and inhibit the integration. A part of the voltage swing reduction could be compensated by, for example, using P-channel MOSFETs in the pixel. But in this case the N well area would reduce the quantum efficiency by competing with the main photodiode for photo-carrier collection. Another possibility would be to use negative voltages which may not be acceptable in some applications.

VII. Summary

Several radiation hardened by design photodiodes have been designed, integrated in a CMOS image sensor, manufactured, irradiated and characterized. It appears that the tested sensors are fully functional after a TID of 2.2 Mrad(SiO_2) without any use of radiation tolerant layout outside the pixel. As regards the photodiode, most of the tested radiation hardened layouts lead to a reduction of radiation induced dark current increase by more than one order of magnitude. In most of the studied structures, the largest recess distances led to the lowest dark currents by reducing the electric field enhancement effects. The best structure over the full TID range appears to be the surround P+ photodiode with a recess distance of 0.5 μm. The large increase observed in the standard photodiode and associated with a conversion factor reduction was not seen in the best radiation hardened by design photodiodes tested, and seems to be due to the full depletion (or even the inversion) of the isolation oxides. This work demonstrates several tested solutions and parameters to use (recess distance, gate voltage) to insure a good radiation hardness of photodiodes for 3T-pixel based APS devices manufactured in DSM CMOS image sensor processes.

Acknowledgment

The authors would like to thank Barbara Avon (ISAE) for her involvement in device characterization and Guy Berger (UCL) for having taken care of the irradiation.

References

[1] E. R. Fossum, “CMOS image sensors: electronic camera-on-a-chip,” *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.

[2] B. Hancock and G. Soli, “Total dose testing of a CMOS charged particle spectrometer,” *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 1957–1964, Dec. 1997.

[3] H. L. Hughes and J. M. Benedetto, “Radiation effects and hardening of MOS technology: devices and circuits,” *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 500–501, Jun. 2003.

[4] B. R. Hancock, T. J. Cunningham, K. P. McCarty, G. Yang, C. J. Wrigley, P. G. Ringold, R. C. Stirbl, and B. Pain, "Multi-megarad (Si) radiation-tolerant integrated CMOS imager," in *Proc. SPIE*, vol. 4306, 2001, pp. 147–155.

[5] B. Pain, B. R. Hancock, T. J. Cunningham, S. Seshadri, C. Sun, P. Pedadda, C. J. Wrigley, and R. C. Stirbl, "Hardening CMOS imagers: radhard-by-design or radhard-by-foundry," in *Proc. SPIE*, vol. 5167, 2004, pp. 101–110.

[6] W. Dulinski, G. Deptuch, Y. Gornushkin, P. Jalocha, J.-L. Riester, and M. Winter, "Radiation hardness study of an APS CMOS particle tracker," in *IEEE Nucl. Sci. Symp. Conf. Rec.*, vol. 1, Nov. 2001, pp. 100–103.

[7] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts, "Total dose and displacement damage effects in a radiation-hardened CMOS APS," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 84–90, Jan. 2003.

[8] W. Dulinski, A. Besson, G. Claus, C. Colledani, G. Deptuch, M. Deveaux, G. Gaycken, D. Grandjean, A. Himmi, C. Hu, K. Jaaskeleinen, M. Szelezniak, I. Valin, and M. Winter, "Optimization of tracking performance of CMOS monolithic active pixel sensors," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 1, pp. 284–289, Feb. 2007.

[9] M. Szelezniak, A. Besson, C. Colledani, A. Dorokhov, W. Dulinski, L. Greiner, A. Himmi, C. Hu, H. Matis, H. Ritter, A. Rose, A. Shabetai, T. Stezelberger, X. Sun, J. Thomas, I. Valin, C. Vu, H. Wieman, and M. Winter, "Small-scale readout system prototype for the STAR PIXEL detector," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3665–3672, Dec. 2008.

[10] M. Battaglia, D. Contarato, P. Denes, D. Doering, P. Giubilato, T. S. Kim, S. Mattiazzo, V. Radmilovic, and S. Zalusky, "A rad-hard CMOS active pixel sensor for electron microscopy," *Nucl. Instr. Meth. A*, vol. 598, no. 2, pp. 642–649, Jan. 2009.

[11] V. Goiffon, P. Magnan, O. Saint-Pé, F. Bernard, and G. Rolland, "Total dose evaluation of deep submicron CMOS imaging technology through elementary device and pixel array behavior analysis," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3494–3501, Dec. 2008.

[12] J. R. Srour, C. J. Marshall, and P. W. Marshall, "Review of displacement damage effects in silicon devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 653–670, Jun. 2003.

[13] V. Goiffon, P. Magnan, O. Saint-P, F. Bernard, and G. Rolland, "Ionization versus displacement damage effects in proton irradiated CMOS sensors manufactured in deep submicron process," *Nucl. Instr. Meth. A*, vol. 610, no. 1, pp. 225–229, Oct. 2009.

[14] V. Goiffon, M. Estribeau, and P. Magnan, "Overview of ionizing radiation effects in image sensors fabricated in a deep-submicrometer CMOS imaging technology," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2594–2601, Nov. 2009.

[15] V. Goiffon, C. Virmontois, P. Magnan, S. Girard, and P. Paillet, "Analysis of total dose induced dark current in CMOS image sensors from interface state and trapped charge density measurements," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3087–3094, Dec. 2010.

[16] B. P. Beecken and E. R. Fossum, "Determination of the conversion gain and the accuracy of its measurement for detector elements and arrays," *Appl. Opt.*, vol. 35, pp. 3471–3477, Jul. 1996.

[17] H. Tian, B. Fowler, and A. El Gamal, "Analysis of temporal noise in CMOS photodiode active pixel sensor," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 92–101, Jan. 2001.

[18] T. R. Oldham and J. M. McGarrity, "Comparison of ^{60}Co and 10 keV X-ray response in MOS capacitors," *IEEE Trans. Nucl. Sci.*, vol. NS-30, pp. 4377–4381, Dec. 1983.

[19] A. S. Grove and D. J. Fitzgerald, "Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions," *Solid-State Electron.*, vol. 9, no. 8, pp. 783–806, Aug. 1966.

[20] I. Chen, C. Teng, D. Coleman, A. Nishimura, T. Inc, and T. Dallas, "Interface trap-enhanced gate-induced leakage current in MOSFET," *IEEE Electron Device Lett.*, vol. 10, no. 5, pp. 216–218, May 1989.

[21] M. J. J. Theunissen, "Analysis of the soft reverse characteristics of n^+p drain diodes," *Solid-State Electron.*, vol. 28, no. 5, pp. 417–425, May 1985.

[22] G. Vincent, A. Chantre, and D. Bois, "Electric field effect on the thermal emission of traps in semiconductor junctions," *J. Appl. Phys.*, vol. 50, no. 8, pp. 5484–5487, Aug. 1979.

[23] G. A. M. Hurkx, H. C. De Graaff, W. J. Kloosterman, and M. P. G. Knuvers, "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Trans. Electron Devices*, vol. 39, no. 9, pp. 2090–2098, Sep. 1992.

[24] A. S. Grove, *Physics and Technology of Semiconductor Devices*. Wiley International, 1967.