CMOS Detectors for Space Applications: From R&D to operational program with large volume foundry

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ABSTRACT

Nowadays, CMOS image sensors are widely considered for space applications. The use of CIS (CMOS Image sensor) processes has significantly enhanced their performances such as dark current, quantum efficiency and conversion gain. However, in order to fulfil specific space mission requirements, dedicated research and development work has to be performed to address specific detector performance issues. This is especially the case for dynamic range improvement through output voltage swing optimisation, control of conversion gain and noise reduction. These issues have been addressed in a 0.35µm CIS process, based on a large volume CMOS foundry, by several joint ISAE- EADS Astrium R&D programs. These results have been applied to the development of the visible and near-infrared multi-linear imager for the SENTINEL 2 mission (LEO Earth observation mission for the Global Measurement Environment and Security program). For this high performance multi-linear device, output voltage swing improvement is achieved by process optimisation done in collaboration with foundry. Conversion gain control is also achieved for each spectral band by managing photodiode capacitance. A low noise level at sensor output is reached by the use of an architecture allowing Correlated Double Sampling readout in order to eliminate reset noise (KTC noise). KTC noise elimination reveals noisy pixels due to RTS noise. Optimisation of transistors's dimensions, taking into account conversion gain constraints, is done to minimise these noisy pixels. Additional features have been also designed: 1) Due to different integration times between spectral bands required by mission, a specific readout mode was developed in order to avoid electrical perturbations during the integration time and readout. This readout mode leads to specific power supply architecture. 2)Post processing steps can be achieved by alignment marks design allowing a very good accuracy. These alignment marks can be used for a black coating deposition between spectral bands (pixel line) in order to minimise straight light effects. In conclusion a review of design improvements and performances of the final component is performed.

Keywords: CMOS image sensors – Conversion gain – RTS noise – KTC noise – Low noise – Post-processing

1. INTRODUCTION

CMOS image sensors are nowadays extensively considered for several space applications. CMOS standard processes, which are developed for digital and mixed signal applications, are really attractive particularly because of their low power consumption, applicability for on-chip signal processing and large availability. However, electro-optic performances are often inadequate for high end applications. Several ways have been explored to improve image sensor performances to a very high level [1] [2] [3]. Image sensors performances are described by key parameters which are Quantum Efficiency (QE), Conversion gain (CG), Dark Current (DC), Noise, Full Well Capacity (FWC), Photo-Response and Dark Signal Non-Uniformities (respectively PRNU and DSNU) and Modulation Transfer Function (MTF). Most of these key parameters were addressed by joint ISAE-EADS Astrium R&D programs leading to the development of space CMOS image sensors flight models. ISAE-CIMI team has developed recently the COBRA2M component for the GOCI (*Geostationary Ocean Color Imager*) instrument of the COMS (*Communication, Ocean,*

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Sensors, Systems, and Next-Generation Satellites XIV, edited by Roland Meynart, Steven P. Neeck, Haruhisa Shimoda,
Proc. of SPIE Vol. 7826, 78261P · © 2010 SPIE · CCC code: 0277-786X/10/$18 · doi: 10.1117/12.868442

Meteorological Satellite) satellite and the VNIR (*Visible and Near InfraRed*) component for the Sentinel2 satellite for the GMES (*Global Monitoring for Environment and Security*) program from ESA. This paper presents the work done during R&D programs leading to the development of the VNIR component [4].
The VNIR component needs a high SNR (Signal to Noise Ratio), different conversion gains and integration times for each line (spectral band). Section 2 describes optimisations done on the key parameters during the R&D programs. Section 3 presents the architecture of the VNIR component and additional features. Measurement results for the key parameters are also depicted. Finally, a review of design improvements and performances of the final component is performed in the conclusion.

2. KEY PARAMETERS OPTIMISATION

During R&D programs, we developed technological blocks needed to meet the VNIR requirements. R&D programs are focused on SNR improvement thought dynamic range (DR) enhancement, and conversion gain control [5].

2.1 SNR optimisation

High SNR can be achieved in different ways. Equation (1) gives the DR for an image sensor. SNR can be improved by improving DR, hence by increasing the maximum usable output linear voltage swing and/or by reducing the noise.

$$DR = \frac{Maximum\_usable\_output\_linear\_voltage\_swing}{noise\_in\_dark} \quad (1)$$

Figure 1 shows the classical architecture of a CMOS image sensor for witch the DR is defined by:

$$DR = \frac{V_{MAX} - V_{DARK}}{\sqrt{V_{NOISE\_DARK}^2 + 2V_{RESET}^2 + \frac{V_{READOUT\_NOISE}^2}{A_{TOT}^2}}} \quad (2)$$

With :
V_{MAX} = Maximum linear voltage on the photodiode (or readout node)
V_{DARK} = Voltage due to dark current
V_{NOISE_DARK} = Noise voltage due to dark current
V_{RESET} = Noise voltage due to reset phase
$V_{READOUT\_NOISE}$ = Noise voltage due to readout circuit *
A_{TOT} = Readout circuit gain*
* including pixel column and output stage

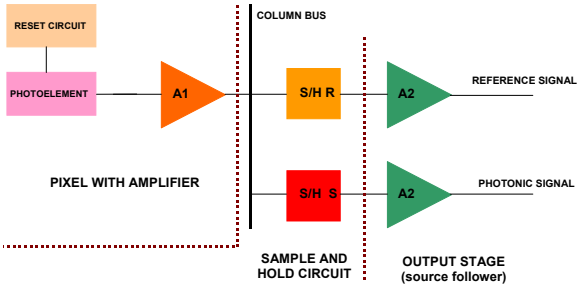


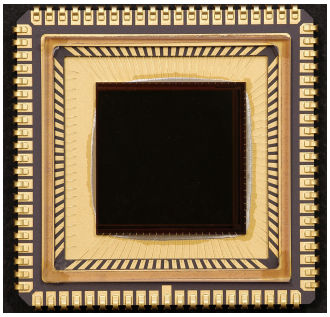
Figure 1 : Photo element and readout circuit synoptic

Equation 2 shows the impact of maximum linear voltage on the photodiode (or the readout node for 4T photodiode) and noise on the dynamic range.
The readout circuit is generally differential. The reset noise is affected by this differential readout: reset noise is doubled. The $V_{READOUT\_NOISE}$ takes into account this readout circuit feature. In the 3T photodiode case, reset noise is the major noise contributor. Optimisation of the dynamic range can be done in two ways: 1) improving the maximum linear voltage on the photodiode and 2) removing the reset noise.

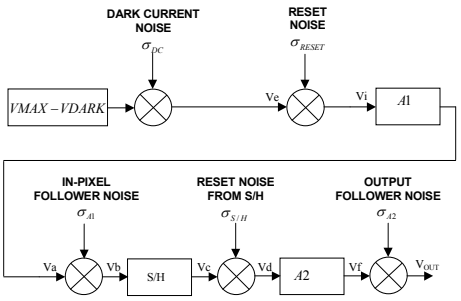
2.1.1 Optimisation of Photodiode voltage swing on dynamic range

CIMI laboratory has designed, in collaboration with the UMC foundry, a test vehicle enhancing the photodiode voltage swing without degradation of photodiode dark current. The process, coming from UMC, is 0.35µm CIS (CMOS Image Sensor) dedicated to detection applications. This process is optimized for good quantum efficiency, charge collection and low dark current thanks to special photodiode doping profile. The test vehicle, named COBRA1M, is a 1Kx1K common (3T) photodiode array. The pixel pitch is 13µm. Readout circuit architecture is the same as depicted in Figure 1. A photography of COBRA1M is depicted on Figure 2a.

The readout circuit is composed of two amplification stages and a sample and hold circuit to perform sampling on reference signal and photonic signal. The two amplification stages are based on source follower structures.



a) Photography



b) Noise equivalent model for a CMOS image sensor in dark

Figure 2: Photography and noise equivalent model of COBRA1M

The noise equivalent model associated to this readout circuit is shown in Figure 2b. The output dynamic range for this CMOS image sensor, when taking into account the readout architecture is defined by:

$$DR = \frac{Maximum\_usable\_output\_linear\_voltage\_swing}{noise\_in\_dark} \quad (3)$$

$$Maximum\_usable\_output\_linear\_voltage\_swing = A_1 A_2 (V_{MAX} - V_{DARK}) \quad (4)$$

$$Noise\_in\_dark = \sqrt{A_1^2 A_2^2 \sigma_{NOISE\_DARK}^2 + 2A_1^2 A_2^2 \sigma_{RESET}^2 + 2A_2^2 \sigma_{A1}^2 + 2A_2^2 \sigma_{SH}^2 + 2\sigma_{A2}^2} \quad (5)$$

With :
V_{MAX} = Maximum linear voltage on the photodiode (or readout node)
V_{DARK} = Voltage due to dark current
σ_{NOISE_DARK} = Noise voltage due to dark current
σ_{RESET} = Noise voltage due to reset phase
σ_{A1} = Noise voltage due to first stage amplifier
σ_{A2} = Noise voltage due to second stage amplifier
σ_{SH} = Noise voltage due to S/H phase
A_1 = First stage gain
A_2 = Second stage gain

The dynamic range can be expressed by:

$$DR = \frac{(V_{MAX} - V_{DARK})}{\sqrt{\sigma_{NOISE\_DARK}^2 + 2\frac{kT}{\alpha . C_{PH}} + 2\frac{\sigma_{A1}^2}{A_1^2} + 2\frac{\sigma_{SH}^2}{A_1^2} + 2\frac{\sigma_{A2}^2}{A_1^2 A_2^2}}} \quad (6)$$

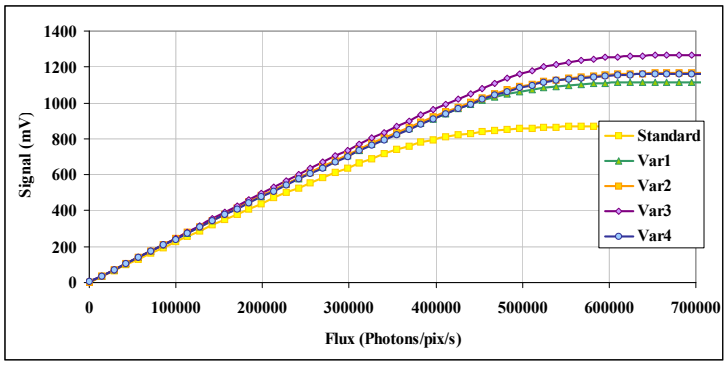
$\alpha = 1$: hard reset
$\alpha = 2$: soft reset
C_{PH} = Photodiode capacitance

With the assumption about reset noise predominance compared to the other noise for this kind of pixel, the dynamic range can be expressed by:

$$DR \approx \frac{(V_{MAX} - V_{DARK})}{\sqrt{2 . \frac{kT}{\alpha . C_{PH}}}} \quad (7)$$

The 3T pixel of this test vehicle is composed of a reset transistor, a source follower transistor and the row selection transistor. These 3 in-pixel transistors are impacted by special doping implant. Features as threshold voltage and leakage current of the reset and the source follower transistors are very important. If threshold voltage of source follower decreases, the photodiode output voltage increases. A special care must be taken to keep a low leakage current in order to avoid dark current.

Four variations of photodiode doping implant were implemented to decrease threshold voltage without changing leakage current. Figure 3 presents the measurement results made on the test vehicles. Voltage swing at the output of the readout circuit is strongly depending on the variations. An increase up to 45% can be reached at saturation level for process variation #3. However, an increase of dark current can be seen for this process variation. A trade off must be made because process variation #4 offers an improvement of the voltage swing at the output (33% of increase at saturation level) with a slight increase of dark current.



a) Sensitivity curve for the standard process and the 4 process variations

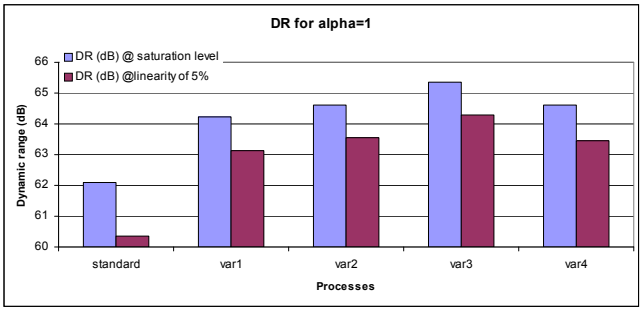
PROCESS	Linearity @5% (mV)	Saturation level (mV)
STANDARD	716	872
VARIATION #1	984	1115
VARIATION #2	1029	1166
VARIATION #3	1121	1266
VARIATION #4	1021	1163

	Dark Current density @30°C in nA/cm²
Standard	0,33
Variation #1	0,82
Variation #2	0,72
Variation #3	0,71
Variation #4	0,40

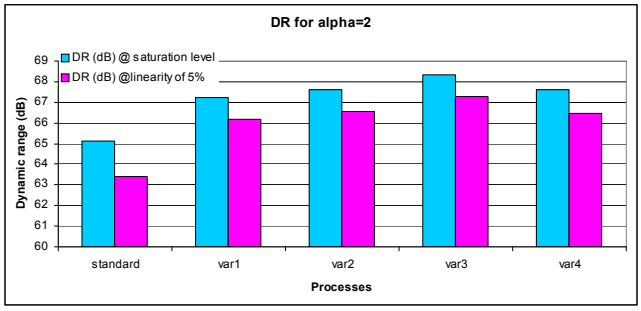
b) Measured voltage swing at the output of circuit and dark current density

Figure 3 : Linearity, voltage swing at the output of the readout circuit and dark current density measurement results

Using the result of the dynamic range equation for this readout circuit, a comparison of dynamic range in dB can be made between the different process (standard and variations) for an integration time of 100ms. Calculations are made using the saturation level (ie V_{MAX}) and the maximum voltage allowing a non-linearity inferior to 5%. Figure 4 shows the dynamic range with regard to the process variation and for α=1 and α=2.



a) $\alpha = 1$



b) $\alpha = 2$

Figure 4 : Dynamic range in dB

A real improvement of the dynamic range can be reached, up to 4 dB for the process variation #3. A trade-off between DR and dark current can be made and process variation #4 is the more efficient in this case. Indeed, an increase of 3.5dB is obtained without a significant degradation of dark current.

2.1.2 Noise optimization

The other way to enhance the dynamic range is to minimize the noise. For a common 3T photodiode with a classical readout circuit (two stages, c.f. previously), the reset noise is dominant. If the reset noise is eliminated, the dynamic range increases and becomes, without neglecting the other noise terms:

$$DR = \frac{V_{MAX} - V_{DARK}}{\sqrt{V_{NOISE\_DARK}^2 + \frac{V_{READOUT\_NOISE}^2}{A_{TOT}^2}}} \qquad (8)$$

New readout circuit architecture can be implemented to eliminate reset noise. This architecture is composed of 3 sample-and-hold circuits allowing sampling of reference signal and photonic signal in the same frame as required for a

Correlated Double Sampling (CDS) readout mode [6][7] as shown on Figure 5. This architecture is suitable for linear or multi linear sensors. So, the DR becomes:

$$DR = \frac{V_{MAX} - V_{DARK}}{\sqrt{\sigma^2_{NOISE\_DARK} + \sum \sigma^2_A + \sum \sigma^2_{SH}}} \quad (9)$$

V_{MAX} = Maximum linear voltage on the photodiode (or readout node)
V_{DARK} = Voltage due to dark current
σ_{NOISE_DARK} = Noise voltage due to dark current
σ_{RESET} = Noise voltage due to reset phase
$\Sigma\sigma_A$ = Sum of noise voltage due to amplifier stages
$\Sigma\sigma_{SH}$ = Sum of noise voltage due to S/H phases

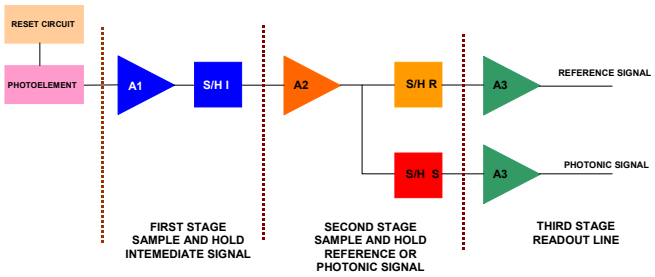


Figure 5: Readout circuit architecture

This architecture was implemented in a test vehicle named COBRANxK. Photography of COBRANxK is depicted in Figure 6. This test vehicle is a multi-linear sensor.

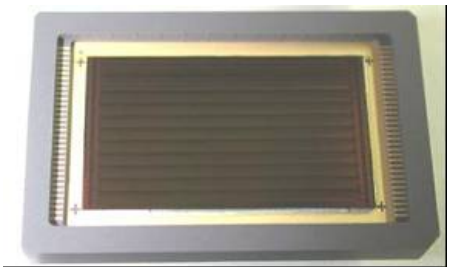


Figure 6: COBRANxK vehicle photography

This multi-linear sensor is composed of lines with 7.5µm pixel pitch and lines with 15µm pixel pitch. Each line has a readout circuit dedicated with a CDS (Correlated Double Sampling) implemented. Pixel rate on the 2 video output is close to 3 MPix/s. The UMC CIS 0.35µm process was used. Variation 3 for the photodiode doping implant was re-used for this test vehicle (cf previous section). Conversion gain of the 7.5µm pixel pitch is close to 7.8µV/e. Conversion gain of the 15µm pixel pitch is close to 3µV/e.

Measurements made on this vehicle allow computing the dynamic range value for this sensor. A comparison with the same sensor without CDS stage can be made when taking into account reset noise. This comparison is made with the "hard reset mode", i.e. reset noise is equal to $\sqrt{\frac{kT}{C_{PH}}}$. Results on dynamic range are presented in Figure 7 for the both pixel pitch. An output readout noise of 147µV was found in both cases.

An output swing voltage close to 840mV was measured for the readout circuit allowing a 1% maximum non-linearity. The output swing voltage was close to 1.06V at saturation level. A gain of 0.6 was measured for the readout circuit.

For comparison, the reset noise was carried out with photodiode capacitance close to 12fF for 7.5µm pixel pitch and close to 32fF for 15µm pixel pitch.

Results show an increase of 8dB in terms of dynamic range for the small pixel and an increase of 6dB for 15 µm pixel pitch.

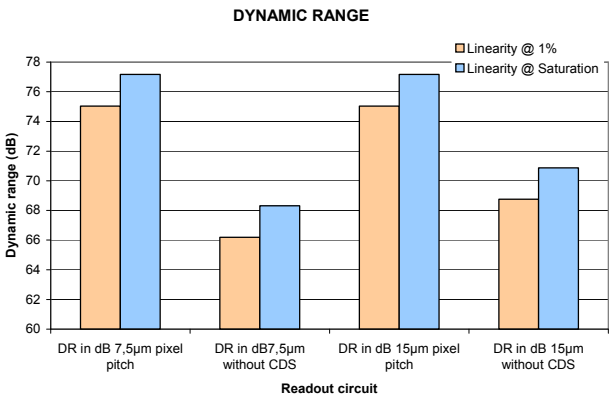


Figure 7 : Dynamic range comparison

As expected, the dynamic range increases when reset noise, the dominant noise, is eliminated. The dynamic range becomes independent of the photodiode size, i.e. the capacitance value. A real improvement of dynamic range is achieved by architecture design. However, reset noise elimination implies noisy pixels apparition. Pixel output noise

distribution at the sensor output shows these noisy pixels (Figure 8) [8][9]. In this case, a positive skew appears on the distribution.

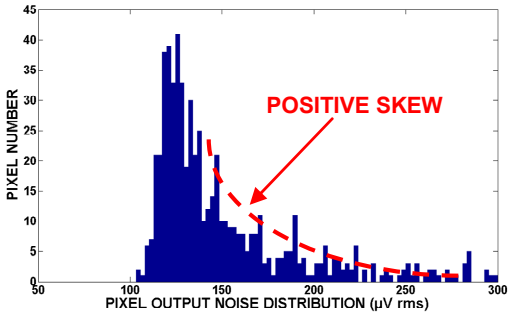


Figure 8: Pixel output noise distribution at the sensor output

These noisy pixels are the consequence of the RTS noise of the in-pixel source follower transistor which has small dimensions. A test vehicle, named COBRANxK_P was designed by CIMI team to study this RTS noise. Variations of in-pixel source follower dimensions were done as shown by Table 1.

	IN-PIXEL SOURCE FOLLOWER: W/L IN MICRONS			
	PART N°1	**PART N°2**	**PART N°3**	**PART N°4**
LINE N°1	1.5/0.5	1.5/0.65	1.5/0.8	1.5/1
LINE N°2	1/0.5	1/0.65	1/0.8	1/1

Table 1: In-pixel source follower size variation

Twelve circuits were tested from 3 different wafers:

- 7 circuits from wafer #4
- 4 circuits from wafer #5
- 1 circuit from wafer #1

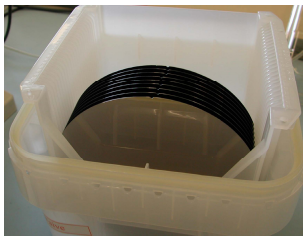
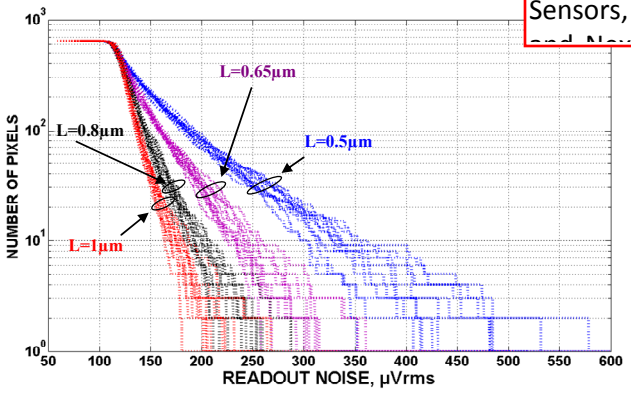
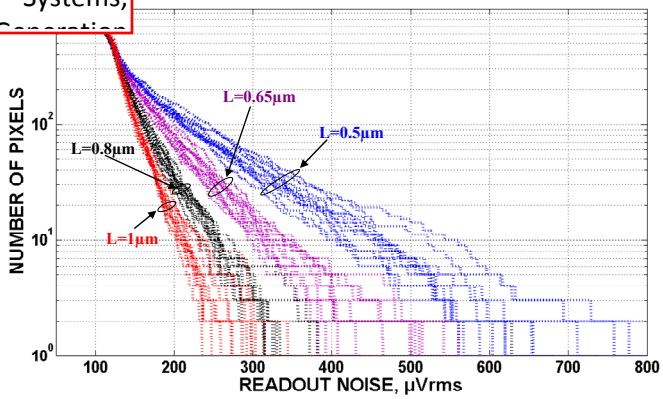


Figure 9: Wafers tested

Noise measurement results are depicted in Figu gram with log scale is chosen to have the best view of the positive skew of the distribution whi behaviour.



a) Cumulative histogram of the pixel output noise dispersion from 12 circuits for W=1.5µm and L variations



b) Cumulative histogram of the pixel output noise dispersion from 12 circuits for W=1µm and L variations

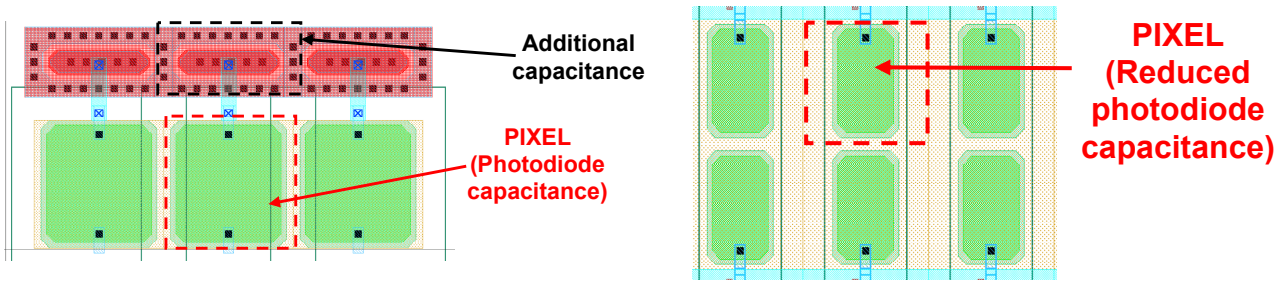
Figure 10: Noise measurement results at the sensor output for the different size variation of the in-pixel source follower transistor and for the different circuits

The results show a clear tendency of the RTS noise reduction when L increases (W=1.5µm) despite the circuit to circuit dispersion (Figure 10a).This is also confirmed by Figure 10b showing the cumulative histogram of the pixel output noise dispersion from the twelve circuits for W=1µm and L variations.
In conclusion, higher in-pixel source follower transistor dimensions reduce RTS noise impact, thus the number of noisy pixel decreases.

2.2 Conversion gain control

Conversion gain control is needed in order to adjust the maximum photon flux level to the output swing voltage. In this case, SNR will be optimized. Due to different maximum photon flux level between each line for VNIR component, different conversion gain must be adjusted.

Conversion gain on the photodiode is defined by $G_{C\_PH} = \frac{q}{C_{PH}}$. To increase conversion gain, photodiode capacitance (C_{PH}) has to be minimized. To decrease conversion gain, a capacitance has to be added to photodiode capacitance. Figure 11a shows implantation of an additional capacitance in order to minimize the conversion gain [5]. Figure 11b depicts the reduction of the photodiode capacitance.



a) Conversion gain decrease b) Conversion gain increase

Figure 11: Conversion gain control

COBRANxK_P test vehicle was used to implant the conversion gain control techniques. Measurements show very good results in the conversion gain prediction versus measurements. Table 2 illustrates results for two pixel pitch.

Pixel pitch	Control type	Native Conversion gain	Final Conversion gain
7.5µm²	↗	6.2µV/e	7.5µV/e
15µm²	↘	2.9µV/e	1.9µV/e

Table 2 : Conversion gain control

Key parameters opitimisation done during R&D programs allows us to develop the VNIR component. The next section describes the VNIR component architecture developed with additional features such as post processing for black coating and a description of the power supplies architecture.

3. VNIR COMPONENT DEVELOPEMENT

Sentinel 2 is a LEO Earth observation mission in the frame of Global Measurement Environment and Security (GMES) program. The instrument is equipped with VNIR and SWIR Focal Plane Arrays, each one being made of twelve detectors in staggered configuration. The VNIR detector offers tens spectral bands with 10m, 20m and 60m resolution, and the SWIR detector offers three spectral bands with 20m and 60m resolution.
For each spectral band, a SNR corresponding to a reference flux and the maximum integration time is specified. A maximum flux is also specified for each spectral channel. The detector sensitivity has therefore to be adjusted band per band through conversion gain adjustment in view of meeting SNR specification for a reference flux while avoiding saturation for maximum flux.

3.1 VNIR component description

VNIR component is a multi-linear sensor with 10 single or double lines which correspond to 10 spectral bands [10].

Band name	Central wavelength (nm)	Spectral width (nm)	Pixel surface (µm²)	Frame period (ms)	Pixels number by line
B2	490	65	7.5²	1,51	2596
B8	842	115	//	//	//
B3	560	35	7.5²	//	//
B4	665	30	//	//	//
B5	705	15	15²	3,02	1298
B6	740	15	//	//	//
B7	775	20	//	//	//
B8a	865	20	//	//	//
B1	443	20	15x45	9,06	//
B9	940	20	//	//	//

Table 3 : Line description

Features of each line are illustrated in the Table 3. VNIR component architecture is depicted in Figure 12.

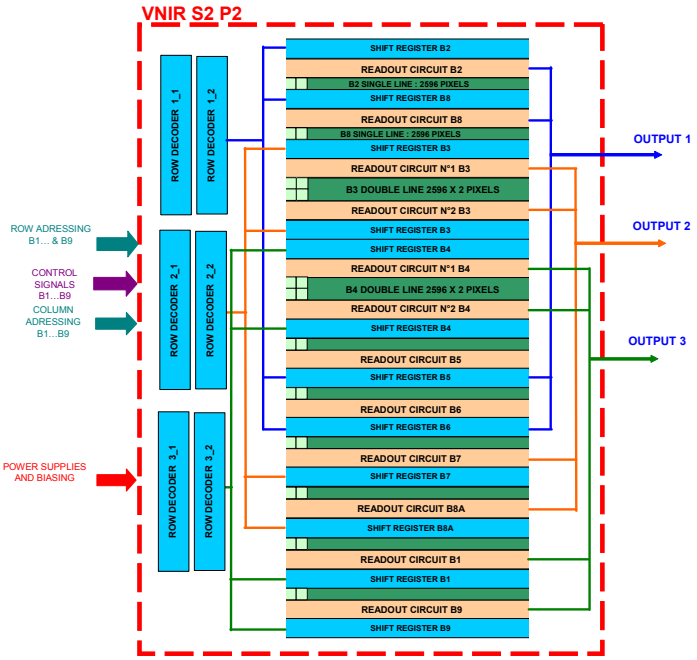


Figure 12: VNIR component architecture

The VNIR component is composed of:

- 10 lines with 100% fill factor photodiodes with 7.5x7.5, 15x15 and 15x45 µm² pixel pitch
- Conversion gain and photodiode geometry tuned for each spectral band in order to optimize SNR and MTF to meet requirements
- 3 outputs read out at 4.8Mpix/s (OUTPUT1 : B2, B8, B5, B6; OUTPUT2 : B3, B7, B8a; OUTPUT3 : B4, B1, B9)
- Lines are selected by row decoders
- Columns are selected by shift registers

UMC CIS 0.35µm foundry is used to fabricate VNIR component.

3.2 Additional features

Due to high performances and specific requirements, additional features are implanted in the VNIR component: specific power supplies architecture and post processing for black coating.

3.2.1 Power supplies architecture

As mentioned previously, three different integration times are used. For B2, B8, B3 and B4 lines, integration time is 1.51ms. Integration time is 3.02ms for B5, B6, B7 and B8a lines and finally, integration time is 9.06ms for B1 and B9 lines. These different integration times imply asynchronous readout. In addition, voltage drops appear due to large number of pixels and current consumption. In order to avoid voltage drops during readout, B1 and B9 lines power supplies are segregated.
A specific care has to be taken to power supplies decoupling for all stages: integrated circuit, package and electronic board.

3.2.2 Post processing: black coating

Due to VNIR channel straylight requirements, a post processing step is needed in order to strongly reduce the CMOS die global reflectivity. Black coating deposition on the non photosensitive area of the die is used in order to meet these requirements [11]. Such process has been validated thanks to COBRA NxK wafers availability. Figure 13 illustrates COBRANxK black coating device. For VNIR component, CIMI team designed black coating mask set. Black coating processing is performed by E2V.

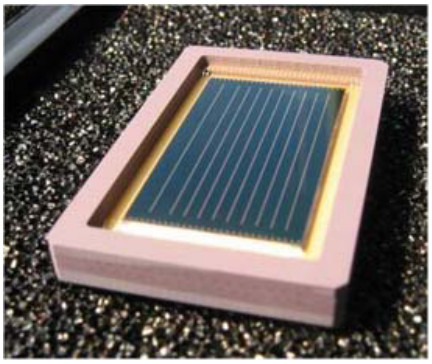


Figure 13 : COBRANxK black coated device

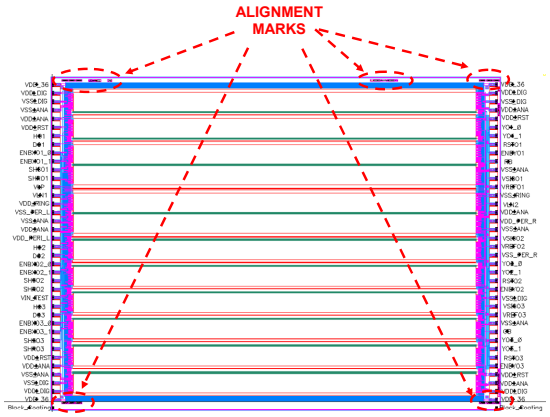


Figure 14: Reticule layout with alignment marks

In order to ensure a low misalignment, alignment marks were implanted. Alignment marks are compatibles with E2V equipments (Figure 14). So, black coating can be performed by using alignment marks or step X and Y provided by foundry.

Figure 15 depicts a packaged engineering model (EM) of VNIR with black coating processing.

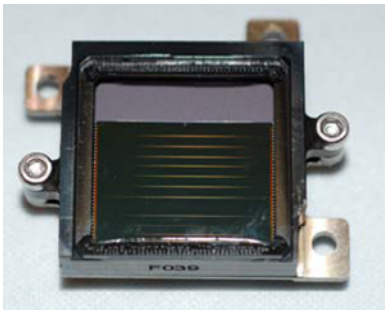


Figure 15 : A packaged VNIR engineering model with black coating

3.3 VNIR Performances

Figure 16 shows VNIR component packaged. The specific package was developed by E2V and EADS-Astrium to ensure space requirements. Figure 17 illustrates four EM models in staggered configuration which is a part of the final configuration for the focal plane.

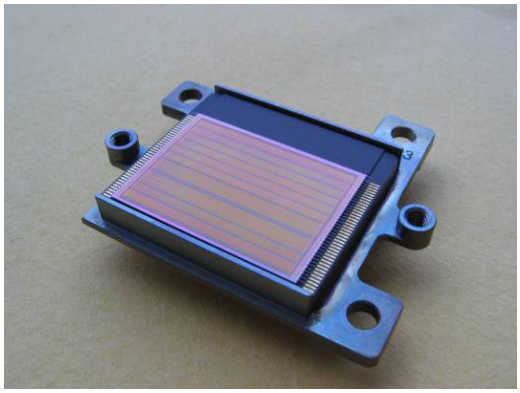


Figure 16 : VNIR component packaged

Figure 17 : Four EM models in staggered configuration

Table 4 sums up the key parameters electro-optical performances of the VNIR EM.

Technology	UMC CIS 0.35µm 3.3V
Pixel pitch	B1, B9 : 15x45µm² B2, B3, B4, B8 : 7.5x7.5µm² B5, B6, B7, B8a : 15x15µm²
Output swing (non-linearity<5%)	> 1V for each output @ 4.8 Mpix/s (output load 6pF)
Conversion gain	B1: 0.2µV/e, B2 : 3.5µV/e, B3: 5.8µV/e, B4: 6.1µV/e, B5: 1.9µV/e, B6: 2.1µV/e, B7: 1.7µV/e, B8: 4.4µV/e, B8a: 3.3µV/e, B9: 1.2µV/e
QE	B1: 81%, B2 : 67%, B3: 70%, B4: 71%, B5: 59%, B6: 50%, B7: 46%, B8: 30%, B8a: 26%, B9: 14%
Readout Noise max (including noisy pixels due to RTS noise)	B1: 180µV rms, B2 : 246µV rms, B3: 243µV rms, B4: 291µV rms, B5: 228µV rms, B6: 196µV rms, B7: 206µV rms, B8: 304µV rms, B8a: 199µV rms, B9: 1. 270µV rms

Table 4 : Main VNIR EM performances

4. CONCLUSION

This paper describes the work done to develop the flight model for the VNIR component. Several joint ISAE- EADS Astrium R&D programs were done to optimise image sensor key parameters to meet VNIR component requirements. SNR improvement and conversion gain control are performed. Additional features such as specific power supplies architecture and black coating post processing were also implemented. Key parameters performances of the engineering models show good agreement with the expected performances. Flight model measurements are in progress.

ACKOWLEDGMENTS

The authors want to thank Saï Guiry (EADS Astrium), Eric Havard and Paola Cervantes from ISAE CIMI for numerous test vehicles characterizations. The authors are grateful to ESA for financial support.

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