Custom transistor layout design techniques for random telegraph signal noise reduction in CMOS image sensors

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Interface and near oxide traps in small gate area MOS transistors (gate area $<1\ \mu m^2$) lead to RTS noise which implies the emergence of noisy pixels in CMOS image sensors. To reduce this noise, two simple and efficient layout techniques of custom transistors have been imagined. These techniques have been successfully implemented in an image sensor test chip fabricated in a 0.35 μm CMOS image sensor process. Experimental results demonstrate a significant reduction of the noisy pixels for the two different techniques.

Introduction: CMOS image sensors are nowadays extensively used in commercial and scientific applications. CMOS standard processes, which are developed for digital and mixed signal applications, are really attractive particularly because of their low power consumption, applicability for on-chip signal processing and large availability. Several ways have been explored to improve image sensor performance to a very high level and performance has been significantly enhanced with the use of CMOS image sensor (CIS) processes [1]. In addition, the use of aggressive technologies and small MOS transistors (gate area $<1\ \mu m^2$) in the pixel are required in order to maximise the pixel photosensitive area. This leads to an increase of MOS transistor low frequency noise impact. The use of correlated double sampling (CDS) circuits and readout mode allows elimination of photodiode reset noise (KTC noise) which is usually the major noise contributor. At the same time, it reveals the random telegraph signal (RTS) noise impact of the in-pixel source follower transistor. This RTS noise becomes an issue for low light sensitivity applications [2]. Fig. 1 depicts the cumulative histogram of the image sensor pixel output noise showing noisy pixels emergence due to in-pixel source follower transistor RTS noise.

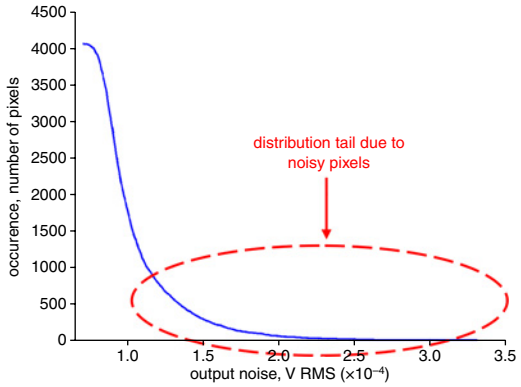

Fig. 1 *Cumulative histogram of image sensor pixel output noise*

RTS noise impact can be reduced by increasing the length and width of the in-pixel source follower transistor [3, 4]. However, this implies an increase of the in-pixel source follower transistor gate capacitance, so also a decrease of the conversion gain value. Thus, this technique leads to a decrease of the image sensor sensitivity. In this Letter, we propose custom transistor layout design techniques in order to minimise the number of noisy pixels by reducing in-pixel source follower transistor RTS noise.

Proposed techniques: Fig. 2 shows the cross-section of a standard NMOS transistor with a local oxidation of silicon (LOCOS) technology. When the transistor is on (weak, moderate and strong inversion), the channel is in contact with the gate oxide but also with the isolation oxide, which is in our case the LOCOS, along the gate length. For shallow trench isolation (STI) technologies, the channel is in contact with STI walls instead of LOCOS. As RTS fluctuations arise from traps located at the silicon and oxide interfaces, a part of these fluctuations comes from the silicon and LOCOS interfaces. The principle of our RTS noise reduction techniques is to minimise or eliminate transistor channel areas which are in contact with oxide isolation. The first technique is depicted in Fig. 3*a* for a LOCOS technology. Oxide isolation is recessed from the channel by layout design. Thus, as channel area in contact with isolation oxide (LOCOS) is eliminated, the probability to have traps at the silicon/oxide interface and in oxide, inducing RTS noise, is reduced. The transistor layout for the second technique is shown in Fig. 3*b*. The goal is to strain current flow in the centre of the channel in order to avoid electron flow near oxide isolation. The gate is enlarged at the silicon and oxide interface. Hence, the channel resistance is lower in the middle of the transistor leading to the fact that current is canalised far away from oxide isolation. This technique minimises the impact of traps located in the silicon and oxide isolation interfaces.

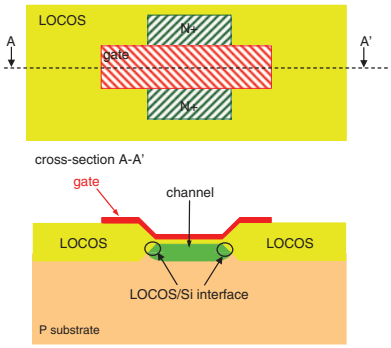

Fig. 2 *NMOS transistor cross-section for LOCOS technology*

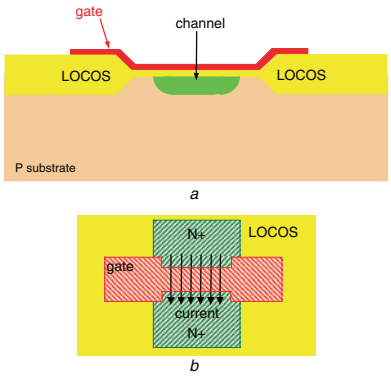

Fig. 3 *Modified NMOS transistors*

a NMOS transistor with recessed oxide technique (type 1)
b NMOS transistor with enlarged gate length near isolation oxide (type 2)

Test image sensor: To verify the performances of the proposed RTS noise reduction techniques, a test image sensor was designed and fabricated in a 0.35 μm CIS process (which is a LOCOS technology). Sensor format is 128 × 128 pixels with a 13 μm pixel pitch. A three transistors pixel structure is used with a special readout sequence allowing correlated double sampling in order to eliminate reset noise. The test sensor is composed of four sub-arrays of 4096 pixels. Three sub-arrays are tested in this Letter. One of these sub-arrays has a standard layout in-pixel source follower transistor and the two others have the proposed modified layout transistors. Gate length is 0.5 μm and gate width is 1.5 μm for the in-pixel source follower transistor. Type 1 and type 2 MOS transistors are defined as the modified transistors depicted in Figs. 3*a* and *b*, respectively.

Measurements results: Output noise measurements were performed with an in-pixel source follower transistor current bias of 18 μA. Spatial output noise means for each sub-array, i.e. standard, type 1 and type 2 in-pixel source follower transistors, are 106, 103 and 102 μV RMS. Cumulative histograms, depicted in Fig. 4, represent the pixel output noise distribution of each sub-array. Cumulative histograms show noisy pixels which can reach around 330 μV RMS for the standard MOS transistor type and 275 μV RMS for the type 1 and 2 transistors. A significant reduction of noisy pixels is achieved with the modified in-pixel source follower transistors. For example, the number of pixels having an output noise beyond 200 μV RMS is reduced by roughly 30% for the two proposed custom in-pixel source follower transistors.

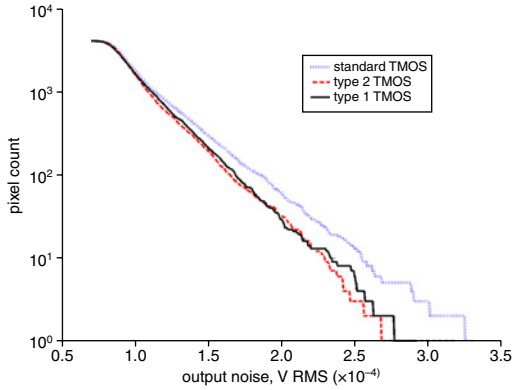

Fig. 4 *Cumulative histogram of pixel output noise distribution for each in-pixel source follower transistor type*

Conclusion: Two simple and efficient layout design techniques of custom transistors for random telegraph signal noise reduction in CMOS image sensors are proposed. The in-pixel source follower transistors are the major RTS noise contributors in CMOS image sensors leading to an increase of noisy pixels. In-pixel source follower transistors are designed and laid out in order to minimise contact between the transistor channel and isolation oxide. Measurement results performed on a test image sensor fabricated in a 0.35 μm CIS process confirm that the layout design techniques proposed in this Letter allow a significant reduction of noisy pixels.

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One or more of the Figures in this Letter are available in colour online.

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