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Direct Control Strategy for a Four-Level Three-Phase Flying-Capacitor Inverter

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***Abstract*—A direct predictive control strategy is proposed for a three-phase four-level flying-capacitor (FC) inverter in this paper. The balancing of the FC voltages, a challenge in applications with small capacitors and low switching frequencies, is done without any modulation, simply using tables calculated offline. These allow the realization of fast-dynamics output currents with reduced dv/dt in the output voltages and reduced switching frequencies. Moreover, no interharmonics are created when operating at low switching frequencies and with reference currents containing multiple harmonic components, which is a key feature for active power filters. Simulations and experimental results are presented to demonstrate the excellent performance of the direct control strategy in comparison with a conventional pulsewidth-modulation control technique, mostly for operation at low switching frequencies.**

***Index Terms*—Active power filter, direct control, flying-capacitor (FC) inverter.**

I. Introduction

DURING THE last years, electric power quality has become a challenge due to the increase of nonlinear loads, power electronic-interfaced distributed generation, and a growing energy demand. Industrial applications of multilevel converters are increasing [1]–[3] since they offer significant advantages for high-power applications by reducing voltage stress on the power switches and current distortion while operating at a low switching frequency. Flying-capacitor (FC) inverters are a promising multilevel topology that can be used in several industrial applications including active power filtering [4], [5]. This structure presents several advantages such as low current distortion, low conduction losses, and small dV/dt. Moreover, it presents the potential of an increased bandwidth, in comparison with the "conventional topologies," for a given switching frequency [6]–[9]. The correct operation of this converter needs the FC voltages to be regulated in order to limit the voltage stress on each commutation cell to its rated value. The dynamic performance achieved with the natural balancing method is often not good enough [10]–[12]. Better overall performance, including capacitor voltage balancing, can be achieved either by increasing the capacitor's size and cost or by increasing the switching frequency, which reduces the converter's efficiency. These inconveniences have lead to a significant effort to develop improved voltage-regulation methods for the FCs [12]–[17].

The method discussed in this paper for the control of the FC inverter aims at finding a compromise between capacitor size and switching frequency, while achieving a bandwidth suitable for operation as an active power filter. Predictive control is used for calculating the required average output voltage that yields a desired inverter current in each sampling period. This average voltage is produced with the direct control algorithm, using sequences of several *state combinations*, called here *profiles*, in a sampling period. Since each *profile* affects the trend (increase/decrease) of the variation of the capacitor voltages in a different way, it is possible to select the profiles so as to drive the capacitor voltages toward desired reference values. Since each profile is composed by several switch state combinations, called here *configurations*, through the adjustment of the application time of each configuration in a sampling period, the calculated average voltage can be obtained. Additional constraints are added in this direct control strategy to limit switch commutation to once per sampling period for each commutation cell and instantaneous output voltage variation from one profile to another to a minimum. The resulting capacitor voltage dynamics is slower than that of the inverter current, and voltage balancing is achieved over a small number of sampling periods.

The next section of this paper presents different approaches to balance the FC voltages. A classical control method, used here for comparison with the direct control method, is discussed in detail. In Section III, the direct control method is described as well as its application to a four-level FC inverter. Finally, experimental results are included in Section IV, showing the excellent current control and voltage balancing for FCs compared with the classical pulsewidth-modulation (PWM) method. An application of both methods for an active power filter is presented, showing the superior performance of the proposed method, mostly at low switching frequencies.

II. FC Voltage Balancing and PWM Control

Fig. 1 shows a three-phase FC inverter which presents a topology based on three series commutation cells on each phase. Two FCs per phase have to be voltage balanced to

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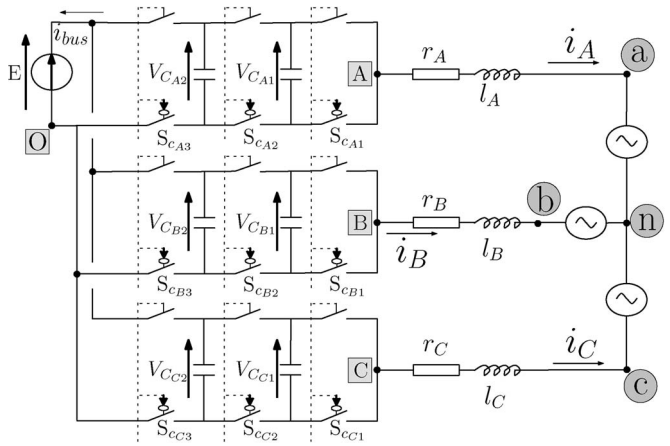

Fig. 1. Block diagram of FC inverter.

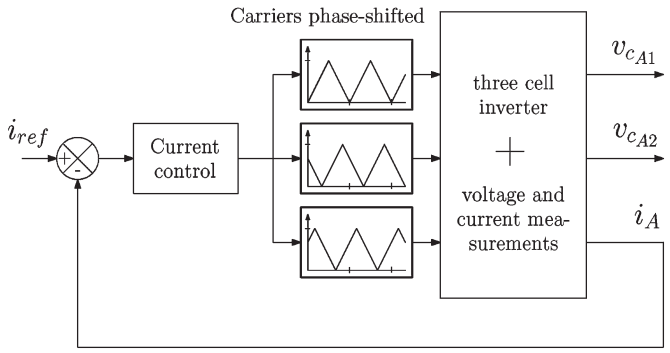

Fig. 2. Principle of the natural balance of FC voltages.

guarantee the same voltage stress on each commutation cell $(E/3)$. For this topology, the corresponding voltages are $E/3$ for $V_{C_{i1}}$ and $2E/3$ for $V_{C_{i2}}$, for each phase $(i = A, B, C)$.

A number of control methods have been developed to obtain this voltage balancing. A popular one is called "natural balancing" [9], [10] which makes use of phase-shifted carrier PWM signals, with identical phase shifts and duty cycles (Fig. 2). It is a passive method and no measurements are needed, but the balancing process is not satisfactory, since the dynamic is low for the FC voltages and the method imposes some constraints to the control signals.

Another method consists in connecting a resonant circuit in parallel to the load, with a natural frequency corresponding to the switching frequency [4], [7]. Under balanced conditions, no current flows in the external RLC circuit. If voltages are unbalanced, harmonic currents are no longer balanced and they are filtered by this circuit; therefore, the dynamics of the natural balancing is increased. This method is interesting but the added elements affect the cost and the losses generated by the resistor must be considered.

The active control of the FC voltages requires the knowledge of these voltages, either by measurement or by estimation. To perform this control, some methods have been investigated [6], [13], [18] but they have not been tested in conditions as low FC values, high load current dynamics, or low switching frequency. One of these methods based on phase-shifted modulation—the decoupling control method—is presented here, since it will be used in a comparison with the proposed direct control method.

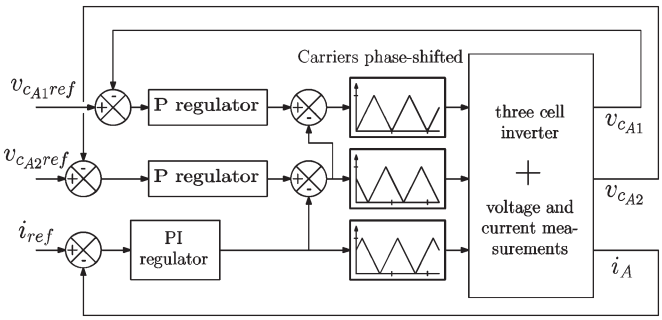

Fig. 3. Principle of the decoupling control method.

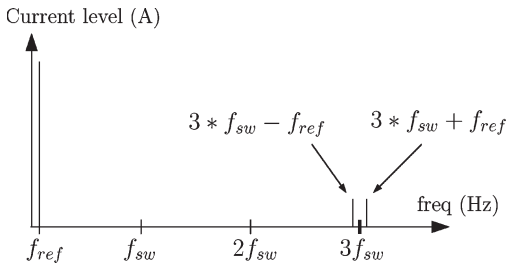

Fig. 4. Harmonics current composition with balanced capacitor voltages.

The principle of the decoupling control method [18] is shown in Fig. 3. Two P regulators per phase are included to control each FC voltage. In addition, a current controller is included in the current loop.

For the three-cell FC converter, this method presents current harmonics at around three times the semiconductor switching frequency ($3 * f_{\rm sw} \pm f_{\rm ref}$, where $f_{\rm ref}$ is the frequency of the reference current signal) [7], as shown in Fig. 4. This property constitutes one advantage that has to be taken into account for the direct control.

All the methods based on phase-shifted modulation are unable to ensure correct capacitor voltage balancing if the ratio between the switching frequency and the current reference harmonics is too low (experimental results for the decoupling method are presented in Section IV). One solution consists in increasing the value of the FC, but this solution implies a higher cost. Another solution is to develop a control method capable of controlling each commutation cell directly, without considering the phase-shifted solution [6]. The direct control presented in this paper and developed in the next section is based on this idea.

III. Direct Control for a Three-Cell Case

A significant effort to develop the application of the predictive control to multilevel inverters [19]–[22] has been done during the last years. In this section, the principal characteristics of the direct predictive control (Fig. 5) applied to a three-cell FC inverter are explained.

In the topology shown in Fig. 1, the grid is represented by V_{an}, V_{bn}, and V_{cn}, where n is the neutral point which is generally not accessible in a three-phase network. These voltages are considered as inputs for the control algorithm. If we consider that the FC voltages are constant during a sampling period, the

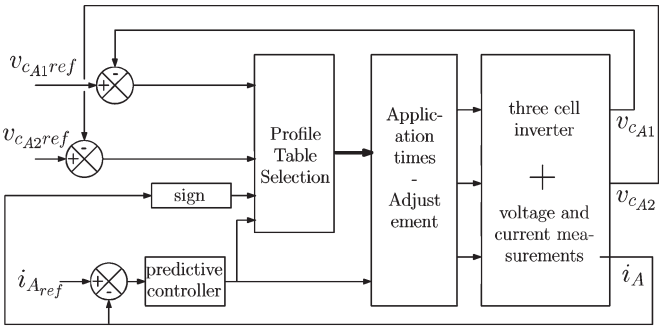

Fig. 5. Direct control of one phase of the four-level FC.

output voltage of phase i, designated as V_{iO}, can be expressed as

$$V_{iO} = \frac{E}{3} * (N_i), \qquad i = A, B, C \tag{1}$$

for a three-cell inverter $(p = 3)$ [7]. The variable N_i (with values 0, 1, 2, and 3) is defined as the instantaneous output level of phase i, and the denominator 3 is due to the three series commutation cells. The system is going to be analyzed using a composed voltage and current reference frame. The composed voltage at the output of the inverter is named v_{AB} which is defined as the difference between the phase voltages v_A and v_B, and the composed current will be i_{AB} (difference between i_A and i_B). Inverter output voltages are expressed in the composed voltage frame (also called *ba–ca* frame) [23] considering that $V_{\mathrm{AB}} = V_{\mathrm{AO}} - V_{\mathrm{BO}}$ and using (1)

$$\begin{cases} v_{\mathrm{AB}} = \frac{E}{3} * (N_A - N_B) \\ v_{\mathrm{BC}} = \frac{E}{3} * (N_B - N_C). \end{cases} \tag{2}$$

The equations of the continuous model describing the system are basically the same as those that were presented in [14]. The model can be discretized, considering that the switching period T_d is the same as the sampling period to obtain

$$\begin{pmatrix} i_{\mathrm{AB}}^{k+1} \\ i_{\mathrm{BC}}^{k+1} \end{pmatrix} = A_k * \begin{pmatrix} i_{\mathrm{AB}}^{k} \\ i_{\mathrm{BC}}^{k} \end{pmatrix} + B_k * \begin{pmatrix} v_{\mathrm{AB}}^{k} - v_{\mathrm{AB}}^{k} \\ v_{\mathrm{BC}}^{k} - v_{\mathrm{BC}}^{k} \end{pmatrix}. \tag{3}$$

The state matrix A of the continuous state space is diagonal, and the coefficients are constant; therefore, the discretization is the exponential form of the continuous state matrices (A, B). The two constant matrix coefficients (A_k, B_k) are

$$\begin{cases} A_k = e^{A*T_d} \\ B_k = A^{-1} * (e^{A*T_d} - Id) * B. \end{cases} \tag{4}$$

At time instant t_k, it is possible to calculate the control action $\overline{v_{\mathrm{AB}}^{k}}$ that has to be applied in order to reach the point i_{AB}^{k+1} at the end of the sampling period. $\overline{v_{\mathrm{AB}}^{k}}$ is the average output voltage of the inverter and can be calculated as shown in (5). $\overline{v_{\mathrm{AB}}^{k}}$ represents the average value of the grid voltage in a sampling period. The sample frequency is more than 20 times higher than the grid period; hence, the average value can be replaced by the discretized value v_{AB}^{k}

$$\begin{pmatrix} \overline{v_{\mathrm{AB}}^{k}} \\ \overline{v_{\mathrm{BC}}^{k}} \end{pmatrix} = B_k^{-1} * \begin{pmatrix} i_{\mathrm{AB}}^{k+1} \\ i_{\mathrm{BC}}^{k+1} \end{pmatrix} - B_k^{-1} * A_k * \begin{pmatrix} i_{\mathrm{AB}}^{k} \\ i_{\mathrm{BC}}^{k} \end{pmatrix} + \begin{pmatrix} \overline{v_{\mathrm{AB}}^{k}} \\ \overline{v_{\mathrm{BC}}^{k}} \end{pmatrix}. \tag{5}$$

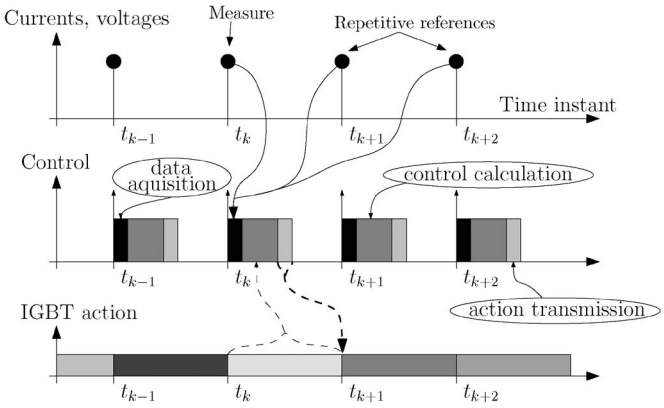

Fig. 6. Control sequences.

The recurrence (5) is written at time instant t_{k+1} (considering that the reference of current i_{AB}^{k+2} is known) and is expressed as

$$\begin{pmatrix} \overline{v_{\mathrm{AB}}^{k+1}} \\ \overline{v_{\mathrm{BC}}^{k+1}} \end{pmatrix} = K_1 \begin{pmatrix} i_{\mathrm{AB}}^{k+2} \\ i_{\mathrm{BC}}^{k+2} \end{pmatrix} + K_2 \begin{pmatrix} i_{\mathrm{AB}}^{k} \\ i_{\mathrm{BC}}^{k} \end{pmatrix} + \begin{pmatrix} v_{\mathrm{AB}}^{k+1} \\ v_{\mathrm{BC}}^{k+1} \end{pmatrix} + K_3 \begin{pmatrix} \overline{v_{\mathrm{AB}}^{k}} - v_{\mathrm{AB}}^{k} \\ \overline{v_{\mathrm{BC}}^{k}} - v_{\mathrm{BC}}^{k} \end{pmatrix} \tag{6}$$

where the three coefficients are constant and defined as

$$\begin{cases} K_1 = B_k^{-1} \\ K_2 = -B_k^{-1} * A_k^2 \\ K_3 = -B_k^{-1} * A_k * B_k. \end{cases} \tag{7}$$

Fig. 6 shows the principle of calculation, data transfer, and application of control actions. Between two sampling time instants, three main operations are realized by the DSP sequencer: 1) the data acquisition (measurements and reference determination); 2) calculation of the next control action, determined by the control algorithm; and 3) transmission of the control actions to the field-programmable gate array (FPGA). These actions are performed between the time instants t_k and t_{k+1}, and the calculated control actions will be applied at the beginning of the period between t_{k+1} and t_{k+2}. The recurrence (6) gives the expression of the control actions which have to be applied at time instant t_{k+1}, which are determined using the measurement of currents and voltages at time instant t_k and the current and voltage references at time instants t_{k+1} and t_{k+2} given by the repetitive principle. This principle consists basically in recording the necessary references for a grid period and considering that it will be unchanged for several periods.

The control actions calculated by the direct predictive control are determined in order to do the following.

1) Obtain the desired average output levels for $\overline{v_{\mathrm{AB}}^{k+1}}$ and $\overline{v_{\mathrm{BC}}^{k+1}}$.
2) Balance the six FC voltages at the correct value.
3) Reduce the switching frequency. Only one state change for each commutation cell is allowed during one sampling period. In this way, the switching frequency is divided by two compared with a classical modulation scheme where each switch turns on and off once per modulation period.

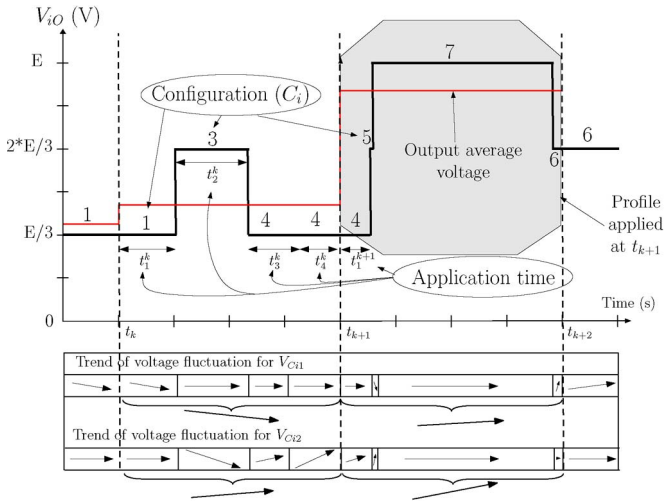

Fig. 7. Example of two consecutive profiles.

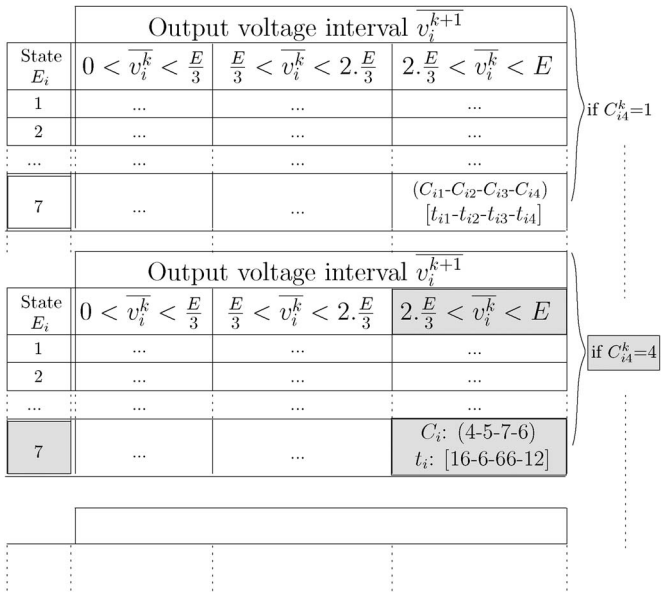

Fig. 8. Example of sequence table.

These three constraints have been respected to elaborate *profiles*, which are sequences of state combinations defined in a sampling period and which will define the "sequence table." A profile is composed of the following:

1) four configurations ($C_{i1}, C_{i2}, C_{i3},$ and C_{i4});
2) four application times ($t_{i1}, t_{i2}, t_{i3},$ and t_{i4});
3) four corresponding output level voltages.

Fig. 7 shows an example of two profiles with the evolution of each FC voltage of phase A.

The desired voltages $\overline{v_{\mathrm{AB}}^{k+1}}$ and $\overline{v_{\mathrm{BC}}^{k+1}}$ calculated by (6) will be applied, considering an algebraic criterion to control the FC voltages used in the sequence-table definition. The criterion chosen to establish the sequence table is based on the variation of the FC voltages and considers the redundancies of the FC converter. This variation is controlled through hysteresis controllers which consider only one binary information per capacitor through a comparison with a threshold. This leads to an additional simplicity where no precise analog-to-digital converters (ADCs) are needed. For the definition of the table, some constraints must be respected.

1) Large level variations are not allowed (output voltage transitions larger than $E/3$ are forbidden).
2) The initial and final output voltage levels of each profile can take only two values ($E/3$ or $2E/3$).
3) The number of output voltage level changes is limited to three on a sampling period in order to reduce the number of possible profiles to apply (several profiles can provide the same output voltage level due to the redundancies of the inverter). Furthermore, it allows the division of the switching frequency by two on the insulated-gate bipolar transistors (IGBTs) because only one state change by commutation cell is allowed during one sampling period.

To respect these constraints for the choice of the next profile to apply, the sequence table has three inputs (Fig. 8), which are as follows: 1) the desired output voltage level ($\overline{V_i^k}$); 2) the last configuration of the previous profile (C_{i4}^k), in order to avoid large level transitions between two consecutive profiles; and 3) the state of the inverter (E_i) related to the output current sign and the trend of variation of FC voltages. From these values, it is possible to find the best profile to apply which contains four configurations and four corresponding application times (as a percentage). These application times can be adjusted if necessary in a later step, in order to obtain exactly the desired average output levels $\overline{v_{\mathrm{AB}}^{k+1}}$ and $\overline{v_{\mathrm{BC}}^{k+1}}$.

An example is shown in Fig. 8, corresponding to the profile calculated at the time t_k and applied between times t_{k+1} and t_{k+2} on Fig. 6. Considering that each configuration imposes a different trend of FC voltage variation ($Trend_{C_{Aj}}$), depending on the current sign, the global trend of each profile can be calculated as

$$Trend_{V_{cA1}} = \sum_{j=1}^{4} (Trend_{C_{Aj}} * t_j) \tag{8}$$

considering that the current is constant during a sampling period. If the trend is positive, the voltage globally increases. The detailed definition and construction of this sequence table is presented in [14] and [24].

The average output voltage for one sampling period is

$$\overline{V_{iO}} = \frac{1}{T_d} * \sum_{j=1}^{4} (t_j * N_{ij}) \tag{9}$$

and the application times can be adjusted, from the values obtained from the table, in order to apply the correct average output voltage given by (9).

IV. Results for a Three-Phase Inverter

Fig. 9 shows the electrical structure of the three-phase FC inverter. The parameters of the experiment are a 2.5- or 10-kHz switching frequency, a 220-V dc bus, a 10-kVA maximum load, and the following:

1) three-phase FC inverter with 18 IGBTs;
2) DSPACE DS1105 controller with 16 fast ADCs;
3) Altera FPGA for protection and IGBT control;
4) six 200-μF FCs.

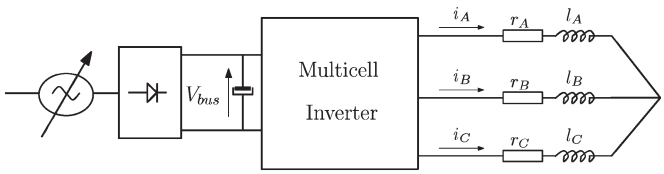

Fig. 9. Principle of the three-phase FC inverter structure.

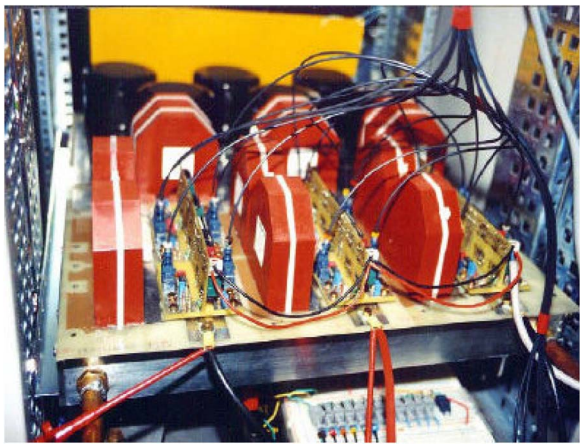

Fig. 10. FC inverter.

The FC control has been extensively tested in simulation with an instantaneous model of the FC inverter. Experimental results have been carried out with the experimental test bench (Fig. 10) which is composed of an FC inverter able to work with a 1800-V dc bus and a 60-A line current. The experimental test bench is formed by the association of a high-performance DSPACE processor board and an FPGA which controls 18 semiconductor switches. A serial communication has been established for their information exchange.

A. *Start-up of the FC Inverter*

After the start-up transient, the FC voltages must be balanced [7], which underlines the practical problem of the capacitor precharge during the start-up transient. In recent years, different methods have been developed in order to obtain good performance in the precharge of FC converters [13]. One possible technique is to connect high-value resistances in parallel with the power semiconductors, which could ensure the equivalent distribution of the charge of the FCs [25]. These components could also contribute to the converter discharge phase. On the other hand, these resistances may induce high temperatures during the precharge transient and should remain connected during the normal operation of the converter. Another technique is to add external sources to charge the FCs, but this solution leads to a more complex system and it is not an optimal solution.

For this application, a method has been developed, which imposes a commutation sequence on the switches in order to charge each capacitor of each phase sequentially. The results shown in Fig. 11 correspond to the start-up of an active power filter application in a 400-V network. Only one commutation cell is active at each time, as shown by the control signals $S_{C_{ij}}$. The evolution of the capacitor voltages $V_{C_{i1}}$ and $V_{C_{i2}}$ is made in two stages of less than 150 V to an intermediate

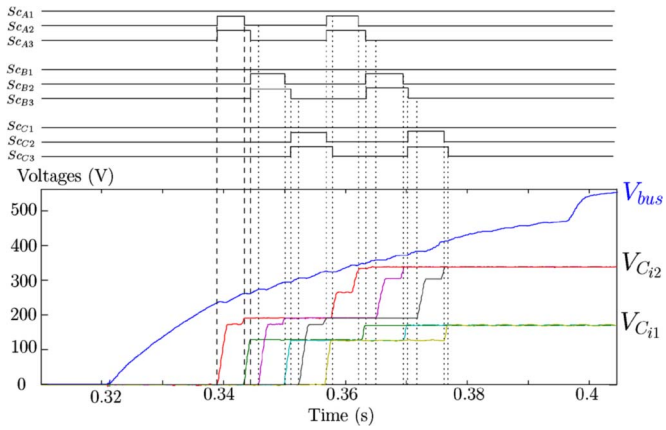

Fig. 11. Bus and capacitor voltages during the precharge sequence.

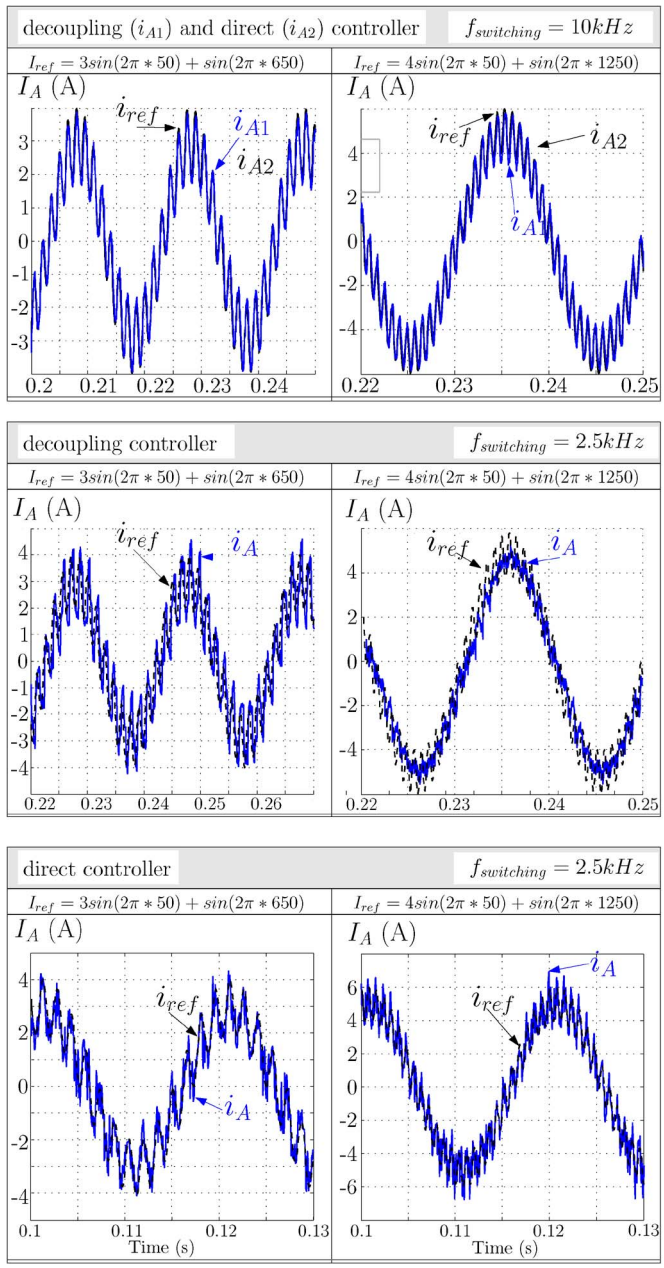

Fig. 12. Current tracking with decoupling PWM and direct control.

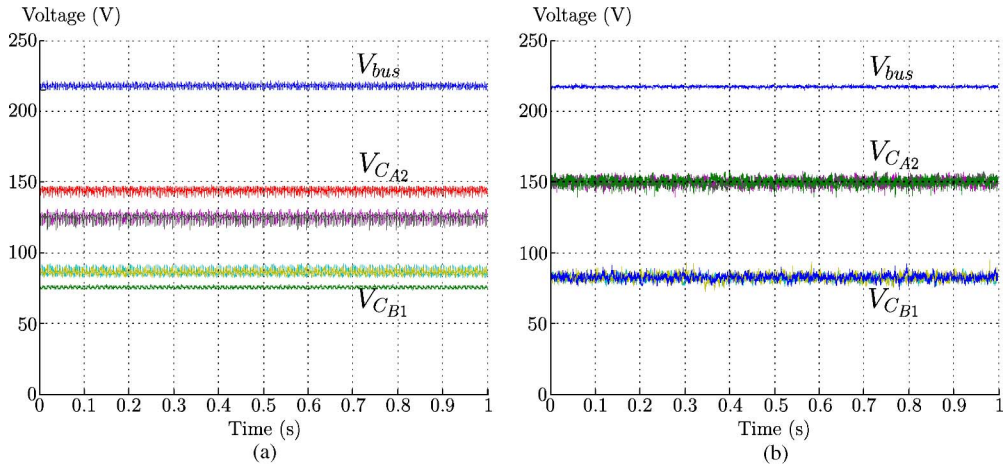

Fig. 13. FC voltage with (a) decoupling and (b) direct control.

value. The capacitor C_{i2} is charged to 350 V, and the capacitor C_{i1} is charged to a voltage of about 175 V. Power switches can withstand a dV/dt up to 200 V. The fast dynamic for the precharge of the capacitors of the three phases can be appreciated. The precharge time is about 0.1 s, which is a very good result. After 0.397 s, the start-up resistances, connected between the filter and the grid, are removed from the system.

B. Comparison of Voltage-Balancing Methods and Current Control

In order to demonstrate the benefits of the direct control, different tests have been carried out. The current regulation is carried out by a proportional–integral (PI) controller for the decoupling voltage balancing (Fig. 3). For the direct control, the predictive controller presented in Section III is combined with the direct control of IGBTs. Some results are shown in Fig. 12 for two switching frequency values (10 and 2.5 kHz) and reference currents with two different harmonics components (1 A at 650 and 1250 Hz).

Results for a 10-kHz switching frequency are quite similar for both methods [Fig. 12 (top)], but those obtained for 2.5 kHz are different. The current tracking is not satisfactory for the decoupling method [Fig. 12 (middle)], whereas the regulation is correct with the direct control for the same switching frequency [Fig. 12 (bottom)].

In addition, the balancing of FC voltages is also better with the direct control [Fig. 13(b)] with a switching frequency of 2.5 kHz and a reference current with a component at 1250 Hz of 1 A. The decoupling method is not able to balance the capacitor voltages [Fig. 13(a)], due to the low ratio between the switching frequency and the highest frequency of the reference current, and the low FC values (200 μF).

Another test is made considering a reference composed of many current harmonics

$$I_{\max(250\,\mathrm{Hz})} = I_{\max(350\,\mathrm{Hz})} = I_{\max(550\,\mathrm{Hz})} = 1\ \mathrm{A}$$
$$I_{\max(650\,\mathrm{Hz})} = I_{\max(750\,\mathrm{Hz})} = 0.75\ \mathrm{A}$$
$$I_{\max(950\,\mathrm{Hz})} = I_{\max(1150\,\mathrm{Hz})} = I_{\max(1250\,\mathrm{Hz})} = 0.5\ \mathrm{A}.$$

As before, two cases are considered: one with a switching frequency of 10 kHz (Fig. 14) and another with 2.5 kHz (Fig. 15), applied to both control strategies. The fast Fourier transform (FFT) analysis is very important for understanding what happens.

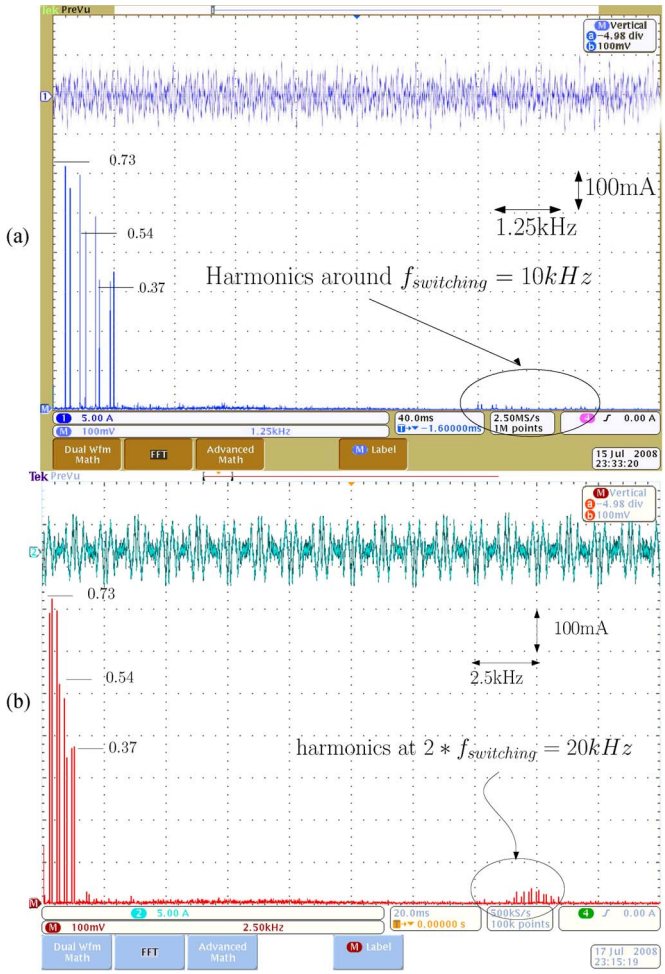

Fig. 14. FFT of direct current for a 10-kHz switching frequency for (a) decoupling control and (b) direct control.

With the decoupling control based on the PWM control of IGBTs, there are no harmonics around $f_{\mathrm{switching}}$ and $2 * f_{\mathrm{switching}}$. All the harmonics due to the switching frequency are concentrated around $3 * f_{\mathrm{switching}}$.

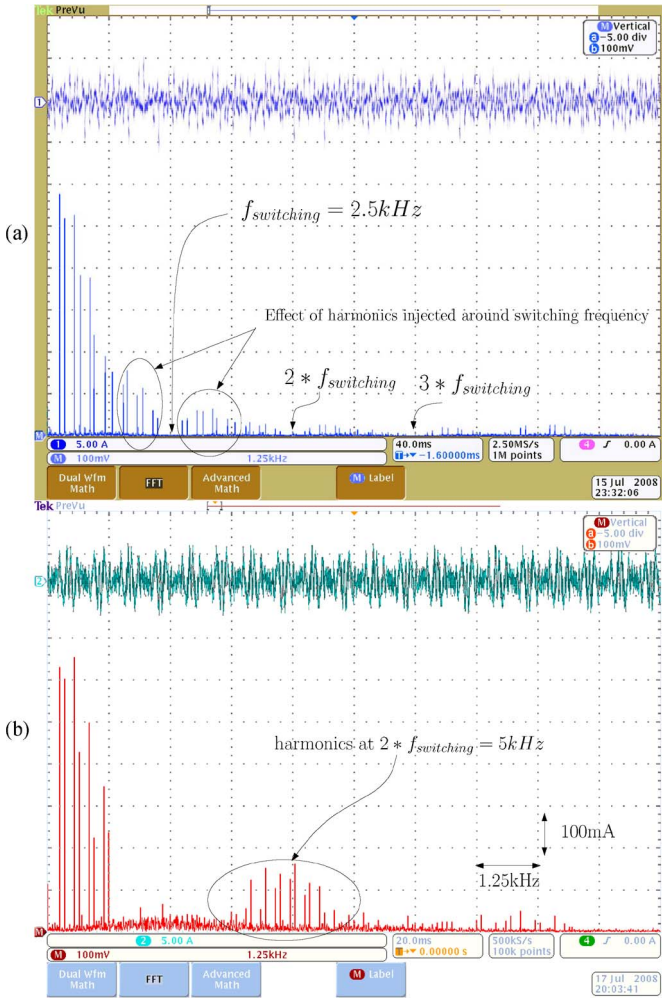

Fig. 15. FFT of direct current for a 2.5-kHz switching frequency for (a) decoupling control and (b) direct control.

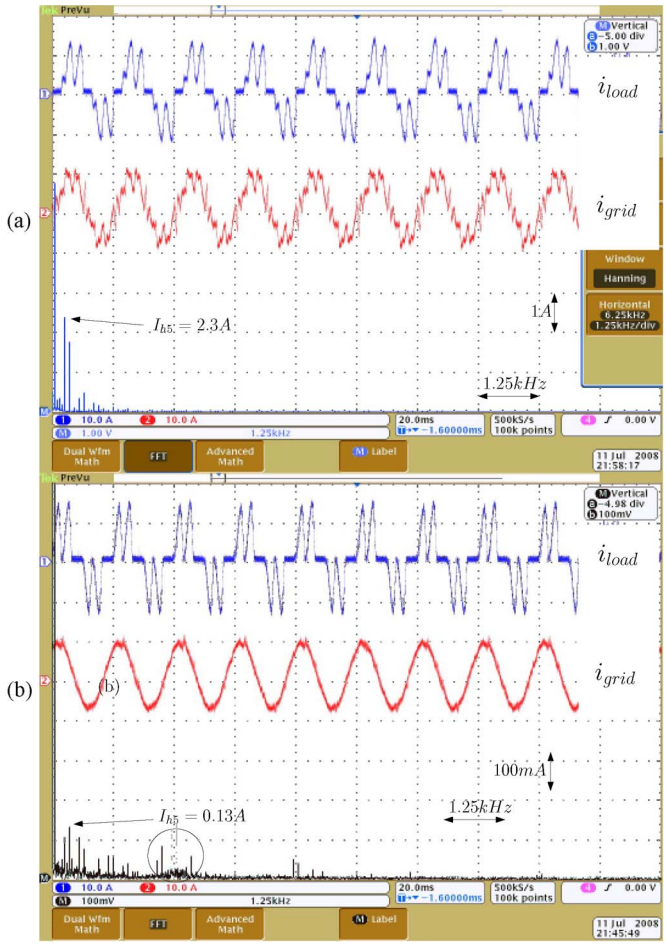

Fig. 16. Harmonics filtering with (a) decoupling control and (b) direct control.

For the direct control, harmonics are located around $2 * f_{\text{switching}}$, as defined in the constraints of the sequence-table definition. The FFT analysis gives the rms value of current harmonics, and for a 10-kHz switching frequency, which is a high value, both control methods perform well (Fig. 14). However, the results are different for a lower switching frequency.

Fig. 15(a) shows the response of the inverter with a switching frequency of 2.5 kHz. Compared with the previous case, the harmonics are constrained around $3 * f_{\text{switching}}$. Current harmonics appear around $f_{\text{switching}}$ and below. This is principally due to the intermodulation harmonics located at $(f_{\text{switching}} - f_{\text{ref}})$ and $(f_{\text{switching}} + f_{\text{ref}})$, which are too important in this case. The ratio between $f_{\text{switching}}$ and f_{ref} is low, and the FCs are only of 200 μF.

Fig. 15(b) shows the results with the direct control of the inverter. In this case, the harmonics are constrained around $2 * f_{\text{switching}}$. As a result, the current tracking is good, and the FC voltages are correctly balanced.

C. Results for Shunt Active Filtering Operation

In this section, the superior performance of the proposed direct control scheme applied to a shunt active power filter based on an FC inverter is presented. Results with the PI controller [18] adapted for active filtering operation are also presented, for the same switching frequency (2.5 kHz). Fig. 16 shows the experimental results for both control strategies. The load is composed of a diode rectifier with a shunt RC load ($C = 3$ mF) and large inductors ($L = 2$ mH) at the input, with a current total harmonic distortion (THD) of 46%. In this figure, the load current, the grid current, and the FFT analysis are presented for both control methods. The direct predictive control allows the THD to be reduced to 3.8%. The PI controller is not able to compensate correctly the harmonics of the load currents (THD about 32%) due to the low sampling frequency and provokes a disturbance on the voltage laboratory grid, which implies that the load currents are not exactly the same in Fig. 16. The excellent bandwidth of the proposed direct predictive control, considered as the ratio between the switching frequency and the highest frequency of the inverter output current, is proven, since the current harmonics are around 5 kHz. In the case of the decoupling control, they are at only 2.5 kHz, considerably disturbing the injected currents.

D. Dynamic Response

To test the robustness of the direct control, a load variation of 100% was made to study the dynamic response of the direct predictive controller for the active filtering operation. The load

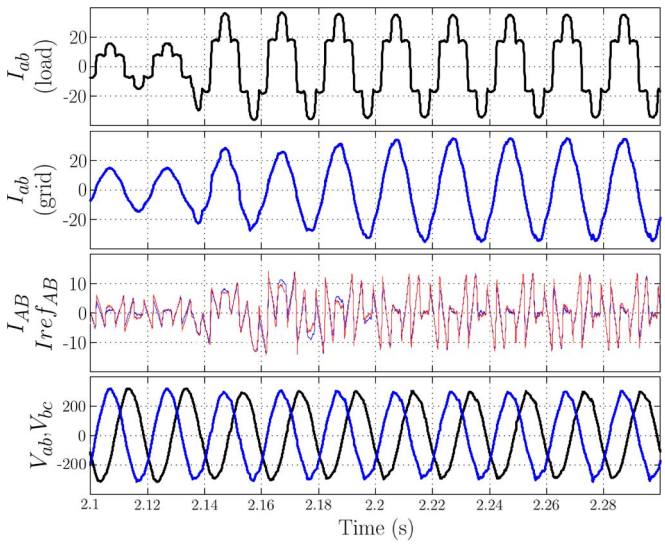

Fig. 17. Composed load, filter, and grid currents between phases A and B.

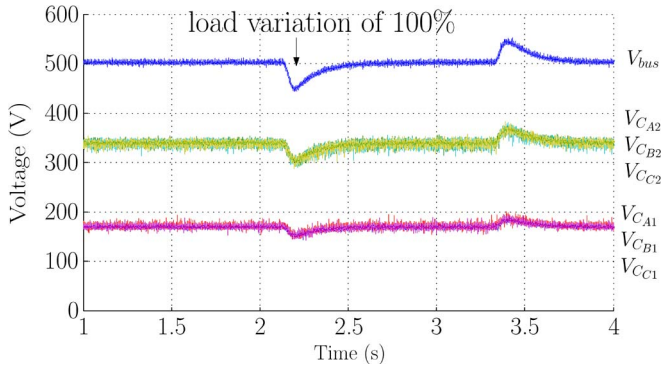

Fig. 18. Capacitor voltage balancing.

current, the grid current, and the injected current in a composed voltage reference frame are shown in Fig. 17. This disturbance is compensated after only one grid period, which means that the dynamic response is quite acceptable for this active filtering application.

Fig. 18 shows the capacitor voltage balancing during the load variation. The first variation is about $+100\%$, and the second is about -50%. The FC voltages are correctly balanced in a 5% interval with only 200-μF capacitors.

V. Conclusion

The use of direct predictive control in a four-level FC inverter has been discussed in this paper. The gating patterns are generated without any modulation, just using sequence tables calculated offline. The approach for defining the sequence tables to achieve high bandwidths for a current-controlled converter, while operating with low switching frequencies and reduced dv/dt in the output voltage, has been presented. Its superior performance with respect to a conventional PWM control has been demonstrated by means of simulations and experimentally. First, it allows better balancing of the capacitor voltages both in steady-state and in transient conditions. Second, it does not produce interharmonics, which is a key feature for active power filter applications operating with low switching frequencies. This control method obtains the maximum performances of the FC, making a good compromise between the switching frequency, the FC values, and the capabilities of the FC inverter.

References

[1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[3] D. Krug, S. Bernet, S. Fazel, K. Jalili, and M. Malinowski, "Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2979–2992, Dec. 2007.

[4] T. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.

[5] D. Krug, M. Malinowski, and S. Bernet, "Design and comparison of medium voltage multi-level converters for industry applications," in *Conf. Rec. 39th IEEE IAS Annu. Meeting*, 2004, vol. 2, pp. 781–790.

[6] C. Martins, X. Roboam, T. Meynard, and A. Carvalho, "Switching frequency imposition and ripple reduction in DTC drives by using a multilevel converter," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 286–297, Mar. 2002.

[7] T. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 356–364, Jun. 1997.

[8] A. BenAbdelghani, C. Martins, X. Roboam, and T. Meynard, "Use of extra degrees of freedom in multilevel drives," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 965–977, Oct. 2002.

[9] R. H. Wilkinson, T. H. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The general case," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1658–1666, Nov. 2006.

[10] B. McGrath and D. Holmes, "Analytical determination of the capacitor voltage balancing dynamics for three phase flying capacitor converters," in *Conf. Rec. 42nd IEEE IAS Annu. Meeting*, Sep. 23–27, 2007, pp. 1974–1981.

[11] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. Meynard, "Multicell converters: Active control and observation of flying-capacitor voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 998–1008, Oct. 2002.

[12] A. Donzel and G. Bornard, "New control law for capacitor voltage balance in multilevel inverter with switching rate control (CVC)," in *Proc. IEEE Power Electron. Spec. Conf.*, 2000, pp. 2037–2044.

[13] B. McGrath, T. Meynard, G. Gateau, and D. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.

[14] F. Defay, A. Llor, and M. Fadel, "A predictive control with flying capacitor balancing of a multicell active power filter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3212–3220, Sep. 2008.

[15] A. Shukla, A. Ghosh, and A. Joshi, "Improved multilevel hysteresis current regulation and capacitor voltage balancing schemes for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 518–529, Mar. 2008.

[16] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted PWM control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 178–185, Jan. 2007.

[17] S. Thielemans, T. Vyncke, and J. Melkebeek, "Balancing and harmonic analysis of flying capacitor multilevel converters," in *Proc. IEEE 25th Conv. IEEEI*, Dec. 2008, pp. 609–613.

[18] O. Tachon, M. Fadel, and T. Meynard, "Control of series multicell converters by linear state feedback decoupling," in *Proc. EPE Conf.*, 1997, pp. 1.588–1.593.

[19] E. Silva, B. McGrath, D. Quevedo, and G. Goodwin, "Predictive control of a flying capacitor converter," in *Proc. ACC*, Jul. 2007, pp. 3763–3768.

[20] P. Zanchetta, D. B. Gerry, V. G. Monopoli, J. C. Clare, and P. W. Wheeler, "Predictive current control for multilevel active rectifiers with reduced switching frequency," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 163–172, Jan. 2008.

[21] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive control of a three-phase neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2697–2705, Oct. 2007.

[22] P. Lezana, R. Aguilera, and D. E. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1839–1846, Jun. 2009.
[23] S. B. Ozturk, O. Yang, and H. A. Toliyat, "Power factor correction of direct torque controlled brushless DC motor drive," in *Conf. Rec. 42nd IEEE IAS Annu. Meeting*, Sep. 23–27, 2007, pp. 297–304.
[24] F. Defay, A. Llor, and M. Fadel, "An active power filter using a sensorless multicell inverter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 4–7, 2007, pp. 679–684.
[25] S. Loudot, "Filtrage actif des rseaux moyenne tension," Ph.D. dissertation, ENSEEIHT Eng. School, Institut National Polytechnique de Toulouse, Toulouse, France, 1997.

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