Low-Frequency Noise Impact on CMOS Image Sensors

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***Abstract*— CMOS image sensors are nowadays extensively used in imaging applications even for high-end applications. This is really possible thanks to a reduction of noise obtained, among others, by Correlated Double Sampling (CDS) readout. Random Telegraph Signal (RTS) noise has thus become an issue for low light level applications especially in the context of downscaling transistor size. This paper describes the analysis of in-pixel source follower transistor RTS noise filtering by CDS circuit. The measurement of a non Gaussian distribution with a positive skew of image sensor output noise is analysed. Impact of dimensions (W and L) of the in-pixel source follower is demonstrated. Circuit to circuit pixel output noise dispersion on 12 circuits coming from 3 different wafers is also analysed and weak dispersion is seen.**

***Keywords*—Low-frequency noise, CMOS image sensor, RTS noise, Correlated double sampling, noise dispersion**

I. Introduction

CMOS image sensors are nowadays widely used in commercial applications and even for space applications [1]. The use of CMOS standard processes for image sensors, developed for digital and mixed signal applications, are really attractive particularly for their low power consumption, applicability for on-chip signal processing [2] and large availability. During last ten years, lots of works have been done in order to improve image sensor performances to a very high level. These performances have been significantly enhanced with the use of CIS (CMOS image sensor) processes [3], [4], [5].

Image sensor key parameters are Quantum Efficiency (QE), Conversion Gain (CG), Full Well Capacity (FWC), Dark Current (DC), Noise, Photo-Response and Dark Signal Non-Uniformity (respectively PRNU and DSNU) and Modulation Transfer Function (MTF). In order to increase the pixel photosensitive area, the use of aggressive technologies and small MOS transistors in the pixel are required. That leads to an increase of MOS transistor low frequency noise. The use of 4T photodiode pixels, also known as “pinned” photodiode, and a Correlated Double Sampling (CDS) circuit and its associated readout mode allow the elimination of the photodiode reset noise (KTC noise) which is usually the major noise contributor. This noise reduction reveals the Random Telegraph Signal (RTS) noise impact of the in-pixel source follower transistor. This RTS noise becomes an issue for the low light sensitivity applications [6].

The first part of section II gives a description of the low frequency noise and particularly the RTS noise and its parameters. Then, standard CMOS image sensor architecture with CDS readout mode and noise sources are described. The last part of this section is devoted to the impact of RTS noise of in-pixel source follower transistor on the sensor output noise response. Section III presents the test vehicle and the noise measurement results. Circuit to circuit noise response dispersion is also given. Section IV is dedicated to the impact of the in-pixel source follower transistor size on the output noise response of the test vehicle. Cumulative histograms of noise output response are analysed in order to find ways to reduce RTS noise impacts. Finally, in section V, a conclusion is done and the perspectives of this work are given.

II. Low Frequency Noise in CMOS Image Sensors

A. Low Frequency noise and RTS Noise Modelling

The use of large area MOS transistors leads to low frequency noise (LFN) showing a 1/f Power Spectral Density (PSD). This is well characterized by the use of appropriate models known as McWhorter model [7] dealing with carrier number fluctuation, Hooge model [8] dealing with mobility fluctuation or the unified model [9] dealing with carrier number fluctuation inducing mobility fluctuation.

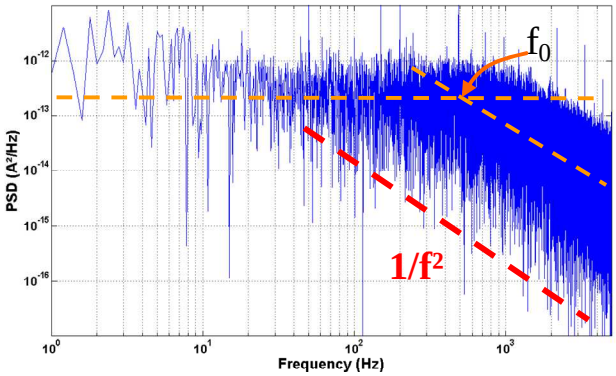


Fig. 1 : Power Spectral Density of a small MOS transistor with RTS noise coming from one defect at Si/SiO2 interface

For small devices (gate area<1µm²), LFN does not show a 1/f PSD. The carrier number becomes small and trapping/detrapping events, caused by individual interface defects at Si/SiO2 interface, yields to discrete drain current

fluctuations. In the case of one defect, the PSD becomes a lorentzian spectrum. Fig. 1 illustrates the PSD measured for a small MOS transistor (gate area<1µm²) in UMC 0.35 µm CIS technology. This result confirms the lorentzian spectrum depicted by the following PSD:

$$S_{LORENTZIAN} = \frac{A}{1+\left(\frac{f}{f_0}\right)^2}$$

Where : A is a constant
f_0 is the corner frequency

Temporal current fluctuation measurements were performed on the same MOS transistor and the results are shown in Fig. 2.

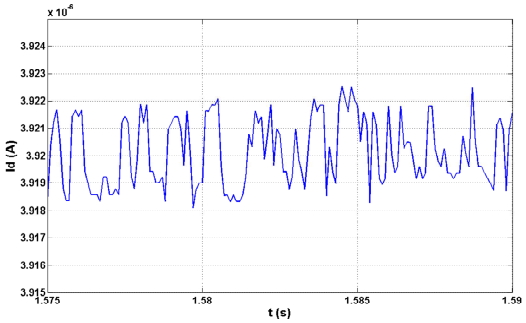
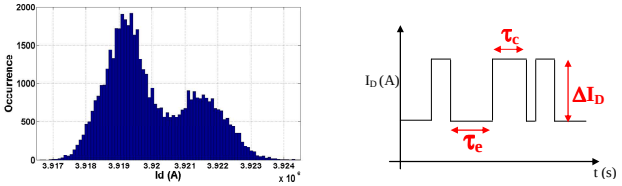


Fig. 2 : Temporal current fluctuations due to RTS noise

Fig. 2 depicts a two level RTS which is confirmed by the output signal temporal histogram in Fig. 3-a showing two peaks.



a) Signal temporal histogram b) Model

Fig. 3 : RTS noise example coming from one defect at Si/SiO2 interface of a small MOSFET

As can be seen in Fig. 3-b, three parameters can describe a two levels RTS noise: τ_e, the average carrier emission time, τ_c, the average carrier capture time and ΔI_D, the drain current RTS amplitude.

$$\tau_c = \frac{e^{\frac{\Delta E_B}{kT}}}{I_D T \sigma_0 \chi} \quad (1) \qquad \tau_e = \frac{e^{\frac{\Delta E_B + \Delta E_{CT}}{kT}}}{T^2 \sigma_0 \eta} \quad (2)$$

$$\frac{\Delta I_D}{I_D} = \eta \frac{g_m}{I_D} \cdot \frac{q}{WLC_{OX}} \cdot \left(1 - \frac{x_t}{t_{OX}}\right) \quad (3)$$

Equations (1), (2) and (3), [10] and [11], depict these parameters where ΔE_B is the trap energy level, ΔE_{CT} is the difference between energy levels of conduction band and trap, σ_0 is the trap section, x_T is the distance between trap and Si/SiO2 interface, t_{OX} is the gate oxide thickness, T is the temperature, k is the Boltzman constant, I_D is the MOSFET drain current, gm is the MOSFET transconductance, W and L are the MOSFET dimensions and η and χ are fabrication process constants.

The probability of trap occupancy (PTO) [12], shown by equation (4), can be deduced from equations (1) and (2).

$$P(t) = \frac{\tau_e}{\tau_e + \tau_c} + K.e^{-\left(\frac{1}{\tau_e}+\frac{1}{\tau_c}\right).t} \quad (4)$$

This equation (4) depicts the trap probability to be occupied at every moment. In steady state, the PTO becomes $\tau_e/(\tau_e+\tau_c)$.

In multiple level RTS noise, 2^N discrete levels of drain current can be observed with N being the number of trap.

In order to model the impact of RTS noise on the CMOS image sensor noise response, a detailed description of sensor architecture and readout sequence is done in the next part of this section.

B. CMOS image sensor architecture and readout sequence

A common CMOS image sensor readout circuit architecture is shown in Fig. 4. It is composed of:

- a photo-element : a photodiode, or a pinned photodiode associated with a transfer gate
- a reset switch allowing to reset the photo-element or the readout node
- an in-pixel source follower which drives the signal from pixel to column readout circuit
- a double sample and hold circuit for reference and integrated signal level
- an output stage allowing to drive the signal off chip or on chip for additional processing

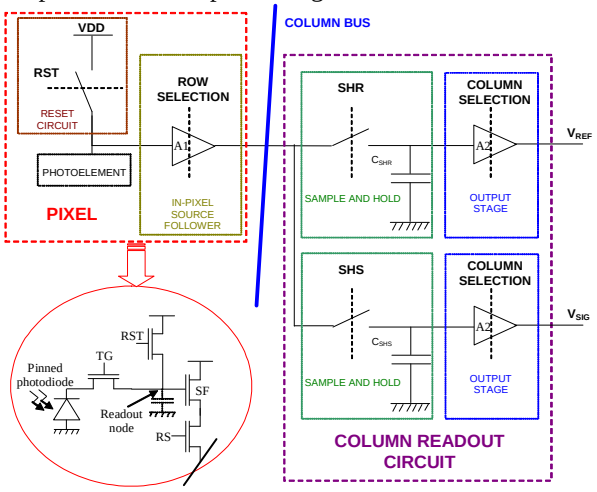


Fig. 4: Common readout circuit architecture of a CMOS image sensor

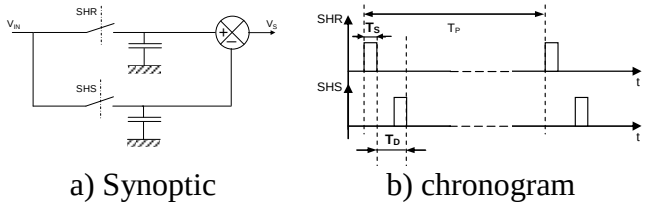
For a pinned photodiode pixel, before the beginning of the integration time, the photodiode is emptied by charge transfer mechanism. Before the end of integration time, the readout node is reset by the reset MOSFET (command signal RST). This level, called reference, is sampled and held (command signal SHR) in the column readout circuit in the reference channel via the in-pixel source follower. At the end of the integration time, charges integrated in the photodiode are transferred (command signal TG) in the readout node. The voltage level corresponding to the integrated charges is

sampled and held (command signal SHS) in the column readout circuit of the signal channel. Video signal voltage level results from the subtraction of the two samples (reference and signal). Thus, CDS readout is done by this sequence. CDS readout allows:

- to eliminate reset noise coming from the reset of the readout node (capacitance) due to RST transistor thermal noise
- to remove pixel to pixel Fixed Pattern Noise (FPN) due to in-pixel source follower offset dispersion from pixel to pixel
- to reduce low frequency noise by CDS high pass filtering function.

Equation (5) shows the time domain operation carried out by the CDS circuit and the chronogram depicted in Fig. 5.

$$V_S(t) = V_{IN}(t).[\delta(t) - \delta(t - T_D)] \qquad (5)$$



a) Synoptic b) chronogram

Fig. 5: Synoptic and chronogram of CDS system

C. RTS noise impact on CMOS image sensor noise response

As can be seen in §II-B, CDS principle requires two samples which are provided by the in-pixel source follower transistor. If this transistor produces significant RTS noise, the pixel voltage response at the image sensor output shows different levels areas as depicted in the output signal temporal histogram (Fig. 6)[13]. Reference level and voltage level corresponding to the integrated charges are the two samples taken at different moment.

This result comes from a test image sensor using 3T photodiodes and designed in UMC CIS 0.35µm (described in section III). A special sequence allows the CDS readout.

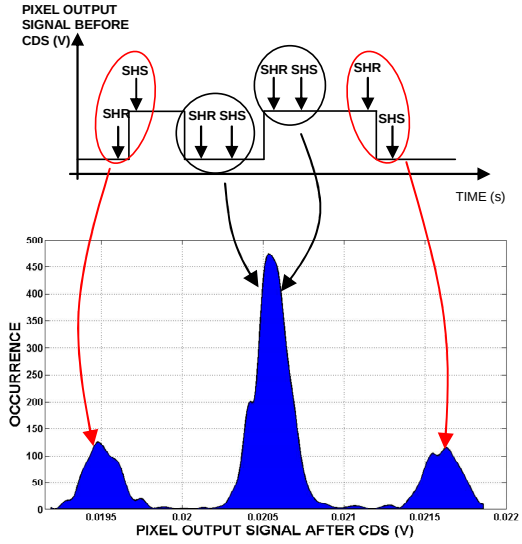


Fig. 6: Histogram of a pixel output signal subject to significant RTS noise of in-pixel source follower transistor

For a two level RTS noise, three states can be seen. These three states correspond to the four ways that the samples are affected by RTS noise.

The histogram shown in Fig. 7 presents the noise spatial distribution at the sensor output. It has a non-gaussian shape with a positive skew. This positive skew comes from the significant RTS noise of the in-pixel source follower impacting on the image sensor output noise response. This is a feature of the RTS noise impact [6].

The next sections deal firstly with the description of the test image sensor used and impact of circuit to circuit dispersion on the pixel output noise distribution. Then, the pixel noise distribution, affected by the RTS noise, is analysed with regard to the in-pixel source follower size impact. This impact is also analysed with regards to circuit to circuit dispersion.

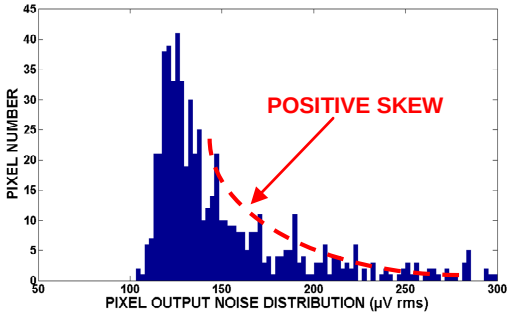


Fig. 7: Pixel output noise distribution at the sensor output

III. Circuit to Circuit Dispersion Impact on Pixel Output Noise Distribution

A. Test Image Sensor Description

The test image sensor of 3T photodiode pixels is a multi-linear sensor with 1 double line and 9 single lines dedicated to pushbroom image acquisition. Pixel pitch of the double line is 7.5µm. Single lines are composed of various pixel pitches: 7.5µm, 15µm and 15x45µm. Reset noise is eliminated thanks to a special sequence allowing CDS readout. Two single lines, with 7.5µm, are dedicated to noise analysis and specially RTS noise analysis. These single lines are composed of 4 groups (638 pixels) of pixels with different in-pixel source follower sizes (W/L). So, eight in-pixel source follower size variations are designed in this test vehicle (see Table 1).

TABLE I
IN-PIXEL SOURCE FOLLOWER SIZE VARIATIONS

	W/L IN MICRONS			
	PART N°1	**PART N°2**	**PART N°3**	**PART N°4**
LINE N°1	1.5/0.5	1.5/0.65	1.5/0.8	1.5/1
LINE N°2	1/0.5	1/0.65	1/0.8	1/1

Twelve circuits were tested from 3 different wafers:

- 7 circuits from wafer #4
- 4 circuits from wafer #5
- 1 circuit from wafer #1

Fig. 8 shows the packaged circuit photography.

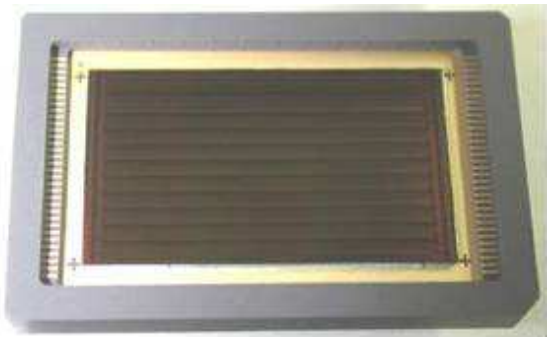


Fig. 8: Test image sensor microphotography

B. Pixel Output Noise Distribution Dispersion

Pixel output noise was measured on the 12 circuits from the different wafers in order to show the noise dispersion. Cumulative histogram with log scale is chosen to have the best view of the positive skew of the distribution which depicts the RTS noise behaviour. Fig. 9 illustrates the measurement results.

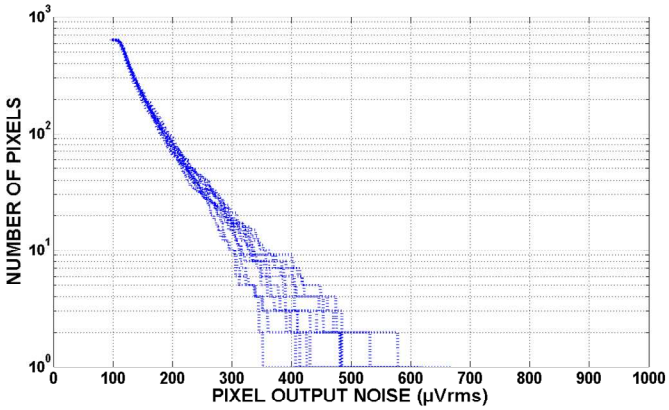


Fig. 9: Cumulative histogram of the pixel output noise dispersion from 12 circuits

It can be noted that dispersion of the pixel output noise distribution is weak. Only some very noisy pixels are spread at the end of the distributions. As a general rule, distribution is well-centred.

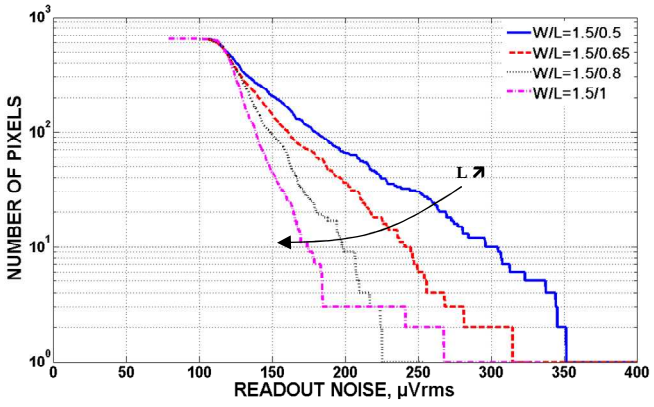


Fig. 10 : Cumulative histogram (log scale) of pixel output noise for W=1.5µm and L variations of in-pixel source follower transistor

IV. Pixel Output Noise Analysis in Function of the In-pixel Source Follower Size

Noise measurements were done with each different in-pixel source follower size. Cumulative histogram of pixel output noise for W=1.5µm and L variations (0.5 to 1µm) of the in-pixel source follower transistor is shown in Fig. 10.

As can be seen, distribution positive skews are not the same for the different W/L. These slopes increase as L dimension increases which means there are less noisy pixels (RTS noise amplitude decrease).

Same measurements were done with a fixed W of 1µm and a L variation (0.5 to 1µm). These measurement results are presented in Fig. 11. Once again, different slopes on the distribution skew are seen. The slopes increase with L dimension.

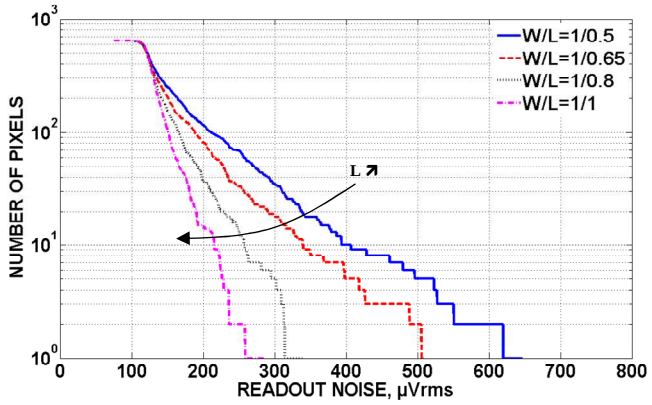


Fig. 11 : Cumulative histogram (log scale) of pixel output noise for W=1µm and L variations of in-pixel source follower transistor

A comparison between two W sizes can be found in Fig. 12. Again, the slope increase when W increases.

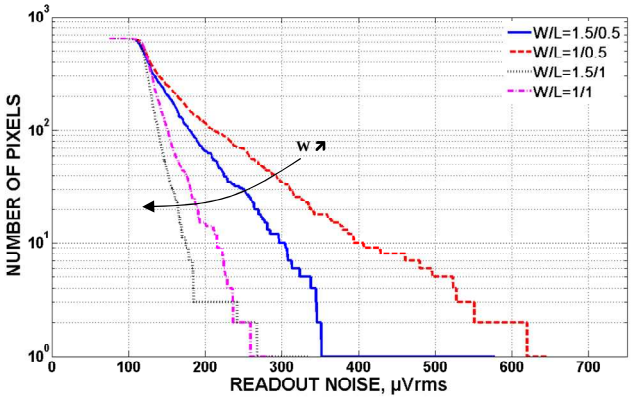


Fig. 12 : Comparison of cumulative histogram (log scale) of pixel output noise for W/L=1.5/0.5, W/L=1.5/1, W/L=1/0.5, W/L=1/ of the in-pixel source follower transistor

Our results indicate dependence of RTS noise amplitude on both W and L. Equation (6) shows this dependency (where α is a constant depending on the technology, biasing and trap location).

$$RTS_{AMPLITUDE} \approx \frac{\alpha}{W.L} \qquad (6)$$

Martin and al [12] show RTS noise dependence only with L dimension. Their work was based on single transistors. Our results, obtained from imagers, demonstrate RTS noise dependence with the both dimensions W and L, as already obtained by Lahav and al [15].

Same measurement on pixel output noise dispersion from circuit to circuit was done with the various in-pixel source follower size variations.Measurement results for W=1.5µm and L variations are shown in Fig. 13.

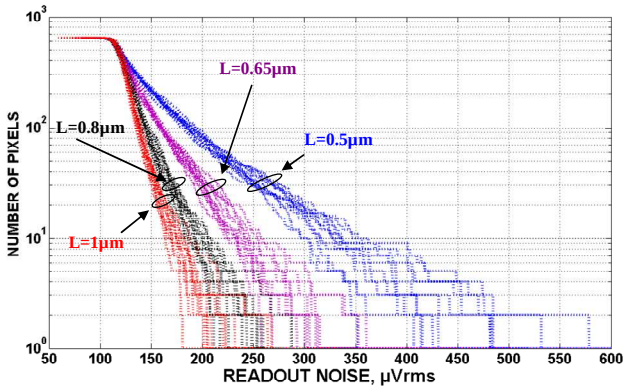


Fig. 13: Cumulative histogram of the pixel output noise dispersion from 12 circuits for W=1.5µm and L variations

The results show a clear tendency of the RTS noise reduction when L increases despite the circuit to circuit dispersion.

This is also confirmed by Fig. 14 showing the cumulative histogram of the pixel output noise dispersion from the twelve circuits for W=1µm and L variations.

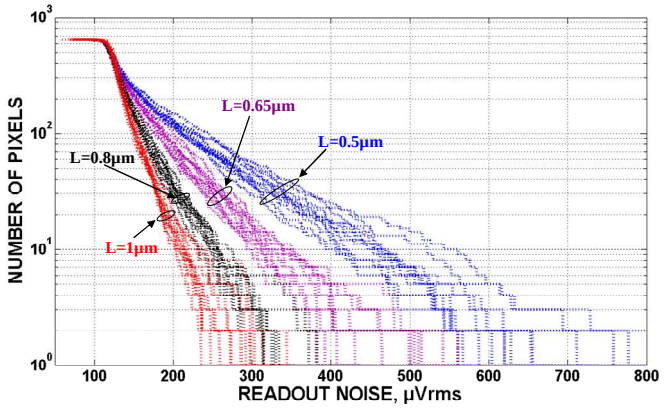


Fig. 14: Cumulative histogram of the pixel output noise dispersion from 12 circuits for W=1.5µm and L variations

V. Conclusions

This work shows the impact of the in-pixel source follower RTS noise on pixel output noise response. CDS filtering with regard to RTS noise is analysed. Measurement results show also a strong dependence of the RTS noise to L and W dimensions of the in-pixel source follower transistor. Increasing L and W decreases the noisy pixel number impacted by RTS noise. Circuit to circuit pixel output noise response is also studied. A clear tendency is demonstrated regarding RTS noise reduction when L and W increase whatever the circuit to circuit dispersion. This work gives several perspectives in order to understand the RTS noise mechanism. Future works will focus on the RTS noise distribution which can be deduced of pixel output noise histogram. This RTS noise distribution will help us to find a model for W and L variations.

Acknowledgment

The authors want to thank Paola Cervantes from ISAE/CIMI group, Saï Guiry and Michel Breart de Boisanger from EADS-Astrium for the measurements, Franck Corbiere and Nicolas Huger both from ISAE/CIMI group for the design of the test vehicle. The test image sensor was co-funded by ISAE and EADS-Astrium.

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