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Efficient optoelectronic de-embedding for VCSEL intrinsic response extraction

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Abstract — In this present work, we propose a new method to remove the parasitics contribution to the VCSEL chip response, in order to obtain the intrinsic transmission behavior. It has been observed that the S_{11} reflection coefficient of the chip is only due to the electrical access to the chip composed by the transmission line and cavity contacts. This allows us to decompose the chip into two cascaded subsystems representing the electrical access and the optical cavity respectively. An equivalent electrical circuit is developed for the electrical access behavior and, combined with the transfer matrix formalism, it becomes possible to remove the parasitics contribution from the measured S_{21} response. In this way, the intrinsic 3-dB bandwidth of the VCSEL can be determined.

I. INTRODUCTION

Long-wavelength Vertical-Cavity Surface-Emitting Lasers (VCSELs) operating in the $1.3\mu m - 1.6\mu m$ wavelength band are becoming available with high single-mode output power, high modulation frequency and large temperature range operation [1]. These devices appear to be low cost solutions for local-area and metropolitan optical fiber networks. Their characterization is then an important tool which can be used to optimize the fabrication process in order to obtain the best performance. Regarding the dynamic properties of VCSELs, we can notice that the frequency modulation response is not a classical second order system defined by the rate equations, even if coplanar access structures are used. The frequency modulation response is often limited by parasitics attributed to package, bonding and transmission line used to carry the electrical signal to the laser cavity. Several techniques have been investigated, to eliminate the parasitics contribution which limits the 3-dB bandwidth. Morton et al. [2] have presented a method using the frequency response subtraction, Majewski et al [3] have suggested the measurement of the relative intensity noise (RIN) and Söderberg et al. [4] have used a three-pole transfer function to model the device behavior under parasitics influence.

We propose a new method to remove parasitics to the measured dynamic response of any VCSELs chip. Our method

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[5] defines the VCSEL chip as a cascaded two-port subsystem that allows the separation of the VCSEL optical cavity response measurement from the total chip response. The electrical access is modeled using an electrical equivalent circuit that gives the parasitics response in terms of S-parameters. This contribution is removed from the measured S_{21} of the chip by applying the transfer matrix formalism and the intrinsic modulation 3-dB bandwidth can be determined.

II. EXPERIMENTAL SETUP

A. VCSELs structure

The devices used in our experiments are double intracavity contact VCSELs at 1.3μ m [6] and 1.55μ m [7] wavelengths. Their fabrication consists of an InGaAlAs quantum wells active region, a tunnel junction and AlGaAs-GaAs DBRs bonded to the active region by wafer-fusion. This fabrication approach is very useful because current passage is not provided through Bragg mirrors which allows to avoid VCSEL over heating problems. The threshold current for both wavelengths is around 2.2mA at room temperature and singlemode operation is achieved.

B. Experiments

Measurements of the S_{11} and S_{21} responses have been performed using an HP8510-C vector network analyzer (VNA) with an integrated optical rack. This rack allows the calibration of the integrated optical detector and isolates its contribution from the measurement process. The bias current and the high frequency signal were combined in the VNA bias-T and sent to the devices through RF probes. All parasitics not associated to the device under test are removed for stable and accurate measurements. The optical beam is then collected by a ball-lensed multimode fiber with ARcoating, tilted to avoid optical feedback. Finally, no temperature control was applied so all the measurements were carried-out at room temperature ($\approx 23^{\circ}$ C). The measured

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 S_{21} response of VCSEL chips emitting at 1.3µm and 1.55µm is presented in Fig. 1. The response slope is -18dB/octave which corresponds to a third-order system. Moreover, it can be observed that the response of the 1.55µm chip is strongly influenced by parasitics associated to the electrical access which diminishes the 3-dB bandwidth even before the resonance frequency. It is therefore difficult to obtain a good characterization of the intrinsic VCSEL behavior.



Figure 1: S_{21} responses of $1.3 \mu m$ (blue curve) and $1.55 \mu m$ (red curve) VCSEL chips.

III. THE DE-EMBEDDING PROCESS

The electrical access of the chip can meanwhile be separated from the measurements following the de-embedding method. The concept of this method is based on the electrical modeling of the VCSEL chip. Even if the electrical model of the active region is known [8], that of the entire chip is more complex to determine because of parasitics related to the electrical access. The equivalent electrical circuit defining the electrical access of the VCSEL chip is presented in Fig. 2.



Figure 2: Electrical Equivalent Circuit of the electrical access for both $1.3 \mu m$ and $1.55 \mu m$ chips.

Impedances Z_A and Z_B correspond to the transmission line and intra-cavity contacts whereas R_S represents the series resistance between intra-cavity contacts and the active region [9]. The equivalent circuit parameters of the electrical access (EA) are gathered into the Z–Matrix as follows:

$$Z_{EA} = \begin{pmatrix} Z_A + Z_B & Z_B \\ Z_B & Z_{RS} + Z_B \end{pmatrix}$$
(1)

$$S_{11EA} = (Z_{EA} + Z_0)^{-1} (Z_{EA} - Z_0)$$
(2)

where Z_0 is the characteristic impedance of the VNA. Parameters of the electrical circuit are fitted to S_{11} measurements using non-linear regression. Comparison between measured and simulated S_{11} are presented in Fig. 3 for both 1.3µm and 1.55µm wavelengths at a bias current of 9mA.



Figure 3: S_{11} comparison between measured (dots) and simulated (line) responses for both wavelengths.

Values of the circuit elements for simulations presented in Fig. 3 are summarized in table 1.

TABLE 1		
Circuit element	1.3µm VCSEL	1.55µm VCSEL
L _e (pH)	49.6	35.5
$R_{e}(\Omega)$	14.1	11.6
$C_e (pF)$	0.88	2.5
$R_{p}(\Omega)$	61.5	95
$C_p (pF)$	0.64	0.78
$R_{s}(\Omega)$	57.2	58

Results presented in Fig. 3 show that the chip S_{11} and the parasitics S_{11} are essentially the same which means that the incoming signal is not influenced by the VCSEL optical cavity (VOC). It then becomes possible to obtain all the S-parameters for the electrical access subsystem. The intrinsic response of the VCSEL could be extracted from the chip response using transfer function matrices, or T-Matrices, since S-Matrices are not commutative.

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The general formula for the transformation of an S-Matrix to a T-Matrix is given by [10]:

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \begin{pmatrix} \underline{S_{12}S_{21} - S_{11}S_{22}} & \underline{S_{11}} \\ S_{21} & S_{21} \\ -\underline{S_{22}} & \underline{1} \\ S_{21} & S_{21} \end{pmatrix}$$
(3)

The transfer matrix of the optical cavity is defined as follows:

$$T_{VOC} = T_{EA}^{-1} T_{tot} \tag{4}$$

where T_{EA} , T_{VOC} and T_{tot} are T-Matrices of the electrical access, the VCSEL optical cavity and the complete chip respectively. T_{tot} is calculated with the entire S-Matrix of the system S_{tot} . Out of the four matrix elements of S_{tot} , only the S_{11} and S_{21} are known as these two parameters were measured using the VNA.

The two other parameters S_{12} and S_{22} obey the following rules:

- The VCSEL is an active unilateral device so the S₁₂=0 (optical feedback is avoided using AR coated fibers);
- The VCSEL is a transducer that converts electrical current into optical power hence it is not bidirectional and does not respond to an electrical input at the optical output ports. The electrical S₂₂ parameter, therefore, is taken equal to 1;



Figure 4: Comparison of S_{21} responses with (Extracted) and without (Measured) the de-embedding method for the $1.3 \mu m$ VCSEL chip.

The resulting S-parameters matrix of the total chip is defined as:

$$S_{tot} = \begin{pmatrix} S_{11}^{m} & 0 \\ S_{21}^{m} & 1 \end{pmatrix}$$
(5)

Using (1) to (5), the electrical parasitics are removed from measurements and results are presented in Fig. 4 for the 1.3μ m chip and in Fig. 5 for the 1.55μ m chip.



Figure 5: Comparison of S_{21} responses with (Extracted) and without (Measured) the de-embedding method for the $1.55 \mu m$ VCSEL chip.

As is evident from Fig. 4 and 5, the measured S_{21} responses of the chips have a -60 dB/decade slope. This slope represents the response of the totality of the VCSEL chip which includes the electrical access and the VCSEL optical cavity, showing a system having an order greater than two. Furthermore, the order of the system can be observed by the dip in the S_{21} curve below the resonance frequency which demonstrates that the transmission line and intracavity contacts influence the overall VCSEL response.

With the method investigated, chip parasitics are removed from measurements and the intrinsic response of the VCSEL cavity is found following a classical second-order system with a -40 dB/decade slope. The resulting curve appears as if measurements were carried out directly at the cavity terminals.

This method also demonstrates that the S_{11} response of the VCSEL chip and the electrical access are essentially the same, implying that the incoming electrical signal is not influenced by the VCSEL optical cavity parameters. Moreover, this method has been applied to the entire current range and shows that the resistance R_s is the only bias current dependent element. This resistance decreases as the bias current increases because the current flow into the active region through the tunnel junction aperture becomes more intense. The extrinsic and intrinsic 3-dB modulation bandwidths are also presented in Fig. 6. Results show that the extrinsic bandwidth is lower than the intrinsic bandwidth and tends to saturate toward a limit defined by the electrical access of the chip. Finally, this method can be applied to any device if the electrical access could be properly modeled.



Figure 6: 3-dB bandwidth evolution as a function of bias current for the overall chips (dotted lines) and with the de-embedding method (solid lines) for both $1.3\mu m$ and $1.55\mu m$ wavelength.

IV. CONCLUSION

We have presented a new method to separate the VCSEL optical cavity S_{21} response from the VCSEL chip response by removing the electrical access contribution. It has been shown that this electrical access influences the transmission response and is responsible for the limitation of the 3-dB bandwidth. Our approach has been applied to two different VCSELs, one emitting at 1.3µm and the other at 1.55µm with different electrical access geometries. With an electrical equivalent model of the parasitics, we have shown that the chip S_{11} represents in fact the electrical access S_{11} . Therefore the chip could be considered as a cascaded two-port system. Since S-matrices are not commutative, T-matrices are used to extract

the intrinsic VCSEL optical cavity response which represents a classical second-order system, characteristic of laser cavities defined by the rate equations. This method allows then to determine the intrinsic 3-dB bandwidth of the VCSEL chips investigated and finally gives a useful tool to model the input stage of coplanar VCSELs.

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