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VCSEL Intrinsic Response Extraction Using T-Matrix Formalism

Alexandre Bacou, *Member, IEEE*, Ahmad Hayat, *Student Member, IEEE*,
Vladimir Iakovlev, Alexei Syrbu, *Senior Member, IEEE*, Angélique Rissons,
Jean-Claude Mollier, *Member, IEEE*, and Elie Kapon, *Fellow, IEEE*

Abstract—We present a new method to remove the parasitics contribution to the VCSEL chip response, in order to obtain the intrinsic S_{21} behavior. The on-chip VCSEL is defined as two cascaded two-port subsystems representing the electrical access and the VCSEL optical cavity respectively. S_{11} and S_{21} parameters measurements are carried-out using a probe station to characterize the chip response. An electrical equivalent circuit defining the behavior of the electrical access is combined with T-Matrix formalism to remove the parasitics contribution from the measured S_{21} response. Results allow us to determine the intrinsic 3-dB bandwidth of the VCSEL.

Index Terms—Long Wavelength VCSEL, electrical equivalent circuit, S-parameters, transfer function matrix

I. INTRODUCTION

VCSEL dynamic response characterization is often limited by parasitics attributed to package, bonding and transmission line used to carry the electrical signal to the laser cavity. Efforts have been made to minimize the parasitics contribution that limits the 3-dB bandwidth and has led to the fabrication of direct coplanar access VCSELs [1]. Despite this development and the fact that a probe station is used for characterization, the measured dynamic response corresponds to a third-order system implying that the electrical access affects the overall transmission.

Several techniques have been used to eliminate the parasitics contribution to dynamic response, such as RIN measurements [2], frequency response subtraction [3] or by fitting the response with a three-pole transfer function [4]. All these methods are efficient to extract the intrinsic properties of the laser but results obtained correspond to a fitting curve.

We propose a new method to remove parasitics to the measured dynamic response of a $1.3\mu\text{m}$ VCSEL chip. Our method defines the VCSEL chip as a cascaded two-port subsystem presented in Fig.1, that allows the separation of the VCSEL optical cavity response measurement from the total chip response. The electrical access is modeled using an electrical equivalent circuit that gives the parasitics response in terms of S-parameters. This contribution is removed from the measured S_{21} of the chip by applying the transfer matrices formalism and the corresponding result shows the well-established second-order system defined by the rate equations.

A. Bacou, A. Hayat, A. Rissons and J-C. Mollier are with DEOS, Institut Supérieur de l'Aéronautique et de l'Espace (ISAE), Université de Toulouse, Toulouse 31055, FRANCE (e-mail: alexandre.bacou@isae.fr). V. Iakovlev, A. Syrbu and E. Kapon are with BeamExpress S.A., Lausanne 1015, Switzerland (e-mail: vladimir.iakovlev@beamexpress.com).

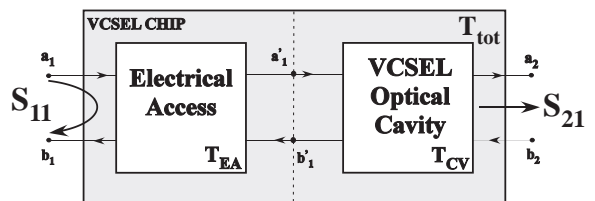


Fig. 1. Schematic representation of the VCSEL chip. The electrical access and the laser cavity are represented as two separate cascaded two-ports with distinct transfer functions.

II. EXPERIMENT

A. VCSEL Structure

The device used in our experiment is a double intracavity contact $1.3\mu\text{m}$ VCSEL [5]. It consists of an InGaAlAs quantum wells active region, a tunnel junction and AlGaAs-GaAs DBRs bonded by wafer-fusion. The threshold current is around 2.2mA at room temperature and the device operates in single-mode emission. Considering that the VCSEL is on-chip, we used a lensed fiber to couple the output optical power. The double intracavity contacts are very useful because they give a direct access to the optical cavity without current passage through Bragg mirrors.

B. Experimental Setup

Measurements of the S_{11} and S_{21} responses have been performed using an HP8510-C vector network analyzer (VNA) with an integrated optical rack. This rack permits the calibration of the optical detector and avoids its contribution to measurements. A probe station with RF probes was used for VNA calibration, giving a direct access to the chip. In this way, all parasitics not associated to the device under test are removed for stable and accurate measurements. The optical beam is then collected by a ball-lensed multimode fiber with AR-coating tilted to avoid optical feedback. Finally, no temperature control was applied so all measurements were carried-out at room temperature ($\approx 23^\circ\text{C}$). The measured S_{21} response of the chip is presented in Fig.2, showing the third-order system verified by the -18 dB/octave slope.

III. METHOD FOR PARASITICS REMOVAL

A. The Electrical Equivalent Circuit

The concept of our method is based on the electrical modeling of the VCSEL chip. Even if the electrical model of

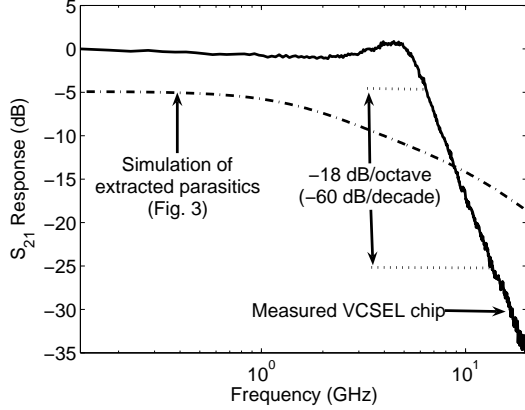


Fig. 2. S_{21} response of the chip (solid line) showing the third order system by the -60dB/Decade slope and the S_{21} simulation of extracted parasitics (dashed line).

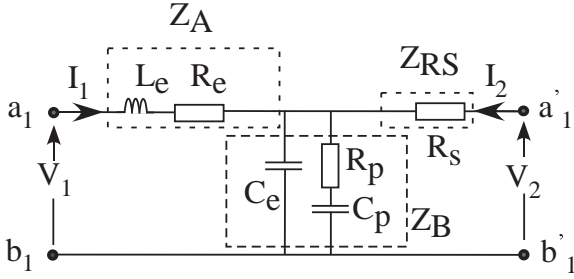


Fig. 3. Electrical Equivalent Circuit of the electrical access: $L_e=49.6\mu\text{H}$, $R_e = 14\Omega$, $C_e = 0.84\text{pF}$, $R_p = 64.6\Omega$, $C_p = 0.58\text{pF}$ and $R_s = 57.7\Omega$ for a bias current of $I/I_{th}=4.09$.

the active region is known to exist [6], that of the entire chip is more complex to determine because of parasitics related to the transmission line. An electrical equivalent circuit is used to model the electrical access of the chip and is presented in Fig.3.

Impedances Z_A and Z_B correspond to the transmission line and intracavity contacts whereas R_s represents the series resistance between intracavity contacts and the active region [7]. The equivalent circuit parameters of the electrical access are gathered into the Z -Matrix as follows:

$$Z_{EA} = \begin{pmatrix} Z_A + Z_B & Z_B \\ Z_B & Z_{RS} + Z_B \end{pmatrix} \quad (1)$$

The matrix S_{11EA} of this reciprocal two-port system can be calculated using the well-known relationship:

$$S_{11EA} = (Z_{EA} + Z_0)^{-1} \cdot (Z_{EA} - Z_0) \quad (2)$$

where Z_0 is the characteristic impedance of the VNA, so $Z_0=Z_{VNA}=50\Omega$. Parameters of the electrical circuit are fitted to S_{11} measurements using non-linear regression. Comparison between measured S_{11} and simulated parasitics S_{11} are presented in Fig.4 for the given bias current and good agreement between both curves is observed. This result shows that the chip S_{11} and the parasitics S_{11} are essentially the same. Therefore we can define the optical cavity and the electrical access separately using T-Matrix formalism.

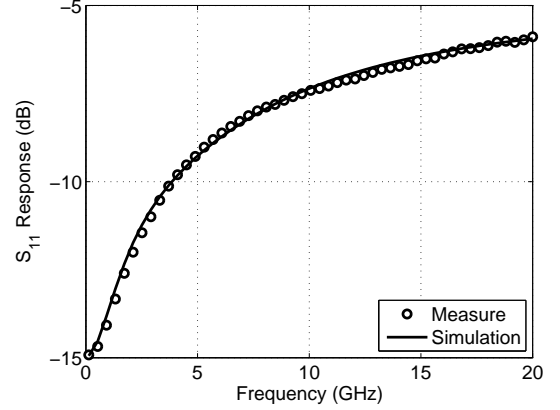


Fig. 4. The measured S_{11} response of the VCSEL chip is compared to the simulated S_{11} response of the electrical access subsystem. The equivalent electrical circuit parameters presented in Fig.3 are used for simulation.

B. The Transfer Matrix Technique

The intrinsic response of the VCSEL could be extracted from the chip response using transfer function matrices, or T -Matrices, since S -Matrices are not commutative. The general formula for the transformation of an S -Matrix to a T -Matrix is given by [8]:

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \begin{pmatrix} \frac{S_{12}S_{21}-S_{11}S_{22}}{S_{21}} & \frac{S_{11}}{S_{21}} \\ -\frac{S_{22}}{S_{21}} & \frac{1}{S_{21}} \end{pmatrix} \quad (3)$$

The T -Matrix corresponding to the VCSEL optical cavity can be calculated as follows:

$$T_{VOC} = T_{EA}^{-1} \cdot T_{tot} \quad (4)$$

where T_{EA} , T_{VOC} and T_{tot} are T -Matrices of the electrical access, the VCSEL optical cavity and the complete chip respectively (See Fig.1).

T_{tot} is calculated with the entire S -Matrix of the system S_{tot} . Out of the four matrix elements of S_{tot} , only the S_{11} and S_{21} are known as these two parameters were measured using the VNA. We found that the S_{12} and S_{22} entries obey the following two rules:

- 1) The VCSEL is an active unilateral device so the $S_{12}=0$ (optical feedback is avoided using AR coated fibers).
- 2) The VCSEL is a transducer that converts electrical current into optical power hence it is not bidirectional and does not respond to an electrical input at the optical output ports. The electrical S_{22} parameter, therefore, is taken equal to $\underline{1}$.

So, S_{tot} can then be written as follows:

$$S_{tot} = \begin{pmatrix} S_{11}^m & 0 \\ S_{21}^m & \underline{1} \end{pmatrix} \quad (5)$$

Where S_{11}^m and S_{21}^m refer to measured VCSEL responses. Therefore T_{tot} and T_{EA} are employed to calculate T_{VOC} with relations (3), (4) and (5). Then, the intrinsic S_{21} of the VCSEL is expressed using the T_{VOC} matrix. Results of the extraction are presented in Fig.5.

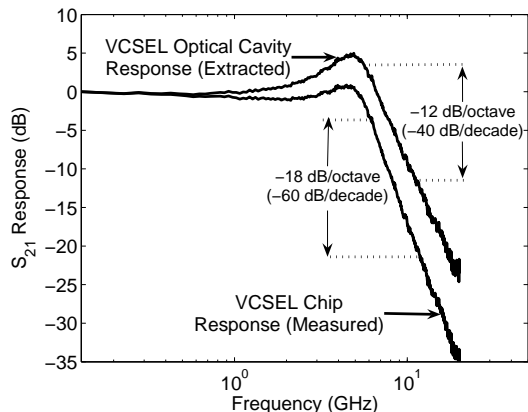


Fig. 5. Measured and extracted S_{21} responses for a $1.3\mu\text{m}$ VCSEL at a fixed bias current. The measurement takes into account the response of the electrical access as well as the cavity while the extracted curve shows the VCSEL cavity response only.

IV. RESULTS AND DISCUSSION

As is evident from Fig.2, the measured S_{21} response of the VCSEL has a -60 dB/decade slope. This slope represents the response of the totality of the VCSEL chip which includes the electrical access and the VCSEL optical cavity, showing a system having an order greater than two. Furthermore, this could be observed by the dip in the S_{21} curve below the resonance frequency and demonstrates that the transmission line and intracavity contacts influence the overall VCSEL response.

With the method investigated, chip parasitics are removed from measurements and the intrinsic response of the VCSEL cavity is found. The response follows the -40 dB/decade slope, which is characteristic of second-order systems, and is the same as if the measurements were carried out directly at the cavity terminals.

This method also demonstrates that the S_{11} response of the VCSEL chip and the electrical access are essentially the same, implying that the VCSEL optical cavity parameters do not influence the incoming electrical signal. Moreover, this method has been applied to the entire current range and shows that the resistance R_S is the only bias current dependent element. This resistance decreases as the bias current increases because the current flow into the active region through the tunnel junction aperture becomes more intense.

The extrinsic and intrinsic 3-dB modulation bandwidths are also presented in Fig.6. Results show that the extrinsic bandwidth is lower than the intrinsic bandwidth and tends to saturate toward a limit defined by the electrical access of the chip. The intrinsic response is also compared with curve generated by the relation in [2] and good agreement is found. Finally, this method can be applied to any device if the electrical access could be properly modelled.

V. CONCLUSION

We have presented a new method to separate the VCSEL optical cavity S_{21} response from the overall VCSEL chip response by removing the electrical access contribution. This

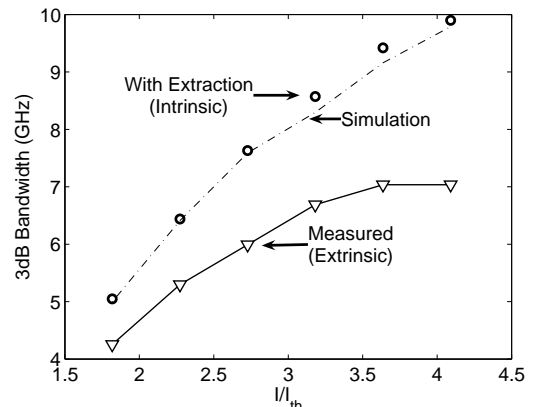


Fig. 6. 3-dB modulation bandwidth of extrinsic (measured) and intrinsic (T-Matrix extraction) responses as a function of bias current for the $1.3\mu\text{m}$ VCSEL. The dashed line correspond to the simulation of the 3-dB bandwidth by the relation taken from [2].

electrical access influences the transmission response and modifies the order of the system. These parasitics are modeled using an electrical equivalent circuit and have shown that the chip S_{11} represents in fact the electrical access S_{11} . Therefore the chip could be considered as a cascaded two-port system allowing us to use the T-Matrix formalism to extract the intrinsic VCSEL optical cavity response. This extraction represents a classical second-order system that is characteristic of laser cavities defined by the rate equations. Finally, The approach employed uses simple measurement and calculation methodology.

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