High performances monolithic CMOS detectors for space applications

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ABSTRACT

During the last 10 years, research about CMOS image sensors (also called APS -Active Pixel Sensors) has been intensively carried out, in order to offer an alternative to CCDs as image sensors. This is particularly the case for space applications as CMOS image sensors feature characteristics which are obviously of interest for flight hardware: parallel or semi-parallel architecture, on chip control and processing electronics, low power dissipation, high level of radiation tolerance...

Many image sensor companies, institutes and laboratories have demonstrated the compatibility of CMOS image sensors with consumer applications: micro-cameras, video-conferencing, digital-still cameras. And recent designs have shown that APS is getting closer to the CCD in terms of performance level. However, the large majority of the existing products do not offer the specific features which are required for many space applications. ASTRI1JM and SUPAERO/CIMI have decided to work together in view of developing CMOS image sensors dedicated to space business. After a brief presentation of the team organisation for space image sensor design and production, the latest results of a high performances 512x512 pixels CMOS device characterisation are presented with emphasis on the achieved electro-optical performance. Finally, the on going and short-term coming activities of the team are discussed.

Keywords: APS, space, CMOS, cameras, image sensors

1. INTRODUCTION

Thanks to the past 10 years intensive work, maturity of the CMOS image sensors is now well established and these detectors are no more laboratory prototypes and are getting currently used in consumer electronics. As the European leader for industrial space activities, Astrium started works on CMOS image sensors in the mid-90s. Indeed, as foreseen by designers of optical instruments and sensors for space applications, such detectors could offer large advantages for many space applications when compared to CCDs. (Figure 1).

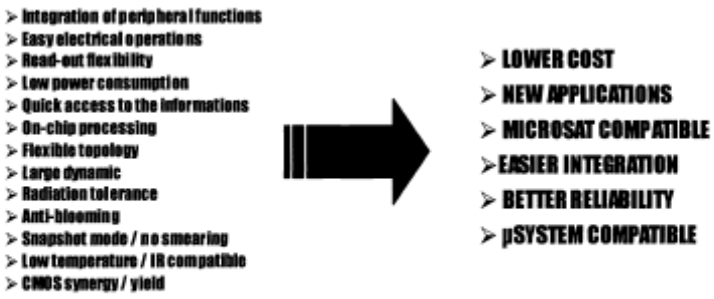


Figure 1: CMOS image sensor characteristics lead to strong system advantages

When looking at the CMOS image sensor market, nearly all the existing products are designed for consumer electronics applications (digital cameras, toys, webcams, cellphones...) and feature characteristics which are not compatible with space application requirements: low fill factor, medium quality colour filters, low dynamic. .. In addition, and as shown on figure 1, important advantages for CMOS sensors are linked to their capabilities to perfectly fit a given application thanks to dedicated read-out mode, topology and integrated electronics/processing. For these two reasons, Astrium decided in 1996 to be in position of mastering the design of CMOS image sensors (following an "ASIC-like" philosophy) in order to prepare the next generation of optical instruments and sensors.

2. THE COOPERATION BETWEEN SIJPAERO/CIMI AND ASTRIUM

The CIMI (Conception d'Imageurs Matriciels Intégrés) group from Supaéro is developing high electro-optical performances CMOS image sensors since 1994 [1], having all the in-house capabilities for their design. Collaboration between Supaéro/CIMI and Astrium started in 1996 in order to develop CMOS detectors for space applications (the Supaéro/CIMI team being at the same time involved in other applicative fields). Emphasis is given on high-level performance and compatibility with severe space environment. As shown below (Figure 2, summarising the organisation of the team), Supaéro/CIPvH is mainly responsible for: (i) research, R&D survey and modelling works (ii) architecture/detailed design (iii) breadboarding activities. Recent research work concerns particularly noise analysis and optimisation [2,3] ,FPN reduction and column readout circuits [4,5], quantum efficiency and MTF improvements. Astrium main tasks are: (i) detector architecture/processing and corresponding specification (ii) packaging/integration (iii) characterisationl/qualification (iv) industrialisation and sales. Delivery of already existing Supaéro/Astrium devices or of new products for space applications are open to any customer demands.

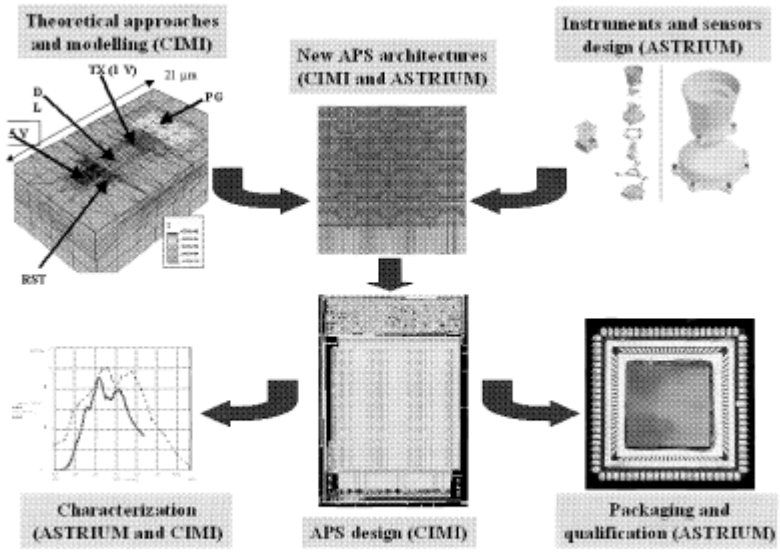


Figure 2: organisation of the Supaéro/Astrium team for development of CMOS image sensor for space applications

3. CMOS512 IMAGE SENSOR DEVELOPMENT AND PERFORMANCES

The CMOS512 image sensor (Figure 3-a) has mainly been designed for sensor applications (star tracker, optical telecommunication. ..) but can also be used for vision needs (Figure 3-b). The device has been built using the Alcatel Microelectronics 0.7 µm CMOS technology. It features 512x5 12 square pixels with 30 µm pitch. The geometrical pixel fill factor is high (around 60%), with a topology of the sensitive zone (detailed further in the text) optimized for applications based on centroiding measurements. Full random access offers flexible windowing capability. The pixel structure is based on a photogate topology, in order to allow real correlated double sampling processing (and therefore lower temporal noise). The design of the internal read-out electronics allows pixel output rates as high as 4 Mpixels/s with excellent linearity and dynamic. Only one output stage is therefore implemented, which is sufficient for most of the sensor applications. Minimum integration time as short as 130 µ is possible. The charge to voltage conversion factor is equal to 4 tV/e-. Even though larger figures are achievable (allowing a read-out noise reduction when expressed in electrons), this figure was selected to offer a large useful dynamic range within the linearity zone of the device photon-voltage transfer function (equal or higher than 200 000 electrons). Antiblooming is implicit for the selected design, this feature being necessary for several sensor applications (Figure 3-c). In addition to the buses devoted to the random access functions, only few TTL clocks and 0 to 5 volts DC bias are required to operate the device. The video output is on-chip sampled, significantly relaxing the external video chain design when compared to CCD. At nominal rate (4 Mpixels/s), the power dissipation is expected to be lower than 100 mW. Two CMOS-temperature probes are integrated on the chip.

Figure 3-a (left-top): view of the CMOS512 image sensor within its package. **Figure 3-b** (right): rough image (only FPN corrected) obtained using the CMOS512 device operated at 4 Mpixels/s. **Figure 3-c** (left-bottom): demonstration of the anti-blooming capability of the device

Since the first published results about this device at the beginning of 2000 [6], several arrays from two wafers where characterized and some of them were provided to customers working in space business. From the results database, it can be seen that even for such a large die surface (17x17 mm2), 50% of the devices do not feature any dead column, dead line or cluster. The main performance figures of the imaging device are presented hereafter. The selected output rate is equal to 2 Mpixels/s, using a 6 MHz noise bandwidth for the acquisition chain downstream the CM05512 output. The devices have been supplied with their nominal 5V bias. Varying the current sources biases can optimize the trade-off between the power dissipation and the pixel rate. For the following, biasing was set to minimize the power dissipation and maximize the dynamic range.

3.1 Dynamic range

The dynamic range has been derived from measurements of the useful voltage swing at device output and from temporal noise measurements. In order to link both input and output parameters, the conversion factor has been measured by plotting the variance of the signal versus its mean value. Except for one device, all the tested CMOS5 12 arrays are featuring a conversion factor in the 3.9 to 4 tV/e- range, very close to the 4jtV/e- targeted value.

Two criteria are defined for the measurement of the useful swing: (i) the linear zone of the transfer function based on a less than 1% deviation with respect to the best fitted straight line; (ii) the useful swing prior to saturation.

Temporal noise measurements are performed in darkness conditions. Thanks to on-chip Correlated Double Sampling (CDS), the noise can be minimized, as the 1/f noise generated by the in-pixel source follower transistor and the kT/C noise sampled on the floating sense node capacitance are removed by the CDS. The measured average value is equal to 140 µV rms (corresponding to 35 e- based on the selected 4µV/e- conversion factor).

The dynamic range of the signal (expressed in dB) is calculated as 20 times the logarithm of the useful swing to the temporal noise. Results are presented below (Table 4).

Useful swing at output (mV)	Corresponding criteria	Temporal noise (µV rms)	Corresponding dynamic range
800	Linear zone (criteria of 1% deviation with respect to best fitted straight line)	140	75 dB
1500	Saturation	140	80 dB

Table 4: CMOS512 dynamic for two different criteria

3.2 Dark current density and its non uniformity

Spatial average dark current density (referred to the total 30x30 µm2 pixel area) has been measured versus temperature (from 0 to 30°C) for several devices (Figure 5), showing an excellent reproducibility. Dark current generation is mainly linked to the technology selected for the processing ofthe die. For this reason, the measured parameters are close to the ones of previous devices made with the same CMOS process [6]. At 20°C, the dark current density is equal to 1.2 nA/cm2. As a comparison, the same parameter measured at the same temperature for the 0.5 µm process from the same founder is equal to 0.15 nA/cm2.

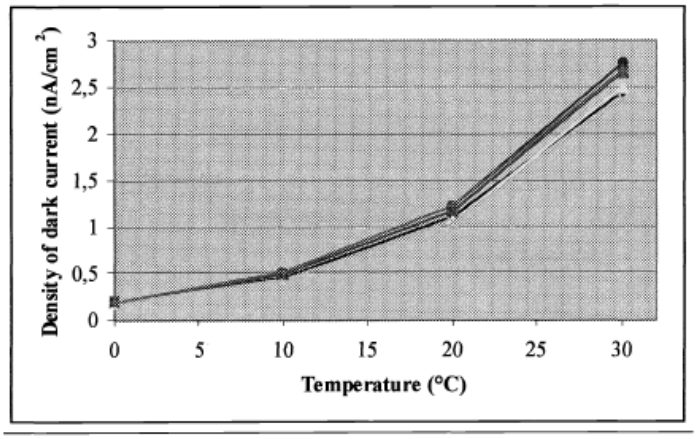


Figure 5: average dark current density versus temperature measured for 7 CMOS512 devices from 2 different wafers

CMOS5 12 dark current 3-D map features an excellent uniformity as shown below (Figure 6-a). Based on the results data base, the standard deviation of the dark current spatial dispersion is in the 3 to 6% range for all the tested devices (singular pixels are not discarded for this processing). Histogram of the dark current density (Figure 6-b) does not depart from a gaussian function.

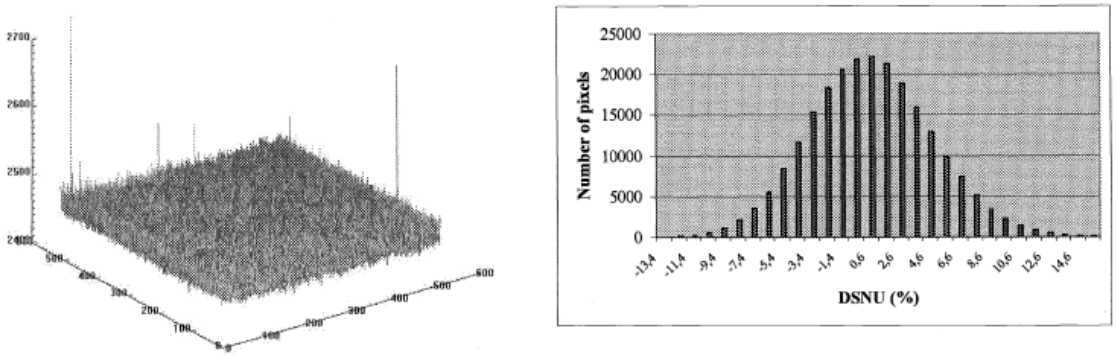


Figure 6-a (left): 3D map of the spatial distribution of the dark current for a CMOS512 device. Only very few singular pixels are present. **Figure 6-b** (right): spatial distribution of the dark current density is close to a perfect gaussian function.

3.3 Overall detection efficiency and Photo Response Non-Uniformity (PRNU)

Overall detection efficiency is defmed as the ratio between the measured amount of electrons versus the total incoming number of photons over the whole 30x30 µm2 pixel area. It has been measured for several devices at 650 nm wavelength and most of the figures are in the 32 to 35 % range for packaged arrays, including a standard BK7 window (which is not anti-reflection coated). Additional measurements were performed for 5 wavelengths using a device without window (Table 7). Decrease ofthe overall detection efficiency between 650 and 750 nm has been explained in previous papers [7].

Wavelength (nm)	Overall detection efficiency (%)
546	18
650	38
700	29
750	39
850	23

Table 7: overall detection efficiency for various wavelengths using a CMOS512 device without window

As shown below (Figure 8-a), the spatial distribution of the photo response is excellent for CMOS512 devices. Based on the results data base, the standard deviation of the PRNU measured at 650 nm is in the 1 to 1 .4 % range for all the tested devices (singular pixels are not discarded for this processing). Histogram of the PRNU (Figure 8-b) is close to a Gaussian function.

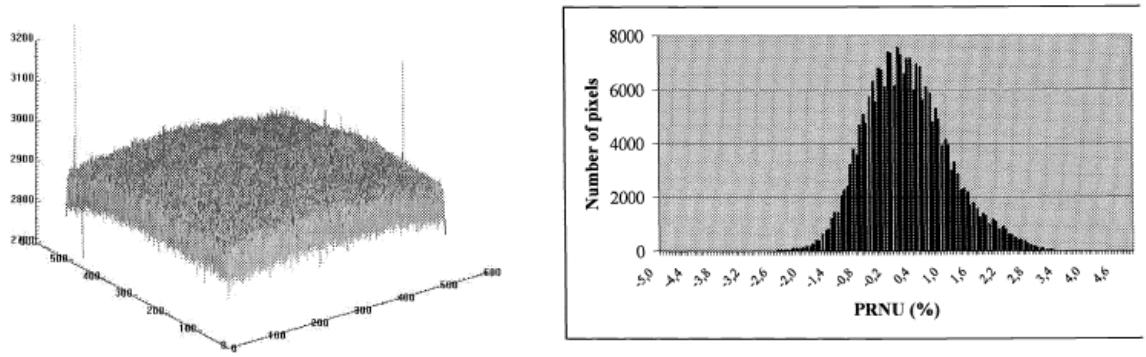


Figure 8-a (left): 3D map of the spatial distribution of photo response for a CMOS512 device. Only very few singular pixels are present. **Figure 8-b** (right): histogram of the Photo Response Non Uniformity is close to a gaussian function.

3.4 Column-to-column Fixed Pattern Noise (FPN)

Column-to-column FPN is known to be the dominant source of FPN for a CMOS image sensor. Even though stable and removable by calibration, on-chip processing or dedicated design [4,5], its amplitude was measured. It can be seen below (Figure 9) that the peak-to-peak dispersion is in the +1-5 mV range for high spatial frequency and within +1- 10 mV for low spatial frequency ("slope" effect). Recent investigations have shown that the slope could be removed by optimization of the device operating conditions.

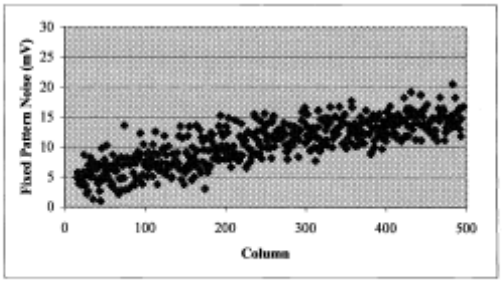
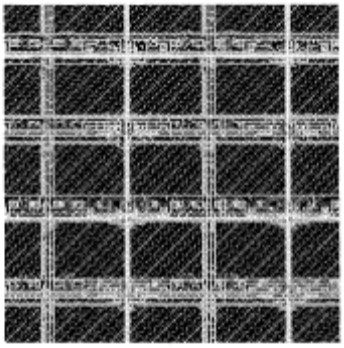


Figure 9: typical column-to-column FPN distribution

3.5 Intra-pixel uniformity of photo response

Intra-pixel photo response uniformity is an important parameter, particularly for sensor applications based on centroiding measurements. Indeed, non uniformity inside the pixel can lead to bias in the measurement of the optical spot center position. Front-side illuminated CCDs do not feature a perfect intra-pixel uniformity due to the location of the polysilicon gates on top ofthe pixels. This was deemed not to be a problem for the CM05512 sensor thanks to the uniformity ofthe inpixel photosensitive surface. Measurements were necessary in order to confirm this hypothesis.

A spot scan test bench was used to characterize experimentally the intra-pixel uniformity. A few microns diameter spot (820 nm wavelength) was focussed on top of the array and its position was moved along the sensitive surface thanks to micropositioning equipment. Results show very good intra-pixel uniformity. Measurements are well correlated with the pixel topology as shown below (Figures 10-a and 10-b).



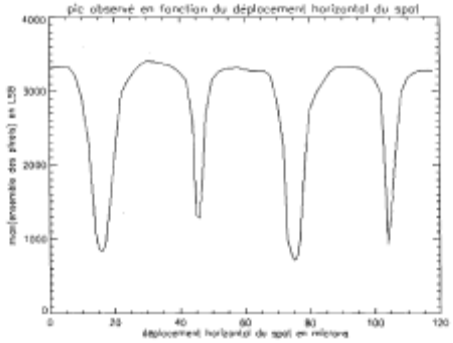


Figure 10-a (left): intra-pixel topology for the CMOS512 array. The rectangular dark zone represents the photosensitive surface. **Figure 10-b** (right): microscan along the horizontal axis. Data along X axis are expressed in microns and data along Y axis are proportional to the output signal.

3.6 Power consumption

Low power consumption is one of the major advantages of CMOS image sensors when compared to CCDs. This is particularly the case when considering the power requested for the total imaging function thanks to the low number of peripheral chips required for the CMOS device operation (no clock drivers, simplified video chains...). However, the power consumption of the device alone can also be an important criteria (for the sizing of an associated Thermo-Electrical Cooler for instance). For all the tested CMOS5 12 devices, the power consumption was found to be in the 50 to 60 mW range for continuous 2Mpixels/s read-out operation.

3.7 Temperature probes

Two temperature probes are integrated within the CM05512 chip. This allows an easier operation when compared to external probes mounted in the package. In addition, the measurement is considered to be more accurate as it is done on the die itself Finally, the design of the CMOS probe can be optimized in order to get a higher sensitivity than the one offered by standard 2N2222 transistor as usually integrated in CCD packages (sensitivity in the 2 to 3 mVI°C range). A typical curve of output voltage versus temperature for the CMOS temperature probe integrated in the CM05512 image sensor is provided below (Figure 1 1). The sensitivity is about 10 mV/°C.

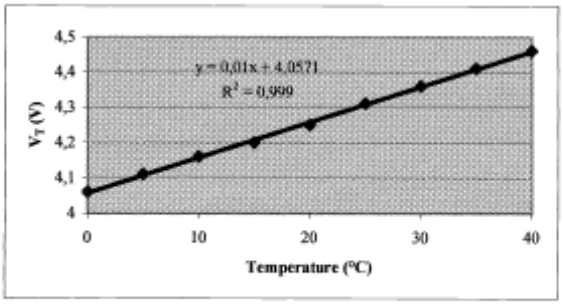


Figure 11: output voltage versus temperature for the temperature sensor integrated in the CMOS512 device

4 ON GOING AND COMING ACTIVITIES

The development of the CMOS5 12 image sensor can be considered as a great success thanks to its excellent electro-optical performance. Since 2000, new directions devoted to space applications are being explored by the team, some under internal funding and others under contracts awarded by CNES,DGA or external customers. System studies performed in 2000 have shown that tens of space applications can be covered by CMOS image sensor technologies. Among others, the main trends for the on going and short-term activities are:

- to even improve pixel performance (particularly quantum efficiency and MTF) and to evaluate deeper CMOS technologies, following the trend ofthe microelectronics industry
- to improve the integration of on-chip peripheral functions as far as it is compatible with the performance requirements. Indeed, addition of such functions (ADC. ..) is considered as "nice to have" but can lead to degradation ofthe useful signal (EMC effects, coupling. ..) which can be non-acceptable for very-demanding space applications
- to evaluate the capability for advanced on-chip processing, this axis being ofprime importance for sensor applications

The design and the development of a 750x750 pixels array devoted to highly integrated star sensor products are in progress at Astrium/CIMI under CNES contract. This device is designed for a 0.5 tm CMOS process and incorporates an on-chip sequencer dedicated to the star sensor applications (Figure 12). In parallel with the development of the main device, a specific 0.5 µ CMOS 128x128 pixels test vehicle is today ready for the evaluation of this technology against radiations (total dose and latch-up behaviour). Several types of pixels (including photogate and photodiode), on-chip sequencer and new generation read-out chain are incorporated within this device (Figure 13).

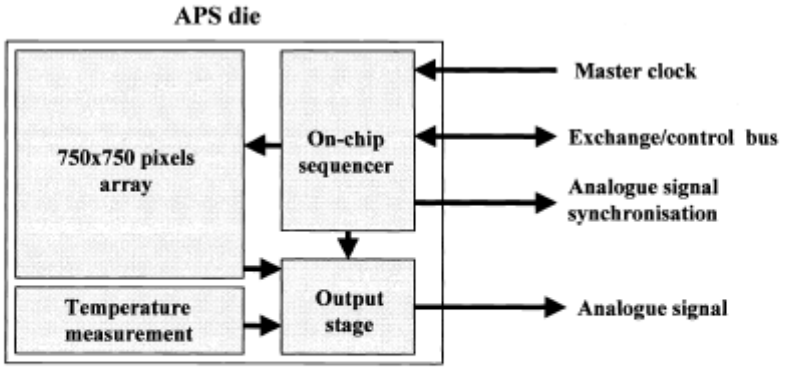


Figure 12: block-diagram of the 750x750 pixels SSM CMOS image sensor devoted to star sensor applications

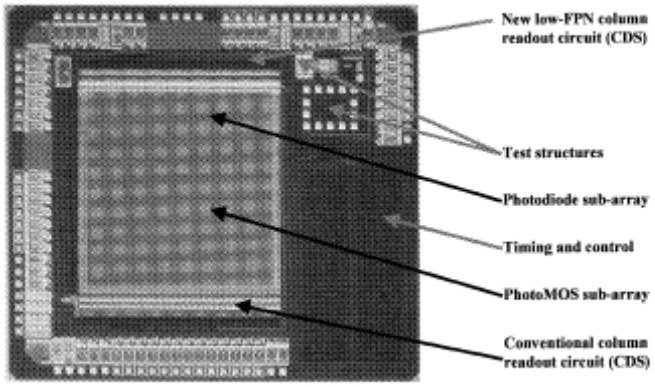


Figure 13: photography of the radiation test vehicle with location for the main on-chip functions

Following a first R&D contract awarded by CNES in 1999, a second study will start at the end of 2001 with the development of enhanced photodiode pixels featuring improved quantum efficiency and MTF. In complement with internal funding, this CNES activity will allow detection arrays devoted to Earth observation applications to be developed from 2002.

Another study awarded by DGA (French DoD) started in July 2001 in collaboration with LETIJLIR to evaluate the CMOS technology for very large focal planes for Earth observation.

Finally, the design and the development of a test vehicle devoted to helioseismology applications was performed in 2001 for the astrophysics department from CEA (Figure 14). Indeed, this institute has to determine between several detector technologies the best candidate for this application .The test vehicle is currently evaluated by the customer in order to determine the compatibility of CMOS device with the very stringent stability specifications as required by the application.

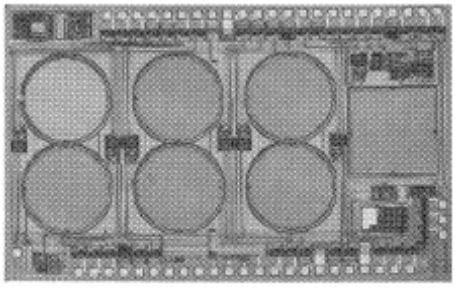


Figure 14: CMOS test vehicle devoted to heliosismology applications

The growing interest that space industry and institution show in CMOS imaging devices through the undertaken activities definitively demonstrates that this technology is now considered at short term as a serious candidate for visible detectors for space missions.

ACKNOWLEDGMENTS

The authors wish to acknowledge CNES and DGA for their support to the CMOS optical sensor activities for space applications. The authors also whish to thank their colleagues at Supaéro/CIMI laboratory and at Astrium Detection laboratory, and particularly Olivier Donnadieu, Cyril Vetel, Laurent Boireau, Yavouz Degerli, Cécile Marques and Magalie Estribeau.

REFERENCES

1. J. Soffiusvik, C. Bellito, C. Cavadore, A. Bourricaud, J. Farré, " Development of CMOS Active Pixel Image Sensors suitable for Space Applications -some preliminary results ", Proc. ofthe SPIE, Sensors, Systems and New Generation Satellites, Vol.2583, Paris, 1995.

2 Y. Degerli, F. Lavemhe, P. Magnan and J. Farré, "Analysis and reduction of signal readout circuitry temporal noise in CMOS image sensor for low-light levels", IEEE Trans. on Electron Devices, Vol.47, No 5,pp. 949-962, May 2000.

3 Y. Degerli, F. Lavernhe, P. Magnan and J. Farré, "Non-stationary noise responses of some fully differential on-chip readout circuits suitable for CMOS image sensors", IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, n° 12, pp. 1461- 1474, December 1999.

4 Y. Degerli, F. Lavemhe,P. Magnan and J. Farré, "Column readout circuit with global charge amplifier for CMOS APS imagers", Electronics Letters, vol.36, no. 17, pp. 1457-1459, Aoflt 2000.

5 Y. Degerli, F. Lavemhe, P. Magnan, J. Farré, " Dispositif de lecture de pixels notamment pour capteur d'images matriciel a pixels actifs CMOS", Patent PCT/FROO/O1 757

6 P. Magnan, A. Gautrand, Y. Degerli, C. Marques, F. Lavemhe, C. Cavadore, F. Corbière, J. Farrë, 0. Saint-Pé, M. Tulet and R. Davancens, "Influence of pixel topology on performances of CMOS APS imagers", ", in Proc. of SPIE, vol.3965, Sensors and Camera Systems for ScientjfIc, Industrial and Digital Photography Applications, January 2000 (San Jose, CA), pp.1 14-125.

7 J. Solhusvik, C. Cavadore, F.X. Audoux, N. Verdier, J. Farré, 0. Saint-Pë, R. Davancens and J.P. David, "Recent experimental results from a CMOS active pixel image sensor with photodiode and photogate pixels", in Proc. of SPIE, vol.2950, Advanced Focal Plane Arrays and Electronic Cameras, October 1996 (Berlin, Germany), pp.18-24.