Development of high-performances monolithic CMOS detectors for space applications

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ABSTRACT

This paper describes the development of a 750x750 pixels CMOS image sensor for star tracker applications. A first demonstrator of such a star tracker called SSM star tracker built around a 512x512 detector has been recently developed and proves the feasibility of such instrument. In order to take fully advantage of the CMOS image sensor step, the 750x750 device called SSM CMOS detector which will take part of the final star tracker, can be considered as a major technical breakthrough that gives a decisive advantage in terms of on satellite implementation cost and flexibility (sensor mass and power consumption minimisation, electronics and architecture flexibility). Indeed, built using the 0.5µm Alcatel Microelectronics standard CMOS technology, the SSM CMOS detector will feature on-chip temperature sensor and on-chip sequencer. In order to evaluate the radiation tolerance of such manufacturing technology, a radiation campaign that contains studies of total dose and latch-up effects has been led on a specific test vehicle.

1. INTRODUCTION

Thanks to the past 10 years intensive work, maturity of the CMOS image sensors is now established and these detectors are no more laboratory prototypes and are getting currently used in consumer electronics. As foreseen by designers of optical instruments and sensors for space applications, such detectors could also offer large advantages for many space applications when compared to CCDs. As the European leader for industrial space activities, Astrium started works on CMOS image sensors in the mid-90s mainly because off the shelf products do not offer the specific features that are required for many space applications. The CIMI laboratory from Supaéro is developing high electro-optical performances CMOS image sensors since 1994, having all in-house capabilities for their design. Collaboration between Astrium and Supaéro-CIMI started in 1996 in order to develop CMOS detectors for space applications. These two last years, this team has been selected by various space industries and institutions for delivery of existing devices or study/development of new products for space applications:, improved photodiode pixels, large CMOS detectors for Earth observation, sensors devoted to heliosismology... and especially the SSM CMOS detector for star tracker applications which is the subject of the present document. This paper first presents the architecture of such star tracker and also the technical choices that led to the first demonstrator built with a 512x512 detector. The specifications and the architecture of the future SSM CMOS detector are then discussed. The pre and post irradiations electro-optics performances of a dedicated test vehicle are finally reported.

Keywords: space, CMOS, camera, image sensor, star tracker, radiation

3. SSM STAR TRACKER ARCHITECTURE AND PERFORMANCES

The SSM star tracker is a CMOS image sensor-based 3 axis miniaturized star tracker. It is designed around a dedicated CMOS sensor and takes fully advantages of this technology step (Tab. 1).

CMOS image sensor features	Advantage for star trackers
Direct access to windows of interest	♦ efficient and robust algorithms
	♦ immunity to false-star (solar flare…)
CMOS well proved technology	♦ secured development
	♦ reliable star tracker
Less sensitive to radiation that CCD	♦ good end-of-life performances
Very simple proximity electronics required	♦ compact digital camera
	♦ allow "centralised architecture"
Possibility to integrate logical functions on the chip	♦ no ASIC nor FPGA required
	♦ compact digital camera
Possibility to optimise the packaging	♦ efficient thermal control

Tab. 1: CMOS technology advantages

The use of a dedicated CMOS detector allows to optimise the design of a compact digital camera that can be easily driven by any processor board. In particular, the "centralised" approach leads to (Fig. 1):

- a compact stand alone optical head (Starcam) which minimizes the mass and power dissipation of the part of the sensor that must be precisely stabilized. Therefore, the mechanical interface is very simplified.

- the integration of the StarCam driving electronics within the satellite platform avionics allows to drastically reduce the recurrent cost.

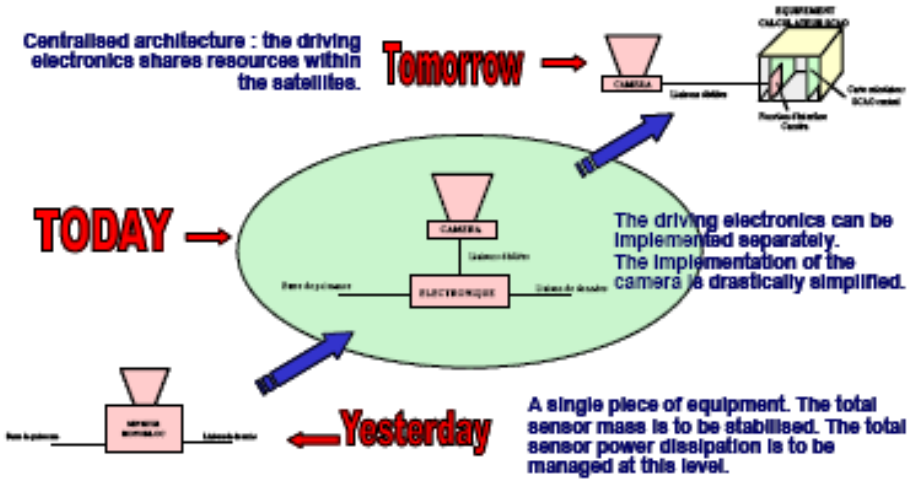

Fig. 1: "Centralized" architecture approach

The following figures (Fig. 2, Fig. 3, Fig. 4, Fig. 5) present photographs of the first demonstrator that has been manufactured and tested in from a dynamical optically simulated sky. The future SSM CMOS detector is replaced by a 512x512 detector and external FPGA simulates the future on chip sequencer. The proximity electronics (electronics within the digital camera) is limited to single 25mm2 board. Excellent robustness (to false stars and to high speeds) has been demonstrated.

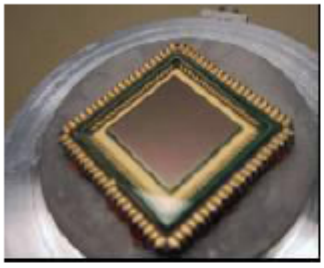

Fig. 2: 512x512 sensor mounted on the camera focal plane

Fig. 3: Camera with titanium objective

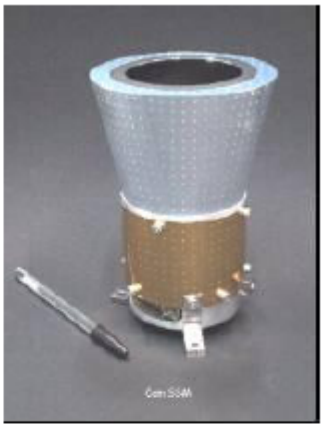

Fig. 4: Digital star tracker camera

Fig. 5: Star tracker camera under functional test

The expected star tracker main features are listed below:

- Main attitude restitution performances (EOL)
  - Thermoelastic : 0.0002°/K
  - Noise equivalent angle at 4 Hz (including pixel)
    - 10" (3σ) along X- and Y-axis
    - 40" (3σ) along Z-axis (line of sight)
  - FOV error (X,Y/Z) : 5" / 20"

- Tracking up to 5°/s
- Digital StarCam : up to 10 meters cables allowed
- Compatible multi-head
- Sun exclusion angle : modular baffle ; typical = +/-40° ; min=+/- 25°C,
- Operation with Moon in the FOV : degraded performances
- StarCam volume : diameter 80 mm; height 80 mm. (baffle : diam.120; height 150)
- StarCam mass : 900 g (with radiation shielding ; baffle<500g)
- Power budget : < 2 W including APS thermal control
- Compatible with GEO 15 years radiation environment and therefore (>10 mm equivalent shielding) with Galileo 15 years environment

4. SSM CMOS DETECTOR SPECIFICATIONS

The SSM CMOS detector radiometric specifications, which lead to the SSM star tracker performances just mentioned, are presented in Tab. 2. The correspondence between some radiometric performances of the CMOS image sensor and the global accuracy of the star tracker is given in the Fig. 6 through the example of the dark current and PRNU dependence of the Noise Equivalent Angle.

Performances	Value
Dark current	225 pA/cm^2
DSNU	8% (1σ)
QQE	20% peak
PRNU	3% (1σ)
Conversion gain	10 µV/e$^-$
Read-out noise	<30 e$^-$
Dissipation	100 mW

Tab. 2: Main radiometric performances of the SSM CMOS detector @0°C @ 10 krad End-Of-Life

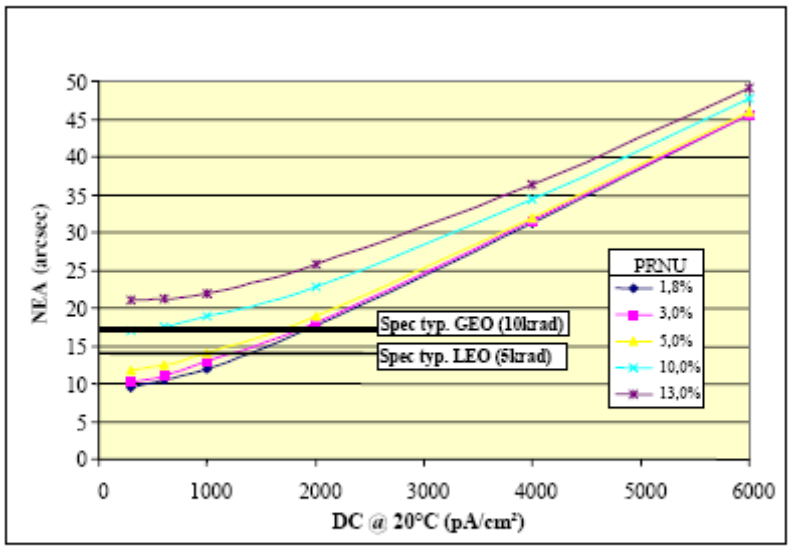

Fig. 6: Dependence of the SSM star tracker Noise Equivalent Angle on the dark current and PRNU of the SSM CMOS detector

5. SSM CMOS DETECTOR ARCHITECTURE

The CMOS image sensor dedicated to the miniature star tracker is built using the Alcatel Microelectronics 0.5µm CMOS technology. The general overview of the device is provided in the Fig. 7. It features 750x750 rectangular pixels with 20µm pitch. The geometrical pixel fill factor is high (around 60%) with a topology of the sensitive zone optimised for applications based on centroiding measurements. The pixel structure is based on a photogate topology in order to allow real correlated double sampling processing (and therefore lower temporal noise). Only one output stage is implemented which is sufficient for most of the sensor applications. The charge to voltage conversion factor is equal to 10µV/e-. Masked lines are used to measure the dark current and the fixed pattern noise. The video output is on-chip sampled, significantly relaxing the external video chain design compared to CCDs. The main feature of this device is the on chip sequencer. Owing to master clock and control bus, such a sequencer operates the image sensor and generates synchronization signals for the treatment of the analog output signal (numerical conversion…). The on-chip sequencer makes easier the operating of the device by drastically reducing the number of clocks to be applied. In addition, a temperature probe is integrated within the CMOS chip. When compared to external probes mounted in the package, this measurement will be more precise as it is done on the die itself. The sensitivity is expected to be about 10mV/°C. Low power consumption is one of the major advantages of CMOS image sensors compared to CCDs. This is particularly the case when considering the power requested for the total imaging function thanks to the low number of peripheral chips required for the CMOS device operation (no clock drivers, simplified video chains…). The consumption is expected not to exceed 100mW.

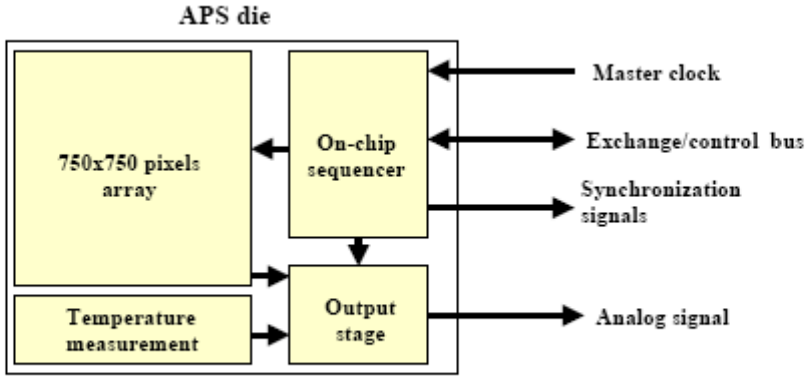

Fig. 7: General overview of the CMOS image sensor dedicated to the miniature star tracker

6. EVALUATION OF THE 0.5µm ALCATEL MIROELECTRONICS TECHNOLOGY RADIATION TOLERANCE

Evaluation of the behaviour of a 0.5 µm Alcatel Microelectronics built test vehicle under radiation environment was performed. This evaluation contains two test campaigns:

• a Co60 irradiation campaign motivated by the need to understand how to optimise the SSM CMOS detector in order to choose an enough radiation tolerant pixel topology and establish the End Of Life figures to be taken into account for the modelling of the star tracker EOL performances

• a heavy ions campaign motivated by the study of the latch-up sensitivity of the SSM CMOS detector logic sequencer

6.1 Description of the test vehicle

The prototype array is organised as 22 sub-arrays of pixels having 20µm pitch. It includes both photodiode and photogate topologies. Even if the pre and post-irradiation characterization of the photodiodes arrays were performed, only the photogate results were fully processed as this type of topology was selected for the SSM CMOS detector. Starting from the baseline photogate pixel, large transfer gate pixels (n°9, 13, 17 and 21), pixels with local substrate to ground ties (n°2, 8, 9, 16 and 17) and pixels with different conversion gain have been designed. All the pixels share a common column-parallel readout circuitry providing analog output, thus allowing to identify behaviour differences between pixel types. For the latchup tests, the vehicle test also includes on-chip logic sequencers that are representative of the one implemented on the SSM CMOS detector. The Fig. 8 shows the organization of the test chip.

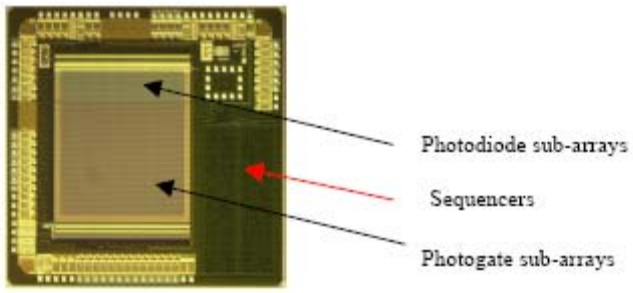

Fig. 8: Photograph of the test vehicle

6.2 Total dose effects: irradiation by Co60

The irradiation of the devices was performed at CERT/ONERA. 4 devices were irradiated at 5, 10, 18 and 48 krad, all powered and clocked. As photogate topology was selected for the SSM CMOS detector instead of photodiode one, the corresponding clocking was applied to the test vehicles and only photogate characteristics are presented below. The dies were mounted in PGA84 packages without window. All the devices were characterized before irradiation in order to get a reference level for the main electro-optical parameters. An additional device was characterized before irradiation and was used as a reference along the tests. Platinum temperature probes were glued on the package in order to measure device temperature during current characterizations.

6.2.1 Conversion factor

The conversion gain CVF has been determined by plotting the variance of the signal versus its main value [1]. The Tab. 3 summarizes the results for the 10 krad irradiated device which corresponds to a GEO 15 years radiation environment. The measured values for conversion gain are very close from those expected from design and are slightly degraded at 10 krad.

Photogate pixel	CVF mes. (µV/e-) before irradiation	CVF mes. (µV/e-) EOL (10 krad)
n°2	5,60	5,35
n°5	5,60	5,40
n°8	7,35	7,25
n°9	7,80	7,60
n°12	7,50	7,80
n°13	7,90	7,20
n°16	9,40	9,60
n°17	9,10	9,40
n°20	9,10	9,50
n°21	8,80	9,20

Tab. 3: Evolution of the conversion gain for 10 krad total dose

6.2.2 Read-out noise

The r.m.s temporal noise is measured in darkness conditions for different integration time by suppressing the photon and dark current shot noise and by addressing all the pixels of each sub-array. The CVF value is the average of all the pixels of the sub-array. The system noise is well below the noise generated by the sensor. For all the photogate pixels except for the large transfer gate ones which exhibit a higher temporal noise, the read-out noise is very close from 30 electrons and is not degraded at 10 krad.

6.2.3 Dark current and its non-uniformity

The Fig. 9 shows the evolution of the dark current (referred to the total pixel area) with radiation total dose obtained for the various pixel topologies at 20°C. Except for the singular point for the 10krad-irradiated device, the slope is about 80pA/cm2/krad. It is important to notice that all the devices exhibit very close dark current values before irradiation.

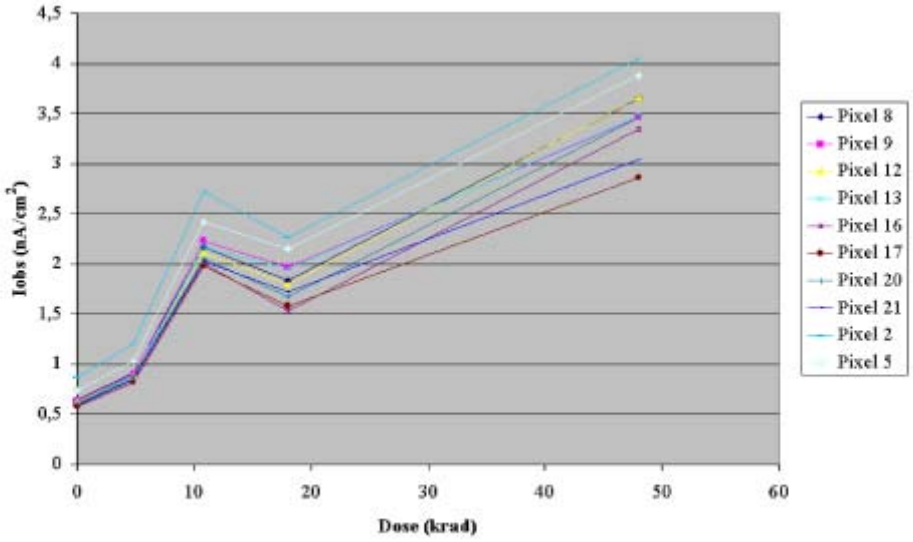

Fig. 9: Evolution of the dark current with radiation dose

The dark current non-uniformity represents the standard deviation of the relative darkness signal for all the pixels of each pixel sub-array. The Tab. 4 summarizes the results for the 10 krad-irradiated device.

Photogate pixel	DSNU (% à 1 σ)	
	before radiation	EOL (10 krad)
n°2	6,8	3,4
n°5	7,2	3,5
n°8	7,2	3,5
n°9	9,3	3,4
n°12	7,0	3,5
n°13	9,3	3,7
n°16	7,7	3,6
n°17	8,3	3,6
n°20	7,4	3,5
n°21	7,6	3,3

Tab. 4. : DSNU for the various pixels

6.2.4 Photo response non uniformity

The photo response non uniformity (PRNU) represents the standard deviation of the relative response for all the pixels of each photogate pixel sub-array. It is given for a 650nm wavelength before radiation and for a 10krad total dose in Tab. 5.
We can notice that the large transfer gate pixels exhibit a higher EOL PRNU.

Photogate pixel	PRNU (% à 1 σ)	
	before radiation	EOL (10 krad)
n°2	1,25	2,4
n°5	1,45	2,4
n°2	1,25	1,65
n°9	1,89	2,9
n°12	1,3	1,8
n°13	1,89	2,8
n°16	1,4	2
n°17	1,8	3
n°20	1,4	2,1
n°21	1,65	2,84

Tab. 5: PRNU for the various pixels

6.2.5 Overall quantum efficiency

Tab. 6 represents the overall efficiency for various photogate pixels before radiation and for a 10krad total dose. Overall detection efficiency is defined as the ration between the measured amount of electrons versus the total incoming number of photons over the whole pixel area.

Photgate pixel	OQE (%)	
	before radiation	EOL (10 krad)
2	35,3	27,1
5	35,5	27,9
8	32,5	25,6
9	32,8	25,5
12	31,9	25,1
13	32,4	25,2
16	30,5	23,9
17	32,7	25,2
20	31,1	24,4
21	33,5	25,8

Tab. 6: OQE for the various pixels

6.2.6 Fixed Pattern Noise

Fig. 10 represents the measured fixed pattern noise before irradiation and for the 48 krad-irradiated device. Radiation has nearly no effect on this parameter: less than 1 mV drift is observed for a 5mV peak to peak feature.

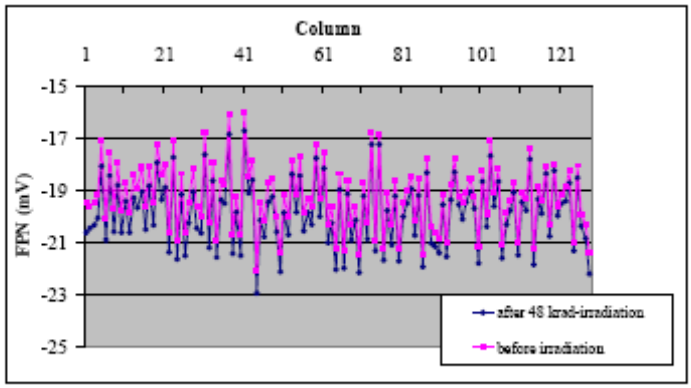

Fig. 10:FPN evolution for the 48krad irradiated device

6.2.7 Power consumption

Supplied current was followed during the irradiations. Fig 11 shows the evolution of the power consumption of the 48krad irradiated device. The consumption is stable up to 20 krad. A large increase is observed from 20 krad (Tab. 7).

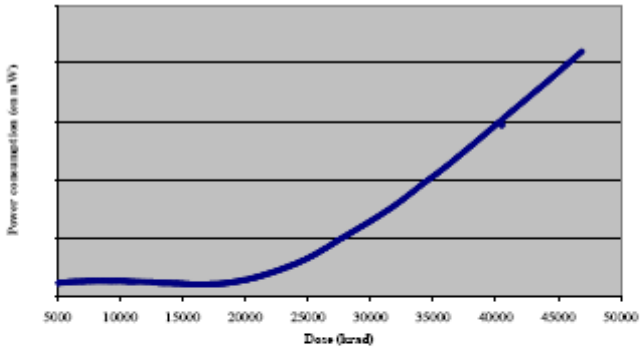

Fig. 11: Evolution of power consumption during the 48krad irradiation

Tab. 7: Power consumption of the irradiated devices

Dose (krad)	Consumption (mW)
0	40-45
5	40-45
10	40-45
18	40-45
48	130-150

6.3 Latch-up behavior: heavy ions effects

These tests were led owing to the IPN Orsay facilities (CNES tests campaign). Two devices were tested and no latch-up sensitivity was observed on the logic sequencers up to 58.2 MeV/(mg/cm2).

7. CONCLUSION

This study has demonstrated the feasibility of the SSM star tracker. A 512x512 image sensor-based star tracker demonstrator has been first presented and shows the functional feasibility of the sensor. Then, once the specifications and the architecture of the SSM CMOS detector were exposed, we have presented the conclusive experimental results concerning the radiation tolerance of the 0.5µm Alcatel Microelectronics sensor manufacturing technology.

All the radiometric characteristics measured after Co60 irradiations on a specific test vehicle are in accordance with the End-Of-Life sensor specifications. This radiation campaign also led us to make a choice for the topology of the photogate pixel even if most of the pixel sub-array test vehicle behaviors are similar: large transfer gate pixels that exhibit bad read-out noise and bad PRNU and pixels with local substrate to ground ties were rejected. These Co60 radiation tests make us confident about the SSM star tracker performances.

The second part of this evaluation has concerned the technologic step introduced in the SSM star tracker: the on-chip sequencer and its sensitivity to the latch-up effects. Two representative logic sequencers were thus implemented on the test vehicle and tested under heavy ions beams. No latch-up effect was observed up to 58.2 MeV/(mg/cm2).

The SSM CMOS detector is now in foundry and the first characterization results are expected for the end of 2002.

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