Research-grade CMOS image sensors for remote sensing applications

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ABSTRACT

Imaging detectors are key elements for optical instruments and sensors on board space missions dedicated to Earth observation (high resolution imaging, atmosphere spectroscopy...), Solar System exploration (micro cameras, guidance for autonomous vehicle...) and Universe observation (space telescope focal planes, guiding sensors...). This market has been dominated by CCD technology for long. Since the mid-90s, CMOS Image Sensors (CIS) have been competing with CCDs for consumer domains (webcams, cell phones, digital cameras...). Featuring significant advantages over CCD sensors for space applications (lower power consumption, smaller system size, better radiations behaviour...), CMOS technology is also expanding in this field, justifying specific R&D and development programs funded by national and European space agencies (mainly CNES, DGA and ESA). All along the 90s and thanks to their increasingly improving performances, CIS have started to be successfully used for more and more demanding space applications, from vision and control functions requiring low-level performances to guidance applications requiring medium-level performances. Recent technology improvements have made possible the manufacturing of research-grade CIS that are able to compete with CCDs in the high-performances arena. After an introduction outlining the growing interest of
optical instruments designers for CMOS image sensors, this paper will present the existing and foreseen ways to reach high-level electro-optics performances for CIS. The developments and performances of CIS prototypes built using an imaging CMOS process will be presented in the corresponding section.

Keywords: APS, space, CMOS Image Sensor, cameras

1. INTRODUCTION

With respect to CCDs, the technical advantages featured by CMOS Image Sensors (CIS) for space applications have been extensively presented in previous papers [1]-[4]. Some of them are shortly listed here: integration of peripheral functions, low power consumption, read-out flexibility, high speed operation, good behaviour in radiations environment, flexible topology, on chip analogue or digital signal processing... At system level, this leads to lower mass/power budgets, better reliability and easier integration. Moreover, some systems that can hardly be designed using CCDs are now easily carried out thanks to CIS. About cost saving, the criteria that should be considered is the cost of the global imaging function rather than the one of the device itself. It would be misleading to think that the price of a state-of-theart CIS dedicated to an ambitious space mission will be low. On the other hand, it is true that the price of the associated imaging function would be lower using a specific CIS instead of a CCD for a great number of space applications. For all these reasons, an engineering team today starting the design of a visible space instrument or sensor has to lead a tradeoff between CCD and CIS at the beginning of the program.

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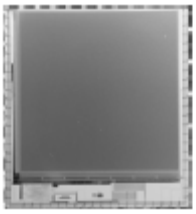
Based on an "ASIC-like" approach, the design of a specific CIS has to be integrated into the system definition phase. This has convinced EADS-Astrium to be in position of mastering the design of CMOS image sensors. This is done since 1998 through an agreement with the CIMI laboratory of Supaero (also located in Toulouse), which started to work on high performances CIS since 1994. Thanks to internal funding and the gain of agencies contracts, several devices were developed by this team in order to provide an efficient answer to space requirements. An example of such a dedicated device is presented in figure 1. Based on a first version developed in 2002 for miniature star tracker application through a CNES contract, a 750x750 pixels CIS was specifically designed for the LOLA demonstrator, which is a DGA (French defence procurement agency) program allowing to test the feasibility of high rate laser optical links between an aircraft or drone and a satellite.



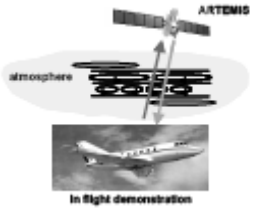


Figure 1: left: 750x750 pixels CIS dedicated to optical communications: right: the LOLA demonstrator will test the feasibility of high rate laser optical links between an aircraft or drone and a satellite

One of the most interesting features of this CIS is a powerful integrated programmable timing and control function able to randomly read a large number of windows even if superimposed. The first version of the device was extensively characterised and was space radiation qualified (total dose, latch-up and high energy protons). Its main performances have been presented in a previous paper [5].

2. THE NEED FOR ELECTRO-OPTICS PERFORMANCES IMPROVEMENTS

Monolithic CIS developed by both EADS-Astrium and Supaero-CIMI in the 1998-2002 periods and built using standard CMOS processes are featuring very good electro-optics performances, close to the ones achieved by standard front-side illuminated CCDs. Table 2 summarizes typical performances that were measured when testing the 750x750 pixels CIS.

Parameter	Typical figure
Format	750 x 750 pixels
Pixel pitch	20 x 20 μm^2
Geometric fill factor	60%
Charge to voltage conversion factor	10 µV/e-
Peak detection efficiency	28 % (including Fill Factor contribution)
Photo Response Non Uniformity	< 1% standard deviation
Read-out noise (rms)	30 e- rms
Linear dynamic range	60 000 e-
Dark current density	600 pA/cm^2 @ 293 K
Dark Signal Non Uniformity	< 10% standard deviation
MTF at Nyquist frequency	0.46 row / 0.54 column at 500 nm 0.31 row / 0.40 column at 650 nm 0.28 row / 0.35 column at 800 nm

Table 2: typical electro-optics performances reached by EADS-Astrium/Supaero-CIMI 750x750 pixels CIS 2D array

With such characteristics, and thanks to their numerous advantages over CCDs, monolithic CIS manufactured using standard CMOS technologies are today the right answer for several space applications, such as Star Trackers, Optical Communications, miniature scientific cameras.... Nevertheless, some of these electro-optical performances are not sufficient in view of allowing CIS to compete with scientific CCDs for very demanding applications such as high resolution Earth Observation and scientific instruments operated in low flux regime.

3. POSSIBLE WAYS TO IMPROVE CIS ELECTRO-OPTICAL CHARACTERISTICS

At least three ways can be foreseen to improve the electro-optical performances of CIS. All of them are described below:

3.1 Improvements by design

For a fabless company, the easiest way to improve CIS performances is to optimise its design, and particularly the intrapixel circuitry. [6]-[7] describe for instance new photodiode pixel architectures offering kTC noise reduction. EADSAstrium and Supaero-CIMI are investigating advanced pixel designs in view of improving important parameters such as read-out noise and linearity at low flux. A study awarded by CNES to our team has allowed producing a test vehicle dedicated to these investigations (see Figure 3-a). This device is currently being tested.

In collaboration with CEA/LETI, a study awarded by DGA to our team has allowed evaluating the CMOS technology capabilities for very large focal planes dedicated to Earth Observation (both linear and TDI devices architecture being investigated). Figure 3-b presents an example of linear array design with CTIA injection stage implemented at pixel level, allowing image acquisition at high frame rate even for very low flux conditions.

Figure 3: (a) left: test vehicle built through a CNES R&T contract in order to improve pixel performances using standard CMOS technologies; (b) right: layout of a linear array with CTIA injection stages devoted to pushbroom Earth observation

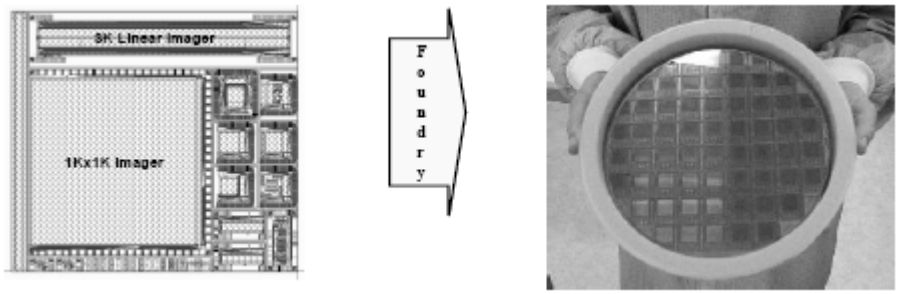
CMOS design rules are continuing to decrease following Moore's law and 0.13 µm CMOS process are now used for the most advanced imaging devices production. For consumer market, this allows to get good electro-optics performances even for tiny pixels (pitch smaller than 3 µm is the today standard for cell phones imaging modules). For specific applications, such as space or military ones, this will allow to increase the fill factor for a given pixel pitch or to add advanced in-pixel electronics, widening the way of by-design performance improvements.

3.2 CMOS processes dedicated to imaging applications

The second way in order to get better CIS performances is the improvement of CMOS mixed signal process in view of offering specific features useful for imaging applications [8]. The main parameters that request improvements in order to allow CIS to compete with high performances CCDs are the

detection efficiency, the dark current density and the Modulation Transfer Function (MTF). Detection efficiency can be improved by maximising the pixel fill factor, the optical transmission of the layers located above the photons absorption level and the photoelectrons collection efficiency, this last parameter being also one of the main contributor to the MTF performance. As mentioned in the previous paragraph and for a given pixel pitch and architecture (i.e. a given amount of transistors per pixel), the geometric fill factor can be improved by using advanced CMOS processes thanks to the use of smaller design rules and additional interconnection levels. On the other hand, this would lead to a decrease of the top layers transmission. Moreover, the continuous decrease of modern CMOS process design rules would lead to a reduction of the thickness of the interaction layer between photons and silicon (due to the use of heavily doped epi layers), leading to a detection efficiency decrease and a loss of MTF as part of the carriers being created in the substrate and being diffusion collected by the neighbouring pixels. These effects are worst for the longest wavelengths that penetrate deeper in the silicon (see MTF results presented in table 2 as an illustration).

As the photonics market (including the imaging business one) is strongly growing, several CMOS foundries have invested huge amount of money in order to develop technologies able to offer at the same time deep sub-micron lithography and high electro-optics performances. In 2003, EADS-Astrium and Supaero/CIMI carried out the design of a 1k x 1k 2D array (13 µm pitch) and of a 3k linear array (6.5 µm pitch) based on the use of a 0.35 µm CMOS process optimised for imaging applications. Figures 4 shows the assembled reticule before launch into foundry and an 8 inches wafer back from foundry before dies dicing.

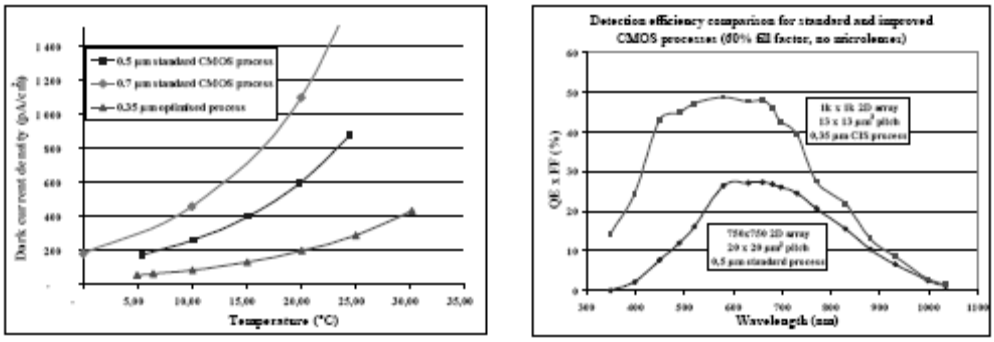


Figures 4: left: assembled reticule designed by EADS-Astrium and Supaero-CIMI ready for launch into 0.35 µm foundry optimized for imaging applications: the two largest devices consist in a 1k x 1k 2D array (13 µm pitch) and a 3k linear array (6.5 µm pitch); right: corresponding 8 inches wafer back from foundry

Figures 5 present the two arrays mounted in their packages. The 2D array has been extensively characterized and the corresponding results are presented below. The linear array will be tested before the end of 2004.

Figures 5: 1k x 1k 2D array (left) and 3k linear array (right) in their corresponding packages

The improvements of the performances achieved using the selected 0.35 µm CMOS process optimized for imaging applications are impressive. Figure 6-a compares the dark current density measurements (defined over the full pixel area) versus temperature for 2 standard mixed signal processes (0.7 and 0.5 µm) and for the 0.35 µm improved process. It should be noticed that a constant 60% pixel geometric fill factor applies for the three devices, despite the pixel pitch change (respectively 30, 20 and 13 µm pitch for the 0.7, 0.5 and 0.35 µm processes). For 293 K, 200 pA/cm2 is now achieved. Using the most advanced CMOS processes, dark current density lower than 50 pA/cm2 at 293 K (equivalent to the performance of CCD operated in inversion mode) have been reported [9]. Figure 6-b compares the spectral detection efficiency for the standard 0.5 µm and improved 0.35 µm processes. Peak detection efficiency close to 50% has been measured for the new device (no microlenses have been implemented). Using microlenses, that improves the geometrical fill factor, Rockwell Scientific have demonstrated spectral detection efficiency as high as 70% even for 5 µm pixel pitch using a 0.25 µm optimized CMOS process [10]. Referring to figure 6-b, the better sensitivity achieved in the blue part of the spectrum for the new device is mainly due to the use of photodiodes instead of photoMOS.



Figures 6: (a) left: dark current density (defined over the full pixel area) versus temperature for a 0.7 µm (30 µm pixel pitch) and a 0.5 µm (20 µm pixel pitch) standard CMOS processes and for a 0.35 µm (13 µm pixel pitch) optimized CMOS process; (b) right: spectral detection efficiency for a 0.5 µm (20 µm pixel pitch, photoMOS detector) standard CMOS process and for a 0.35 µm (13 µm pixel pitch, photodiode detector) optimized CMOS process

Maybe the most impressive improvement concerns the image quality evaluated through the measurement of the Modulation Transfer Function (MTF) and the inter-pixel cross-talk. Table 7 compares the spectral MTF at Nyquist frequency for a 0.5 µm standard process (20 µm pixel pitch) and the 0.35 µm optimized process (13 µm pixel pitch).
The improvement is particularly impressive for the longest wavelength.

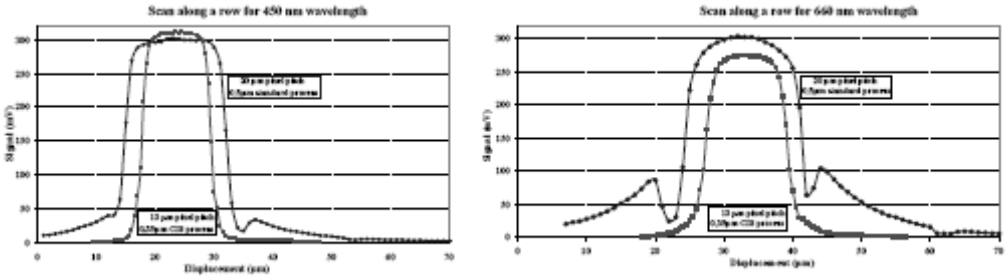
Wavelength (nm)	MTFx for standard 0.5 µm process	MTFx for CIS 0.35 µm process	MTFy for standard 0.5 µm process	MTFy for CIS 0.35 µm process
500	46%	69%	54%	74%
650	31%	67%	40%	73%
800	28%	63%	35%	68%

Table 7: for three wavelengths, MTF measurement at Nyquist frequency along the row and the column for a 0.5 µm standard process and a 0.35 µm optimized process

It should be noticed here that the MTF measurements corresponding to the improved process feature values higher than 63%, which is the expected maximum limit due to the spatial sampling effect. This

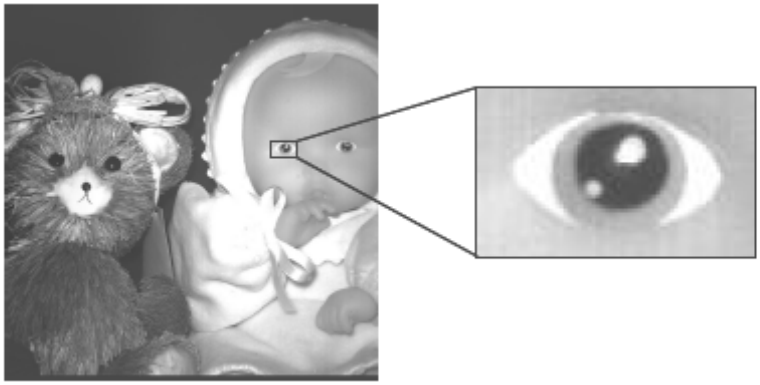
is explained by the non 100% pixel fill factor. Calculations of the theoretical geometric MTF using the real shape of the photosensitive area lead to 70% for MTFx and 78% for MTFy, very close to the experimental figures measured for 500 nm wavelengths.

As expected, the same behavior arose during the spot scan characterizations. Figures 8 compares intra-pixel responses and cross-talk measurements at two wavelengths for both 0.5 µm standard and 0.35 µm optimized CMOS processes. Once again, the improvement is particularly noticeable for the longest wavelength.



Figures 8: left: comparison of an intra-pixel spot-scan response along the row (450 nm wavelength) for a 20 µm pixel manufactured using a standard 0.5 µm CMOS process and for a 13 µm pixel manufactured using an optimized 0.35 µm CMOS process: right: same figure for 660 nm wavelength. Nearly no cross-talk can be seen for the optimized process, while in the case of the standard process, the response is non negligible when the spot is located in the neighboring pixel, particularly for the longest wavelength.

As a consequence, the quality of rough images is excellent, as shown by figure 9, acquired though a camera lens without any filter (and therefore including the NIR range of the spectrum).



Figures 9: rough image acquired using the 13 µm pixel pitch 1k x 1k CIS built with a 0.35 µm CMOS process optimized for image applications.

Some of the CIS performances can even more be improved by using pinned photodiode. Associated to a four-transistor intra-pixel circuitry, this type of photo detector offers a simple way to cancel the kTC noise and to adjust the conversion factor independently of the photodiode design (conversion factor in the 50 to 100 µV/e- range have been demonstrated), leading to few electrons read-out noise [9]. In

addition, pinned photodiodes offer a reduced dark current due to the pinning of surface-interface traps, an improved blue response and very low lag. Some large foundries over the World offer now pinned photodiodes through their CMOS process optimised for CIS. It is difficult to bet that this type of pixel will replace the widely used 3T pixels soon as the standard pixel architecture.

3.3 The hybrid approach

The third way that is considered for CIS performances improvements is the hybrid approach. The idea is the same as the one used for second generation cooled IR focal plane manufacturing, but exotic material (such as MCT, InSb...) is replaced by a silicon detector array. The main advantage of this approach is that it allows the independent optimisation of the photodetection layer on the one hand and of the read-out circuit layer on the other hand. In addition, hybridisation approach permits to reach 100% fill factor for the photodetector and gives more rooms for the associated in-pixel circuitry.

Today, manufacturers are investigating two different approaches. The first one [10] consists in the use of silicon monocrystalline detection layer hybridised on top of a CMOS read-out circuit, using indium bump techniques. The two main drawbacks linked to this approach are the minimum pitch, fixed by the limitation of hybridisation technology (typically 10-15 μm), and the cost of the detection layer manufacturing and the hybridisation process. At least two US manufacturers are today offering such visible hybrid arrays, relying upon their IR focal planes background. A first development started last year in Europe through an ESA contract.

The second approach [11] is based on the deposition of amorphous silicon (a-Si:H) thin film on top of the read-out circuit. When compared to silicon monocrystalline device, this approach avoids the need for a hybridisation technique, lowering the cost and allowing small pixel pitch manufacturing. Amorphous silicon detectors are expected to offer high quantum efficiency, low dark current and excellent MTF (due to its low lateral diffusion rate). On the other hand, the spectral response of standard a-Si:H rapidly falls down over 700 nm. In addition, some electro-optical parameters are expected to be worse than for monocrystalline silicon, such as technological noise, cosmetics and lag. Today, several institutes and manufacturers are working on this promising approach.

4 CONCLUSIONS

Today, the availability of CMOS processes optimised for imaging applications allows the design and the manufacturing of research grade CMOS imagers featuring low read-out noise (few electrons to few tens of electrons), high detection efficiency (up to 70% peak), low dark current density (in the 20 to 200 pA/cm2 range for 293 K) and high MTF, even at long wavelength (higher than 0.6 for Nyquist frequency). This has been confirmed by EADS-Astrium / Supaero-CIMI team via electro-optics characterisation of a 1k x 1k array featuring 13 μm pixel pitch and manufactured using a 0.35 μm CMOS process optimised for imaging applications.

The CIS performances will continue to improve in the near future thanks to design refinement and use of state of the art CMOS processes or hybrid approaches. Coupled to the numerous advantages offered by CMOS imagers, these electrooptics performances improvements definitively confirm that CIS will be the right answer for several short-term space applications including remote sensing ones.

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