View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by UTHM Institutional Repository

EEE_04

THE FIRST INVERTER FABRICATION IN UTHM CLEANROOM USING COST EFFECTIVE MASK

Mohd Zainizan Sahdan, Hashim Saim, Siti Hawa Ruslan, Rahmat Sanudin and Mohd Helmy Abd. Wahab
Faculty of Electrical & Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Batu Pahat, Johor, Malaysia.
Email: zainizan@uthm.edu.my

ABSTRACT

In MOSFET fabrication process, the process recipe is very important. A good process recipe will produce good MOSFET device. Universiti Tun Hussein Onn Malaysia (UTHM) has setup a cleanroom for ISO Class 100 and Class 1000. However, our cleanroom do not have its own recipe to develop MOSFET device. Therefore, it is a challenge for UTHM research group to develop this recipe. In this work, the first attempt to develop a process recipe for nMOS inverter has been done, which involved three stages. The first stage was designing and fabrication of cost effective mask using transparency films with channel length range from 500um to 30um. Then, the second stage was optimizing the process parameters. Finally, the third stage was fabrication of nMOS inverter using Modu-lab fabrication toolset. The nMOS inverter was successfully fabricated and this work becomes a starting point for the UTHM research group to do further research in nanoscale transistor and Microelectromechanical System (MEMS) device.

***Keywords**: Cleanroom, process recipe, nMOS inverter and MEMS.*

INTRODUCTION

Semiconductor wafer fabrication is one of the most complex manufacturing processes found today [1]. A lot of research has been done by industries and universities to reduce the manufacturing cost. In MOSFET fabrication process, several modules are involved such as photolithography, oxidation, diffusion and metallization [2]. Each modules involved several processing equipments and chemical which is very expensive to handle. Photolithography process module is very critical since it needs to produce an accurate dimension of the pattern, which is called pattern transfer.

In the photolithography process, mask design is very important because it will determine whether the circuit designed is able to be fabricated. However, advanced mask especially for smaller scale microchip is very expensive [3]. This advanced mask can be replaced with a low cost simple mask technology using transparency film. This simple technology can reduced the manufacturing cost.
The process recipe is a set of optimized process parameters which is obtained from experimentation. The parameters of each module will be optimized by controlling the gas flow, time and temperature. There are two methods of finding the process parameters; using software and using experimentation. Software such as TCAD Synopsis will provide good result of determining the process recipe. However, experimentation will provide more accurate result.

In this paper, the first nMOS inverter has been fabricated using Modu-lab toolset. The nMOS inverters are the building blocks of nMOS digital circuits. They use only n-channel MOSFETS, which have low channel resistance because of greater mobility of electrons in an n-channel. There are several types of nMOS inverter but for this project enhancement load nMOS inverter type was used which fabrication procedure becomes simpler with this type. The nMOS inverter is a combination of two enhancement-type transistors and used as the driver because it will be off when the input voltage V_{in} is low and because its drain and gate voltages have the same polarity as shown in Figure 1. This feature allows direct coupling between stages (that is, one stage can be connected to the next one without any coupling capacitor) [4].

ISBN 978-983-41705-6-1 ©2007 FEIIC

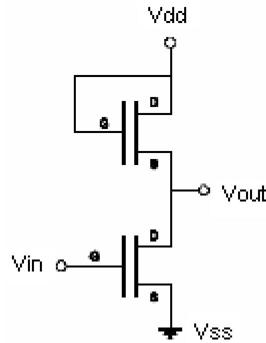

Figure 1: The nMOS inverter circuit

MASK DESIGN AND CREATION

The processes and equipments used in the MOSFET fabrication will determine the number of steps in the process flow. The process flow developed in Virginia Polytechnic Institute and State University comprised of nine processing steps for nMOS transistor [2]. This process flow was modified and used to fabricate the nMOS inverter as shown in Figure 2.

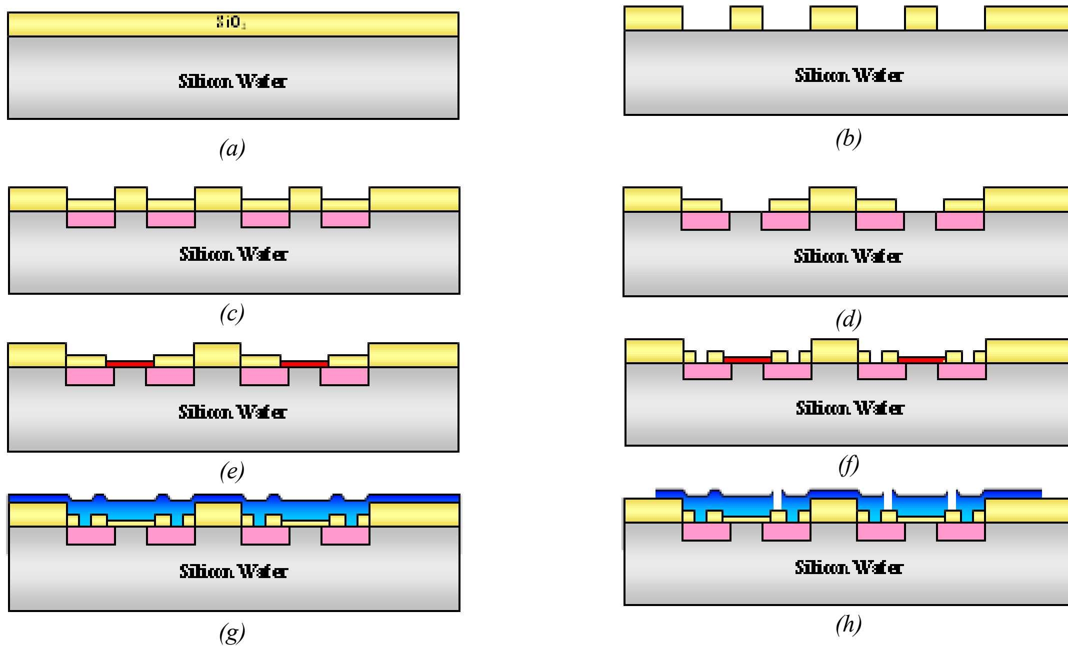

Figure 2:The nMOS Inverter Proces Flow; (a) wet oxidation process (b) photolithography 1 (c) diffusion process (d) photolithography 2 (e) dry oxidation (f) photolithography 3 (g) metallization (h) photolithography 4

This process flow comprised of eight steps which involved four photolithography processes as shown in (b), (d), (f) and (h). This photolithography process requires different mask design to protect the pattern of nMOS inverter circuit. Using this process flow, four masks have been designed for diffusion, dry oxidation, contact etching and metal etching processes. The mask designed using AutoCAD is shown in Figure 3 below.

ISBN 978-983-41705-6-1 ©2007 FEIIC

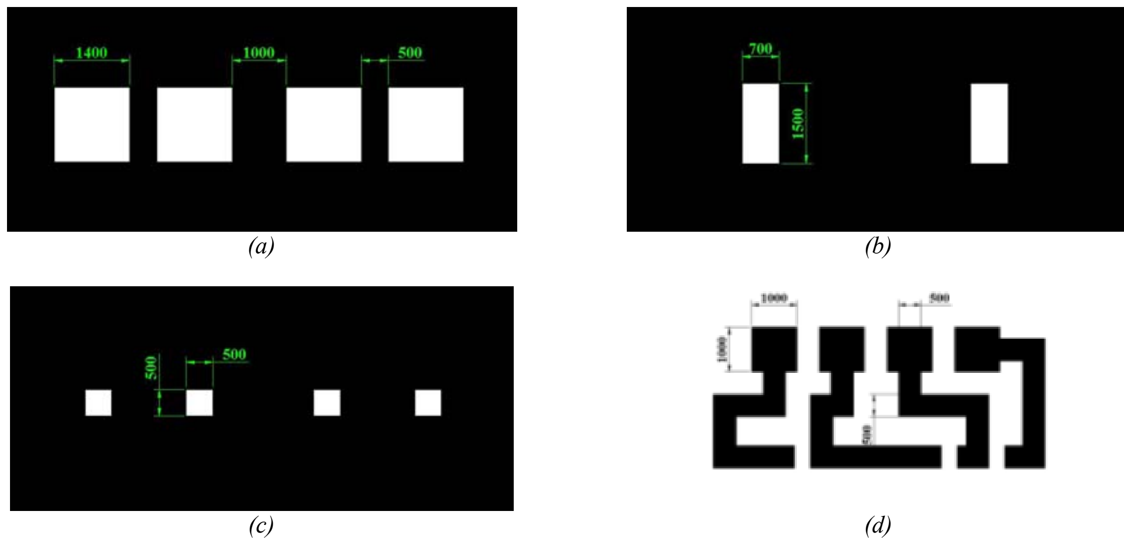

Figure 3: The mask design using AutoCAD (a) diffusion mask (b) gate mask (c) contact mask (d) metallization mask

Mask in Figure 3(a) was designed for diffusion process to define the source and drain region. Mask in (b) was designed to develop thin oxide layer using dry oxidation process. The mask in (c) is designed to make contact holes for routing purpose and (c) is used to define the metal line for nMOS inverter.

The masks designed using AutoCAD™ were fabricated using standard transparency film. Standard transparency film was used since it is very cost effective and reliable. The mask set is shown in Figure 4 below.

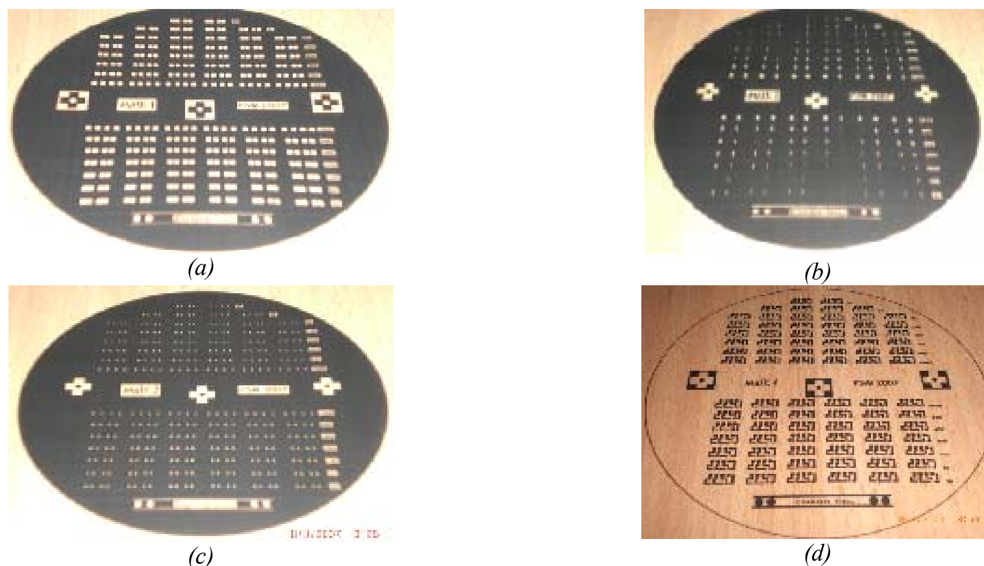

Figure 4: The mask fabricated using standard transparency film (a) diffusion mask (b) gate mask (c) contact mask (d) metallization mask

PROCESS OPTIMIZATION

Process optimization has been done using experimentation in the UTHM cleanroom. There are three processes that have been optimized in this work; wet oxidation, dry oxidation and metallization. The purpose of wet oxidation is to grow a physical mask that act as a barrier between the dopant. Since the rate of diffusion of the dopant is much slower in SiO_2 than in single crystal, a thick oxide layer will not allow the dopant to penetrate the oxide layer and diffuse in the substrate [2]. In wet oxidation process, the silicon wafer was preheated to 600^oC for one minute. Then, it will be oxidized in 1000^oC oxidation furnace using parameters shown in Table 1 below;

Table 1: Variation of wet and dry oxidation time

Wafer	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6
Oxidation Time (Hour)	1	1 ½	2	2 ½	3	3 ½

The dry oxidation process has been done to grow high quality thin oxide for the gate. It will serve the dielectric between the source and drain. The thickness of the gate oxide is chosen specifically for the scaling requirements of the nMOS inverter. The thickness of this oxide layer must consider the theory that any cutback in the gate oxide thickness will enhance the gate controllability as an effect of the tunnelling limitation in the inverter. The variation of gate oxide thickness using dry oxidation process is shown in Table 1.

The metallization process provides proper interconnection of circuit for the nMOS inverter. Aluminium is the most popular metal used since it adheres well to both silicon and silicon dioxide. The optimisation of metal usage was needed because if it is too little it will not spread flatly and if it is too much will cause wasting of sources. Hence, it will increase the manufacturing cost. The variation of aluminium film area that will be used is shown in Table 2.

Table 2: Variation of Aluminum film area

Wafer	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6	Wafer 7
Aluminum film area (mm)	15x15	20x20	25x25	30x30	35x35	40x40	45x45

RESULTS

The cost effective mask design using AutoCAD™ has been used in photolithography processes. The patterns of nMOS inverter have been successfully transferred and the images are shown in Figure 5.

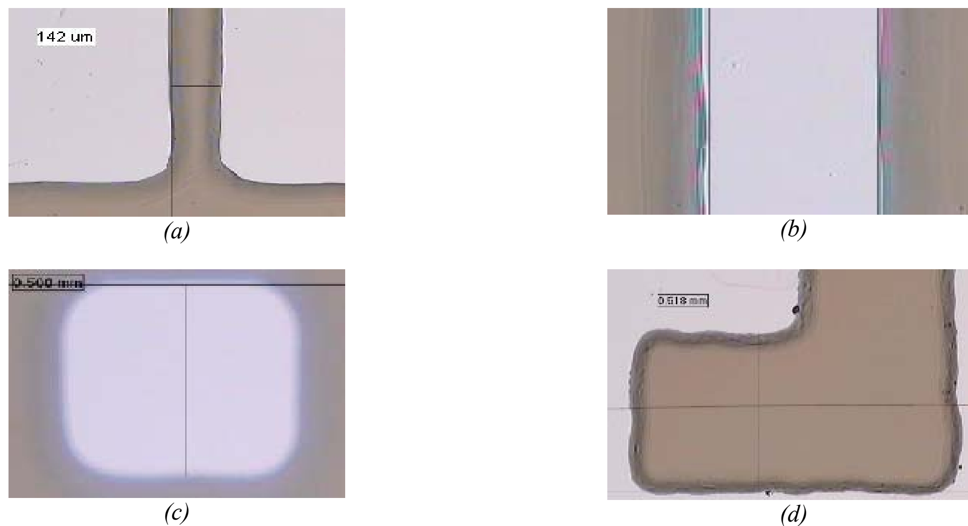

Figure 5: Then nMOS inverter pattern after photolithography process (a) diffusion region and channel length (b) gate (c) contact (d) metal line

Figure 5(a) shows the diffusion area with channel length of 142 um. The darker area is the oxide layer while the bright area is the diffusion region. In this case phosphorus is used. The gate region is shown in (b) and the contact region is shown in (c). In (d), the darker area is the aluminium metal line while the bright area is the oxide layer. This metal line is used to probe the nMOS inverter and to check the electrical characteristic.

ISBN 978-983-41705-6-1 ©2007 FEIIC

After the wet oxidation process has been done, the growth rate for the wet oxidation process was obtained as shown in Figure 6.

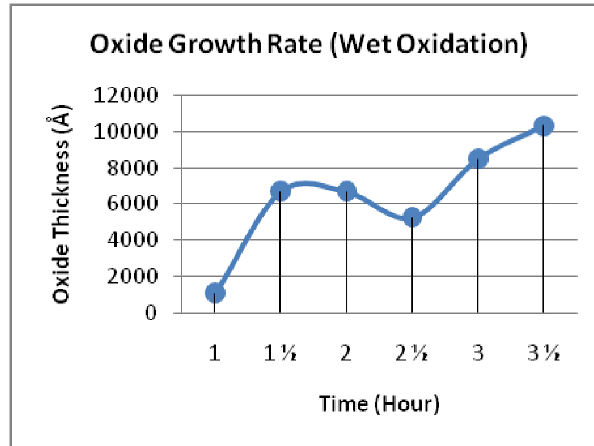

Figure 6: The growth rate for wet oxidation process

From the graph in the Figure 6, the oxide growth for the given time is not uniform, as can be seen that for 2 hours and 2 ½ hours oxidation time gave a slight drop in oxide thickness. This is inconsistent with the theory that longer oxidation time will increase oxide thickness. The reason for this problem is because of the positioning of the wafer during the oxidation process. For a good oxidation growth, the boats need to be filled with wafer during any oxidation process. In this case, the oxidation is done only with a single wafer and four oxide dummy is used. For the wet oxidation, the oxidation time is set for three hours.

However, the growth rate for dry oxidation process for gate oxidation depicts the correct graph compared to the theory. Figure 7 shows the oxide growth for the given time is uniform. Based on the graph, the selected dry oxidation time for the recipe is three hours since the oxide thickness is sufficient for the MOSFET structure.

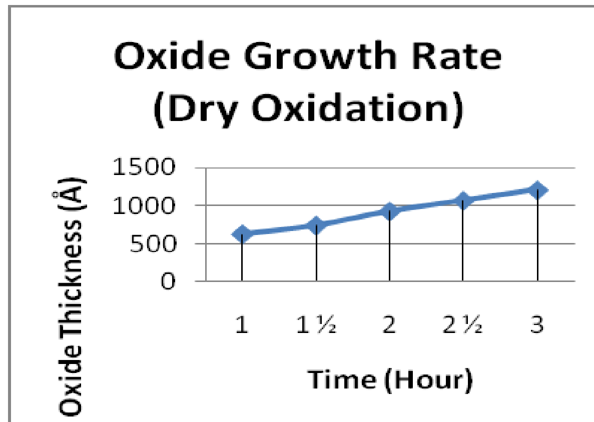

Figure 7: The growth rate for dry oxidation process

After metallization process is done, the thickness of aluminum is measured in unit of Angstrom (Å) at 21 point on wafer surface. Figure 8(a) and (b) show the samples results of aluminum thicknesses with different parameter after metallization process.

ISBN 978-983-41705-6-1 ©2007 FEIIC

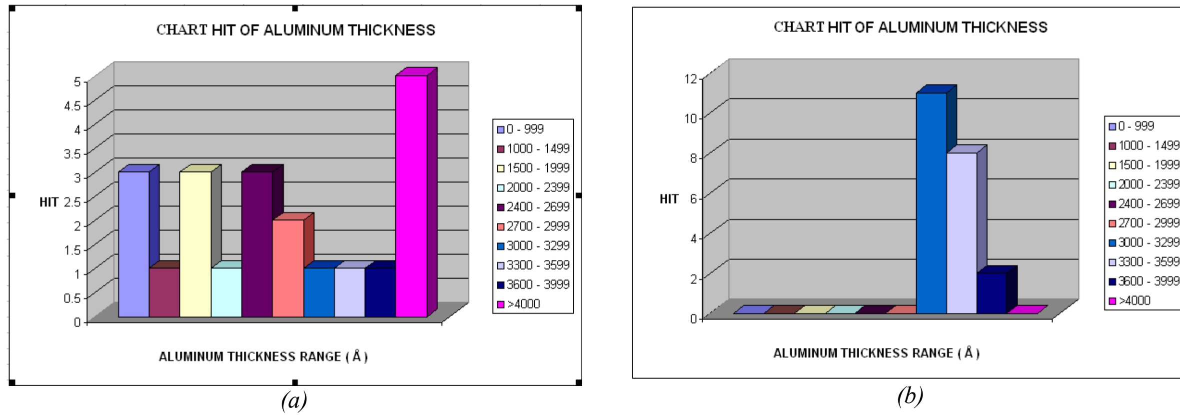

Figure 8: The hit value of aluminum thickness

To acquire uniformity of aluminium thickness, the obtained hit value should be in one range only as shown in Figure 8(b). The result from the experimentation shows that metallization using aluminium foil of 40mm × 40mm results the best uniformity compared to the other parameters.

CONCLUSIONS

The UTHM Microelectronic Cleanroom has been actively doing research in semiconductor fabrication process. An nMOS inverter has been fabricated using cost effective masks and process optimization for wet oxidation, dry oxidation and metallization was done completely. The nMOS inverter masks using standard transparency film has greatly reduced the manufacturing cost. These cost effective masks have been used in photolithography process and the nMOS inverter pattern has been successfully transferred on silicon wafer. The nMOS inverter process flow was developed and has been successfully used to fabricate the nMOS inverter. After the process optimization, the wet and dry oxidation parameter obtained is 3 hours. The metallization process is using 40mm x 40mm aluminium foil. This nMOS inverter is the first inverter fabricated in UTHM cleanroom and the recipe will be used for teaching undergraduate program.

ACKNOWLEDGEMENT

The authors would like to thank En. Ramlan Ralim for the technical support in the UTHM Microelectronic cleanroom.

REFERENCES

[1] Qi Chau and Appa Iyer Sivakumar (2004) *Simulation Based Cause and Effect Analysis in Semiconductor Wafer Fabrication,* Journal of The Institution of Engineers, Singapore, Vol. 44.
[2] David Gray (2002) *Optimization of the Process for Semiconductor Device Fabrication in the MICRON636 Whittemore Cleanroom Facility*, Virginia Politechnic Institute and State University.
[3] Jeffrey Bonn, Sharon Sisler and Patricia Tivnan (2001) *Balancing Mask and Lithography Costs* Proc. IEEE/ Advanced Semiconductor Manufacturing Conference.
[4] Peter Van Zant (2004) *Microchip Fabrication 5th Edition*, Mc Graw Hill.
[5] Michael Quirk & Julian Serda (2001) *Semiconductor Manufacturing Technology*, Prentice Hall, New Jersey

ISBN 978-983-41705-6-1 ©2007 FEIIC