Simulation Study on NMOS Gate Length Variation Using TCAD Tool

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Abstract ? The process of scaling in silicon transistor has consistently resulted in smaller device geometry, higher device density and better performance. In conventional MOSFETs, control of Ioff for scaled devices requires very thin gate dielectrics and high doping concentrations. The industry roadmap predicts the barriers of continuous scaling will be due to physical limitations as well as practical technology. As the downscale of CMOS technology approaches physical limitations, the need arises for alternative device structures. Thus, this paper intends to study the effect of various gate lengths on the NMOS electrical characteristic by means of simulation study.

INTRODUCTION

Silicon CMOS has emerged as the predominant technology in semiconductor industry. It has been continuously scaled down in terms of size but higher capacity and complexity. As device size as came into nanoscale regime, therefore novel structure is needed. Conventional MOSFET also suffers from higher leakage current, short channel effect and doping uniformity. NMOS structure is proposed in order to reduce the leakage current and offer better handling of short channel effect.

The purpose of this paper is to show NMOS structure is able to eliminate the problems in conventional MOSFET and to prepare for nanoscale device. In this paper, the effect the gate length on the transistor characteristic is shown by means of simulation work using the Sentaurus TCAD software. In other words, the output of NMOS transistor is plotted in order to see the difference yield by various transistor gate length.

RELATED WORK

Simulation of MOSFET performance has been done since three decades ago. A two-dimensional simulation of MOSFET with 0.25 micron technology shows that the two dimensional energy distribution was stably calculated using several algorithms [1]. This technique is also useful in analyzing the effect of hot carrier in short channel MOSFET. Based on the two-dimensional technique, the substrate and gate current resulting from impact ionization are calculated. This ionization is due to the electron-hole generation and their injection into gate oxide [2]. The improved injection model uses non-Maxwellian distribution function and taking into account of separate contribution to the gate current from both of thermionic emission and oxide-barrier tunneling. The simulation model is improved further by including the quantum effect of electrons in inversion layer and surface scattering effect due to the interfacial charges. The improvement shows that the quantum broadening effect has been proven significant in simulation model [3]. In addition, it also shows the modeling of Coulomb scattering plays important role in simulating hot-carrier-induced MOSFET degradation.

The introduction of multicolor contour, average-energy based, substrate current model for silicon submicrometer gives significant improvement to local-field model used in modern drift-dimensional device simulators [4, 5]. The model used shows strong outstanding agreement between simulation and experiment result over a wide range of bias conditions and channel lengths. Further improvement implements other techniques such as for highly doped NMOS [6], quantum mechanical effect [7, 8], low-voltage super-junction application [9] and quantum confinement effect with Gaussian wave packet [10]. Software package tool is then widely used in simulation that integrates with circuit fabrication [11], followed by analog performance in MOS device assessment [12] and modeling of the nanoscale MOSFET has emerged as new trend in MOS simulation process [13].

EXPERIMENTAL PROCEDURE

MOSFETs operate in such a way that the current from the source to drain is carried by electrons (NMOS), by holes (PMOS) or by both electrons and holes in the case of

complementary MOSFET (CMOS). Figure 1 shows a schematic of an NMOS device with p-type substrate. A voltage is applied to the gate that 'inverts' the polarity of the carriers and produces electrons near the oxide-semiconductor interface. The gate length is one of the most critical parameters controlling device performance. The body or substrate of a MOSFET can also be contacted and a bias applied to it.

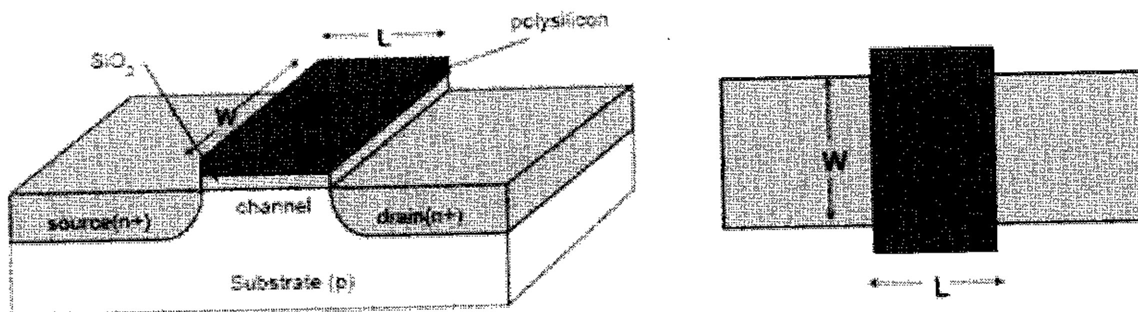


FIGURE 1 The side and top view of n-type MOSFET structure

Sentaurus includes a comprehensive suite of core TCAD products for multidimensional process, device, and system simulations, embedded into a powerful user interface. The comprehensive Sentaurus TCAD suite bridges the needs of development and manufacturing engineers by improving semiconductor process control in manufacturing. In this paper, Sentaurus TCAD is used extensively right from the start of the device modeling, construct the device structure, determining the process flow and finally plotting the device output characteristic. Upon plotting the device characteristic, all process parameters have been established. Figure 2 depicts the process flow in simulating the NMOS transistor in the Sentaurus TCAD.

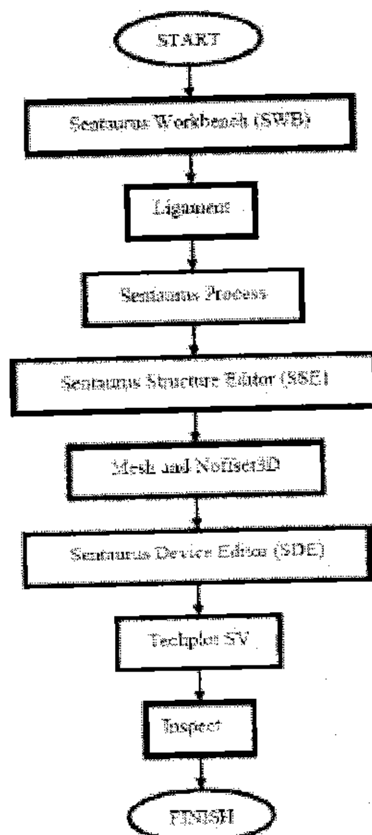


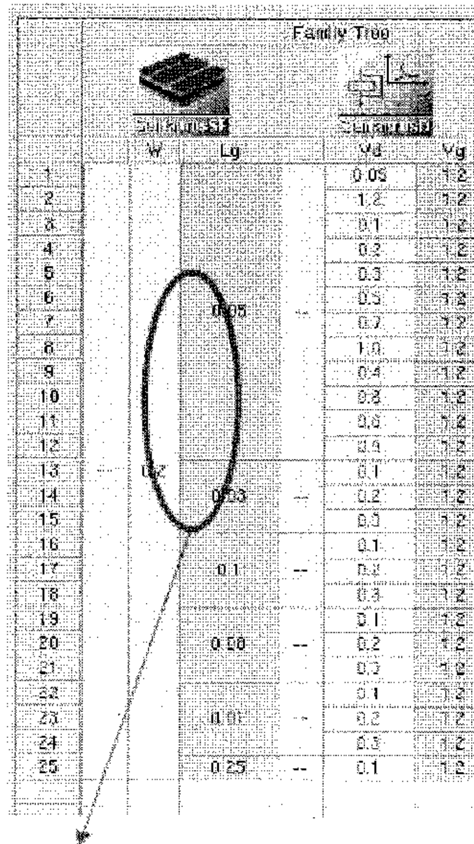
FIGURE 2 Flow chart of n-channel MOSFET simulation process

RESULT AND ANALYSIS

A. Device Simulation

The gate length of device used in this project is shown in Figure 3. The physical gate length, Lg has been varied from 30nm to 100nm and 200nm width (W) for more detail parameter comparison such as on Ioff and Ion ratio, threshold voltage(VT), subthreshold swing (SubVT), short channeleffect (SCE) and also DIBL (Drain Induced Barrier Lower) effect. In order to get nearly ideal subthreshold swing (SubVT) and small DIBL effect, the silicon body must be very thin and fully depleted.

Figure 3 also shows that gate length and gate voltage, Vgs also has been varied from different values. Drain voltage, Vd is fixed at same value 0 to 1.2V only. All these can be done using Sentaurus Workbench (SWB) interface that employs device simulator 3D Sentaurus TCAD. While it is currently impractical for experiments, this study can be used to project performance goals for aggressively scaled devices.



Variation of gate length values : 30nm, 50nm and 100nm

Figure 3 SWB interface with project loaded

B. Device Structure

The simulations of device structure for every gate length were shown in Figure 4, 5 and 6. The device structure is design and simulated using Sentaurus TCAD software package. It has been reported that 30nm in Figure 4 gate length n-channel MOSFET's can be

fabricated by reducing the source and drain junction depths to 10nm. These shallow junctions were successfully produced by solid-phase diffusion achieving a sheet resistance of less than 10kohm/sq. The current drive and transconductance of these devices showed a 30% improvement over the Figure 6 for 100nm MOSFET's. Although not very large, this increment can be considered reasonable considering the technological difficulties faced in increasing current drive beyond the 100nm regime. The rather limited improvement can be partially attributed to the fact that the sheet resistance of the ultra-shallow source and drain layers is not very low and partially to the fact that the carrier velocity reaches saturation in 30nm devices.

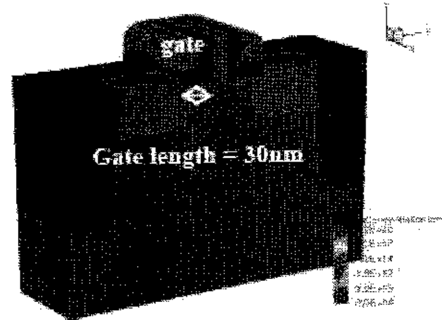


Figure 4 Device structure of gate length 30nm NMOS simulation

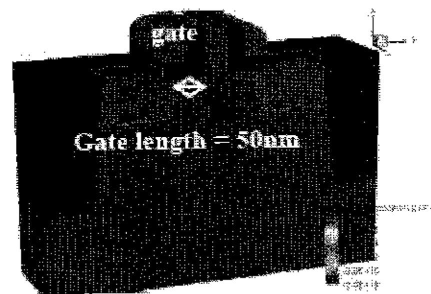


Figure 5 Device structure of gate length 50nm NMOS simulation

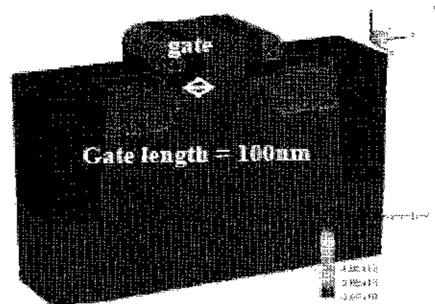
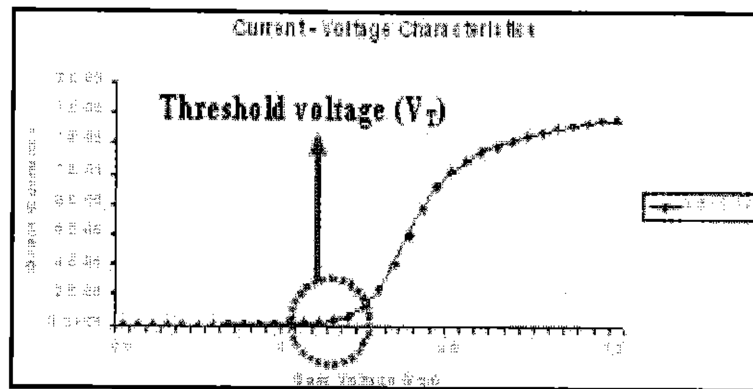


Figure 6 Device structure of gate length 100nm NMOS simulation

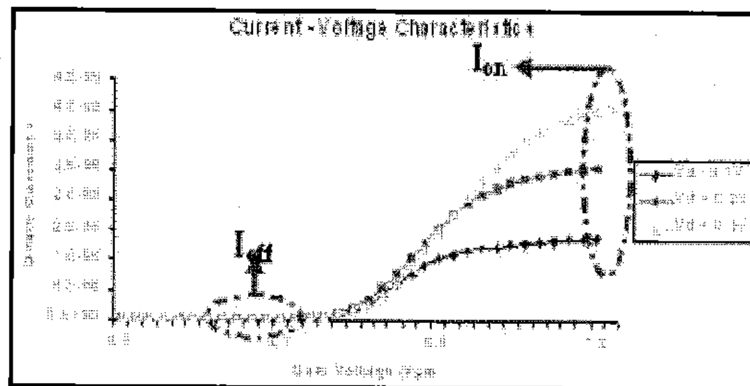
C. Electrical Characteristic

Figure 7, 8 and 9 illustrate the current-voltage (Id-Vgs) characteristics and subthreshold curves for NMOS device of channel length Lg at 30nm, 50nm and 100nm respectively with uniform boron doping concentration of 10^{12} cm^{-3} to 10^{20} cm^{-3}. The measured threshold voltage is shown in Figure 7(a). In Figure 7(b), three curves represent simulated output at Vds = 0.1V, 0.2V and 0.3V separately for gate length 30nm. In Figure 7(c), Vgs sweeps from 0V to 1.2V which produced Ion – Ioff current ratio, subthreshold

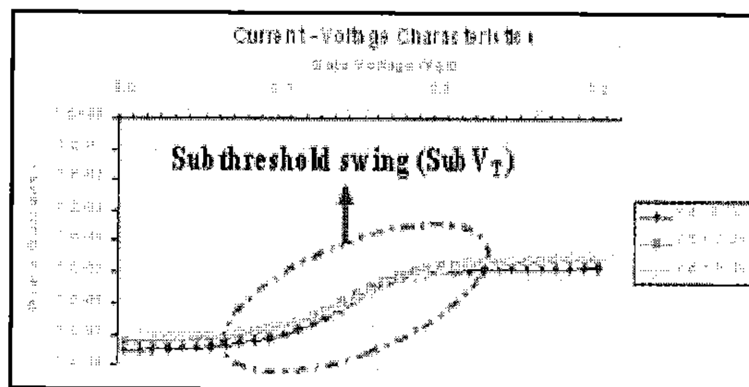
swing and leakage current. All these characteristics are the same for the gate length at 50nm and 100nm respectively.



(a) Threshold voltage at Vd – 0.1V



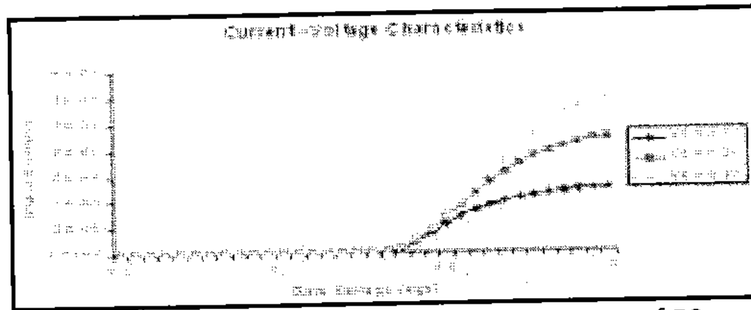
(b) Current-Voltage (Id – Vgs) characteristics of 30nm



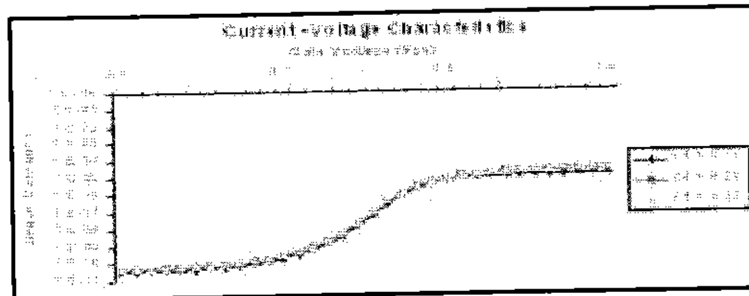
(c) Subthreshold curves of 30nm with SubVT = 116mV/dec, I_{off} = 31nA/μm and Ion = 14μA/μm at Vds = 0.1V

Figure 7 I-V characteristics of NMOS with Lg = 30nm and VT = 0.12V taken at Vds = 0.1V, 0.2V and 0.3V

For comparison between 30nm with 50nm and 100nm gate length as shown in Figure 8 and 9, the results obtained show a good off-state leakage current I_{off} of 0.61pA/μm and drive current Ion of 7μA/μm at 100nm gate length because the I_{off} is lower than I_{on} current. When gate voltage decreases, drive current goes higher because the gate length expands from 30nm to 100nm and this will provide more current to pass through it.

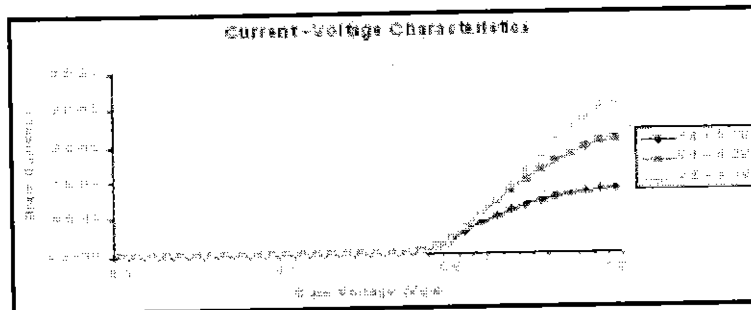


(a) Current-Voltage (Id – Vgs) characteristics of 50nm

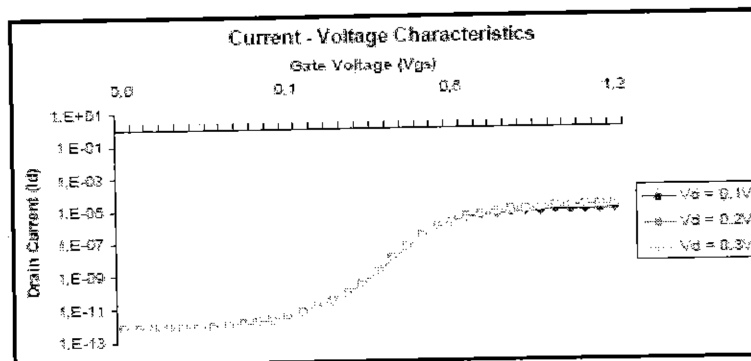


(b) Subthreshold curves of 50nm with $SubV_T$ = 85mV/dec, I_{off} = 34pA/µm and Ion = 12µA/µm

Figure 8 I-V characteristics of NMOS with Lg = 50nm andVT = 0.32V taken at Vds = 0.1V, 0.2V and 0.3V



(a) Current-Voltage (Id – Vgs) characteristics of 100nm



(b) Subthreshold curves of 100nm with SubVT = 81mV/dec, I_{off} = 0.61pA/µm and I_{on} = 7µA/µm

FIGURE 9 I-V characteristics of NMOS with Lg = 100nm and VT = 0.41V taken at Vds = 0.1V, 0.2V and 0.3V

CONCLUSION

The design and simulation of gate length effect on NMOS electrical characteristics based on the gate length variation has been successfully done using commercial 3D Sentaurus TCAD tools. By employing the inversion layer mobility model from Lombardi combined with SRH (Shockley-Read-Hall Recombination), a detailed investigation on the n-channel MOSFET performance was done. With a good drive current I_{on} of 7μA/μm and a low off-state leakage current I_{off} of 0.61pA/μm was explicitly shown for 100nm NMOS. Besides, the subthreshold characteristics also highlighted a reasonably well-controlled SCE with subthreshold swing $SubV_T$ = 81mV/decade and threshold voltage V_T = 0.41V. Efforts to reduce the sheet resistance still further are continuing, with the aim of further improving current drive.

ACKNOWLEDGMENT

The authors would like to thank Universiti Tun Hussein Onn Malaysia for the facilities and technical support in completing this work.

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