Structure Design Challenge in Nano-CMOS Device

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Abstract

This paper intends to report the problems and challenges that lie ahead in transistor design methodology in nano-CMOS structure. Thus, it is desired to see the options in improving the device design on top of continuing the scaling process of transistor in the next few years to come. The main concern is to see how the transistors behave as the size of device shrinks down to below 100nm range. Besides, the demand of future generations is expected as a result of more compact of digital circuit. It is concluded that although several problems surfaces as the transistor enters the nano-CMOS era, there are excellent options to solve those problems and thus could help to reduce the transistor size and yet uncompromised the device performance.

1. INTRODUCTION

Since the inception of first transistor in 1965, the development of this remarkable device moves in exponential curve. The Moore's Law, which introduces by Gordon Moore, has become the catalyst to drive the transistor technology and thus the advancement of the semiconductor industry. As the industry has reached the technology of 65nm gate length, it is obvious that the sub-100nm era will conquer device technology in future. Apparently, there are challenges in term of the physical design and process control as the existing design and process may no longer suitable applied in nanoscale semiconductor device.

The first part of this paper gives an overview the transition period of transistor scaling within the past 30 years. The second part presents several challenges and problems that may ruin the performance of transistor. The final part discusses the needs in changing the design methodology to cater the solution of building the nano-CMOS device.

2. TRANSISTOR EVOLUTION TO NANO-CMOS

The first transistor was invented in 1964 and it is not a surprise it has dominated the digital applications since then. High reliability, low power consumptions and can be packed in large numbers in a single package of relatively small size are the advantages of this device. Scaling is a process, first introduced in 1974, to reduce the size of transistor and to improve its performance. A reduction of transistor size through scaling process results in improvement of device density, switching speed and power consumption [1]. For example in ideal scaling, as the dimension and the operating voltage reduces by a factor of 0.7, the area density is doubled, switching delay reduced by factor of 0.7 and the switching energy is halved. Reduction of switching energy is very important especially if the system has been operated for a long period. Scaling process has significantly helps to reduce the transistor size and to improve the switching energy and speed. As shown in Fig. 1, the transistor size has reduced from 3µm in 1970s to 0.13µm in 2000 and it leads to tremendous increment the density of integrated circuit in the past 30 years as in Figure 2. Both figures do, indirectly, verify the prediction of Moore's Law.

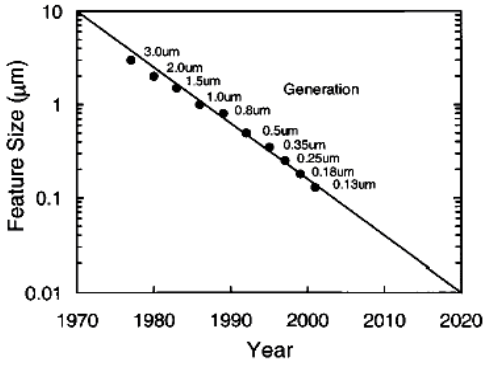

Figure 1. Semiconductor technology minimum feature size trend

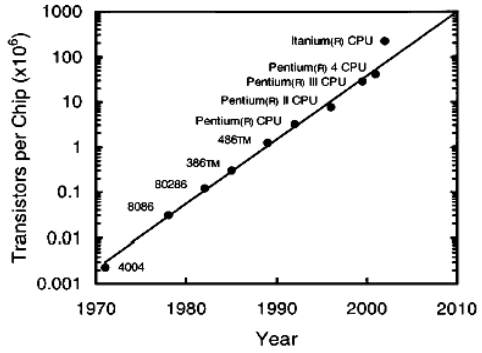

Figure 2. Intel CPU transistor count trend

Nevertheless, as the transistor size continues to decrease even further, the scaling process will not be able to meet the demand for future expectation and application. This is due to the fact that there are several factors that could affect the device performance as its size approaches sub-100nm scale.

3. CHALLENGES AND PROBLEMS IN NANO-CMOS

There are several problems that appear as the transistor size reaches nanometer scale and thus become the limiting factor on the device performance. Among the problems is short channel effect, tunnelling effect, ballistic transport, oxide thickness and threshold voltage.

Short-channel effect is a notable effect that introduces several leakage current mechanisms as shown in Figure 3 [2], [3].

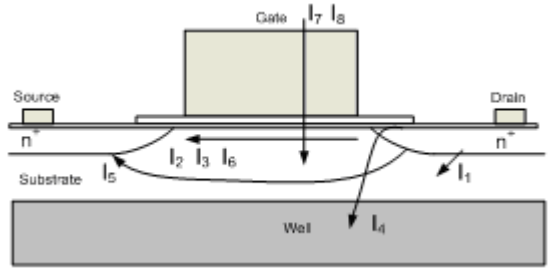

Figure 3. Short-channel-transistor leakage current mechanisms: reverse-bias p-n junction leakage (I_1), weak inversion (I_2), drain-induced barrier lowering (I_3), gate-induced drain leakage (I_4), punch-through (I_5), narrow-width effect (I_6), gate oxide tunneling (I_7), and hot-carrier injection (I_8).

Reverse-bias p-n junction exists due to minority carriers' diffusion near the depletion region and electron-hole pair generation in depletion region. Weak inversion current occurs when gate voltage is lower than threshold voltage. Drain induced barrier lowering (DIBL) current exists when source potential barrier is reduced as a result of the drain's depletion region interacts with the source and could lower the threshold voltage. Gate-induced drain lowering (GIDL) current occurs along the channel width between gate and drain. Punchthrough happens when both drain and source depletion regions touch deep in the channel. Narrow-width current arises when the channel length is reduced to less than 0.5µm. Gate-oxide tunnelling current occurs when the oxide layer is made very thin and causes gate leakage current tunnelling through oxide bands. Hot-carrier injection, on the other hand, occurs when hot carriers are injected into the oxide.

Another effect occurs as transistor is scaled down is tunnelling effect between neighbouring transistors. Normally, the transistors are separated sufficiently enough so that the operation of one transistor does not affect another transistor as shown in Figure 4 [2].

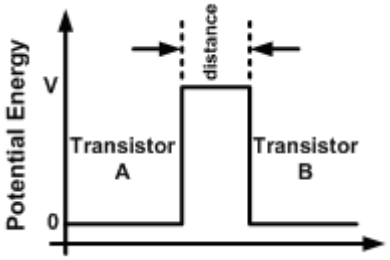

Figure 4. Potential barrier between two transistors

The separation is made by inserting material that acts as a barrier between any two transistors. However, as the transistor size approaches nanoscale and thus the barrier distance becomes extremely small, there is possibility that the carriers of one transistor cross the barrier. The tunnelling effect increases exponentially as the barrier distance is decreased.

The ballistic transport, carrier transport mechanism in transistor, is also affected as transistor size reaches nanoscale [4]. When an electron travels from source to drain, it experiences scattering effect that causes its energy to decrease. However this mechanism deviates as the device size is in nanoscale as shown in Figure 5. The electron travels without scattering effect due to small travelling distance. Ballistic transport effect caused the on-current to improve due to less scattering and hence it is seen as a desired effect on transistor performance.

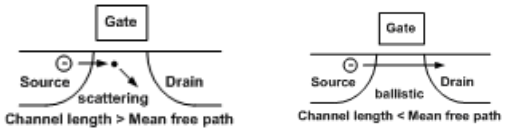

Figure 5. Ballistic transport in transistor channel

Another problem as transistor reaches nanoscale is that the threshold voltage is not decreasing proportional to channel length. The threshold voltage is almost held constant when channel length is 1µm – 0.1µm but as channel length drops below 0.1µm, the current does not drop to zero immediately but

decreases exponentially inversely proportional to thermal energy as shown in Figure 6 [5]. This is due to some thermally distributed electrons at source terminal have enough energy to overcome potential barrier controlled by gate voltage. Higher threshold voltage gives higher leakage current in the transistor since leakage current, I_{off}, is given as

$$I_{off} = I_0\left(-\frac{qV_t}{mkT}\right)$$

where I_0 is extrapolated current per width at threshold voltage, m is dimensionless factor (≈1.2) and V_t is the threshold voltage. The leakage current is reduced ten times for every 0.1V reduction of threshold voltage. Thus the threshold voltage should be seriously considered in order to have strong performance of nanoscale transistor.

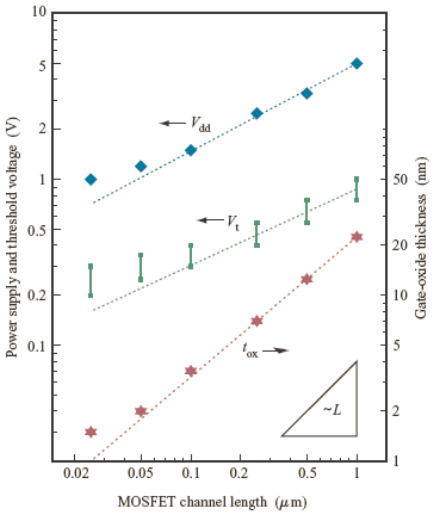

Figure 6. Measured and calculated oxide tunnelling current vs. gate voltage for different oxide thickness

As the transistor size is reduced, the gate-oxide thickness must also be reduced [5]. Reduction in gate oxide thickness will ensure that gate terminal have more control than drain terminal but eventually cause gate leakage current to increase since it is related to quantum effect tunnelling. The resulting tunnelling current probably looks negligible compared to on-state current as depicted in Figure 7, but it is significant when the chip is at standby mode. Furthermore, there is loss of inversion charge and transconductance as a result of inversion-layer quantization and polysilicon-gate depletion effect [6].

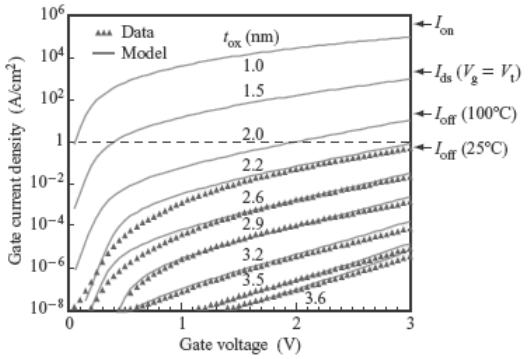

Figure 7. Trends of threshold voltage and gate oxide thickness vs. channel length for CMOS technology

4. DESIGN METHODOLOGY OF NANO-CMOS

Leakage current becomes one of the main concerns in designing nano-CMOS. It must be addressed since it contributes to higher power consumption especially during the standby mode. Memory should tolerate higher leakage but not to drop off the efficiency significantly. To have better leakage management, a longer channel length and higher threshold voltage can be introduced. In turn, it will introduce higher access time and hence lower leakage power. Trade-off between power consumption, performance and process complexity becomes more difficult and therefore it must be weighted against the cost.

Introduction of copper as the interconnection has eliminate the effect of electromigration and improve the interconnect performance in 130nm technology. Low-κ dielectric has been imposed to improve the performance of interconnection but due to low thermal conductivity and coupled with higher signal speed, the problem of electromigration is increasing.

5. CONCLUSION

This paper presents the issue of transistor as the size approaches below 100nm scale. It starts with great achievement of scaling process that leads to enormous development in term of transistor size and chip density. It then reveals some problems that arise as the size of transistor decreases in nanoscale. Finally, the needs in design changes in building nano-CMOS is presented as to eliminate the problems and thus to improve the performance of nanoscale transistor.

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