

FPGA-based Architectures of Finite Radon Transform for Medical Image De-noising

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Abstract—This paper presents the design and implementation of finite Radon transform (FRAT) on field programmable gate array (FPGA). To improve the implementation time, Xilinx AccelDSP, a software for generating hardware description language (HDL) from a high-level MATLAB description has been used. FPGA-based architectures with three design strategies have been proposed: direct implementation of pseudo-code with a sequential or pipelined description, and block random access memory (BRAM)-based approach. Various medical images modalities have been deployed for both software simulation and hardware implementation. An analysis on the image de-noising using the FRAT is addressed and demonstrates a promising capability for medical image de-noising. Moreover, the impact of different block sizes on reconstructed images has been analysed. Furthermore, performance analysis in terms of area, maximum frequency and throughput is presented and reveals a significant achievement.

Keywords— Finite Radon transform, medical image de-noising.

I. INTRODUCTION

The contributions of transform domains in various spectrums of operations including image de-noising, enhancement, and compression are undebatable facts. As an example, the wavelet transform has been extensively used as a solution to the short time Fourier transform (STFT), and excels in isolation discontinuities and spikes [1]. However, the wavelet suffers from inflexible directionality as it does not isolate the smoothness along edges.

These demerits of wavelet are well addressed by the ridgelet and curvelet transforms, as they extend the functionality of wavelets to higher dimensional singularities, and it is proven as an effective tool to perform sparse directional analysis. The basic building block of these transforms is the finite Radon transform (FRAT).

In medical imaging applications, three-dimensional (3-D) modalities have been widely exploited for more truthful

assessment of pathological changes [2]. Although remarkable contributions for screening and diagnosis can be achieved with 3-D modalities, the complexities of their algorithms are computationally demanding. Since medical images contain several objects and curves, the ridgelet, curvelet and the FRAT as its basic building block play a significant role for better medical image analysis. The FRAT algorithm is inherently serial, iterative and has long latency. By off-loading the intensive processing procedures into a properly hardware platform, computational acceleration can be achieved whilst maintaining the outcomes quality. Field programmable gate arrays (FPGAs) with massive parallelism options, multimillion gate counts and special low-power packages appears an attractive solution for FRAT's hardware implementation.

A comprehensive survey of literature indicates that the research is still in its infancy as demonstrated by the limited contributions for the FRAT's FPGA implementations and have only been investigated in the context of general image processing [1], [3]–[6]. From the programming approaches and hardware implementation perspectives, various approaches were used: Verilog HDL [4], Handel-C [5], [6] and the latest by Chandrasekaran *et al.* [1] with the combination of Handel-C and parameteriseable VHDL core (Coregen).

This paper presents the design and implementation of FRAT's FPGA-based architecture for medical image de-noising by employing Xilinx AccelDSP tool. The Xilinx AccelDSP has been selected, since it can converts automatically from high-level languages (HLLs) to register transfer level (RTL) HDL and even directly to FPGA configuration bitstream [7]. Apparently, this feature is important to reduce the design cycle as well as to allow more optimisation to be carried out on the algorithmic and architectural level. The proposed architectures will be deployed in a reconfigurable environment for adaptive

medical image compression. Three design strategies have been proposed: direct implementation of pseudo-code with a sequential and pipelined description, and block random access memory (BRAM)-based method. Analysis for both software simulation and hardware implementation with different medical image modalities has been carried out and discussed. An evaluation of FRAT's capability on medical image de-noising is also addressed.

The structures of this paper are as follows. Discussions on the design methodology with an overview of the proposed systems applications, Xilinx AccelDSP [8] design flow and the proposed FRAT architecture are presented in Section 2. Experimental results, comparison and analysis for medical image de-noising, software simulation and hardware implementation are explained in Section 3. Finally, concluding remarks are given in Section 4.

II. DESIGN METHODOLOGY

A. Proposed systems applications

Figure 1 illustrates an overview of the proposed 3-D compression system including the transform, quantisation and entropy coding blocks with the pre-processing block. In each block, buffers have been used for storing intermediate results to be processed.

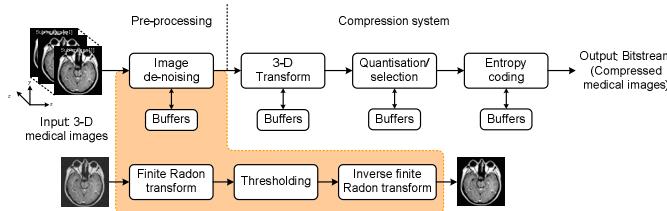


Fig. 1 Proposed system applications

This research aims at developing an adaptive compression system for medical images, where all of its blocks are reconfigurable. It is well known that noise on medical image resulting in low image quality, hence limited the diagnostic effectiveness. Therefore, noise reduction for medical images is significantly vital for the pre-processing stage before compression systems. This paper emphasises on FPGA-based architecture of FRAT for the image de-noising block in pre-processing stage.

B. Xilinx AccelDSP design flow

To ease the process of transforming a MATLAB [9] floating point design into a hardware module, Xilinx introduced the Xilinx AccelDSP software for rapid prototyping of an algorithm in MATLAB into hardware. The main feature of the Xilinx AccelDSP can be summarised as follows:

- A synthesisable RTL design can be obtained from the floating point M-code;
- A set of test bench can be automatically generated; and
- Capability to invoke HDL simulation, synthesis and implementation tools.

There are two main parts in M-code: a script and function file [8]. The script files works to create stimuli, feeds the stimuli to the function in a streaming loop and verifies the output from the function. Moreover, the script file also serves as a source file for future test bench auto generation.

Furthermore, the function file comprises the actual function to be translated into HDL, and it is written as an ordinary MATLAB function with an interface of input and output variables. The Xilinx AccelDSP verifies the generated module in each step to be as true as the previous one, or to be subjectively acceptable with a minor difference during the conversion from floating point design to fixed point [7], [8].

C. Proposed FRAT architecture

Figure 2 shows the architecture for the FRAT, and it is obtained based on the pseudo-code [1] for hardware implementation. To exploit the hardware resources available, the operations of the various counters used to track the addresses of the output vectors are parallelised and pipelined (by changing rollover conditions and count limits suitably).

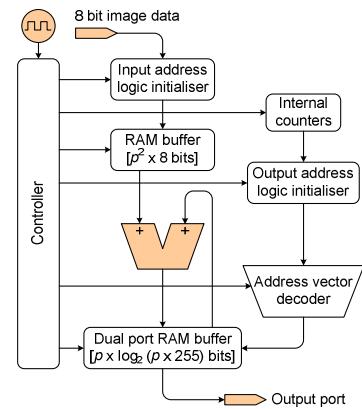


Fig. 2 FRAT architecture based on the pseudo-code

The number of counters required remains the same, only the triggering conditions, order and reset logic are modified suitably. It must be highlighted that whilst the algorithm is still serial and cycles through $p \cdot (p+1)$ iterations, the number of steps in the algorithm have been reduced, thereby improving latency. The architecture has serial inputs/outputs (I/Os) and a serial core. The total latency of the core is $O(p^2(p+1))$. The input section consists of a one-dimensional (1-D) random access memory (RAM) of width eight-bits and a depth of p^2 .

Although each input image block is a square tile of side p , buffering it in a 1-D RAM reduces the computational complexity of the control logic associated with data access. This is because, a two-dimensional (2-D) RAM is implemented on FPGA as a number of 1-D RAMs and uses additional multiplexing logic to dereference the address locations.

The FRAT operation requires reading and writing from the same memory location within a single clock pulse. This is

compactly and effectively implemented using a dual ported RAM at the output section instead of an array based buffer. The output buffer is a 1-D dual port RAM of width $\log_2(p \cdot 255)$ and depth p . Only a single FRAT vector is buffered and the final values are written to the output port in serial fashion at the end of each iteration. At the end of $(p+1)$ iterations, the entire image block is transformed to the FRAT domain.

Based on the FRAT architecture, three design strategies have been proposed as shown Figure 3 (a)–(c), with ‘R’, ‘E’ and ‘W’ refer to ‘Read’, ‘Enable’ and ‘Write’ processes, respectively.

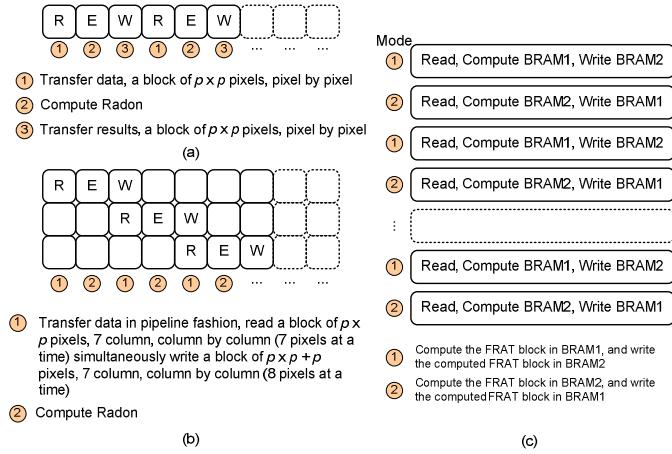


Fig. 3 Implementation strategies (a) Sequential (b) Pipelined (c) BRAM-based method.

III. RESULTS AND ANALYSIS

Three types of images have been used for software simulation and hardware implementation: medical resonance imaging (MRI) scan of human brain (940×940), chest body computerised tomography (CT) (128×128), and positron emission tomography (PET) scan of normal human brain (109×109).

A. Medical image de-noising

TABLE I
QUANTITATIVE RESULTS WITH GAUSSIAN NOISE FOR MRI IMAGE

Variances	Noisy (dB)	De-noising (dB)		
		Block sizes (p)		
		7	17	31
0.01	31.15	43.60	39.51	36.48
0.02	30.63	41.68	37.75	34.67
0.04	30.30	39.34	35.47	32.38
0.08	30.06	36.98	32.95	31.14
0.16	29.91	34.48	30.44	30.29

To analyse the effectiveness of the FRAT in medical image de-noising, a Gaussian noise with mean (μ) zero and various variances (σ) has been added to the experimental images. By utilising FRAT in medical image noise reduction, results obtained shown promising achievement. The de-noising

results achieved reveal that the FRAT implementation is effective to reduce Gaussian noise.

Table I shows quantitative results for MRI images, whilst Figure 4 (a)–(c) present a significant achievement of 13.25% Gaussian noisy de-noising for the MRI image using the FRAT.

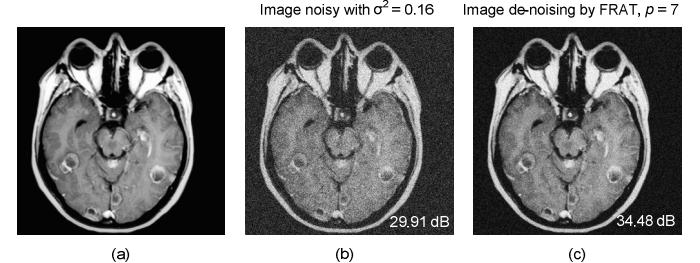


Fig. 4 Gaussian noise reduction experimental results on MRI image (a) Original image (b) Noisy image (c) De-noising image

B. Software simulation

Figure 5 (a)–(h) show the FRAT domain visualisation of MRI and PET images. The averaging impact of the FRAT on the image blockiness in the transform domain can be observed as p increases.

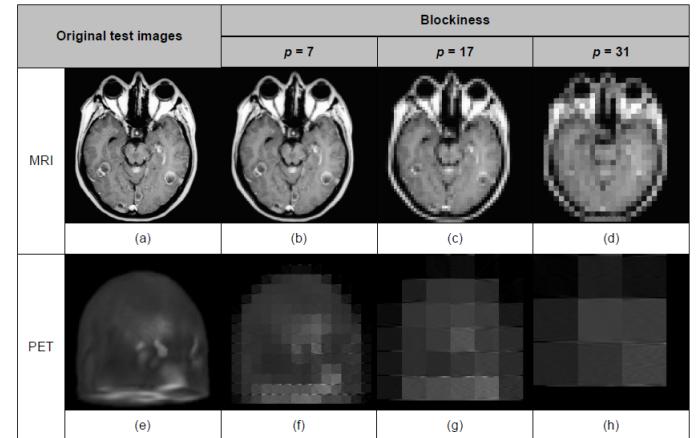


Fig. 5 Original and blockiness images.

It is worth noting that the filtered back projection (FBP) is a mathematically perfect inversion for the FRAT, and the peak signal to noise ratio (PSNR) depends only on the accuracy required [1]. The truncation or rounding step that follows the FRAT, determines the PSNR values.

As it is usually used as a sub-block in other transforms such as FRIT and curvelets, and it is followed by a wavelet stage in these transforms, the rounding or truncation process can easily be incorporated along with the wavelet block with no extra computational effort by suitably modifying the wavelet coefficients.

However, to illustrate the effect of bit-width limitations on the PSNR, Figure 6 shows the relationship of the PSNR values for the reconstructed medical images with various block sizes (p).

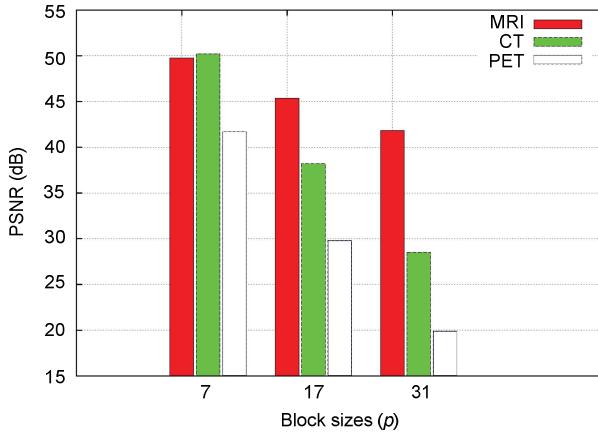


Fig. 6 Analysis of PSNR and different block sizes (p)

Results obtained exhibit that the PSNR of the reconstructed image drops by 7.93, 21.70 and 21.80 dB for MRI, CT and PET, respectively when the block size increases from $p = 7$ to 31. This is because as p increases, the rounding error becomes more significant. Using a divider with greater precision can reduce the rounding error.

C. Hardware implementation

For all three cases of hardware implementation: sequential, pipelined and BRAM-based method, pseudo-codes have been implemented in MATLAB and the Xilinx AccelDSP has been used for architecture and synthesis exploration.

TABLE II
COMPARISON OF PROPOSED ARCHITECTURES FOR THE CASE OF $P = 7$.

Type	Platform	Refs.	Max. freq. (MHz)	Through-put (MSPS)	Area (Slices)
Sequential	Virtex-II	[1]	79.97	37.32	215
		[4]	100.13	9.87	159
		[5]: A1	112.87	11.13	198
		[5]: A2	67.30	6.64	131
	Virtex-E	[1]	94.46	45.01	245
		[6]	69.00	6.90	345
	Virtex-5	Prop. LR	174.30	0.12	669
		Prop. LU	127.80	8.52	2,704
Pipelined	Virtex-5	Prop. LR	161.40	13.31	2,044
		Prop. LU	103.50	48.30	5,286
BRAM-based	Virtex-5	Prop.	188.90	6.30	637

Note: Refs.: References, Max. Freq.: Maximum frequency, A1: Architecture 1, A2: Architecture 2, Prop.: Proposed, LR: Loops rolled, LU: Loops unrolled

The designs have been implemented on Virtex-5 (XC5VSX50T) FPGA devices. As the prime aim of this paper is to examine the best hardware implementation applied for medical image de-noising, results for both medical image de-noising as well as the software simulation justify the hardware implementation with $p = 7$. Comparison of performance

metrics for the proposed FRAT architectures with existing work is presented in Table II.

Results achieved for the hardware implementation demonstrate various trade-offs with sequential and pipelined descriptions yielding better achievement for maximum frequency and throughput, respectively. Moreover, BRAM-based method also reveals less area occupied and better maximum frequency.

A detail comparison for both hardware implementation and software simulation with test medical images has been carried out. As shown in Table III, software simulation achieved better PSNR over hardware implementation with the percentage different 12.92%, 21.47% and 33.09% for $p = 7$, 17 and 31, respectively. This is due to the use of floating point in MATLAB, which yields better PSNR values compared with fixed point model in the hardware implementation.

TABLE III
COMPARISON OF PSNR FOR CT IMAGES

Experiments	PSNR (dB)		
	7	17	31
Hardware implementation	46.30	38.13	30.30
Software simulation	53.71	48.56	45.29

IV. CONCLUSIONS

In conclusion, an FPGA-based architecture with three different design strategies has been proposed and an analysis with various medical imaging modalities has been conducted. Image de-noising implementation using FRAT exhibits a significant achievement to reduce Gaussian noise in medical images. An evaluation of the implementation results indicates promising trade-offs achievement in terms of maximum frequency, throughput and area.

REFERENCES

- [1] S. Chandrasekaran, A. Amira, S. Minghua, and A. Bermak, "An efficient VLSI architecture and FPGA implementation of the finite ridgelet transform," *J. Real-Time Image Process.*, vol. 3, pp. 183–193, 2008.
- [2] A. Mayer and H. –P. Meinzer, "High performance medical image processing in client/server-environments," *Comput. Meth. Prog. Biomed.*, vol. 58(3), pp. 207–217, 1999.
- [3] J. Wisinger and R. Mahapatra, "FPGA based image processing with the curvelet transform," Texas A & M University, TR-CS-2003-01-0 Tech. Rep., 2003.
- [4] C. A. Rahman and W. Badawy, "Architectures the finite Radon transform," *IEE Electronic Letters*, vol. 40(15), pp. 931–932, 2004.
- [5] I. S. Uzun and A. Amira, "Design and FPGA implementation of finite ridgelet transform," in *Proc. ISCAS'05*, 2005, pp. 5826–5829.
- [6] S. Chandrasekaran and A. Amira, "High speed/low power architectures for the finite Radon transform," in *Proc. FPL '05*, 2005, pp. 450–455.
- [7] G. Yu, T. Vladimirova, X. Wu, and M. Sweeting, "A new high-level reconfigurable lossless image compression system for space applications," in *Proc. AHS'08*, 2008, pp. 183–190.
- [8] (2010) The Xilinx website. [Online]. Available: http://www.xilinx.com/AccelDSP_Synthesis_Tool_User_Guide, Xilinx, 2009.
- [9] (2010) The Mathworks website. [Online]. Available: <http://www.mathworks.com>
- [10] F. Matus and J. Flusser, "Image representation via a finite radon transform," *IEEE Trans. on Pattern Analysis and Mach. Intell.*, vol. 15, pp. 996–1006, 1993.