MASK DESIGN, FABRICATION AND TEST NMOS TRANSISTOR

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JUDUL: **MASK DESIGN, FABRICATION AND TEST NMOS TRANSISTOR**

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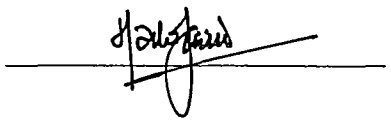
Signature : 

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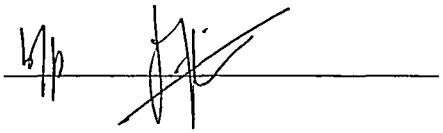
Signature : 

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This thesis is submitted as partial fulfillment of the requirements for the award of the Master Degree of Electrical Engineering

Faculty of Electrical and Electronic Engineering
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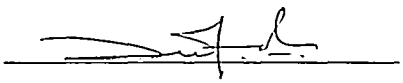
Signature : 

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For My Mother Iswati Binti Khamis,

My Father Sahdan Bin Saikon,

And My Fiancé Azrini Binti Idris

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ABSTRACT

Dalam proses fabrikasi MOSFET, satu set topeng digunakan bagi tujuan menutup atau membuka sesuatu kawasan pada *silicon wafer*. Set topeng yang digunakan dalam fabrikasi piawai adalah sangat tinggi kosnya dan tidak praktikal untuk tujuan pendidikan. Satu set topeng yang ekonomik adalah penyelesaiannya dengan menggunakan filem *transparency* yang mempunyai panjang saluran daripada 250um hingga maksimum 20um telah dihasilkan. Sebanyak 4 empat topeng telah direkabentuk dalam perisian AutoCAD 2002 *drawing tools* dan telah dicetak ke atas filem *transparency*. Kaedah *contact printing* digunakan untuk memindahkan bentangan topeng ke atas *silicon wafer* 4 inci menggunakan teknik *standard photolithography* untuk memastikan keseragaman lapisan. Proses fabrikasi MOSFET dilakukan selepas kesemua parameter dioptimumkan.Selepas MOSFET selesai dihasilkan, *probe station* dan MOSFET *characterization analyzer software* digunakan untuk menganalisa ciri-ciri MOSFET. Set topeng yang digunakan dalam projek ini adalah praktikal untuk tujuan pendidikan dan MOSFET yang dihasilkan juga berfungsi seperti yang dikehendaki.

ABSTRACT

In MOSFET fabrication, mask set was used to define certain region on a silicon wafer. The mask sets that used in standard fabrication are very expensive and not practical for education purposes. An economical solution of masks using transparency films with various channel length from 250um to 20 um was produced. Four mask set of MOSFET were designed using AutoCAD 2002 drawing tools and then printed on the transparency film. Contact printing method was utilized to transfer the mask layouts on a 4-inch silicon wafer using standard photolithography technique to check the line uniformity. The MOSFET fabrication process was done after optimizing the parameters. Probe station and MOSFET characterization analyzer software was used to characterize the fabricated MOSFET. The mask used in this project was practical for education purpose and the MOSFET was successfully fabricated.

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GLOSSARY OF ABBREVIATIONS

V_{GS}	-	Voltage gate to source (V)
V_{DS}	-	Voltage drain to source (V)
V_{TH}	-	Threshold Voltage (V)
i_D	-	Drain current (mA)
IV	-	Current (mV) versus Voltage (V)
C_{ox}	-	oxide capacitance (F)
Si	-	Silicon
IC	-	Integrated Circuit
CVD	-	Chemical Vapor Deposition
R_s	-	Sheet Resistance (Ohm)
t_{ox}	-	Oxide thickness (um)

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CHAPTER I

INTRODUCTION

1.1 Background

The microelectronic history start in December 1947 when three scientists Bardeen, Walter Brattain and William Shockley from Bell Laboratory of United State, invented the first semiconductor device, called transistor [1]. It was the component that gave birth to the solid state electronic era with all its famous progeny. Since that year, the semiconductor industry has seen the continuous development of new and improved processes.

The improvement of the process has in turn led to the more highly-integrated and reliable circuits that have fuelled the continuing electronics revolution [2]. This improvement falls into two broad categories; process and structure. Process improvements are those that allow the fabrication of the device and circuits in smaller dimension, higher density, quantity and reliability. The structure improvements are the

invention of new device designs allowing greater circuit performance, power control and reliability.

In the process development, semiconductor is the materials that are used to fabricate ICs. Semiconductors are useful in electronics because their electronic properties can be greatly altered in a controllable way by adding small amounts of impurities. These impurities, called dopants, add extra electrons or holes. A semiconductor with extra electrons is called an n-type semiconductor, while a semiconductor with extra holes is called a p-type semiconductor.

In IC fabrications, there are two type of semiconductor used, which are Silicon (Si) and Gallium (GaAs). The two main classes of transistor types are bi–polar and uni-polar. Bi-polar devices are normally used in high speed semiconductor and low noise application. The main type of uni-polar is MOSFET (Metal Oxide Semiconductor Field Effect Transistor).

MOSFET device is a digital device and it can either be n-channel (NMOS transistor) or p-channel (PMOS transistor). This project will study the NMOS transistor only and will not be considering the PMOS transistor. Figure 1 below will show the common symbol for NMOS transistor.

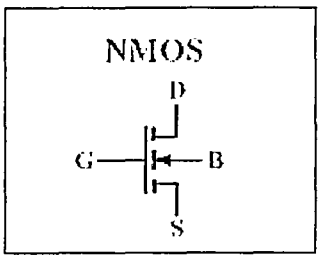

Figure 1.1: Common symbol of NMOS transistor

1.2 Problem Statement

In IC fabrication, mask sets are needed to transfer the designed pattern onto a wafer. The mask set produced by company in the market is very expensive and not practical for education purpose. In fabrication process, the most important thing is to get the correct recipe to fabricate transistor. This correct recipe will determine the performance of NMOS transistor that will give the best characteristic. This project was done experimentally to design a low cost mask set and to fabricate NMOS transistor using optimized parameters that would give the best characteristic.

1.3 Project Objective

There were four main objectives to be achieved in this project. The objectives are as follows;

i. To design a low cost mask set using transparency films.

ii. Optimize and characterize the process parameters and process flow of the transistor.

iii. Fabricate NMOS transistor using spin-on dopant technique.

iv. Test NMOS transistor to get the characteristics of the device.

1.4 Scopes

This project will be done by limiting the scopes into five. These scopes of the project are as follows;

i. To establish process module, process parameter, process flow and process run card.
ii. To design and produce a set of mask for MOSFET fabrication process.
iii. To optimize and characterize process module.
iv. To integrate the process module and start fabricates process of NMOS transistor.
v. To analyze and test the product.

CHAPTER II

LITERATURE REVIEW

2.1 Background

Before doing this project, the first thing that was done was studying the characteristic of NMOS transistor. This chapter will explain the important part that must be known before implementing this project.

2.2 The Geometric Parameter of NMOS

A 3-D structure in Figure 2.1 below illustrate the component of NMOS transistor source (S), drain (D) and gate (G). The gate of the NMOS transistor is usually made of polysilicon, which is formed from polycrystalline silicon and relatively good conductance. The gate is insulated by the layer of the silicon dioxide, SiO_2, from a

conducting channel existing between two diffusion areas which form the drain and the source of the transistor.

Diffusion areas (source and drain) are created inside a substrate (also known in some technological context as the well) of the opposite type, e.g. n+ diffusion inside the p substrate, where 'n+' indicates silicon highly doped with donors.

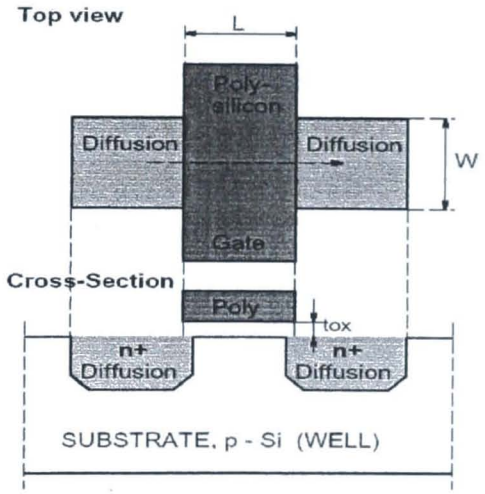

Figure 2.1: Basic geometric parameter of NMOS transistor

From the top and cross-sectional views of the MOS transistor presented in Figure 2.1 we found that three basic geometrical parameters of the transistor are the following;

i. L and W – the length and width of the conducting channel between the source and drain.

ii. t_{ox} — thickness of the oxide layer between the gate and the diffusion/substrate areas.