CORE
Metadata, citation and similar papers at core.ac.uk
Provided by UTHM Institutional Repository

SIMULATION, FABRICATION AND CHARACTERIZATION OF PMOS TRANSISTOR DEVICE

SITI IDZURA BINTI YUSUF

KOLEJ UNIVERSITI TEKNOLOGI TUN HUSSEIN ONN

PERPUSTAKAAN UTHM
30000001883609

KOLEJ UNIVERSITI TEKNOLOGI TUN HUSSEIN ONN

PENGESAHAN STATUS LAPORAN PROJEK SARJANA

TITLE: SIMULATION, FABRICATION AND CHARACTERIZATION OF PMOS TRANSISTOR DEVICE

SESI PENGAJIAN : 2006/2007

Saya **SITI IDZURA BINTI YUSUF** mengaku membenarkan Laporan Projek Sarjana ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Laporan Projek Sarjana adalah hakmilik Kolej Universiti Teknologi Tun Hussein Onn.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan tesis ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. ** Sila tandakan (√)

☐	SULIT	(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)
☐	TERHAD	(Mengandungi maklumat TERHAD yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan
√	TIDAK TERHAD	

Disahkan oleh

(TANDATANGAN PENULIS)

(TANDATANGAN PENYELIA)

Alamat Tetap:

PEJABAT LADANG FELDA LEPAR
UTARA 13,
WAKIL POS LEPAR UTARA 1,
84300 BANDAR PUSAT JENGKA,
PAHANG

PROF. Dr. HASHIM BIN SAIM
Nama Penyelia

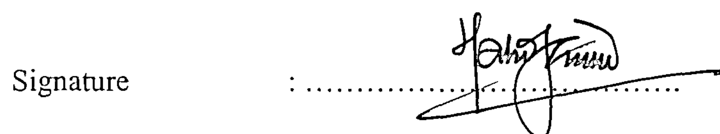
Tarikh: 21 DISEMBER 2006

Tarikh: 21 DISEMBER 2006

CATATAN:

** Jika Laporan Projek Sarjana ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa/organisasi berkenaan dengan menyatakan sekali sebab dan tempoh laporan ini perlu di kelaskan sebagai SULIT atau TERHAD.

"I hereby declare that I have read this thesis and in my opinion this thesis in terms of content and quality requirement fulfills the purpose for the award of the Master of Electrical Engineering"

Signature : 

Name of Supervisor : PROFESSOR Dr. HASHIM BIN SAIM

Date : 21 DECEMBER 2006

SIMULATION, FABRICATION AND CHARACTERIZATION OF PMOS TRANSISTOR DEVICE

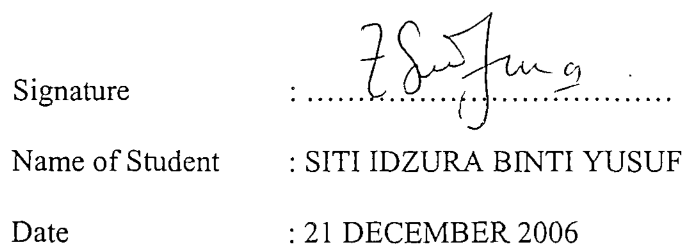
SITI IDZURA BINTI YUSUF

This thesis is submitted in partial to fulfillment of the requirement for the Master of Electrical Engineering

Faculty of Electrical And Electronic Engineering
Tun Hussien Onn University College of Technology

DECEMBER, 2006

" I hereby declare that the work in this thesis in my own except for quotations and summaries which have been duly acknowledged"



Signature : ....

Name of Student : SITI IDZURA BINTI YUSUF

Date : 21 DECEMBER 2006

Khas buat tunang Muhammad Syukur Bin Ismail

Setiap kejayaanku milik kita bersama

ACKNOWLEDGEMENTS

I would like to express my deep gratitude especially to my project supervisor, Prof. Dr. Hashim B. Saim for the oppurtunity and encouragement given throughout the entire process of my project. Iam deeply indebted for his advices and by providing the laboratory facility to me along the way.

Beside that, my special thanks to my father Yusuf B Hamdan, my mother Zainon Bt Kasran and my siblings who have always behind me to support during critical time. You are always in my heart.

Not forgeting, to all my Sarjana MEE members who have helped me along the way. Thank you for the suggestions and encouragements.

ABSTRACT

In a low supply voltage CMOS technology, it is desirable to scale threshold voltage and gate length for improving circuit performance. Therefore, a project has been carried out inside KUiTTHO's microelectronic cleanroom to produce a method that has better low power/low voltage current concentrate on p-channel (PMOS). An experiment was also done to determine the right parameter value to be used for fabrication process such as oxidation process thickness rate, sheet resistance and metal thickness. From the parameter value obtained, 0.3 mm and 0.5 mm PMOS transistor had been successfully produced. Fabrication simulation was performed to produce a 0.1μm and 0.3μm PMOS transistor by using the ISE-TCAD software. The trade off between threshold voltage (V_{TH}), gate length (L_G) and thin oxide thickness (t_{ox}) are discussed to determine the characteristics of the transistors. It shows that for 0.3mm (t_{ox} = 860Å) PMOS transistor the value of V_{TH} =-3.33V and 0.5 mm (t_{ox} = 910Å), V_{TH} value =-4.3V. From the simulation result show for 0.1μm (t_{ox} = 200Å), V_{TH} = -0.314V and for 0.5μm (400Å) V_{TH} = -0.634V. The result shows that, with decreasing gate length and oxide thickness will produce lower value of threshold voltage. Minimum value of threshold voltage can result in a better performance of transistor. Another parameter must be taken into consideration such as leakage current, resistivity and conductivity to get a better design of PMOS transistor in future research.

ABSTRAK

Untuk menghasilkan sumber voltan yang rendah dalam CMOS teknologi, penskalaan voltan ambang, V_{TH} dan lebar gate, L_G untuk menghasilkan litar yang berkeupayaan tinggi ,merupakan isue yang sangat penting. Oleh itu, projek ini telah dijalankan di dalam makmal mikroelektronik bilik bersih KUiTTHO untuk menghasilkan resepi bagi PMOS transistor dengan saiz yang minimum dan berprestasi tinggi. Eksperimen juga telah dijalankan untuk menentukan nilai parameter yang sesuai untuk digunakan dalam proses fabrikasi iaitu proses pengoksidaan untuk mencari kadar ketebalan oksida get, rintangan keping dan ketebalan metal. Daripada nilai parameter yang diperolehi, 0.3mm dan 0.5mm PMOS transistor telah berjaya dihasilkan. Fabrikasi secara simulasi juga telah dijalankan untuk menghasilkan 0.1μm and 0.3μm PMOS transistor dengan menggunakan perisian ISE-TCAD. Perubahan antara voltan ambang (V_{TH}), lebar gate (L_G) dan ketebalan lapisan oksida (t_{ox}) telah dibincangkan untuk menetukan ciri-ciri bagi PMOS transistor tersebut. Hasil dapat daripada fabrikasi sebenar menunjukkan untuk transistor bersaiz 0.3mm (t_{ox}= 860Å) PMOS transistor V_{TH} = -3.33V dan 0.5mm(t_{ox} = 910 Å), nilai V_{TH} = -4.3V. Dapatan hasil simulasi menunjukkan untuk 0.1μm (t_{ox} = 200Å), V_{TH} = -0.314V dan 0.5μm (t_{ox} = 400Å), nilai V_{TH} = -0.634V. Daripada keputusan yang diperolehi menunjukkan bahawa dengan kelebaran get yang minima dan ketebalan oksida yang lebih nipis akan menghasilkan PMOS transistor dengan nilai voltan ambang yang lebih rendah. Nilai voltan ambang yang lebih rendah akan mempengaruhi keupayaan transistor. Parameter-parameter lain perlu diambil kira seperti arus bocor, kerintangan dan kekonduksian untuk menghasilkan PMOS transistor yang berprestasi tinggi untuk kajian akan datang.

TABLE OF CONTENT

CHAPTER	TITLE		PAGE
	DECLARATION		ii
	DEDICATION		iii
	ACKNOWLEDGEMENT		iv
	ABSTRACT		v
	ABSTRAK		vi
	TABLE OF CONTENT		vii
	LIST OF FIGURES		xi
	LIST OF TABLES		xiii
	LIST OF SYMBOLS / ABBREVIATION		xiv
CHAPTER I	INTRODUCTION		
	1.1	General	1
	1.2	Problem Statement	2
	1.3	Project Objectives	3
	1.4	Project Scope	3
	1.5	Project Flow	4

CHAPTER II LITERATURE REVIEW

2.1	Introduction	5
2.2	The MOS Transistor	5
2.3	P-Channel MOSFET (PMOS)	6
	2.3.1 Structure of P-Channel MOS (PMOS) Transistor	6
2.4	Qualitatitive I-V Behavior of PMOS Transistor	7
2.5	Characteristics of the PMOS Transistor	9
2.6	Relationship between Gate Length, Threshold Voltage and Gate Oxide Thickness	13
	2.6.1 Gate Length	13
	2.6.2 Gate Oxide Thickness	14
	2.6.3 Threshold Voltage	15
2.7	Fabrication Process	15
	2.7.1 Cleanroom Cleanliness	16
	2.7.2 Cleaning Process	17
	2.7.3 Oxidation Process	18
	2.7.3.1 Horizontal Tube Furnace	19
	2.7.3.2 Dry Oxygen	20
	2.7.3.3 Water Vapor Source	21
	2.7.4 Diffusion	22
	2.7.5 Photolithography	23
	2.7.6 Metallization	24
2.8	Simulation Fabrication Process	25
	2.8.1 Strongly Varying Length Scale	26
	2.8.2 High Performance in Key Operations	27
	2.8.3 Stability	27
2.9	Previous Research	28

CHAPTER III METHODOLOGY

3.1	Introduction	30
3.2	Mask Design and Creation	31
3.3	Fabrication Process Module	33
	3.3.1 Drain and source regions	33
	3.3.2 Gate Oxide Grown	35
	3.3.3 Define Contact Hole	36
	3.3.4 Aluminium Film Deposited	37
3.4	PMOS Characteristics and Performance	38
3.5	Simulation Fabrication Process	38

CHAPTER IV RESULTS AND DISCUSSION

4.1	Introduction	40
4.2	Recipes of PMOSFET Devices	40
	4.2.1 Process Parameter	41
	4.2.1.1 Oxidation Process	41
	4.2.1.2 Diffusion	45
	4.2.1.2.1 Sheet Resistance	45
	4.2.1.3 Metallization Sheet Resistance	48
	4.2.2 Fabrication Process	51
4.3	PMOS Characteristics Analysis	57
	4.3.1 Simulation Fabrication Result	58
	4.3.1.1 Conclusion	64
	4.3.2 Real Fabrication Result	65
	4.3.3 Conclusion	71
4.4	PMOS Characteristics and Performance	72

CHAPTER V CONCLUSION AND RECOMMENDATION

5.1 Introduction 74

5.2 Conclusion 74

5.3 Problems and Recommendation 77

5.3.1 Uniformity in Diffusion Process 77

5.3.2 Measurement of V_{TH} Value 77

5.3.3 Alignment 77

5.4 Suggestion for Future Research 78

REFERENCES 79

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
1.1	The project flowchart	4
2.1	An internal structure of p-channel MOS transistor	7
2.2	Cross section of an enhancement-mode PMOS transistor	8
2.3(a)	$V_{SG} \leq V_{TH}$ – cut off region	10
2.3(b)	$V_{SG} \geq V_{TH}$ – linear region	10
2.3(c)	PMOS with channel just pinch off at the drain	11
2.3(d)	Pinch off for $V_{SD} \geq (V_{SG} + V_{TH}) \geq 0$	11
2.4	Class 100 yellow room for photolithography process	16
2.5(a)	Cleaning Process Section	18
2.5(b)	D.I water	18
2.6	Furnace Equipment	20
2.7	Bubler water vapor source	21
2.8(a)	Spin on-dopant Equipment	24
2.8(b)	Transfer Patern Equipment	24
2.9	Physical Vapor Deposition(PVD) Equipment	25
2.10	ISE TCAD product overview	27
3.1	PMOS transistor layout	31
3.2	Masking drawing steps in TurboCAD 2002	32
3.3	Modules of MOSFET PMOS fabrication process	33
3.4	Gate Oxide Grown	35

3.5	Define Contact Hole	36
3.6	Completion of PMOS transistor fabrication	37
4.1	Oxidation thickness versus time for wet oxidation	43
4.2	Oxidation thickness versus time for dry oxidation	44
4.3	Five Point of measurement	44
4.4(a)	Example of sheet resistance graph measured by four point probe for wafer A at point 1	47
4.4(b)	Example of sheet resistance graph measured by four point probe for wafer B (b) at point 1	47
4.5	Graph Aluminium thickness with different size of aluminium	50
4.6(a)	I_D-V_D characteristics of 0.1um PMOS, thin oxide 400Å	58
4.6(b)	Transfer charateristics of 0.1 μm PMOS, thin oxide 400Å	59
4.7(a)	I_D-V_D characteristics of 0.3um PMOS, thin oxide 400Å	60
4.7(b)	Transfer charateristics of 0.3 μm PMOS, thin oxide 400Å	60
4.8(a)	I_D-V_D characteristics of 0.1um PMOS, thin oxide 200Å	62
4.8(b)	Transfer charateristics of 0.1 μm PMOS, thin oxide 200Å	62
4.9(a)	I_D-V_D characteristics of 0.3um PMOS, thin oxide 200Å	63
4.9(b)	Transfer charateristics of 0.3 μm PMOS, thin oxide 200Å	64
4.10	I_D-V_D characteristics of 0.3 mm PMOS;V_D=-6V; thin oxide 910Å	66
4.11	I_D-V_D characteristics of 0.5 mm PMOS;V_D=-6V; thin oxide 910Å	67
4.12	I_D-V_D characteristics of 0.3 mm PMOS;V_D=-6V; thin oxide 860Å	69
4.13	I_D-V_D characteristics of 0.5 mm PMOS;V_D=-6V; thin oxide 860Å	69

LIST OF TABLES

NO. TABLE	TITLE	PAGE
2.1	Cleanroom cleanliness measurement	17
3.1	Modules of MOSFET (PMOSS) fabrication process	33
3.2	Equipment of device and process parameter	38
4.1(a)	Wet oxidation thickness of wafer 1	42
4.1(b)	Wet oxidation thickness of wafer 2	42
4.2	Oxidation thickness for dry oxidation	43
4.3	Sheet resistance value different wafer	46
4.4	Metal thickness with different size of aluminium	50
4.5	The recipes of PMOS transistor	51
4.6	Simulation fabrication result	65
4.7	Real fabrication result	70
4.8	Relationship between different gate oxide and gate length versus gate delay	73
4.9	Gate delay with load capacitance	73

LIST OF SYMBOLS / ABBREVATIONS

Å	symbol for 10^{-10}cm or 10^{-8}m
C	Capacitance
C_{ox}	Oxide capacitance per unit area
D	Diffusion coefficient
I	Current
I_D	Drain current
I_D-V_D	Drain Current versus Drain / source Voltage
k	Boltzmann's constant
L	Length
L_G	Gate Length
n	Electron density
n_i	Intrinsic carrier density
N	Doping density
N_a	Acceptor doping density
N_c	Effective density of states in the conduction band
N_d	Donor doping density
R	Resistance
R_s	Sheet Resistance
S_i	Silicon
t	Thickness
t_{ox}	Oxide thickness
T	Temperature
v	Velocity

V_D	Drain voltage
V_{DS}	Voltage gate to source
V_B	Body voltage
V_G	Gate voltage
V_{GS}	Voltage gate to source
V_{TH}	Threshold voltage
W	Width
x_d	Depletion layer width
xj	Junction depth
x_n	Depletion layer width in an n-type semiconductor
μ_p	Hole mobility

CHAPTER I

INTRODUCTION

1.1 General

The MOSFET circuit technology has dramatically changed over the last three decades. Starting with a ten-micron PMOS process with an aluminum gate and a single metallization layer around 1970, the technology has evolved into a tenth-micron self-aligned-gate CMOS process with up to five metallization levels. The transition from dopant diffusion to ion implantation, from thermal oxidation to oxide deposition, from a metal gate to a poly-silicon gate, from wet chemical etching to dry etching and more recently from aluminum (with 2% copper) wiring to copper wiring has provided vastly superior analog and digital CMOS circuits. The choice and centering of target transistor parameters- modeling (such as threshold voltage, gate length, gate oxide thickness, etc) for high speed low-power/ low voltage CMOS technologies is a current concern (Chang, 2000)[7]. If proper CMOS scaling rules are utilized, high speed CMOS technologies can be achieved even in conjunction with reduced supply voltage requirements. The dynamic power dissipation in CMOS inverter circuits is given by

$$P = f.\, C_L.\, V^2_D \tag{1.1}$$

where f is operating frequency, C_L is the loading capacitance, and V_D is the supply voltage. Clearly, reducing the supply voltage is the simplest approach in reducing the dynamic power consumption. The time delay, τ_D in a CMOS gate is approximately given by

$$\tau_D \approx \frac{C_L V_D}{I_D} \infty \frac{C_L L_G t_{ox} V_D}{(V_D - V_{TH})^2} \tag{1.2}$$

where L_G is the transistor gate length, t_{ox} is the gate oxide thickness, I_D drain current and V_{TH} is the MOS transistor threshold voltage. Equation 1.2 demonstrates the need for reducing the gate oxide thickness, the gate length, and the transistor threshold voltage in order to preserve the high-speed in a reduced voltage supply technology.

1.2 Problem Statement

Since the semiconductor industry growth rapidly, competition among companies to fulfill market demands has become increasingly intense. Therefore, many data and parameters obtained from researches were not published and kept confidential. Hence, each fabrication laboratories have created their own technologies. KUiTTHO as an education institution is also making an effort to produce a MOSFET technology transistor with the equipment provided in the KUiTTHO's Microelectronic Cleanroom. Therefore, the purpose of this project was to build a first MOSFET technology transistor, which was aimed for better low power/low voltage current concentrate on p-channel (PMOS) transistors.

1.3 Project Objectives

The objectives of this project are:

1. To produce a recipe of MOSFET devices (PMOS transistor).
2. To determine the minimum mask design that can be fabricated in KUiTTHO's cleanroom to produce transistor with minimum gate length.
3. To determine transistor region operation which are very important in low-voltage and low-power application from the IV characteristics of PMOS transistor.
4. To determine the trade-off between threshold voltage (V_{TH}) and the minimum gate length (L_G) for optimizing the performance of PMOS transistors for low voltage/low power high-speed digital CMOS circuit.

1.4 Project Scope

1. The project was done with the process equipments in Microelctronic Cleanroom at KUiTTHO. The data that was obtained might be different with other clean-room. It depends on the equipment capability and the class of the cleanroom.
2. The project concentrated on PMOS transistor device, including the effect of threshold voltage(V_{TH}) thin oxide thickness (t_{ox}) and gate length (L_G) to I_D-V_D characteristics.
3. There were 4 steps that were taken in this project which were:
   i. Establishing process module, process parameters, process flow and process run card.
   ii. Optimizing and characterizing process module.

iii. Integrating the process module and starting the fabrication process of MOSFET (PMOS) device.

iv. Analyzing and testing product.

1.5 Project Flow

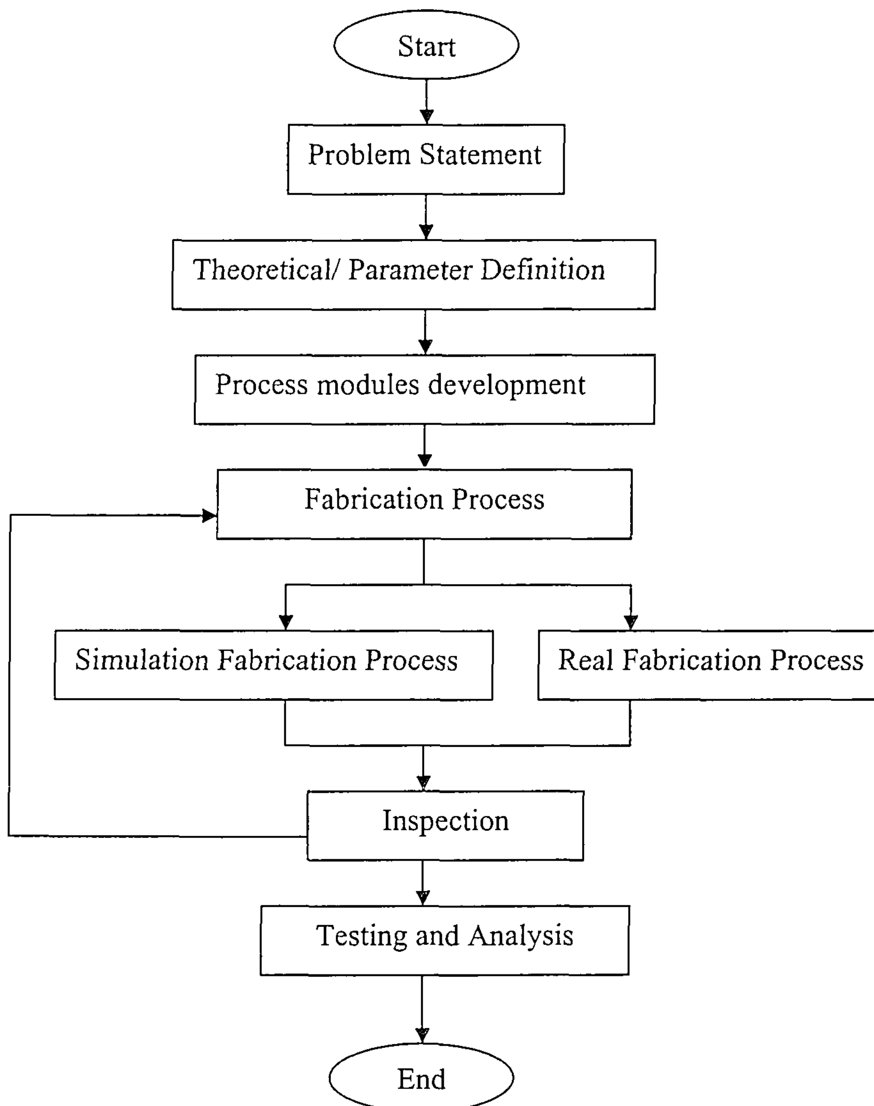


Figure1.1: The project flowchart

CHAPTER II

LITERATURE REVIEW

2.1 Introduction

This chapter will highlight on the understanding of transistor device mainly MOSFET (Metal Oxide Semiconductor Field Effect Transistor). This project focuses on the fabrication process of MOSFET devices. Prior to that, the characteristics and physical structure of PMOS transistor was studied.

2.2 The MOS Transistor

These devices are known as FET's (Field effect transistors), which consist of three regions; source, drain and gate. The resistance path between the drain and source is controlled by applying a voltage to the gate. This varies the depletion layer under the gate and thus reduces or increases the conductance path. The FET input impedance (unlike the BJT which is a few kΩ) is very high (~MΩ's) and as a result the gate current can be considered as zero.