Measurements of Magnetic Field Emission of Various Digital Circuit Layouts

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***Abstract*–Signal or power to ground traces on a printed circuit board (PCB) of digital products may act as an efficient loop antenna radiating magnetic field when the length is greater than the wavelength of the high frequency current. Employment of proper routing of the return current path, filtering and damping resistor is best practices in the design criteria to minimise sources of electromagnetic emission at PCB level. It is important to indicate that the use of guard traces, filtering at supply network of critical component and damping resistor on signal traces can be the options of emission reduction techniques on double sided assemblies as it will reduce the emission level. In this paper, three double sided test boards are developed to evaluate the impact of the aforementioned mitigation methods on near magnetic field emission. The magnetic field distributions over each layout are measured in order to reveal the profile of radiation to gain further understanding on the net current distribution on the traces of the digital circuit. It is seen that by proper design of return current path, the magnetic field is reduced by average of 16.5 dB.**

I. INTRODUCTION

The demand on smaller, faster and lower cost of electrical and electronic devices has increased the number of new creation of portable product incorporated with microcomputer application. Nowadays, the use of high speed and fast rise time of a digital clock is inevitable in order to fulfil the requirement of a faster microcomputer system. Consequently, complying with related electromagnetic compatibility (EMC) requirement becomes more challenging for an electrical and electronic manufacturer.

In general, a printed circuit board (PCB) carrying digital circuitry encompasses of active and passive components, clock generator, traces routing, wire connectors and heat sink. All of them have a possibility to be an unwanted antenna structure that generates unwanted electromagnetic energy. EMC design practices are important to be considered during the process of board layout for minimising the effectiveness of antenna structure exists on the PCB. Designing and fabrication of the PCB layout with good EMC design is usually handled by well-versed EMC engineer. The rule of thumb that often used is based on experience and only valid for some specific products and dependent on the number of PCB layers. In addition not all the EMC design rules recommended by other authors [1] – [4] can easily be followed when dealing with high-speed circuit design due to the space and circuit operation constraints. Thus, it is important to understand the principles of a source potential that causes the radiation as well effective method to minimise or eliminate the source.

Compliance with the EMC requirements at first time testing with few extra suppression components of electromagnetic interference (EMI) is a target for many manufacturers to save product development time and cost. It can be achieved if attention is given on the design of signal and power traces routing, proper return current path, physical location of critical components and input or output attaching cables.

According to [4], many EMI problems associated with high-speed circuit are due to improper design of the return current path that completes the current loop. This means the routing of trace carrying a high-speed clock signal or current spikes caused by switching logic, which has very broad ranges of spectral content cannot be mistreated. A lot of research efforts have been conducted to study the impacts of different mitigation technique on reduction of electromagnetic emission level. Some of the works are given in [5] – [7]. In [7], *See et al.* have shown that a poor layout of digital circuits on PCB would results high in emission level and fails to comply with EMC standard requirement. Testing for EMC compliance at an open area test site (OATS) or in a semi-anechoic chamber (SAC) generally only figures out the total performance of the product. The root cause of the problem needs to be identified for non-compliance product so that trouble-shooting process with proper mitigation techniques can be applied effectively. A near magnetic field probe is one of the options that can be used in prediction of near field radiation at PCB level.

In this paper, three different double-sided test boards are designed and fabricated to evaluate the impact of return current path of power and signal traces, filtering and damping resistor on the electromagnetic emission. The magnetic field distributions are measured by using a magnetic field probe with a spectrum analyzer in x, y and z axis over each layout in order to reveal the profile of net current distribution at the frequency of 25 MHz and distance 2.5 cm. In addition, a loop antenna is then used to measure far-field magnetic field for each test board at a distance of 1.2 m.

II. PCB LAYOUT CONFIGURATION

In an effort to investigate the near field distribution of a digital circuit with different EMI mitigation techniques, three different PCB layouts as shown in Fig. 1 to Fig. 3 are designed, fabricated and tested similar to the schematic circuit as in [7]. Double-sided FR4 board with relative permittivity 4.7 and thickness of 1.6mm has been employed in this study.

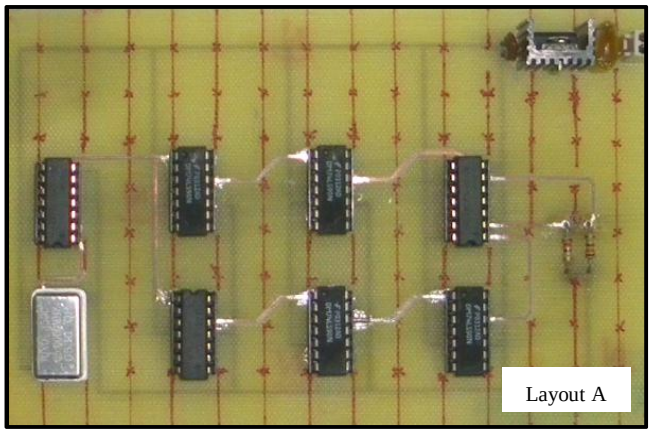


Fig. 1 Printed Circuit Board of Layout A

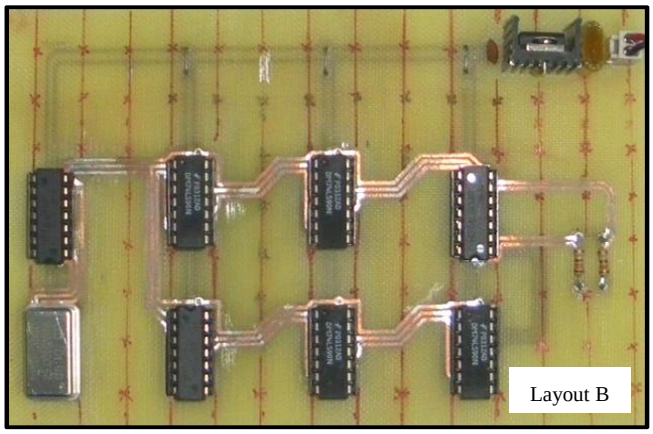


Fig. 2 Printed Circuit Board of Layout B

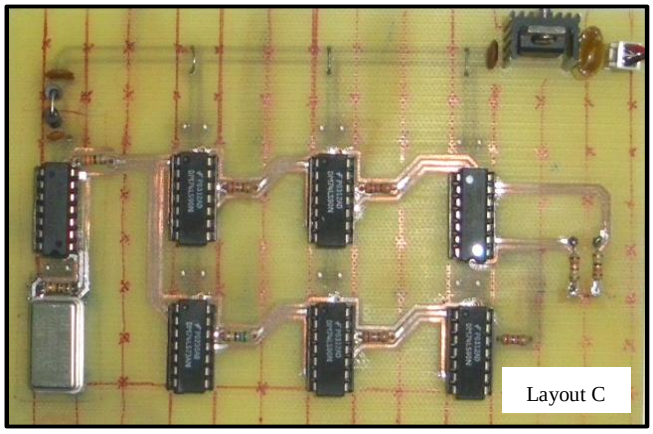


Fig. 3 Printed Circuit Board of Layout C

Fig. 1 shows the first PCB layout (Layout A) which is designed with large power to ground and signal to ground loops. In contrary, for the Layout B in Fig. 2, both power and ground return traces are routed in parallel to each other separated by small distance in order to reduce the loop area. Guard trace is applied around every clock signal trace to provide a low impedance alternative path home for high frequency current and minimize signal to ground loop areas. In the third layout as shown in Fig. 3, damping resistors are employed at each signal trace to improve its signal quality. Moreover, a filter consists of a ferrite and capacitors is included at power distribution system of 25 MHz oscillator and its driver in order to reduce high frequency logic gate's switching noise.

In this study, a 5 V regulated voltage is used as a supply voltage to operate the circuit which is driven by 25 MHz square wave clock signal. The 25 MHz clock signal is then divided by two and ten to drive other integrated circuits (ICs) and finally terminated with load resistor as shown in Fig. 4. Thus, the digital circuit is carrying various signals of frequencies 25 MHz, 12.2 MHz, 2.5 MHz, 1.25 MHz, 250 kHz and 125 kHz.

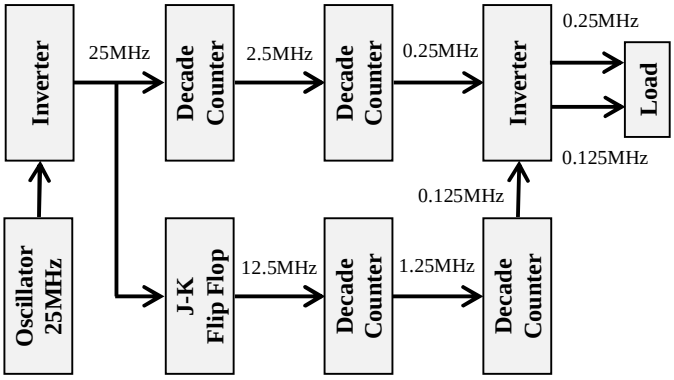


Fig. 4 Signal layout of digital circuit on PCB

III. Experimental Setup

The near magnetic field probe and the spectrum analyser has been utilised for magnetic field measurement at distance of 2.5 cm. Then the 0.6 m x 0.6 m loop antenna is used to measure the far magnetic field intensity at a distance of 1.2 m. Firstly, the magnetic field distribution is measured by placing the magnetic field probe at the distance of 2.5 cm above the PCB layouts as shown in Fig. 5. The readings of magnetic field are recorded at a different point of locations at mesh grid of size 1 cm x 1 cm. The positions of the magnetic field probe over the digital circuit under study are shown in Fig. 6 (a), (b) and (c) which represent the x, y, and z orientations respectively.

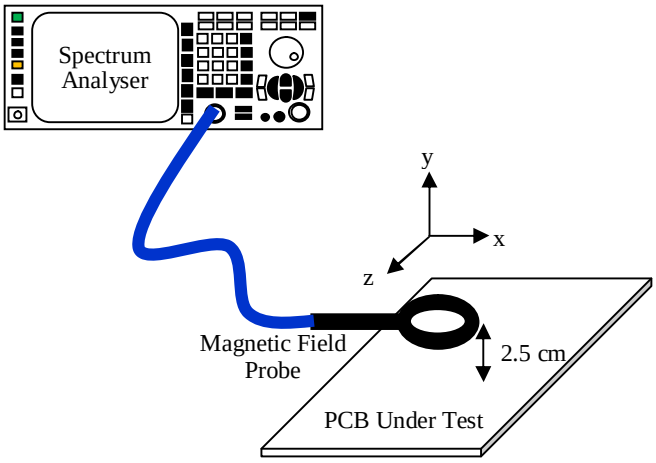
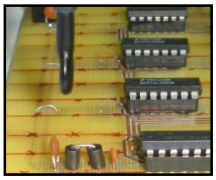
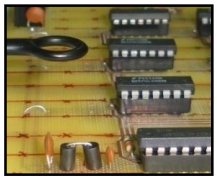


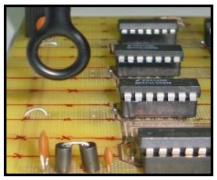
Fig. 5 Near magnetic field measurement setup at 2.5 cm



(a) Measurements of magnetic field radiation at x-axis (**H**x)



(b) Measurements of magnetic field radiation at y-axis (**H**y)



(c) Measurements of magnetic field radiation at z-axis (**H**z)

Fig. 6 Orientations of the near magnetic field probe

The total magnetic field distributions over each PCB layout are calculated by vector addition of **H**x, **H**y, and **H**z with the probe correction factor values which is available in [8]. The data are then plotted in a 2-D layout. Secondly, for the measurement of magnetic field strength at 1.2 m, an arrangement of the loop antenna, the spectrum analyser and the board under test are as shown in Fig. 7.

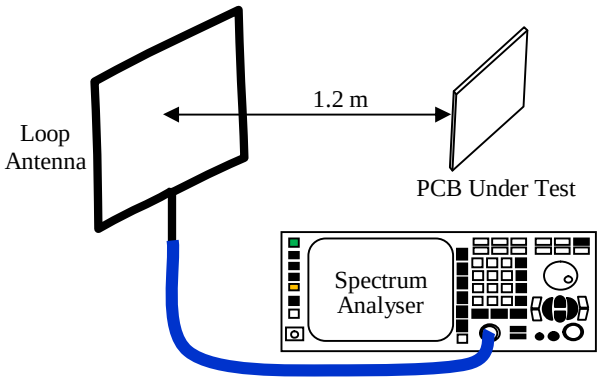


Fig. 7 Magnetic field measurement at 1.2 m

IV. RESULTS AND DISCUSSIONS

In this section, experimental results of magnetic field measurement at the distance of 2.5 cm and 1.2 m from the PCB under study for frequency 25 MHz are presented in two dimensional (2-D) views. The magnetic field distributions of the test boards in the aspect of different EMI mitigation techniques are presented and discussed. Fig. 8 – Fig. 10 show the results of radiation layout of magnetic field above 2.5 cm distance of PCB Layout A, B and C respectively.

Observation on Fig. 8 shows that Layout A generated higher magnetic field emission in comparison to Layout B and Layout C. This is due to large loop areas of power and signal traces of Layout A. Improvement in grounding design of Layout B by routing the power and ground traces in parallel and employment of guard traces placed in a close distance to signal traces in order to reduce loop areas, have reduced the source region of magnetic field radiation. Based on the 2-D contour plots in Fig.8 and Fig. 9, the peak level of magnetic field varies in a range of 120 dBuA/m to 160 dBuA/m for Layout A was somehow reduced to the range of 100 dBuA/m and 140 dBuA/m in Layout B. The average reduction is calculated to be 16.5 dB. The regions of the magnetic field radiation seem to be smaller as well.

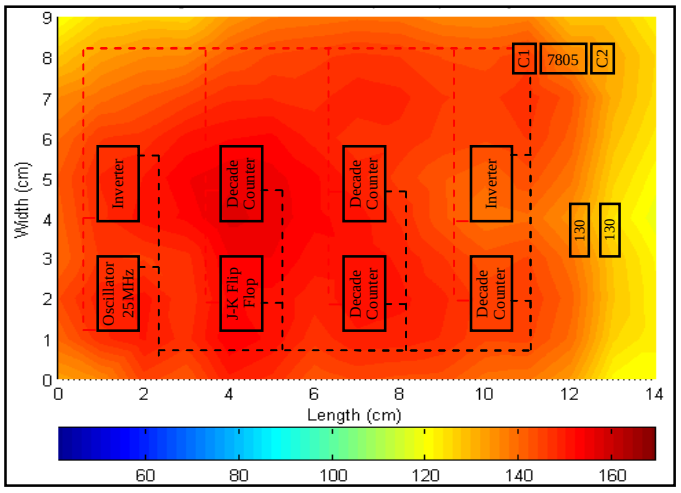


Fig. 8 Magnetic fields distribution of Layout A at 25 MHz

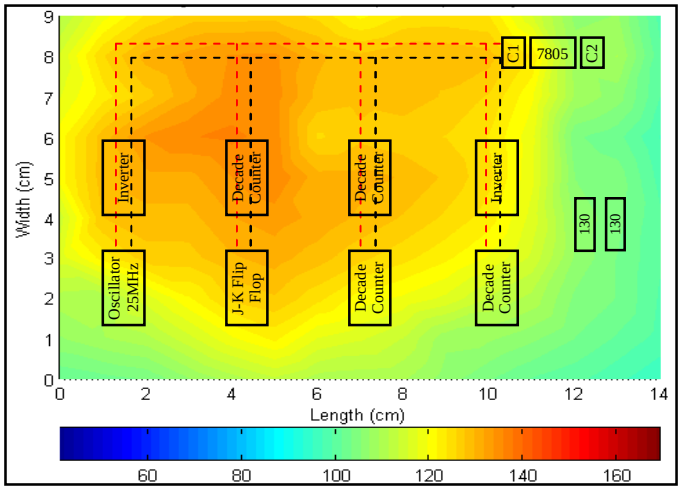


Fig. 9 Magnetic fields distribution of Layout B at 25 MHz

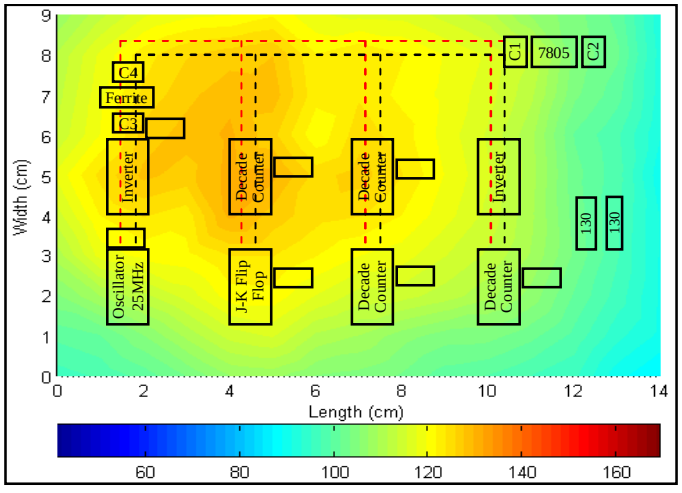
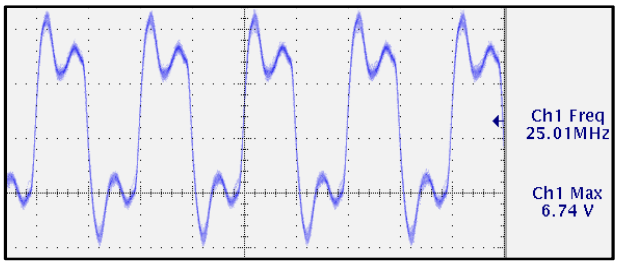


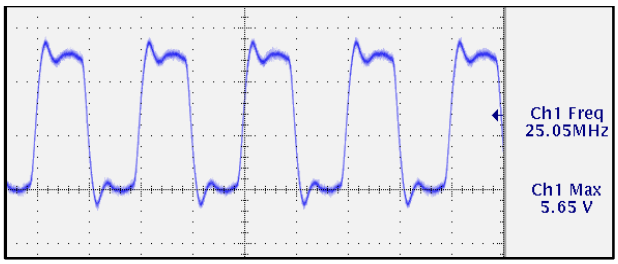
Fig. 10 Magnetic fields distribution of Layout C at 25 MHz

Thus, consideration of proper grounding technique in the early design stage will offer a cost effective means of resolving high EMI problem at PCB level. In Fig. 10, adding a filter at critical area like clock and its driver plus damping resistors at each signal trace have further reduced the peaks of magnetic field distribution to the range of 90 dBuA/m to 125 dBuA/m or an average of 5.08 dB. The employment of ferrite and capacitor at a critical component managed to block the switching logic noise from entering the power distribution network. This can be seen clearly by comparing in the top portion of Fig. 8 and Fig. 9. In circuit design, impedance matching plays an important role to minimise the effects of ringing and reflection. The employment of damping resistor has improved the quality of the signal as well as reducing on overshoot effect due to reflection on the clock signal that flows through signal trace as shown in Fig. 11.

The outcome of the magnetic field measurements at 1.2 m from the test boards are shown in Fig. 12. It can be observed that the magnetic field for Layout C is higher compared to Layout A and Layout B. This is probably due to the cumulative effect of the common- mode current on the PCB which is highest for Layout C.



(a)



(b)

Fig. 11 Clock signal (a) without and (b) with damping resistor

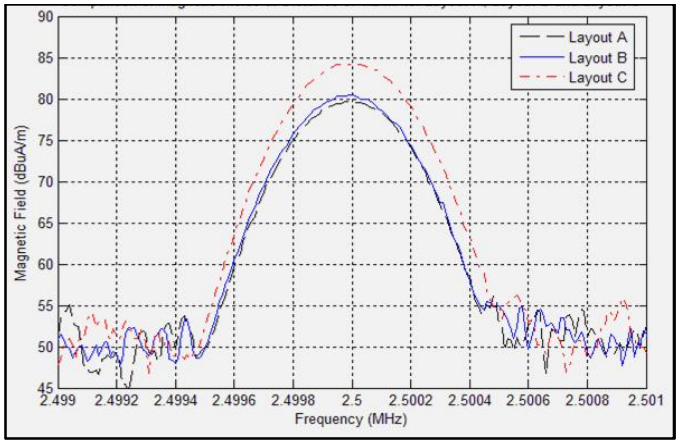


Fig. 12 Magnetic fields at 1.2 m for Layout A, Layout B and Layout C at 25 MHz of frequency

V. Conclusions

In this paper, we presented the work related to the magnetic field measurement of the digital circuit with different mitigation techniques such as good return current design, integrating of filter at critical component and application of damping resistor on each signal trace. According to the results obtained from the magnetic field measurement, proper design of return current path of power and signal traces has a significant effect in the reduction of emission level. Filtering at the power supply network and damping resistor on signal traces should also be considered in EMI reduction. The far field magnetic field will not necessarily reduce for good design due to the significant of common-mode current.

Acknowledgment

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References

[1] T. Williams, *EMC for Product Designers*, 4th ed., Great Britain: Elsevier Science & Technology, 2007.

[2] M. I. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, 2nd ed., New York, USA: IEEE Press, 2000.

[3] M. Mardiguian, *Controlling Radiated Emission by Design*, 2nd ed., United States of America: Kluwer Academic, 2001.

[4] B. R. Archambeault, *PCB Design for Real-World EMI Control*, Boston: Kluwer Academic, 2002.

[5] P. K. Saha and D. Jim, "Reduction of EM radiation from electronic equipment at design stage," in *proc. EMC '97*, 1997, pp. 171-174.

[6] S. R. Macatee, "Considerations in Grounding and Shielding Computer-Controlled Audio Devices," *in proc. AES*, 1997, pp. 135-139.

[7] K. Y. See, M. Oswal, W. Khan-ngern, F. Canavero, C. Christopoulos and H. Grabinski, "Impact of PCB layout design on final product's EMI compliance," in *Proc. EMC-Zurich '06*, 2006, pp. 553-556.

[8] J. Hacker. (2009) Langer-EMV Technik GmbH homepage on Correction characteristics for magnetic field probes. [Online]. Available: http://www.langer-emv.de/en/products/disturbance-emission/near-field-probes/correction-characteristics-for-rf-magnetic-field-probe