Design, Simulation and Characterization of 50nm p-well MOSFET Using Sentaurus TCAD Software

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Abstract—Device 50nm p-well MOSFET was designed, developed and optimized based on 90nm recipe using Sentaurus TCAD Software. In this project, there are two sub-programs used which are Sentaurus Process and Sentaurus Device. Sentaurus Process is a simulation process which in designing the semiconductor technology. While Sentaurus Device work as a device simulator to find the characteristic for each semiconductor design. The simulation results are shown in two dimensions (2D) in INSPECT and TECPLOT SV. The threshold voltages (V_{th}) for NMOS and PMOS of 50nm are 0.187V and -0.071V, the drain saturation current (Id_{sat}) are 6.897e-04A and 1.22e-03A with the leakage current (Ioff) are 2.799e-07A and 2.507e-08A. The simulation results are almost the same with the theoretical.

Keywords: P-well MOSFET, Sentaurus Process, Sentaurus Device

I. INTRODUCTION

The MOS (Metal Oxide Semiconductor) transistor is the most promising active component for silicon VLSI circuits at the present time. There are a number of reasons for this choice. First, it is self – isolating, so that the devices can placed side by side on a chip without the needs for providing isolation tubs. As a result, it is considerably smaller than its bipolar counterpart, and requires less processing steps [1]. Furthermore, it can be made in bulk silicon, thus avoiding the costly epitaxial growth. However, epitaxial structures are increasingly used in high – density application, to minimize latch–up problems, caused by devices interactions through a common substrate [2].

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The MOS transistor contains two types, the p –channel MOSFET (PMOS) and n- channel MOSFET (NMOS). Both of these MOS transistors have their own characterization that differentiates each other. The p – channel transistor (PMOS), based on aluminum – gate technology, was the earliest practical MOS device structure [3]. The PMOS transistor consists of two categories which are depletion (DMOS) and enhancement (EMOS).

A transistor is considered as depletion type if both source and drain are connected by a channel. This channel is created by implantation ion or diffusion process. If there are no channel exists, the operation of transistor is known as depletion operation. The depletion mode is used mainly in analog circuit. A p- channel depletion mode transistor, although in conceptually possible, has never been used in practical circuits.

In this project, the enhancement PMOS and NMOS transistor are used to design p-well MOSFET. It is relatively easy to make as an enhancement mode device, which is the preferred choice for digital applications since it minimize the standby power dissipations [4].

II. 50NM P-WELL MOSFET DESIGN

Designing p-well CMOS semiconductor must go through several processes. The designing process involves modifying the recipe of MOSFET 90nm to MOSFET50nm. The first process is the simulation of fabrication process 50nm MOSFET which is done using Sentaurus Process. Then, the process for structure and mesh are done onto fabricated MOSFET using Sentaurus Structure Editor. The final step is electrical testing using Sentaurus Device.

The development of the CMOS starts with the formation of p-well (for n-substrate), where the n-substrate is layered with a 100Å thick oxide layer by oxidation process. Forming of active area with oxide layer with this thickness will act as a protector when doing ion implantation process. Furthermore, phosphorus will be implanted with the positive resistive which act as a mask during the annealing process in 900-1200 ˚ Celsius temperature.

The formation of active area process of transistor NMOS and PMOS are defined using photolithography. The active edge of NMOS which is p-well is normally covered by lithography. It is followed by the implantation of boron ion to increase the density of n-type surface which is act as obstacle of p-channel under the field oxide.

The next process is the formation of the polysilicon gate where the oxide layer will be growth and also implantation of boron ion. The pattern of the gate is designated by lithography action for drain (D) and source (S). The formation process of drain (D) and source(S) for MOSFET is carried with resistive electron layer by all over the wafer for S and D pattern.

The final process for development of MOSFET is metallization. The aluminum materials are doped on wafer surface. The resistive layer is coated and the related patterns are made by lithography process.

In process simulation, processing steps such as etching, deposition, ion implantation, thermal annealing and oxidation are simulated based on physical equations, which govern the respective processing steps. The simulated part of the silicon wafer is discretized (meshed) and represented as a finite-element structure. After the fabrication processes are completed, the electrical testing called device simulation is done onto the fabricated MOSFET.

Device simulations can be thought of as a virtual measurement of the electrical behavior of a semiconductor device, such as a transistor or diode. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration. For each node, the carrier concentration, current densities, electric field, generation and recombination rates, and so on are computed.

III. RESULT AND ANALYSIS

The results for process and device simulation are shown in figure 1-6. The graphs display in two dimension (2D) in INSPECT and TECPLOT SV tools in Sentaurus TCAD.

Figure 1 and 2 depict the layout for NMOS and PMOS transistor. For both transistors, the metal used is aluminum. The metals are used for interconnection and routing. The insulator used in this device is polysilicon. The source and drain areas are shown in green color and placed in between gate region for both transistors.
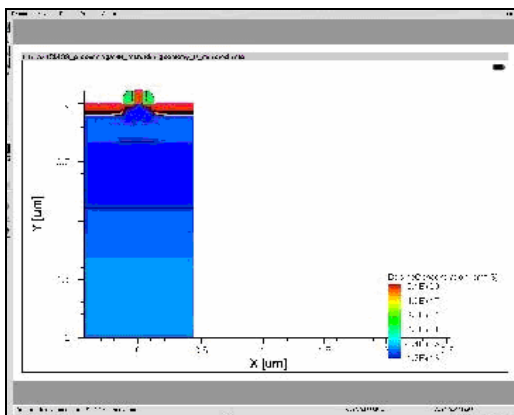

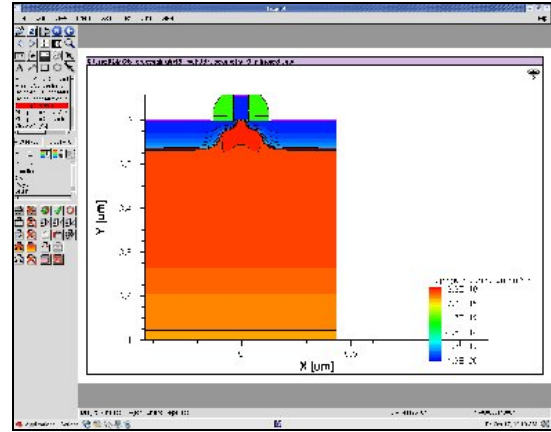Figure 1: Layout for 50nm NMOS transistor

Figure 2: Layout for 50nm PMOS transistor

The electrical DC analysis are done for both transistors and the results are shown using TECPLOT SV tools.

There are two electrical DC analyses done onto the NMOS and PMOS transistors to obtain the curve for I_D (Drain Current) versus V_{GS} (Gate to Source Voltage) and I_D (Drain Current) versus V_D (Drain Voltage). The results for each graph are depicted in figure 3-6.
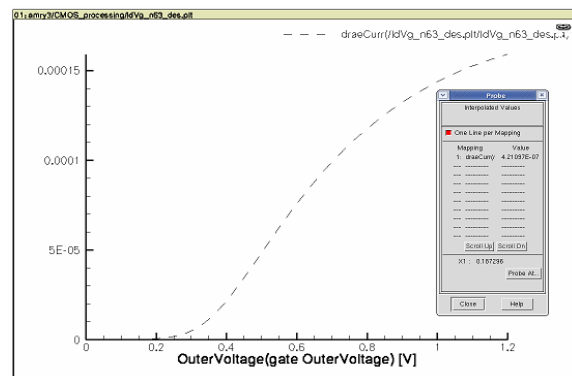

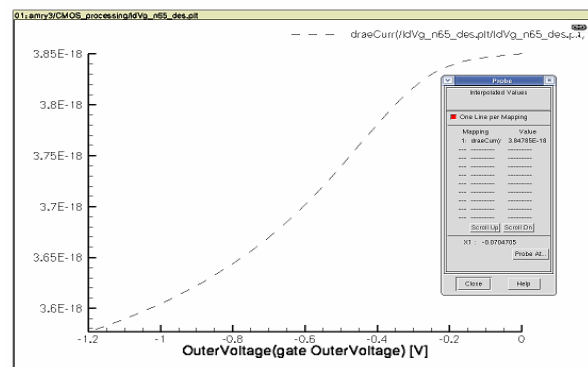Figure 3: I_D (Drain Current) -V_{GS} (Gate to Source Voltage) graph for 50nm NMOS transistor

Figure 4: I_D (Drain Current) -V_{GS} (Gate to Source Voltage) graph for 50nm PMOS transistor
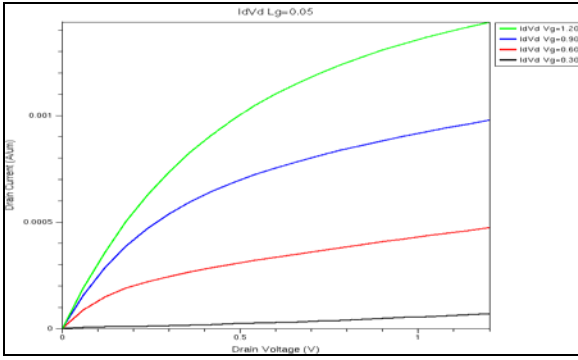
Figure 5: I$_D$ (Drain Current)-V$_D$ (Drain Voltage) graph for 50nm NMOS transistor
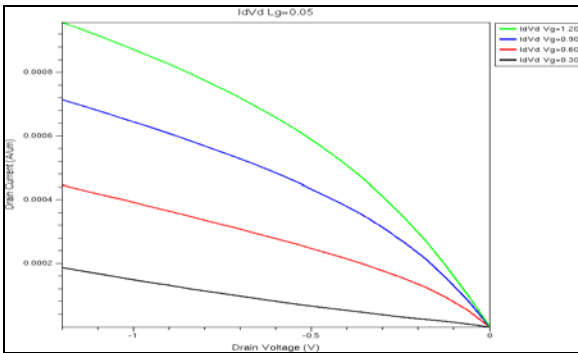

Figure 6: I$_D$ (Drain Current) -V$_D$ (Drain Voltage) graph for 50nm PMOS transistor

The main parameters for 50nm p-well MOSFER are shown in Table 1. The data obtained from the graph in figure 3- 6.

Table 1: Simulation values for 50nm MOSFET

Type	NMOS	PMOS
Vth (V)	0.187296	-0.070747
Idsat (A)	6.897e-04	1.220e-03
Ioff (A)	2.799e-07	2.507e-08

The threshold voltage (Vth) for transistor MOSFET is also know as the voltage that was generated between get and source at MOS device where current drain-source, drop until zero value. Vth is the starting voltage to operate for certain MOS transistor. If the value of voltage that is being use is below than Vth, the transistor will be in cut-off area. The threshold voltage (Vth) for 50nm p-well MOSFET is 0.187296V for NMOS and -0.070740V for PMOS transistor.

Majority carrier for NMOS transistor is electron, but for PMOS transistor is hole. Speed operation for NMOS is two (2) times faster comparing with PMOS transistor. This happen because the effective mass at the hole is better compared with electron, but electron has higher mobility value compare with hole.

Table 1 show the value of drain saturation current (Idsat) for NMOS transistor is 6.897e-04A while for PMOS transistor is 1.220e-03A. The Idsat is increasing proportionally with the increasing of gate length.

The opposite situation happens for leakage current. For the operating of ideal MOS transistor, the current only flow when it is in linear operation. When the transistor is off, no current will flow. But due to some geometrical effects, there is leakage current in small amount though the transistor in cut –off operation.

IV. CONCLUSION

The development of 50nm p-well CMOS transistor using Sentaurus TCAD software is successful. The design of 50nm p-well MOSFET transistor is done in two main processes which are device simulation and process simulation. Three main parameters are obtained and analyzed which are Threshold Voltage (Vth), Drain Saturation Current (Idsat) and Leakage Current (Ioff).

The downsizing of MOSFET is important due to the technology demand. However, the parameters must be scaled using Scaling Factor (S) to ensure the device can operate well after fabrication process.

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