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Experimental Investigation of High-Speed Digital Circuit's Return Current on Electromagnetic Emission

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***Abstract*—**Low impedance of the return current path and small loop area of return current loop are best practices design criteria to minimise electromagnetic emission from a high speed printed circuit board (PCB). In high-speed digital circuit, the high-frequency return current signal will find its way back to the source by flowing along the path of least inductance. It can either flows over the ground plane or on the guard trace which is physically close proximity to the high-speed signal trace. It is important to indicate that the use of guard trace can be one of the options of emission reduction techniques on double sided assemblies as it will reduce the emission level. In this paper, several double sided test boards were developed to evaluate the impact of different return current paths on radiated emission conducted in a Gigahertz Transverse Electromagnetic (GTEM) cell. Various designs will be presented and important conclusions will be derived.

***Keywords*:** Electromagnetic Emission, High-Speed Digital Circuit, Guard Trace, Emission Reduction.

I. Introduction

Today, most of the digital electronic devices are driven by clock signals which have a wide range of spectral content or harmonics frequency. Electromagnetic radiation induced by the harmonics cannot be ignored since it produces electromagnetic interference (EMI) problems. Electromagnetic compliance issue becomes mandatory for the Malaysian manufacturers for their product to be marketed to the countries that enforce electromagnetic compatibility (EMC) regulations such United States of America (USA), European Union (EU) and Japan. The electromagnetic emission of an electronic devices must not exceed the specified limits and unaffected to the emissions of another electronic device for electronic devices to have achieved EMC standard.

Many works have been done on the suppression of differential-mode (DM) and common-mode (CM) radiations on PCB layout. Figure 1 shows the total current which is decomposing into differential-mode and common-mode components. Basically, the DM radiation is characterised by differential mode currents, I_D flowing on closed loops (power or signal and return path loop) that behave like transmitting antenna, while CM radiation is caused by ground-noise voltage or voltage drops which results in common mode current flowing in interfacing cable [1].

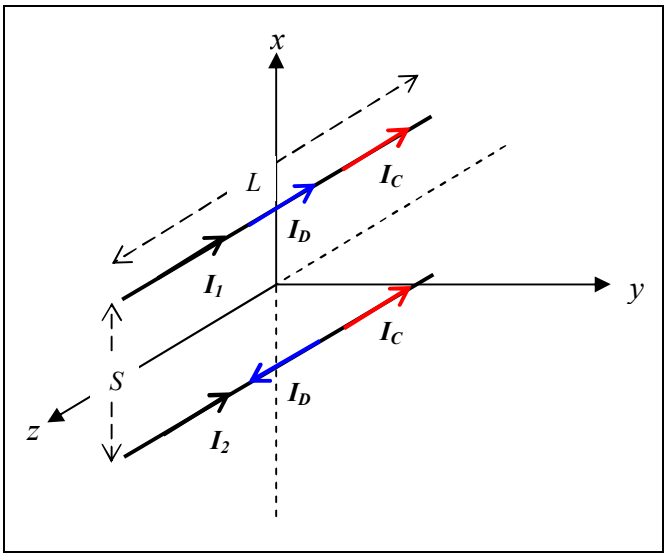

Figure 1 Decomposition of total currents on two wires or PCB lands.

The maximum emission of radiated electric fields, $|E_{D,\max}|$ and $|E_{C,\max}|$ that are broadside on the wires and Printed-Circuit Board (PCB) lands due to DM current and CM current respectively can be estimated by using the formula as given below [1];

$$|E_{D,\max}| = 1.316\times10^{-14}\frac{|I_D|f^2A}{d}\ [\text{V/m}] \qquad (1)$$

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$$|E_{C,\max}| = 1.257\times10^{-6}\frac{|I_C|fL}{d}\ \text{[V/m]} \quad (2)$$

where

$|I_D|$ is DM current in Ampere,
$|I_C|$ is CM current in Ampere,
A is the loop area in m^2,
f is frequency in Hertz,
L is the line length in m,
d is the distance of observation point in m which is fixed by the related standard.

Based on (1) and (2), reducing the loop size and the line length, are basically the effective option for the circuit designer to reduce the level of emission.

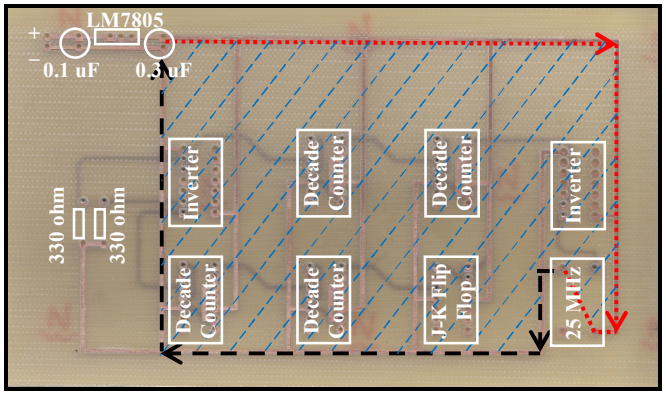
Numerous approaches have been reported in the literature [2]-[6] related to radiated emission from PCB. In [2], it has been proven experimentally that the poor PCB layout design is fail to meet EMC compliance. A digital circuit with high ground bounce indicates large circuit loop which lead to high DM radiation and also CM radiation through interfacing cable [3]. However, in [4] the authors reported that a lower load termination results on higher ground bounce. Reducing the loop size is basically can be done by applying decoupling capacitor [5]-[8] and the use of ground plane as return current path [7]-[9].

In this paper, different designs layout of return path for high-speed digital circuit are studied. This includes a large power to ground and signals to ground loops (layout A), both power and ground traces are route in parallel to each other separated with small distance at the same side (layout B), the return paths are route in physically close proximity to power distribution and signals traces (layout C). Moreover, the Layout D is basically same as in layout C except it has an employment of termination on signal traces.

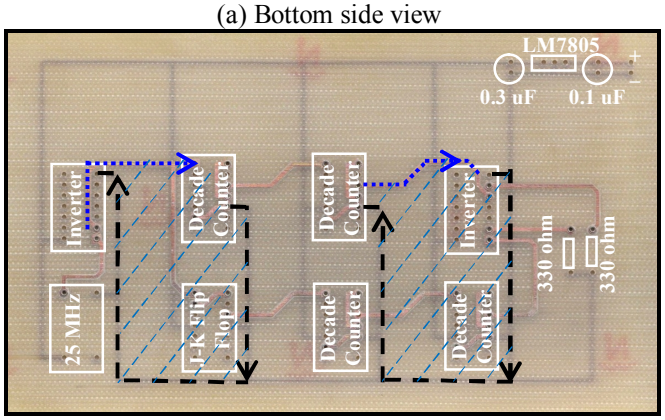
II. PCB LAYOUT CONFIGURATION

A good PCB layout practice is essential to control the emission level radiated from an electronic product. In the effort to investigate the electromagnetic emission of high speed digital circuit, four different PCB layouts as shown in Figure 2 to Figure 5 have been designed and fabricated. Double-sided FR4 board assemblies with relative permittivity 4.7 and thickness 1.6mm has been chosen in this study. The GTEM cell 750 with EMI receiver model SCR3012 utilized for radiated emission measurement. A 9 V battery was used as a supply voltage to operate the circuit which driven by 25MHz clock square wave signal.

The first PCB layout (Layout A) as shown in figure 2 (a) and (b) is designed with large power to ground and signal to ground loops. The red and blue dot-lines represent the power trace and signal trace respectively. Black dash-line shows its return current path. Based on figure 2 (a), the loops areas formed due to a large power to ground is about 79.5 cm^2. In figure 2 (b), it can be seen clearly that, the high-frequency return current signal will find its way back to the source by flowing through a long and large return current path and results in large signal to ground loops. The areas of each loop are 14.3 cm^2 and 15.05 cm^2.



(a) Bottom side view

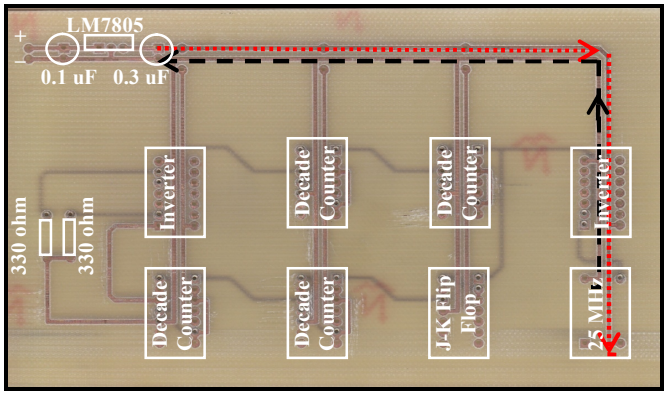


(b) Top side view

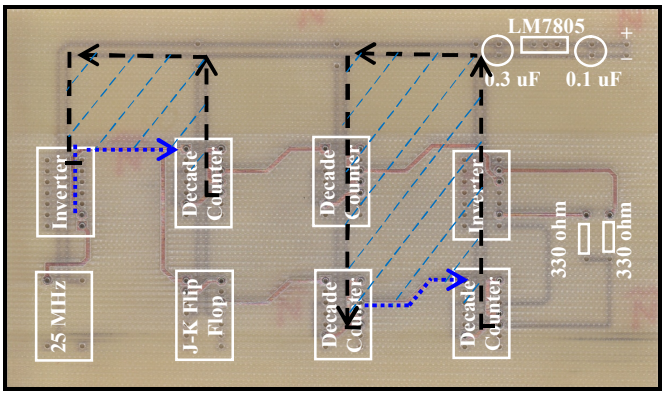
Figure 2 PCB Layout A.

In layout B, both power and ground return traces are routed in parallel to each other separated with small distance in order to reduce loop area of power to ground. By minimising this loop, the radiation due to the currents that may be developed by high frequency logic gate's switching noise into the power distribution system can be minimised. Figure 3 (a) and (b) show the bottom and top side view of Layout B.

According to figure 3 (a), by routing the power and ground traces adjacent to each other with minimal distance of separation, the loop areas become smaller approximately 3.15 cm^2. In contrast, the signal current without return path traces routed closely with signal trace will find its way back to the source by flowing through a large loop as shown in figure 3 (b). When the current flows at two parallel wires placed very close to each other, the magnetic fields generated by the differential mode current on both wires will cancel out each other (flux cancelation).



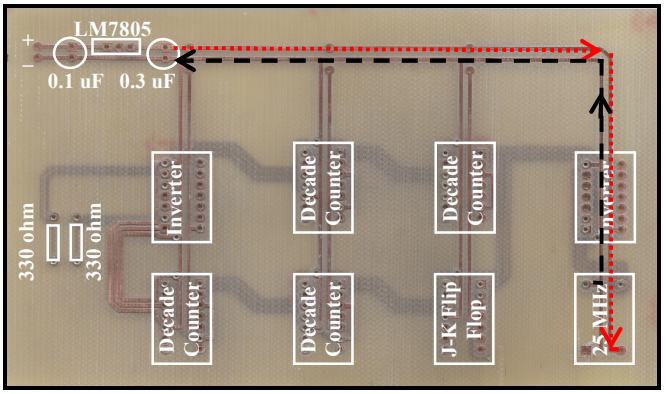
(a) Bottom side view



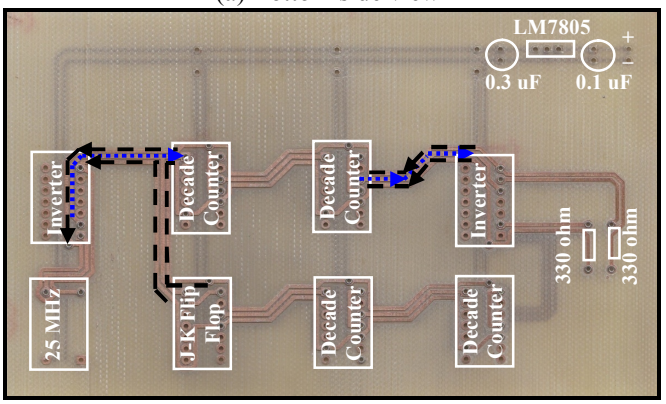
(b) Top side view

Figure 3 PCB Layout B.

In Layout C, the return paths are routed in physically close proximity to power distribution and signals traces as shown in figure 4 (a) and (b). The guard trace is applied around every clock signal traces to provide a low impedance alternative path home for high frequency current and minimise signal to ground loop areas as well as to reduce differential mode radiation.



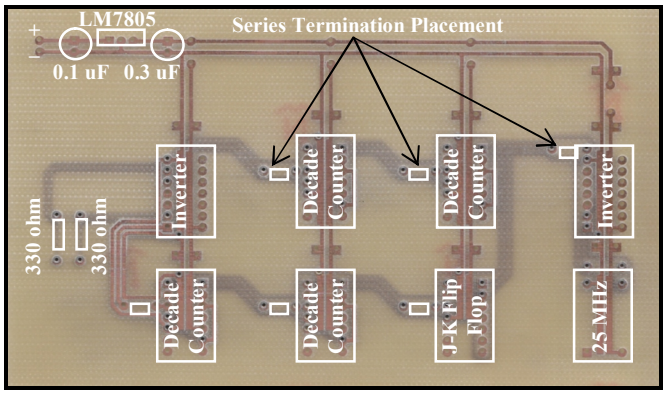
(a) Bottom side view



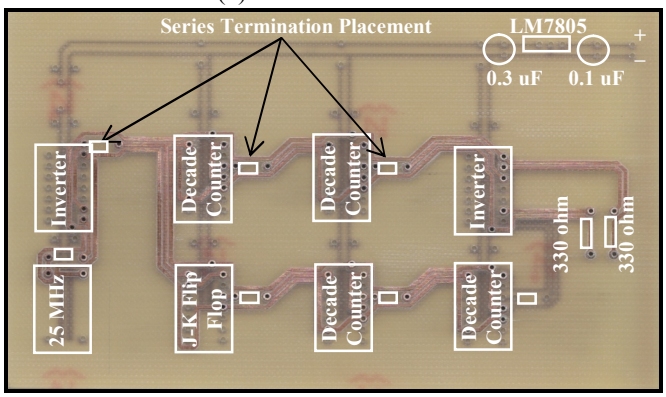
(b) Top side view

Figure 4 PCB Layout C.

Basically, a maximum signal power transfer through traces on a PCB can be achieved with matching impedance. When PCB traces carry high frequency signal with unmatched impedance of the driver, receiver devices, reflection may arises, and results of both overshoot and undershoot on clock signal that known as high frequency noise. In the fourth layout as shown in figure 5, series termination was employed at each signal traces to improve the signal quality and remove high frequency noise radiation.



(a) Bottom side view



(b) Top side view

Figure 5 PCB Layout D.

III. RESULTS AND DISCUSSION

Experimental measurement was carried out to study the effect of loop area forms by a power or signal and return current path of the circuit and the employment of trace termination on radiated emission level. In this section, the measurement results of radiated emission conducted in the GTEM 750 with EMI receiver SCR3012 for high-speed digital circuit PCB layout that operates at various frequencies are presented and discussed. It can be seen clearly that, all measurement results are exceeding the EN55022 limit line especially at the harmonics frequency of 25 MHz clock signal. Thus, they have failed the radiated emission testing and do not comply with EN55022 class B regulation.

Effect of Return Current Path Loops

Initially, we have performed radiated emission measurement to study the loop areas of return current path on emission level. Figure 6 shows the comparison of the different routing of return current path of power and signal traces on radiated emission levels. It can be observed that by routing the power and ground trace in parallel has contributed an additional emission spectrum of frequency below 300 MHz. Moreover, a little increment of emission at frequency of 475 MHz to 850MHz has also been found. It

is believed to be related with the changing of signal loops size as shown in figure 2(b) and figure 3 (b).

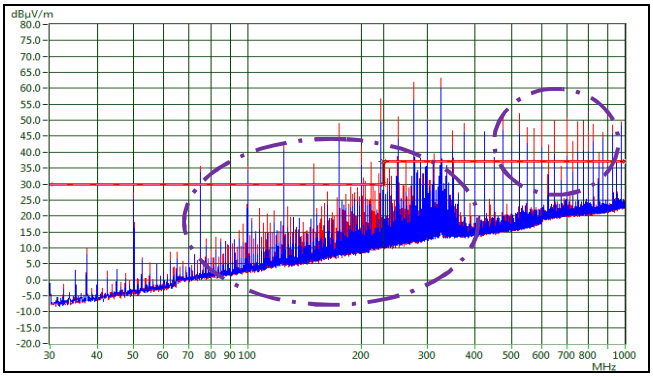


Figure 6 Radiated emission with and without power and ground traces routed in parallel.

Both Layout A and Layout B which have large signal loops areas, radiate high levels of differential mode radiation because of magnetic fields from power or signal and ground traces do not completely cancel as its are routed far apart. Thus, to control radiated emission, the most critical loops which carrying highest-frequency signal should be minimised.

In high-speed digital circuit, the high-frequency return current signal will find its way back to the source by flowing along the path of least inductance. One of the options to reduce loop areas formed by high-speed signal trace and its return path is using the guard trace. When guard traces are used and placed in a close distance to signal trace, the magnetic flux cancelation will occur. Thus, the radiated emission levels reduced significantly as shown in figure 7.

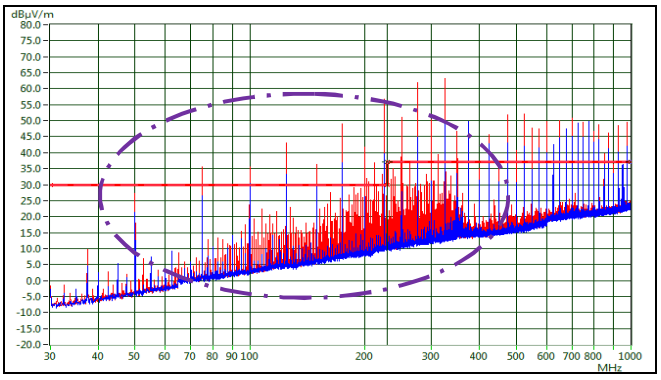
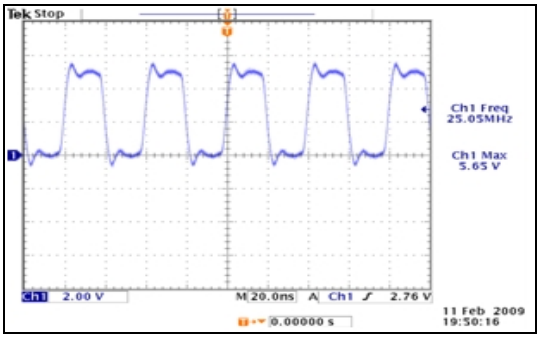


Figure 7 Radiated emissions with and without guard trace.

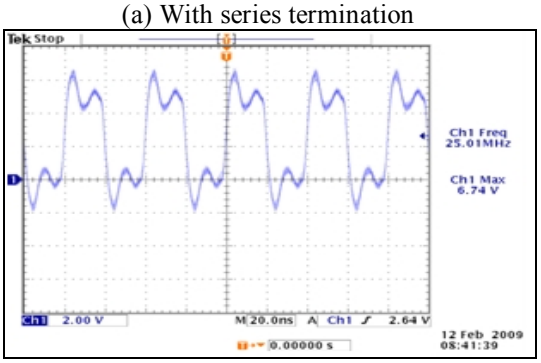
Observation of Figure 7 shows that, by providing a return trace physically close to the signal traces, the emission spectrum due to spectral content radiation of 12.5MHz, 2.5MHz, 1.25MHz, 0.25MHz and 0.125MHz square wave signals are remove significantly except for the frequency range of 500MHz to 800MHz..

Effect of Series Termination

Next, we performed experimental measurement to study the effect of signal termination in reduction of radiated emission. Ideally, in circuit design, it is very important to match the impedance of the transmission line to its termination. The purpose is to ensure that, a ringing on clock signal due to reflection on a trace can be minimised as well as to increases quality of the signal. Trace termination is required to prevent impedance matching problems and provide higher quality signal transfer between circuits [10]. Figure 8 (a) and (b) shows the 25 MHz square wave clock signal with and without a series termination on signal trace. It can be observed that, series termination reduces ringing on clock signal and also remove the high frequency radiation as can be seen in figure 9.



(a) With series termination



(b) Without series termination

Figure 8 25 MHz clock signal waveform with and without series termination at signal trace.

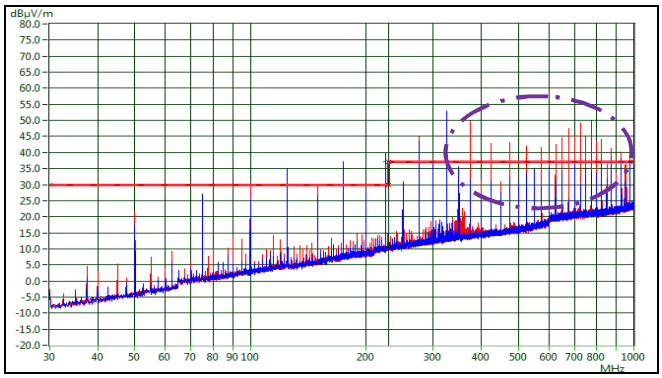


Figure 9 Radiated emissions with and without series impedance termination.

Based on figure 9, it is proven that the high frequency radiation can be reduced by providing a termination for traces which is rich in harmonic frequency. The emission levels at frequency 350 MHz to 1 GHz have been further reduced and within the required EMC standard except at

frequency of 125 MHz, 175 MHz, 225 MHz, 275 MHz, 300 MHz and 325 MHz which are the spectral content of 25 MHz clock signal, the emission levels exceed the EN 55022 Class B.

IV. CONCLUSION

In this paper, we presented the work related to the electromagnetic emission of high-speed digital circuit with different configurations of return current path. This study implemented with a purpose to reduce emission level due to differential mode radiation on various loop areas. According to the results obtained from experimental measurement inside GTEM cell, it was found out that, the use of guard trace has significant effect in reduction of emission level because it offers an alternative return current path with lower impedance for the high frequency current as well as reduction in the signal loop areas. In addition, the use of termination has played an important role to minimise high frequency radiation.

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REFERENCES

[1] C. R. Paul, *Introduction to Electromagnetic Compatibility*, John Wiley & Sons, 2006.

[2] K. Y. See, M. Oswal, W. Khan-ngern, F. Canavero, C. Christopoulos and H. Grabinski, "Impact of PCB Layout Design on Final Product's EMI Compliance", *Proceedings of the 2006 IEEE 17th International Zurich Symposium on Electromagnetic Compatibility,* March 2006, pp. 553-556.

[3] K. Y. See, M. Oswal, Z. H. Liu and K. L. Kyaw, "Correlation between Ground Bounce and Radiated Emission", *Proceedings of the 2004 IEEE,* March Electronics Packaging Technology Conference, December 2004, pp. 640-642.

[4] E. K. Chua, E. P. Li, K. Y. See and W. Y. Chang, "The Effects of Signal Trace's Termination on Ground Bounce and Common-Mode Radiation", *Proceedings of the 2007 IEEE International Symposium on Electromagnetic Compatibility,* July 2007, pp. 1-5.

[5] C. Rostamzadeh, S. Connor, and B. Archambeault, "Numerical and Experimental Investigation of Power Supply Noise Decoupling Strategies on Single-Sided Printed Circuit Boards", *Proceedings of the 2007 IEEE International Symposium on Electromagnetic Compatibility,* July 2007, pp. 1-5.

[6] J. Kim, B. Choi, H. Kim, W. Ryu, Y. Yun, S. Ham, S. Kim, Y. Lee and J. Kim, "Separated role of on-chip and on-PCB decoupling capacitors for reduction of radiated emission on printed circuit board", *Proceedings of the 2001 IEEE International Symposium on Electromagnetic Compatibility,* August 2001, pp. 531-536.

[7] T. Williams, *EMC for Product Designers*, 4th Edition, Elsevier, 2007.

[8] M. Mardiguian, *Controlling Radiated Emission by Design*, 2nd Edition, Kluwer Academic, 2001.

[9] D. Moongilan, "Image and return current modeling of PCB traces for radiated emissions", *Proceedings of the 2001 IEEE International Symposium on Electromagnetic Compatibility,* August 2001, pp. 927-932.

[10] Montrose, M. I. *Printed Circuit Board Design Techniques for EMC Compliance*. 2nd ed. IEEE Press. 2000.