Proceedings of EnCon2008
2nd Engineering Conference on Sustainable Engineering Infrastructures Development & Management
December 18 -19, 2008, Kuching, Sarawak, Malaysia

ENCON2008-F-26

Operational Transconductance Amplifier Design for A 16-bit Pipelined ADC

Nordiana Mukahar, Siti Hawa Ruslan and Warsuzarina Mat Jubadi

Abstract—**In biomedical application, electronic interfacing is fundamental for obtaining information from human body. Designing a high performance analog circuit is becoming increasingly challenging with the persistent trend towards reduced supply voltages and low power consumptions.A fully differential, 5V operational transconductance amplifier (OTA) to be used in a pipeline analog-to-digital converter (ADC) has been designed. The main operational amplifier (Op Amp) circuit is a full differential folded cascode with continuous time common mode feed back (CMFB). The boosting Op Amp is a wide swing OTA circuit. The Op Amp is designed according to a 0.5 µm CMOS14TB technology standard using Tanner Tool. Simulation result shows the unity gain bandwidth of the Op Amp is 9.32 MHz for a 5 pF load and the amplification is 93.27 dB, while the settling time is 163 ns for 0.1 % accuracy to achieve final value with sampling rate of 1 MS/s.**

***Keywords*:** Op Amp, OTA, ADC, wide swing, folded cascode.

I. Introduction

Designing of high performance Complementary Metal Oxide Semiconductor (CMOS) OTA's for use in pipeline ADC is becoming increasingly challenging task. In high performance analog integrated circuits, such as a pipeline A/D converters, Op Amp with very high DC gain and high unity gain frequency are needed to meet both accuracy and fast settling requirements of the systems. However, satisfying both of these aspects leads to contradictory demands, and becomes more difficult since the intrinsic gain of the devices is limited. As the CMOS devices are sized for large transconductance to achieve high gain bandwidth (GBW) and high DC gain for fast and accurate settling time, the attendant of parasitic capacitance severely erode the amplifier phase margin (PM), thus reducing GBW. Furthermore, some amplifier errors which referred to offset, incomplete settling time and finite gain errors limit the accuracy of an Op Amp. In order to get a 16-bit resolution in the ADC, the Op Amp open loop gain must be high enough so that the interstage gain is accurate to 16-bit. Hence, a single stage gain enhanced OTA topology that approximates a single pole system was considered ideal for the above low voltage requirements.

A number of OTA design exists in the literature. In [1], the design achieving 870 MHz GBW and 92 dB DC gain at 1.5V which using 0.35 µm CMOS process. A DC gain of 129 dB and about 161 MHz GBW was achieved in [3] for a 0.35 µm CMOS design but with a 3.3 V operating voltage. The OTA designed in [7] obtained a 105 dB DC gain and 90 MHz GBW at a 3.3 V but consumes 4.8 mW. Based on these previous works, it is well known that active cascode gain boosting technique is used to increase the DC gain of an operational amplifier without degrading its high frequency performance. Thus, the folded cascode amplifier architecture is chosen to design the Op Amp in this project. A gain boosting technique is included to increase the gain of a normal cascode stage without affecting the frequency behaviour to a large extent. The Op Amp circuit implemented with the gain boosting technique is designed as a proof of concept for this topology. It is due to the fact the design will give a better performance in term of high DC gain and high settling time as required.

II. OTA Design Specifications

Op Amps that are designed to provide transconductance should have a very high output impedance, hence provide very good isolation. OTA is an Op Amp without an output driver. It is capable of driving small capacitive loads. This make the OTA well suited for pipeline applications. The amount of current required in the design has to be determined according to the specification. The Op Amp must amplify signals to within ½ least significant bits (LSB) of the ideal value. The closed loop gain, A_{CL} of an amplifier can be determined using (1) where A_{OL} is open loop gain. The feedback factor, β in (2) is defined according to the inverting circuit with capacitor feedback. The capacitive dependence is used to estimate the feedback factor that presents in a discrete analog integrator (DAI).

This work was done using ScienceFund grant from MOSTI.
Nordiana Mukahar is now working with Intel Microelctronic (M) Sdn. Bhd. (e-mail: nordiana_mukahar@yahoo.com).
Siti Hawa Ruslan and Warsuzarina Mat Jubadi are with Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, 86400 Pt Raja, Batu Pahat, Johor (e-mail: sitihawa@uthm.edu.my, suzarina@uthm.edu.my).

$$A_{CL} = \frac{A_{OL}(f)}{1+\beta.A_{OL}(f)} \quad (1)$$

$$\beta = \frac{R_1}{R_1+R_2} \text{ or } \frac{C_F}{C_F+C_I} = \frac{1/j\omega C_I}{1/j\omega C_I + 1/j\omega C_F} \quad (2)$$

The output of the amplifier will be equal to its ideal value minus some maximum deviations, ΔA. If the maximum value of ΔA is at most ½ LSB of the ideal gain, the gain of the DAI over one clock cycle can be calculated using (3). By assuming $\beta = 1/2$ and $C_I = C_F$, the minimum required DC open loop gain, $|A_{OLDC}|$ can be estimated according to (4);

$$\Delta A = \frac{C_I}{C_F}.\frac{\frac{1}{2}\times LSB}{Full\ scale\ output}$$

$$\Delta A = \frac{C_I}{C_F}.\frac{1/2.(V_{REF+} - V_{REF-})/2^N}{(V_{REF+} - V_{REF-})} = \frac{C_I}{C_F}.\frac{1}{2^{N+1}} \quad (3)$$

$$|A_{OLDC}| \geq \frac{1}{\beta}.2^{N+1} \text{ and } |A_{OLDC}| \geq 2^{N+1} \quad (4)$$

Thus, a 16 bit converter must have $|A_{OLDC}| \geq 262144$ or 108 dB. The speed of a data converter is mainly limited by the settling time as it is an important measurement of the dynamic performance. Therefore, the minimum Op Amp gain frequency, f_u required for a specific settling time, τ can be estimated using (6);

$$\tau = \frac{1}{2\pi.\beta.f_u} \quad (5)$$

$$f_u = \frac{f_{clk}.\ln 2^{N+1}}{2\pi.\beta} \text{ and } f_u \geq 0.22(N+1)f_{clk} \quad (6)$$

For a 16 bit pipelined ADC that is clocked at 1 MHz, the required Op Amp must have unity gain frequency, f_u at 3.74 MHz and at least a DC gain of 108 dB.

III. Amplifier Topology

A. Single Stage Amplifier

For a high gain design, two stage configurations might be the appropriate choice. However, the speed of this configuration is limited and it required compensation circuit. In fact, a single stage Op Amp can give high gain and also good bandwidth without any compensation. This is the major advantage of single stage Op Amp over two stage configurations. The gain is rather low due to the relatively low output impedance. This low impedance also leads to high unity gain bandwidth and hence high speed. The small signal low frequency gain, A_{LF} of the single stage Op Amp in figure 1 is equal to (7). The subscripts *N* and *P* denote NMOS and PMOS respectively;

$$A_{LF} = g_{mN}(r_{oN} \| r_{oP}) \quad (7)$$

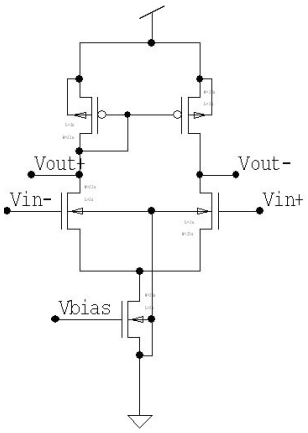


Figure 1: A Single Stage Op Amp Circuit.

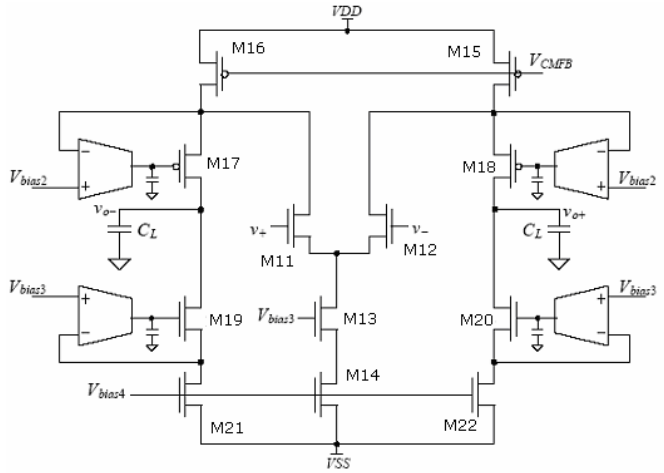


Figure 2: Fully differential folded cascode Op Amp with gain boosting amplifiers.

B. Complete Circuit Design

In the design, a fully differential folded cascode Op Amp that has four single ended OTA has been chosen. In order to achieve high gain and speed, the Op Amp employs NMOS input differential pair. The complete implementation circuit is shown in figure 2. This design incorporates fully differential inputs, outputs, a folded cascode bias circuitry with common mode feed back (CMFB) and gain boosting amplifiers. The OTA can be divided into four parts: the bias circuit, the amplifier circuit, the common mode feedback circuit and the gain boosting circuit.

C. Full Differential Folded Cascode Op Amp

A differential pair is used to sense the input voltage difference. If the pair is operating in saturation region, when one transistor is turned on, the other will turn off. The current through one leg will be sourced to the output while the other leg will sink current from the load. The input transistors were sized with a very large W/L ratio to provide the high transconductance required to quickly move charge onto the test capacitors [9].

The input differential pair must operate in saturation region. Operation in the triode region will cause the behavior of the OTA to be nonlinear and will result in poor transient response as well as a loss in DC gain. Since the OTA is to be used in the multiplying digital analog converter (MDAC) of a 1 MS/s, 16-bit pipeline ADC design, it requires that the output to settle to 0.1 % in ¼ the period (250 ns). The desired ADC input range is 1 V_{P-P} differential and a settling time of about 8τ. Choosing a 5pF load capacitor, the OTA must be able to slew at 36 V/µs. Thus, the required current that is used to charge (or discharge) each load capacitor must be 180 µA in order to meet the slew rate specification. The transistors ratio are shown in Table 1 and sized according to the required current values.

Table 1 The transistor sizes, W/L (in µm) and Drain Current, I_D(µA) for the Op Amp used in the OTACircuit.

Transistor	W/L	$I_D(\mu A)$	Transistor	W/L	$I_D(\mu A)$
M11	10.8/1	90	M17	88.76/1	180
M12	10.8/1	90	M18	88.76/1	180
M13	10.8/1	180	M19	10.8/1	180
M14	10.8/1	180	M20	10.8/1	180
M15	144.31/1	270	M21	10.8/1	180
M16	144.31/1	270	M22	10.8/1	180

D.Gain Boosting Amplifier

A gain enhancement technique is used in this project to increase the gain of the Op Amp. A single ended Op Amp is used as a gain boosting amplifier, A_{OTA}. It has been implemented in the main amplifier circuit as shown in the figure 3. The idea of gain boosting technique is based on negative feedback loop to set the drain of voltage M21. The negative feedback will drive the gate of M19 until V_x has the same value as V_{bias3}. Therefore, the variation of V_{out} has much less effect on V_x because the boosting Op Amp regulated this voltage. Thus, the output impedance, R_{OUT} of the circuit is increased by the gain of the additional gain stage A_{OTA} , as shown in (9);

$$R_{OUT} = \left(g_{m19} r_{o19}\left(A_{OTA}+1\right)+1\right)\times r_{o21} + r_{o19}$$
$$\approx A_{OTA} g_{m19} r_{o21} r_{o19} \qquad (8)$$

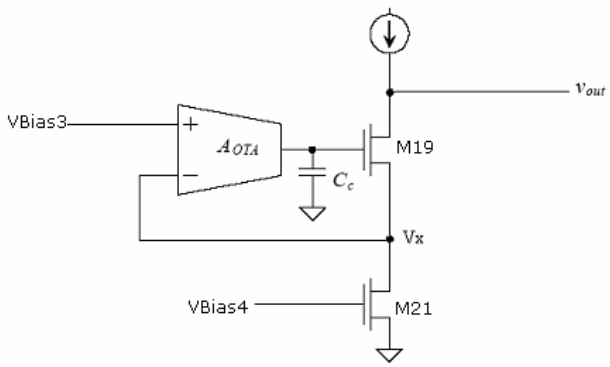


Figure 3: Gain enhancement to increase cascode open circuit gain.

E. Wide Swing OTA

Wide Swing OTA has been used as a gain boosting amplifier in this project. Wide swing means that input common mode range is close to the supply voltage. A technique used to extend the allowable input swing of a differential amplifier is to use two complementary differential amplifier stages in parallel. The wide swing OTA provides an output voltage to bias the gates of M17, M18, M19 and M20 of main amplifier. Both the DC gain and the output impedance of the main Op Amp are multiplied by a factor of about $(1 + A_{OTA})$, where A_{OTA} is the gain of the additional feedback path. The overall DC gain can be increased by several orders of magnitude as shown in (9), by utilising the output impedances.

$$A_{TOTAL} = g_{m21} R_{OUT} = A_{OTA} g_{m21} g_{m19} r_{o21} r_{o19} \qquad (9)$$

F. Common Mode Feedback Circuit (CMFB)

CMFB circuit is indispensable in a fully differential operational amplifier. The CMFB circuit as shown in figure 4 must be added to sense the common mode level of the two outputs and accordingly adjust one of the bias currents in the amplifier [8]. It keeps the outputs from drifting high or low out of range where the amplifier provide plenty of gain. The circuit uses two differential pairs (MF5, MF6, MF7 and MF8) to sense the difference between the average output voltage and a common mode voltage V_{CM} which is supplied externally. The current in the CMFB circuit does not need to be large as long as the current through the top and bottom of the OTA are fairly well balanced.

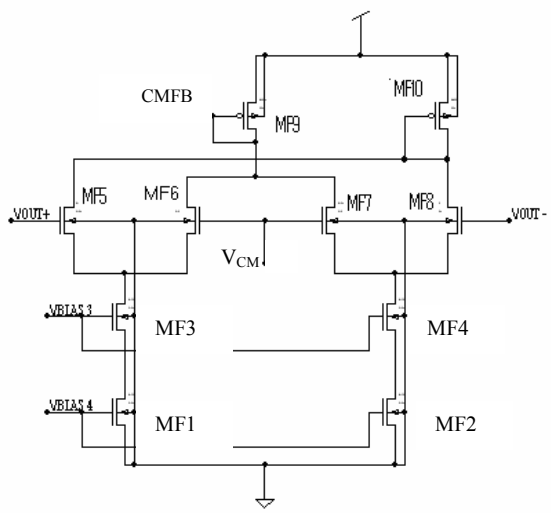


Figure 4: The CMFB circuit.

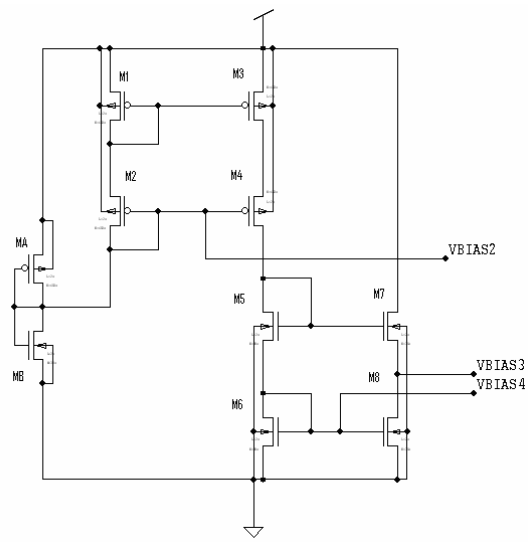


Figure 5: Biasing circuit.

G. OTA Biasing Circuit

The Op Amp, CMFB, and gain boosting amplifiers circuit use the same biasing circuit, as shown in figure 5. High swing cascode current mirrors are used for the biasing circuit. Cascode sources were chosen because it was necessary to keep the bias currents in the top half of the amplifier as constant as possible to ensure accurate settling. The bias current is initially created using a simple voltage reference, MA and MB. These bias voltages enable those transistors of main Op Amp, CMFB and gain boosting amplifiers to work in saturation region. The dimensions of transistors used are listed in Table 2.

Table 2 The transistor sizes, W/L (in µm) for the Op Amp used in the Biasing Circuit.

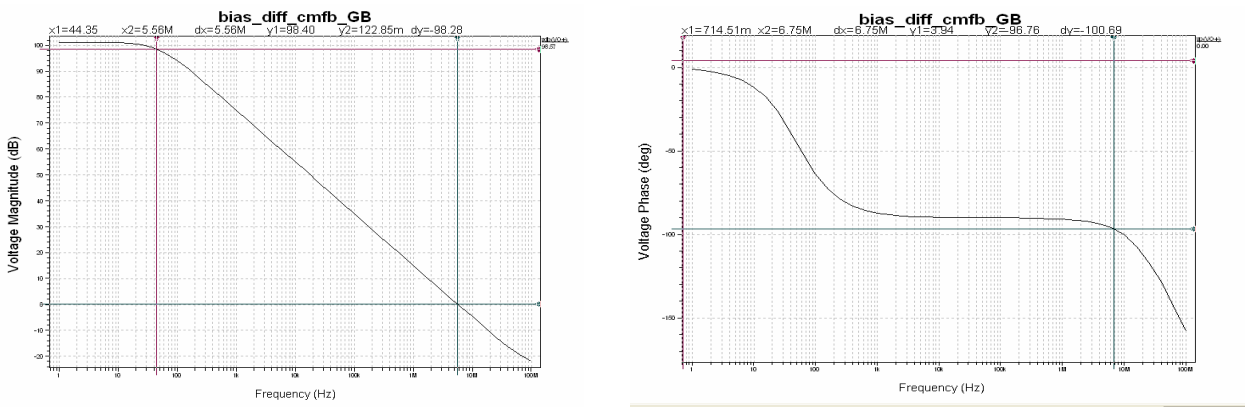
Transistor	W/L	Transistor	W/L
MA	80/1	M4	29.856/1
MB	15.643/1	M5	3.59/4
M1	29.856/1	M6	3.59/1
M2	29.856/1	M7	3.59/1
M3	29.856/1	M8	3.59/1

IV. RESULT & ANALYSIS

Simulation of both schematic and layout of the OTA was done using TANNER EDA Tool. The Op Amp has been implemented in 0.5 µm CMOS14TB process with 5 V power supply. The AC simulation results are shown in figure 6. It shows that the DC gain is 93.27 dB and the unity gain frequency is 9.32 MHz. The phase margin is about 93 ^{o}. In comparison with the theoritical values, the total gain for the OTA circuit, A_{OTA} is given in (10);

$$\boldsymbol{A_{TOTAL}} = \boldsymbol{A_{GB}} + \boldsymbol{A_{ORIG}} = 93.36 \ \boldsymbol{dB} \qquad (10)$$

The gain boosting amplifier has increased the DC gain from 58.483 dB to 93.36 dB. Compared to the result in figure 6(a), the percentage of error is 0.1% or 0.09 dB.



(a) (b)

Figure 6: (a) DC Gain Response. (b) Phase Response

With a unity gain configuration, the slew rate and settling time are measured. The transient response of the test circuit is shown in figure 7. The plot on the top of figure 10 shows the input and output of the OTA while the plot at the bottom shows the differential output voltage. The goal is to achieve a difference of 1 V after settling between the outputs, with at least 16 bits accuracy. Figure 7 shows a typical settling time measurement. The differential output settles to 999 mV in 163 ns, and back down to less than 1 mV in 163 ns.

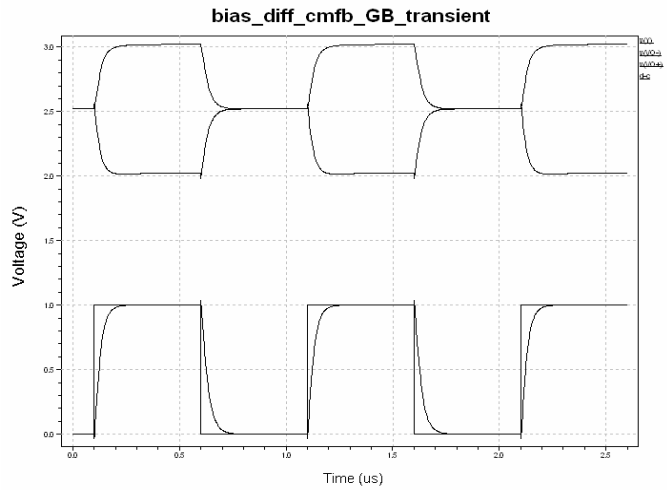


Figure 7: Simulated transient response of Op Amp.

The main characteristics of the Op Amp being designed are summarized in Table 3. The results shows that the gain boosted technique had improved efficiently the DC gain without affecting the speed of Op Amp.

Table 3 Main characteristics of the Op Amp.

Parameter	**Value**
Technology	0.5 um CMOS14TB
DC Gain without gain boosting	48.8 dB
DC Gain with gain boosting	93.27 dB
Phase Margin	93.14 ^{o}
Unity Gain Frequency	9.32 MHz
Slew Rate	36 V/µs
Output voltage swing	1.75 – 4.86 V
Settling time (0.1%) accuracy	163 ns
Supply Voltage	5 V
Power Dissipation	4.88 mW
Load Capacitor	5 pF
Area	0.089 mm^2

V. CONCLUSION

The design of a single stage fully differential operational amplifier with gain boosting amplifier using 0.5 µm CMOS14TB technology is presented in this paper. With the load capacitor of 5 pF, the design demonstrates a DC gain of 93.27 dB with a unity gain frequency of 9.32 MHz and phase margin of 93.14 ^{o}. This design is tailored for high resolution with low sampling rate pipelined ADC and it will be used in a 16 bit pipelined ADC.

VI. REFERENCES

[1] O. A. Adeniran, and A. Demosthenous, "A 19.5mW 1.5V 10-bit Pipeline ADC for DVB-H systems in 0.35 um CMOS." *Circuits and Systems*, IEEE International Symposium, 2006.
[2] O. A. Adeniran, and A. Demosthenous, "A 92dB 560MHz 1.5V 0.35 um CMOS Operational Transconductance Amplifier." *Circuit Theory and Design. Proceedings of the European Conference*. Volume 3. pp. 325-328, 2005.
[3] Wang Jin and Qiu Yulin, "Analysis and design of fully differential telescopic cascode Op Amp." *Solid-State and Integrated Circuits Technology Proceedings, 7th International Conference.* Volume 2. pp. 1457-1460, 2004.
[4] Yun, Chiu., P. R. Gray, P.R., and B. Nikolic, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR." *Solid-State Circuits, IEEE Journal*. Volume 39, Issue 12. pp. 2139 – 2151, 2004.
[5] R. G. Carvajal, B. Palomo, A. Torralba, F. Munoz, and J. R. Angulo, "Low voltage high-Gain differential OTA for SC circuits." *Electronic Letters*. Volume 39. pp. 1159-1160, 2003.
[6] D. Shahrjerdi, B. Hekmatshoar, M. Talaie, and O. Shoaei, "A fast settling, high DC gain, low power Op Amp design for high resolution, high speed A/D converters.", *Proceedings of the 15th International Conference, Microelectronics*. pp. 207-210, 2003.
[7] K. Gulati, and Hae-Seung Lee. "A high-swing CMOS telescopic Operational Amplifier." *Solid-State Circuits, IEEE Journal*. Volume 33, Issue 12. pp. 2010 – 2019, 1998.
[8] Behzad Razavi., *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.
[9] Nordiana Mukahar, "*The Development of Operational Amplifier For A 16 Bit Pipelined ADC*," Thesis, Dept. Elect. Eng.,UTHM, M'sia, 2008.
[10] R. L. Geiger, P. E. Allen, and N. R. Strade, *VLSI Design Techniques for Analog and Digital Circuits*. New York: McGraw-Hill, 1990.
[11] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. IEEE Press Series on Microelectronic Systems: John Wiley & Sons, INC, 1998.
[12] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation.* 2nd Ed. IEEE Press Series on Microelectronic Systems: John Wiley & Sons, INC, 2005.
[13] T. L. Floyd, *Basic Operational Amplifiers and Linear Integrated Circuits*. 2nd .Ed. New Jersey: Prentice Hall. 1999, pp. 48-60.