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PROCESS AND DEVICE SIMULATION OF 80NM CMOS INVERTER USING SENTAURUS SYNOPSYS TCAD

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ABSTRACT

Nowadays, the simple manufacturing process of CMOS transistor is widely used in digital design implementation. Using the latest technology in fabrication, the sizes of semiconductor devices are ever shrinking toward the nanotechnology. This paper presents the development of 80nm gate length of CMOS inverter with modification of the theoretical values in order to obtained more accurate process parameters. Simulation of the process and device fabrication using Sentaurus Synopsys TCAD has been carried out and the electrical characteristics of the device were studied and analyzed. The result of the study indicates that the operational of CMOS inverter was at $V_T = 0.499V$, $I_{off} = 79.08pA/\mu m$ and $I_{DSAT} = 429.3\mu A/\mu m$ for NMOS device. The values were then compared with 90nm CMOS inverter. The study also found that the leakage current of 80nm CMOS transistor is almost twice higher than 90nm CMOS transistor.

Keywords: *CMOS, gate length, Sentaurus Synopsys TCAD, nanotechnology.*

INTRODUCTION

Microelectronics has evolved tremendously in the last century [1]. Nowadays, the simple manufacturing process of CMOS transistor is widely used in digital design implementation. Using the latest technology in fabrication, the sizes of semiconductor devices are ever shrinking toward the nanotechnology. The MOS transistor is extensively used in digital circuits because it is a very good and efficient switch. By designing the MOS transistor in smaller gate length size, automatically the better the transistor in speed. This strategy has been driven by the increased performance that smaller devices make possible and the increased functionality that larger chips provided. Currently, NMOS and PMOS transistor is the most important device to create the CMOS circuit.

CMOS has been used widely in electronic device, which is many CMOS circuit has been designed such as inverter, logic gate, multiplexer, memory and etc. CMOS is under MOSFET family and it provides both NMOS and PMOS on the same chip. The main reasons for the success of CMOS are low power consumption and good noise immunity [2]. Others are low supply voltage, low leakage current, high speed performance, less transit time and etc [3]. In fact, currently only CMOS technology is used in advanced integrated-circuit (IC).

In this paper, 80nm CMOS inverter with normal standard process device development using Sentaurus Synopsys TCAD software have been analyzed and characterized. The standard process of 90nm CMOS inverter was followed. The performance of these devices has been verified via simulation in operation as a transistor. The process was divided to two main parts; device simulation program and process simulation program. In the device simulation, there were discovered a few difference sub-program that was used to simulate a semiconductor designing characteristics. In the process simulation the program was same as device simulation, while it was used to simulate all the fabrication process in step by step. The classification of the project was in term of mirage fabrication project because all the semiconductor result and it characteristics depend on the computer simulation.

PROCESS FLOW

The process flow for 80nm CMOS device was developed using Sentaurus Synopsys TCAD software with several stages as illustrated in Figure 1. The simulation starts with the bare wafer and finishes with device structure. Implantation, diffusion, etching, growth, and deposition process are simulated on a microscopic level.

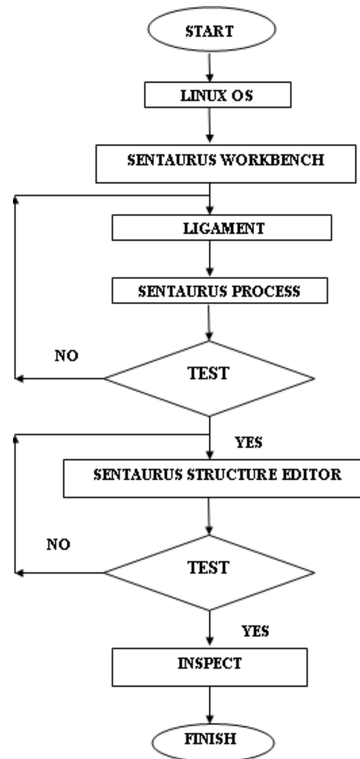

Figure 1: Process flow of Sentaurus Synopsys TCAD

The process flow in this project represents a generic 80 nm technology node and it follows the common CMOS process flow. The major process steps are [4]:

1. Well definition.
2. Gate oxide growth.
3. Polysilicon gate definition.
4. Polysilicon gate reoxidation.
5. Offset spacer creation.
6. Halo implant.
7. Source–drain extension implants.
8. First spike anneal.
9. Spacer creation.
10. Source–drain implants.
11. Second spike anneal.
12. Metallization.

The process start with boron-doped *p*-type silicon as a bare wafer then an oxide layer are grown, followed by applied of photoresist, PR developed, oxide etched, PR removed, phosphorus diffused, field oxide grown, PR applied, PR developed against, oxide etched, PR stripped, PR removed, aluminium film deposited, PR applied against, PR developed and aluminium interconnect etching (metallization). After the final PR stripping, all the NMOS fabrication steps are completed.

All major processing steps are defined as separate local macros. The major process step are defined as well definition (n-well formation), then gate oxide growth in area where silicon nitride was removed (silicon nitride impedes oxide growth). Then polysilicon gate was defined and reoxidation where a high quality thin oxide was grown in the active area. The polysilicon layer was usually arsenic doped (n-type). The photolithography in this step was the most demanding since it required the finest resolution is to create the narrow MOS channels.

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Offset-spacer is to define the n and p diffusion. The process source-drain extension implants, first and second spike anneal in this project were for defined the contact holes which is a thin layer of CVD oxide is deposited over the entire wafer to pattern the contact holes. Etching opens the holes. Last process before run this recipe was metallization. A thin layer of aluminium was evaporated or sputtered onto the wafer used to pattern the interconnection.

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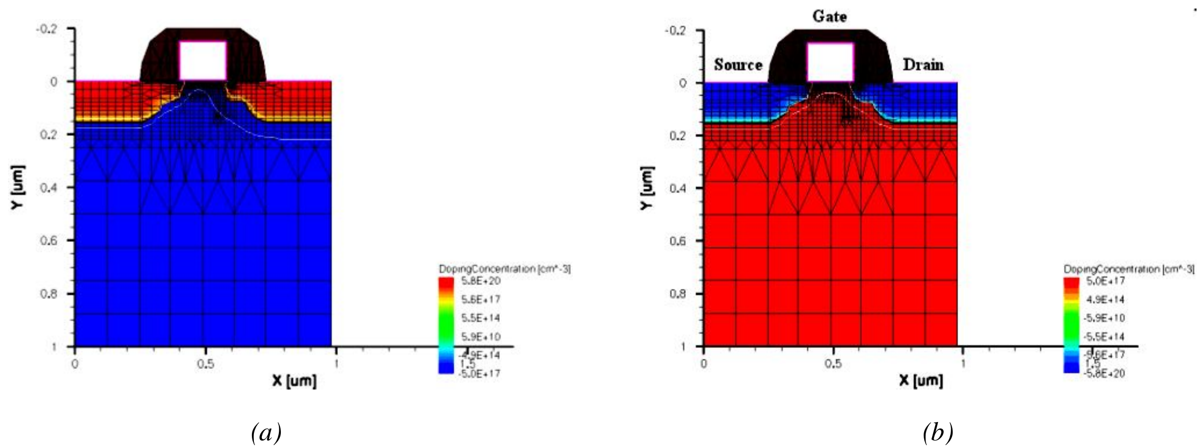
RESULTS AND DISCUSSIONS

The model of 80nm NMOS and PMOS transistor in two dimensions (2D) as shown in Figure 2(a) and 1(b) respectively was the result from the process simulation in the *Tecplot SV*. Both devices were defined from CMOS inverter via Ligament Layout Editor as shown in Figure 3.



(a) *(b)*

Figure 2: a) 80nm NMOS transistor, b) 80nm PMOS transistor

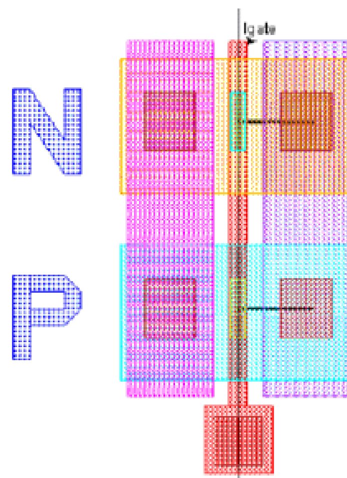
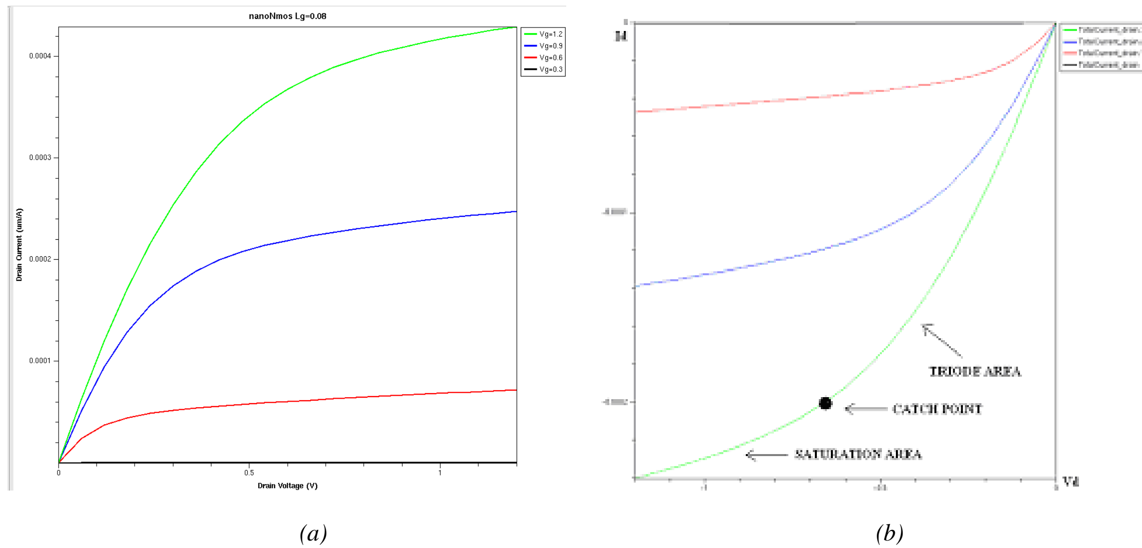


Figure 3: An 80nm CMOS transistor with a parameterized layout

Referring to Figure 3, the two horizontal black lines show the cut lines that define the 2D areas for the NMOS and PMOS devices. The vertical line defines the parameterization; the layout is stretched as a function of the parameter gate length (l_{gate}) [4].

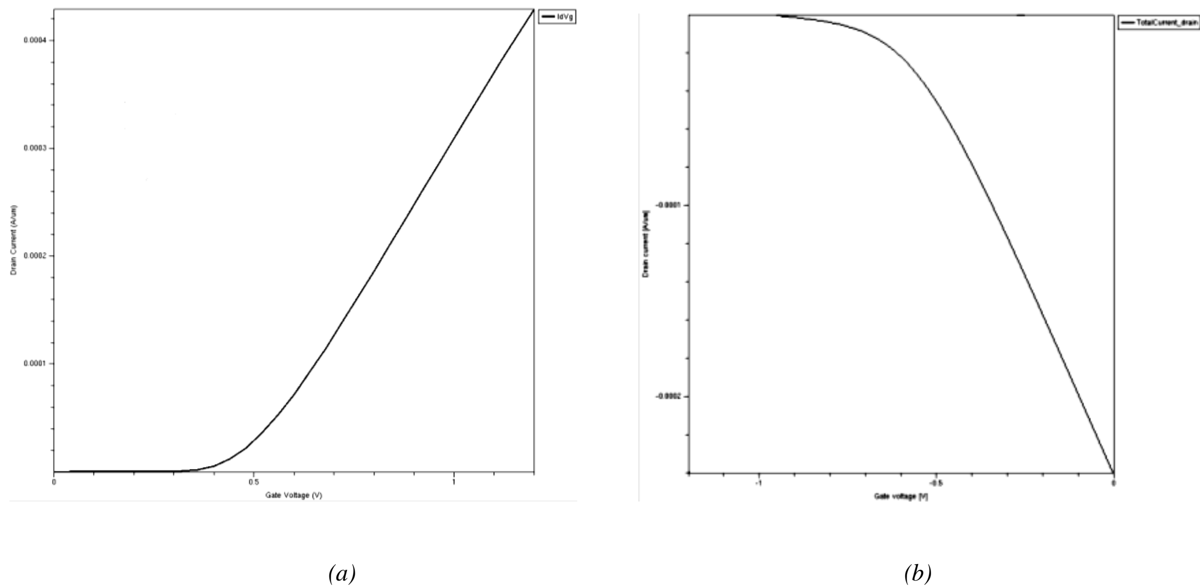
The electrical characteristic of the NMOS and PMOS transistor can be explain by the graph of I_D-V_D and I_D-V_G curve that had run in the *INSPECT* of the Sentaurus WorkBench (SWB). These graphs are illustrated in Figure 4 and 5 respectively. The I_D-V_D characteristics are measured by applying a staircase sweep voltage to the drain

(V_D) of the device and monitoring the drain current. A constant voltage is applied to the gate (V_G) during each sweep, and a group of (I_D-V_D) data curves can be acquired by varying the gate voltage between sweeps. A bias voltage can also be applied to the substrate contact (V_B) and the source is grounded [3].



(a) *(b)*

Figure 4: I_D-V_D characteristics of a) NMOS and b) PMOS transistor



(a) *(b)*

Figure 5: I_D-V_G characteristics of a) NMOS and b) PMOS transistor

For these device simulation of 90nm and 80nm, the *I-V* characteristics was collected in order to determine the analysis. For each of the simulation I_D-V_G curves relevant electrical parameters, the value of threshold voltage (V_T), I_{off} (leakage current) and I_{DSAT} (drain saturation current) are extracted. The I_D-V_D curves obtained in a different applied gate voltage (V_G=0.3 to 1.2V) while the subthreshold I_D-V_G curves measured at V_D=1.2V. The comparison for both NMOS and PMOS device for 80nm and 90nm CMOS inverter were illustrated in Table 1. It was observed that the 80nm NMOS device comprise I_{DSAT}=429.3µA/µm and I_{off} =79.08pA/µm and these values shows much higher value than 90nm device. The percentage of increasing I_{DSAT} for NMOS and PMOS transistor was about 7.1% and 11.4%. Its happened because of the source-drain diffusion can no longer be reduced during fabrication and the poly lines were getting to be quite narrow.

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Meanwhile, an off-state leakage current (I_{off}) of 80nm CMOS transistor is almost twice higher than 90nm CMOS transistor. This shows the smaller gate length of NMOS transistor, the higher leakage current occurred. An ideal MOS transistor only has current flow when it is "on"; when the channel is "off" there was no current. This means that the transistor should consume no power if it is "off". Unfortunately, MOS transistors are not ideal and, as they get smaller, they get less ideal.

Table 1: The comparison between 80nm and 90nm CMOS inverter

Condition	**90nm CMOS inverter**		**80nm CMOS inverter**	
Type	NMOS	PMOS	NMOS	PMOS
V_T	0.518	-0.526	0.499	-0.491
I_{DSAT}	4.008e-04	2.154e-04	4.293e-04	2.400e-04
I_{off}	4.880e-11	1.023e-10	7.908e-11	2.361e-10

The value of V_T (threshold voltage) is the voltage required for MOS transistor device to be operated. The V_T value obtained for 80nm NMOS and PMOS were 0.499V and -0.491V respectively while for 90nm gate length was 0.518V and -0.526V as shown in Table 1.

V_T (the threshold voltage) for a MOS transistor can be defined as the voltage applied between the gate and the source of a MOS device below which the drain-to-source current I_{DS} "effectively" drops to zero [5]. It can be seen that the percentage speed between 90nm and 80nm gate length for NMOS and PMOS transistor was about 3.63% and 6.56%. These are the best value that we have reported. It can be seen that the operation of NMOS transistor is two times faster than PMOS transistor although their size of physical gate length is 80nm. It is because effective mass of hole is greater than electron which means electron have high mobility than hole [6]. A MOS transistor is called a majority carrier device, in which the current in a conducting channel (the region immediately under the gate) between the source and the drain is modulated by a voltage applied to the gate. The majority carriers of an NMOS transistor are the electrons while for PMOS transistor is a holes [7].

Current cannot flow from the drain to the source unless V_{GS} is greater that V_T (device not operated, *cutoff region*). When the applied V_{GS} exceed a critical value, the oxide-layer field begins to draw electrons into the substrate region. It will conducted inversion layer to transfer the electron from the source to drain. I_D will flow and device start operated when V_{GS} increase with conductivity of the inversion layer channel. Note that, the inversion layer just at the surface of the substrate (along the gate length) [7]. This shows that the shorter gate length helps the transfer of electron more strongly from source to drain. This clarify by reduction in gate length provides a shorter transit time (during transferred electron along inversion layer) and hence a faster device to operated. In addition, the size is reduced due to smaller gate length.

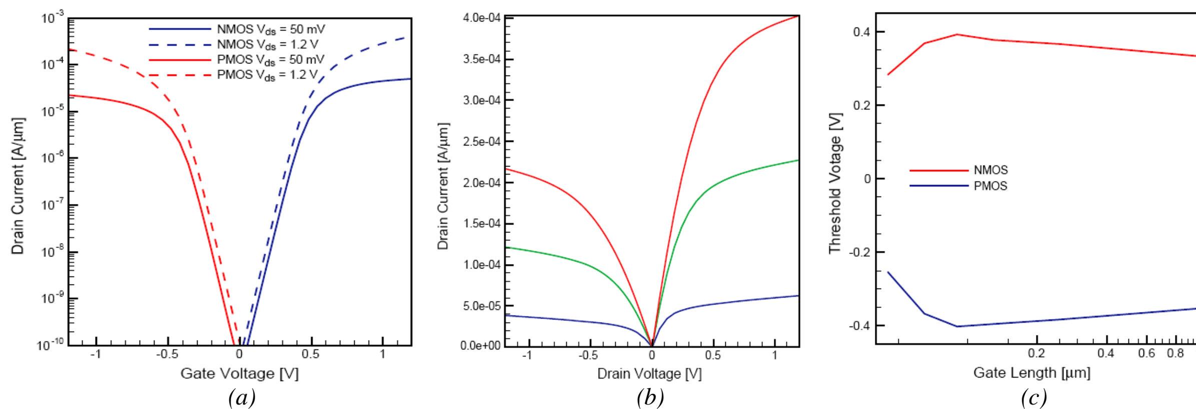

Figure 6: I-V characteristics of 80nm CMOS transistor

Figure 6(a) illustrated the drain current as a function of gate voltage for the 80nm gate length of CMOS devices simulated with Sentaurus Device; lower curves (solid lines) are for a drain bias of 50mV and upper curves (dashes) are for 1.2V. While Figure 6(b) shows the drain current as a function of drain voltage. The gate bias for curves is 0.6V, 0.9V, and 1.2V. Whereas in Figure 6(c) shows the threshold voltage of 80nm CMOS device as a function of gate voltage.

CONCLUSIONS

The simulation of process and device development for gate length of 80nm CMOS inverter has been achieved. It has been demonstrated that the percentage speed between 90nm and 80nm gate length for NMOS and PMOS transistor was about 3.63% and 6.56% and the percentage of increasing I_{DSAT} for NMOS and PMOS transistor was about 7.1% and 11.4%. It was observed that the 80nm NMOS device has lower V_T and higher I_{DSAT} and I_{off} than 90nm device. Further study will look onto lower technology node with standard CMOS process flow.

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