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FORMATION OF ZrO_2 THIN FILMS BY THERMAL OXIDATION OF SPUTTERED Zr ON Si AND SiC SUBSTRATES

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UNIVERSITI SAINS MALAYSIA

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FORMATION OF ZrO_2 THIN FILMS BY THERMAL OXIDATION OF SPUTTERED Zr ON Si AND SiC SUBSTRATES

by

TEDI KURNIAWAN

Thesis submitted in fulfillment of the requirements

for the Degree of

Master of Science

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DECLARATION

I declare that this thesis is the result of my own research, that is does not incorporate without acknowledgement any material submitted for a degree or diploma in any university and does not contain any materials previously published, written or produced by another person except where due reference is made in the text.

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LIST OF ABREVIATION

AFM	:	Atomic Force microscopy
DC	:	Direct current
EDS	:	Energy dispersive spectroscopy
FESEM	:	Field emission scanning electron microscopy
FTIR	:	Fourier transform infrared spectroscopy
HRTEM	:	High resolution transmission electron microscopy
ICDD	:	International Conference for Diffraction Data
IL	:	Interfacial layer
ITRS	:	International technology roadmap for semiconductor
LCR	:	Inductance-capacitance-resistance
m-ZrO_2	:	Monoclinic zirconium dioxide
MOS	:	Metal oxide semiconductor
MOSFET	:	Metal oxide semiconductor field effect transistor
STD	:	Slow trap density
SPA	:	Semiconductor parameter analyser
t-ZrO_2	:	Tetragonal zirconium dioxide
ToF-SIMS	:	Time-of-flight secondary ion mass spectroscopy
XRD	:	X-ray diffraction
XRR	:	X-ray reflectometry

LIST OF SYMBOLS

A	:	Capacitor Area (cm^2)
C_{ox}	:	Oxide capacitance (pF)
C_{tot}	:	Total capacitance (pF)
C_{IL}	:	IL capacitance (pF)
C_{ZrO_2}	:	ZrO_2 capacitance (pF)
d	:	Oxide thickness (nm)
d_{ZrO_2}	:	ZrO_2 thickness (nm)
d_{IL}	:	IL thickness (nm)
D_{it}	:	Interface trap density (eV^{-1} cm^{-2})
E_B	:	Electric field breakdown (MV cm^{-1})
E_C	:	Valence-band edge (eV)
E_F	:	Fermi energy (eV)
E_V	:	Valence-band edge (eV)
I	:	Current (A)
J	:	Leakage current density (A cm^{-2})
k	:	Dielectric constant
q	:	Angle
ε_o	:	Permittivity
F_B	:	Barrier height
q	:	Charge (C)
Q_{eff}	:	Effective oxide charge (cm^{-2})
V	:	Voltage (Volt)
V_B	:	Breakdown voltage (V)
V_{FB}	:	Flatband Voltage (V)

LIST OF PUBLICATIONS

1. Tedi Kurniawan, Foong Chia Choon, Cheong Kuan Yew, Khairunisak Abdul Razak, Zainovia Lockman, Ahmad Nuruddin, Eiichiro Matsubara. (2007) Physical characterization of ZrO_2 thin films formed by thermal oxidation of sputtered Zr on Si substrate. Proceeding. The 4th International Conference in Technological Advances of Thin Films and Surface Coating, 13/16 July 2008, Singapore.

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PEMBENTUKAN LAPISAN NIPIS ZrO_2 MELALUI PENGOKSIDAAN HABA Zr YANG TELAH DIPERCITKAN DI ATAS SUBSTRAT Si DAN SIC

ABSTRAK

Lapisan nipis ZrO_2 untuk aplikasi get dielektrik telah dibentuk di atas substrat Si dan SiC dengan menggunakan kombinasi proses pemercitan logam dan pengoksidaan haba. Kesan suhu pengoksidaan (500-800^oC), masa pengoksidaan (5-60 min) dan masa pemercitan (30-120 s) telah dikaji ke atas substrat Si jenis –p atau –n. Sementara itu, kesan suhu penyepuh lindapan (600-900^oC) di dalam persekitaran Ar telah dikaji ke atas substrat 4H-SiC jenis –n. Proses pemercitan telah dijalankan dengan mengawal tekanan asas, tekanan kerja dan kuasa DC pada at 4.4×10^{-5} Torr, $3 \sim 6 \times 10^{-3}$ Torr dan 250 Watt. Sementara itu, untuk proses pengoksidaan dan penyepuh lindapan, kadar aliran Ar dan O_2 dikekalkan pada 150 ml/min. Kesan suhu dan masa pengoksidaan telah dikaji ke atas Si jenis –p yang telah dipercitkan Zr selama 15-s. Analisis *high resolution transmission electron microscopy* (HRTEM) dan *Fourier transform infrared spectroscopy* (FTIR) menunjukan 3.5 nm ZrO_2 dan 3.5 nm lapisan antarmuka (SiO_x dan $Zr_xSi_yO_z$) telah terbentuk pada suhu pengoksidaan 500^oC selama 60 min. Manakala, profil *time-of-flight secondary ion mass spectroscopy* (ToF-SIMS) menunjukan $Zr_xSi_yO_z$ akan terbentuk selepas pengoksidaan selama 15 min dan peningkatan sifat ketumpatan kebocoran arus (J), kegagalan voltan (V), dan kegagalan medan elektrik (I) telah ditunjukan oleh sampel yang dioksidakan selama 15-60 min, dan nilai optima telah dicapai pada sampel yang dioksida selama 30 min. Nilai pemalar dielektrik oksida (k) yang dihasilkan adalah 4.2 hingga 5.3. Pemerhatian ke atas kesan masa pemercitan pada subsrat Si tipe –n telah dijalankan proses selepas pengoksidaan pada 500^oC selama 15 min. Fenomena pelecuhan telah diperhatikan pada sampel yang dipercitkan selama 90 dan 120 s, sementara pemercitan Zr pada 60-s mempunyai sifat elektrik pelih baik berbanding dengan sampel yang lain. k yang dihasilkan adalah 9.4 hingga18. Pemerhatian ke atas kesan suhu sepuh lindap telah dilakukan ke atas substrat 4H-SiC jenis –n yang telah dipercitkan Zr selama 60 s dan dioksidakan pada suhu 500^oC selama 15 min. Proses penyepuh lindapan telah menurunkan J sebanyak turutan magnitud 2. Selain itu, V_B dan E_B juga turun. k yang dihasilkan adalah diantara 22 sampai 80.

FORMATION OF ZrO_2 THIN FILMS BY THERMAL OXIDATION OF SPUTTERED Zr ON Si AND SiC SUBSTRATES.

ABSTRACT

ZrO_2 thin films for gate dielectric application has been formed on Si and SiC substrates using a combination of metal sputtering and thermal oxidation process. Effects of oxidation temperature (500-800°C), oxidation time (5-60 min) and sputtering time (30-120 s) have been studied on p- or n-type Si substrate. Meanwhile, effects of annealing temperature (600-900°) in Ar ambient were studied on n-type 4H-SiC substrate. Sputtering process has been conducted by regulating base pressure, working pressure and DC power at 4.4x10^{-5} Torr, 3~6x10^{-3} Torr and 250 Watt. Meanwhile, for oxidation and annealing process, Ar and O_2 flow rate were maintained at 150 ml/min. The effects of oxidation temperature and oxidation time have been studied by oxidizing 15-s sputtered Zr on p-type Si. High resolution transmission electron microscopy (HRTEM) and Fourier transform infrared spectroscopy (FTIR) analyses showed that 3.5 nm ZrO_2 and 3.5 nm interfacial layers (IL) in a mixture of SiO_x and $Zr_xSi_yO_z$ were formed from oxidation at 500°C in 60 min. Furthermore, time-of-flight secondary ion mass spectroscopy (ToF-SIMS) profiles show that $Zr_xSi_yO_z$ formed after 15 min oxidation time and interface of ZrO_2/IL contain Si-rich composition. Improvement in leakage current density (J), voltage breakdown (V_B) and electric field breakdown (E_B) properties have been shown by 15-60 min oxidation samples, with the optimum value has been reached by 30-min oxidized sample. Oxide dielectric constant (κ) from this work ranges from 4.2 to 5.3. Observation on the effects of sputtering time on n-type Si was conducted after oxidation at 500°C in 15 min. Blistering phenomenon was observed at 90 and 120-s sputtered samples, while 60-s sputtered Zr has better electrical properties compared with the others. κ value from this work ranges from 9.4 to 18. Observation on the effects of annealing temperature on n-type 4H-SiC substrate has been conducted after 60-s sputtered Zr oxidized at 500°C in 15 min. Annealing process has reduced J as high as 2 order of magnitude. On the other hand, V_B and E_B have also been reduced. k value from this work ranges from 22 to 80.

CHAPTER 1

INTRODUCTION

1.1 Background and Problem Statement

Silicon (Si) material has dominated the electronic industry for many decades. The ability to be produced in a very large single crystal without structural defects, very low and controlled doping level and the ability to grow a native oxide (SiO_2) with good dielectric properties, are the advantages that makes Si-based semiconductor dominated this industry since 1960s (Chante, 1998). However, the requirements of semiconductor for many applications today, such as higher blocking voltages, switching frequencies and efficiency, are at a point that makes Si-based power devices unable to met these demands (Dimitrijev, 2003). Therefore, many alternative solutions have been investigated in order to improve the performance of power devices. One of the most promising approaches is to replace Si with wide bandgap (WBG) semiconductors such as Silicon Carbide (SiC), Gallium Arsenide (GaAs), Gallium Nitride (GaN), or Aluminum Nitride (AlN) (Ozpineci, 2003).

SiC has several unique properties that make them as the choice in developing high power devices compared to Si. The bandgap of SiC is almost three times higher compared to Si. This causes the increase in current due to thermal generation to be much lower than in Si. The breakdown field of SiC is almost nine times higher, which make a similar device built in SiC will have nine times the breakdown voltage rating of the Si.

The thermal conductivity of SiC is over three times that of Si, which would allow dissipated heat to be more readily extracted from the devices (Richmond, 2004).

Although SiC offers substantial advantages over Si, in terms of physical properties and thermal stability, it cannot compete with Si devices in the areas of low cost, functional density, and moderate temperature applications (Dimitrijev, 2003). The most critical and limiting aspect of SiC technology is the material itself. Power devices require low defect, large-area substrates, and high quality low defect uniform epilayers. Micropipes, common crystalline defect in SiC, have been present in nearly all SiC wafers. This defect penetrates the entire crystal along the *c*-axis and caused critical flaws in SiC devices. Recent advanced in physical vapor transport (PVT) for SiC bulk crystal growth technique has led to a continuous reduction in the micropipes density over the past several years (Ohtani, 2008). In 1996, the lowest defect that can be reached in average wafers was $3.5/cm^2$ (Burke, 1996). Meanwhile in 2007, Cree announced that they had demonstrated producing 100 mm (3 inch) diameter of n-type SiC wafer with zero-micropipe (ZMP) defect (www.Cree.com).

In the other side of electronic industry improvement, the continued scaling down in Si-based metal-oxide-semiconductor field effect transistor (MOSFET) technology, as the key component in integrated circuit, has pushed the SiO_2 gate oxide thickness to the order of nanometers, which lead to higher leakage currents and reliability problem. As specified in the latest International Technology Roadmap for Semiconductror (ITRS) website (accessed April 2009), from year 2008, Si-based MOSFETs will require gate dielectrics with thickness below 1.2 nm. This phenomenon will caused the leakage

current flowing through the transistor to be so high since the dominant transport mechanism at this such thin oxide layer (below 3 nm) is direct tunneling of electrons or holes through the oxide (Wallace, 2002). The oxide reliability also becomes another issue for very thin gate oxide since the high leakage current would create defects in the SiO_2 layer or at SiO_2/Si interface. When the critical density of defect is reached, breakdown of the gate layer occurs, resulting in the failure of the device. For very thin layer of SiO_2 this gate dielectric breakdown is not expected to reach 10 years at device operating condition (Ray, 2006). Based on the reasons above, high dielectric constant (high-κ) gate oxide has been studied as the alternative gate oxide for SiO_2. The use of high-κ materials allowed the increase in physical thickness and reduces direct leakage current. By maintaining the low equivalent thickness (EOT), the reduction in device dimensions as required to meet Moore's Law can be achieved (www.intel.com).

Various high-κ materials has also attraceted a lot of interest in metal–oxide–semiconductor (MOS) capacitors prepared on SiC. A high quality gate oxide with low density of interface states, fixed oxide charges, and oxide traps will determine the successful of SiC-substrate as high-power and high-frequency application (Fissel, 2006). Silicon dioxide (SiO_2), as native oxide of SiC fabricated by thermal nitridation, has revealed excellent properties for this purpose. However, even if SiO_2/SiC structures with low enough defect and trap densities can be obtained, the use of SiO_2 as gate oxide for SiC-based MOS structure still have problem due to its low dielectric constant. The maximum blocking voltage of such structures is limited by the gate oxide breakdown instead of SiC breakdown; as the electric field in the oxide is larger than that in SiC by a

factor of 2.5, which is equal to the ratio of their dielectric constants (Bondoux, 2005). This removes the main advantage of the high breakdown field of SiC (10× that of Si) because the maximum voltage of SiC power devices is limited by the field in the dielectric, not by the breakdown of the semiconductor. Therefore, alternative gate oxide with a higher dielectric constant (high-***k*** dielectric) became an alternative way to solve the problem.

Zirconium dioxide (ZrO_2) is one of the attractive candidates for Si and SiC-based gate oxide due to its excellent bulk properties: high-***k*** value (ε_r=20-25), wide band gap (4.7-5.8 eV) and good thermal stability in directly contact with Si (Wong and Iwai, 2006). Numerous works have been done in depositing ZrO_2 on Si substrate. Reactive magnetron sputtering (Zhu, 2005), atomic layer deposition (ALD) (Cassir, 2002), pulse laser deposition (PLD) (Filipescu**,** 2007)**,** metal-organic chemical vapor deposition (MOCVD) (Wu, 2003), and sol-gel processing (Yu, 2002) are some techniques that have been used. As happened in depositing other high-κ materials, formation of interfacial leyer(s) such as silicon dioxide (SiO_2) or silicon oxide (SiO_x) (Kim, 2006), silicate ($Zr_xS_yO_z$) and silicide (Zr_xSi_y) (Gutowski, 2002) is commonly happened. The total dielectric constant of the oxide is reduced by the interfacial layers since its κ values are lower than that of ZrO_2 (e.g., SiO_2 = 3.9, Zr-silicate ≈ 7-12 (Filipescu, 2004)). This will then deteriorate the merit of using ZrO_2 as high-κ gate oxide. One of the examples is the formation of SiO_2 interfacial layer during ZrO_2 deposition by RF sputtering (Ma, 2007). The increase of SiO_2 interfacial layer thickness (4-10 nm) as the effect of O_2 partial

pressure has decreased the accumulation capacitance and the total κ value has been decreased from 20 to less than 10.

Although these interfacial layers can decrease the overall κ value of the oxide, its existence can reduce the leakage current density of the MOS structure. Choi (2005) reported that the increase of interfacial layer thickness (from ~2 nm to ~30 nm) after annealing of 2.8 nm sputtered ZrO_2, has reduced the leakage current density by 2 orders of magnitude. Formation of Zr-free high quality SiO_2 interfacial layer was suggested as the barrier that reduced this leakage current. The reduction of leakage current density as the effect of interfacial layer formation was also reported in HfO_2/Si structure (Callegari, 2002). HfO_2 sputtered on HF last Si has higher leakage current density of about 2 orders of magnitude compared with sample prepared on RTO (rapid thermal oxidation), where a thin oxide layer (SiO_x) was present. This result suggested that thin SiO_x film would be needed to help nucleation of low leakage HfO_2 film on silicon substrate. In another report, Paskaleva (2006) also suggested that high leakage current in high-k materials generated by strong electron-phonon interaction, can be suppressed by the presence of Hf-silicate layer.

In the case of ZrO_2 deposition on SiC substrate, the information found is very limited. The only reference found is Karlsson (2007), which reported that SiO_2 interfacial layer also formed during ZrO_2 deposition by chemical vapor deposition (CVD) process on Si-rich SiC (0001). Heterogeneous layer was forms after annealing to 1000 °C because of the ZrO_2 decomposition and leads to form regions with t-ZrO_2

remnants, metallic Zr silicide and Si aggregates. No electrical result was reported from this work.

Based on the discussion above, further understanding of ZrO_2 and interfacial layers formation as well as their effects to the electrical properties would be needed to provide better knowledge in producing high quality gate oxide layer on Si and SiC substrate. A novel fabrication process in which Zr directly deposited on Si or SiC substrate continued with oxidation process to form ZrO_2 is an interesting topic to be proposed since this process can explore the effects of sputtering conditions (power, pressure, gas, etc), and also oxidation condition (temperatures, dwell time, gas flow rate, type of gases, kinetic growth, etc) in the formation as well as the properties of ZrO_2 and its interfacial layers. Hsieh (2006) has used the same process to study the thermal stability of SiO_2 layer as an oxidation barrier in the Zr (100Å)/SiO_2 (40Å)/Si structure during oxidation at temperature range of 600-900^oC. Monoclinic and orthorhombic ZrO_2 was form in this process. Meanwhile, SiO_2 is found had no barrier function for the structure as it decomposed and allowed Zr atoms to occupy some of Si lattice to form $ZrSi_xO_y$ interfacial layer. The same process also has been used by Kim (2006) to form $ZrSi_xO_y/ZrO_2$ on Si substrate. Further annealing under oxidizing ambient (N_2O and O_2), results in the additional interfacial layer, causing the degradation of equivalent oxide thickness (EOT) property. On the other hand, annealing under N_2 ambient did not show any interfacial layer formation. Nagasato (2005) also used the same process to produce ultrathin ZrO_2 (from 3.5 nm Zr) from low temperature oxidation (200-600^oC for 10 minutes). Dielectric constant of ~20 with 0.9 nm interfacial layer was reached from the

oxidized sample at 300^oC. No degradation of leakage current characteristics was observed after annealing in nitrogen ambient at 850^oC for 30 min. These examples would give consideration that combination of metal sputtering and thermal oxidation method is an effective way in producing high-κ gate oxide, even with the oxidation process was done at lower temperature.

In this work, investigation of sputtering parameter and oxidation parameters will be carried out in order to study the mechanism of ZrO_2 and interfacial layers formation on Si and SiC substrate. Physical, chemical and electrical properties of the film(s) will be analyzed.

1.2 Objectives of the Research

The main objective of this research is to form ZrO_2 thin films on Si and SiC substrates. With this main objective, the following aspects were studied:

- Effect oxidation temperature (200-500^oC and 500-800^oC), oxidation time(5-60 min) and sputtering time (15-60 s) in the formation of ZrO_2 on Si substrate
- Effect of annealing temperature (600-900^oC) under argon gas (Ar) ambient in the formation of ZrO_2 on SiC substrate
- the properties of ZrO_2 and the prospect of the use of ZrO_2 as the dielectric material in MOS-based devices

1.3 Scope of the Study

In this study, combination of metal deposition and thermal oxidation process is selected to produce zirconium dioxide (ZrO_2) thin films on Si and SiC substrate. The effects of various parameters in the formation of ZrO_2 thin films, such as sputtering time, oxidation temperature and annealing temperature will be studied.

Characterizations of physical and chemical properties of ZrO_2 thin films were conducted by using x-ray diffraction (XRD), Fourier transform infrared spectroscopy (FTIR), field emission scanning electron microscopy (FESEM), energy dispersive spectroscopy (EDS), high resolution transmitting electron microscopy (HRTEM), atomic force microscopy (AFM) and time of flight – secondary ion mass spectroscopy (ToF-SIMS). Meanwhile, for the electrical properties of the films, semiconductor parameter analyzer (SPA) and LCR meter were employed.

1.4 Thesis Organization

This thesis is organized in five chapters. The first chapter provides background and problem statement, research objective, and also scope of the study. The second chapter provides theoretical background of the research. The next chapter (third chapter) presents the methodology of the research. The fourth chapter presents results and discussion of the finding. And at the last, the fifth chapter presents conclusion and suggestion for further work.

CHAPTER 2

LITERATURE REVIEW

2.1 MOS Structure

2.1.1 Introduction

Metal-oxide-semiconductor (MOS) is the core structure of the most widely used type of transistor, known as metal-oxide-semiconductor field-effect-transistor (MOSFET). Figure 2.1 shows the structure of MOS, which consists of a metal layer as gate electrode, an oxide layer as gate dielectric, and semiconductor layer. The MOS structure is generally made of Si semiconductor, where the gate dielectric of (SiO_2) is grown on it by thermal oxidation process [Singh, 2001]. Si semiconductor is usually prepared by Czochralski-crystal growth method because of its advantage for the formation of large Si wafers[Chen, 1999].

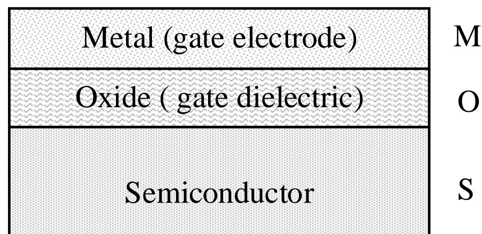

Fig. 2.1: Schematic of a MOS structure.

The gate dielectric insulates gate electrode from semiconductor. SiO_2, which commonly used as the gate dielectric, can be grown by dry (O_2) or wet (H_2O) oxidation. Properties such as uniformity of the thickness, low defect density, low fixed charge and interface state density at the dielectric-silicon interface, and also small roughness at the interface are required for this gate dielectric, since it would determine the properties of MOS structure [Chen, 1999]. Gate electrode that made from metal is usually used for evaluation of a capacitor structure. But in modern MOS technology, gate is also made from heavily doped polycrystalline silicon (poly-silicon) [Misra, 2007].

2.1.2 MOS Operation Principle

The energy band diagram of an ideal MOS structure without bias, for both p-type and n-type is presented in Fig. 2.2, where χ and χ_I are the electron affinities for semiconductor and insulator, and Ψ_{Bn}, Ψ_{Bp}, ϕ_n, ϕ_p are the Fermi potentials with respect to the midgap and band edges for the respective n and p-type semiconductor [Sze, 2006].

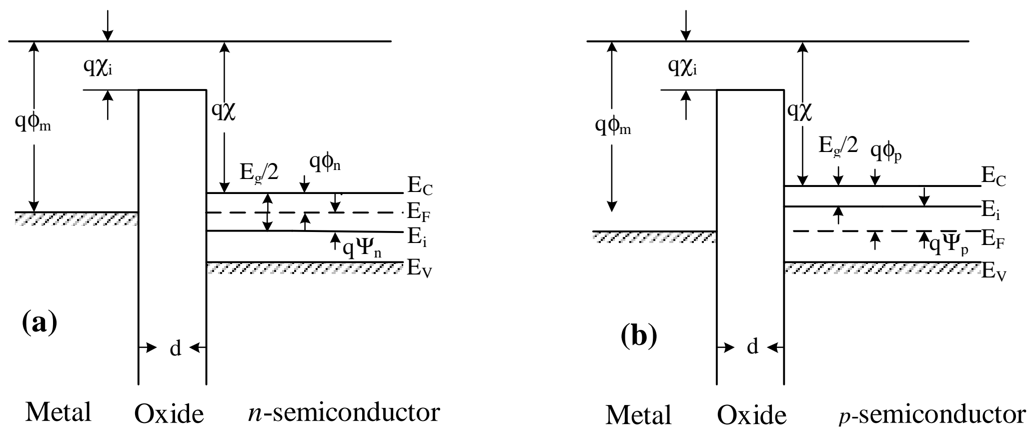

Fig. 2.2: Energy-band diagram of ideal MOS capacitor at equilibrium (V=0). (a) *n*-type semiconductor, (b) *p*-type semiconductor [Sze, 2006].

When an ideal MOS capacitor is biased with positive or negative voltages, there are three cases that basically exist at the semiconductor surfaces [Liu, 2002]. Consider the semiconductor is p-type, when a negative voltage ($V<0$) is applied to the metal plate, the valence-band edge E_v bends upward near the surface and is closer to the Fermi level (Fig. 2.3a). For an ideal MOS capacitor, no current flows in the structure (or $dE_F/dx=0$), so the Fermi level remain flat in the semiconductor. Since the carrier density depend exponentially to the energy difference (E_F-E_V), this band bending causes ac accumulation of majority carriers (holes) near the semiconductor surface, resulting an *accumulation* case. When a small positive voltage ($V>0$) is applied, the bands bend downward, and the majority carriers are depleted (Fig. 2.3b), resulting a *depletion* case. And when a larger positive voltage is applied, the bands bend even more downward so the intrinsic level E_i at the surface crosses over the Fermi level E_F (Fig. 2.3c). At this point the number of minority carriers (electrons) at the surface is larger than the majority carriers (holes), which make the surface inverted. This is called *inversion* case. Similar results can be obtained for the n-type semiconductor, but by changing the polarity of the voltage.

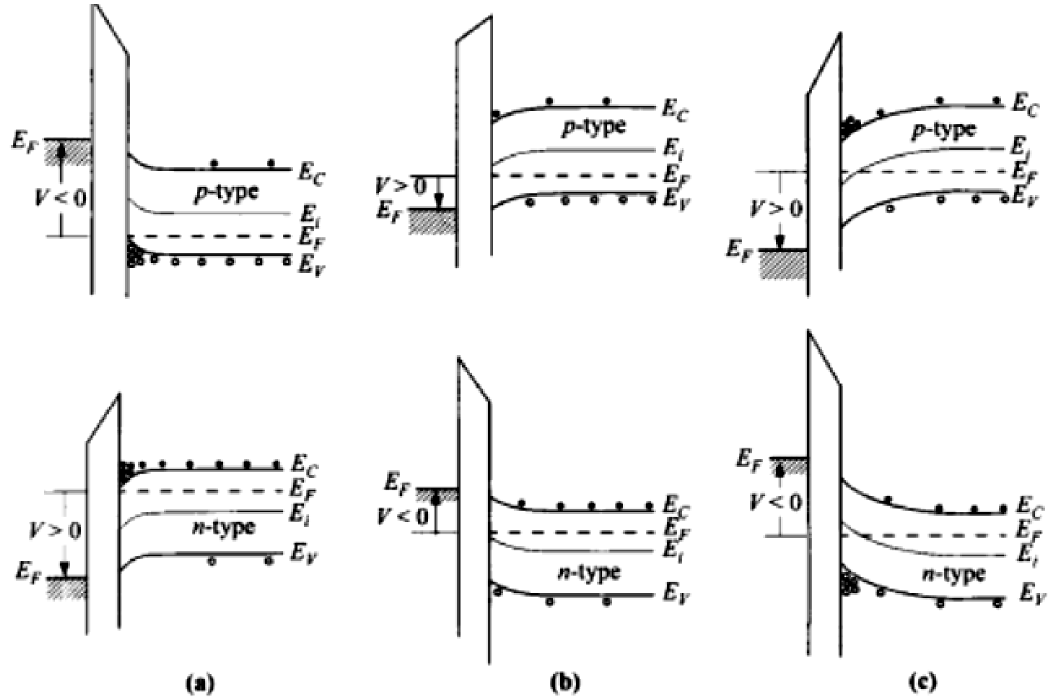

Fig. 2.3: Energy-band diagram for ideal MOS capacitor under different bias, for the condition of: (a) accumulation, (b) deplation, and (c) inversion. Top/bottom figures are for p-type/n-type semiconductor substrates [Sze, 2006].

2.1.3 Capacitance-Voltage (C-V) Characteristics of a MOS Structure

An important consideration of the MOS structure is the capacitance as a function of applied voltage. In the C-V measurements, a small ac signal is applied to obtain the capacitance at the bias applied. The capacitance of the MOS structure is the series combination of the oxide capacitance C_{ox} and the semiconductor capacitance C_s, as shown in Fig. 2.4. Meanwhile, C_s is consist of hole capacitance (C_p), bulk capacitance (C_b), interface trap capacitance (C_{it}) and electron capacitance (C_n) [Schroder, 2005]. The MOS (C_{mos}) capacitance can be expressed by Eq. 2.1:

$$C_{mos} = \frac{C_{ox} C_s}{C_{ox} + C_s} \tag{2.1}$$

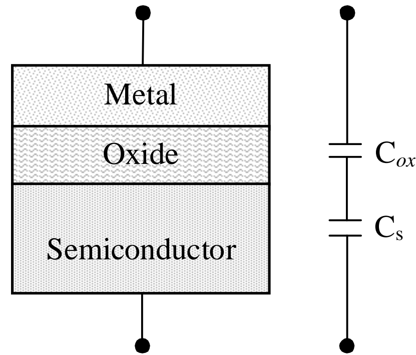

Fig. 2.4: A simple equivalent circuit of the MOS capacitor.

The three important regimes of accumulation, depletion, and inversion are reflected in C-V characteristics (Fig. 2.5) [Liu, 2002]. In the accumulation region (negative V_G), holes are accumulated at the surface and make hole capacitance in semiconductor (C_s) become very high approaching a short circuit condition. Hence, the C_s is shorted and the overall capacitance is referred to oxide capacitance (C_{ox}). As in the positive bias, channel is depleted of holes, C_b and C_{it} are dominated. The total capacitance is then combination of C_{ox} in series with C_b and C_{it}. At the inversion condition, C_n is dominates because of the electron charge density (Q_n) is very high. If the Q_n can follow the ac voltage, then the circuit will increase to C_{ox} level again (as shown in low frequency curve). When the Q_n is unable to follow the ac voltage, then result will be as shown in high frequency curve [Schroder, 2005].

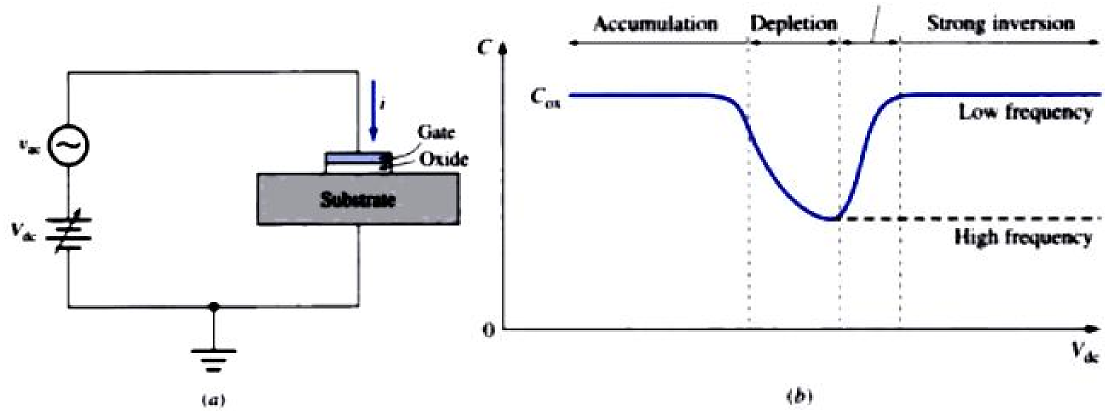

Fig. 2.5: (a) Circuit for measuring capacitance of a MOS capacitor, (b) Capacitance-voltage characteristic of a MOS capacitor [Sze, 2006].

2.2 Silicon and Silicon Carbide Semiconductors

2.2.1 Crystal Structures

Silicon belong to group IV in the periodic table and crystallizes in the diamond cubic structure with lattice constant of a = 5.43Å (Fig. 2.6) [Dwbrowski, 2000]. Commercial available silicon crystals are most frequently grown in (100) plane. Pure silicon is a good electrical insulator at room temperature. To decrease its resistivity, dopants are usually added. Elements of Group III of the Periodic Table (such as boron, aluminum, or gallium) will make silicon to become p-type, which positively conducting via a hole mechanism. Meanwhile, adding elements of Group VI (such as phosphorus, antimony, or arsenic) will add free electrons to the material and make silicon to become n-type, as it is negatively conducting [Mcguire, 1988].

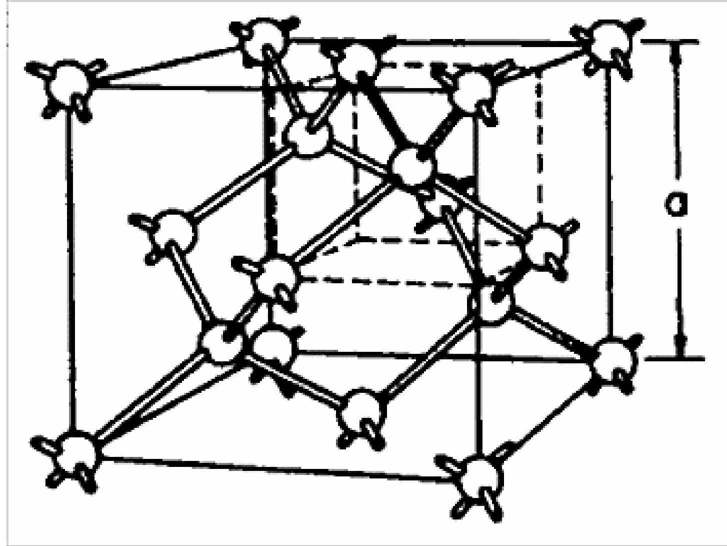

Fig. 2.6: Silicon structure [Dwbrowski, 2000].

Silicon carbide (SiC) occurs in many different crystal structures, called polytypes. There are over 200 known polytypes of SiC, but only a few are grown in a reproducible form for use as an electronic semiconductor. The most common polytypes of SiC are 3C-SiC, 4H-SiC, 6H-SiC and [Shur, 2006]. 3C-SiC, also referred as β-SiC, is the only form of SiC with a cubic crystal lattice structure. 4H-SiC and 6H-SiC are only two of many possible SiC polytypes with hexagonal crystal structure. Different polytypes of SiC are composed of different stacking sequences of Si-C bilayers (also called Si-C double layers), where each single Si-C bilayer can be viewed as a planar sheet of silicon atoms coupled with a planar sheet of carbon atoms. The plane formed by a bilayer sheet of Si and C atoms is known as the basal plane; while the crystallographic c-axis direction, also known as the stacking direction or the [0001] direction, is defined normal to Si-C bilayer plane [Neudeck, 2000]. Figure 2.7 shows the stacking sequence of 6H-

SiC polytype, which requires six Si-C bilayers to define the unit cell repeat distance along the c-axis [0001] direction.

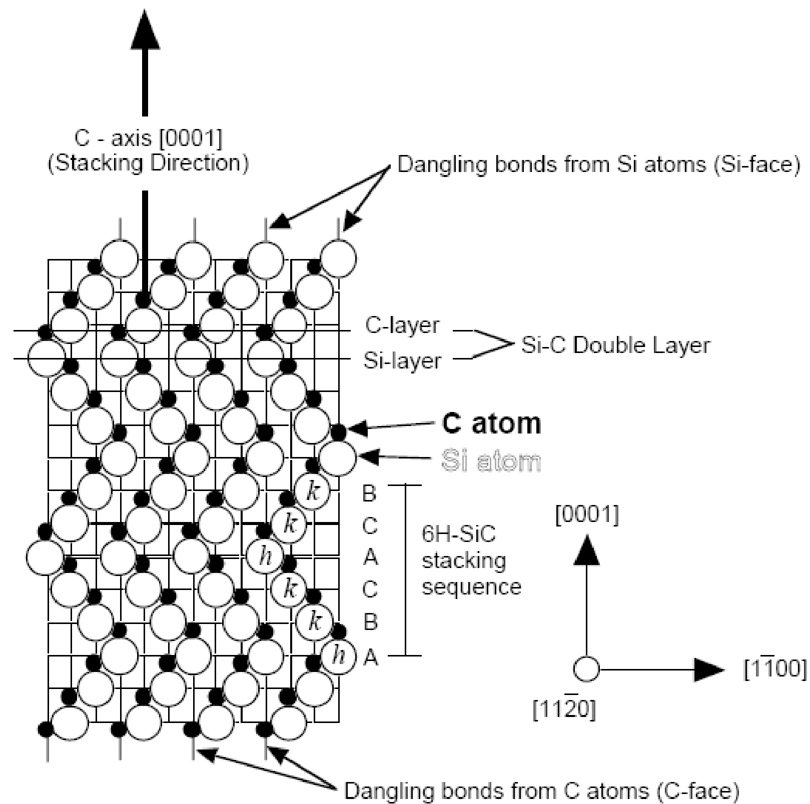

Fig. 2.7: Schematic cross-section { (1120) plane } of the 6H-SiC polytype [Neudeck, 2000].

SiC is a polar semiconductor across the c-axis, in that one surface normal to the c-axis is terminated with silicon atoms while the opposite normal c-axis surface is terminated with carbon atoms. As shown in Fig 2.7, these surfaces are typically referred to as “silicon face” and “carbon face” surfaces, respectively [Neudeck, 2000]. If we consider the locations of the carbon atoms within a bilayer these form a hexagonal crystal lattice structure, labeled "A" in the figure. The next bilayer then has the option of

positioning its carbon atom in the "B" or the "C" lattice sites. It is this stacking sequence that determines the material polytype. Stacking sequence of three common SiC polytypes is presented in Fig.2.8.

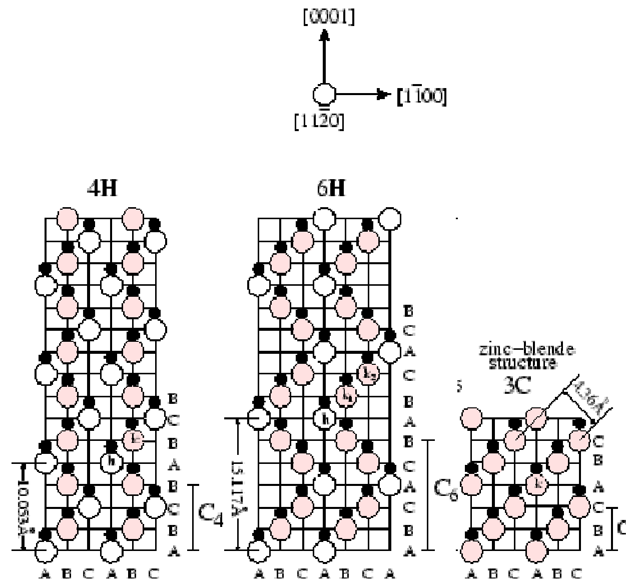

Fig. 2.8: Stacking sequences for different SiC polytypes in the [1120] plane [Powell, 2002].

The main n- and p-type dopants for SiC are nitrogen and aluminum [Powell, 2002]. These are preferred because they create relatively shallow donor and acceptor levels in the SiC bandgap.

2.2.2 Application and Benefit of SiC Electronics

SiC has several unique properties that make them as a potential semiconductor for high performance power devices with the capability of operating at high temperature. Comparison of SiC properties with Si is shown in Table 2.1. Its breakdown field is five times higher than Si, and its bandgap is approximately three times larger than Si. The

wide-bandgap, 3.08 eV for 6H-SiC, allows devices to operate at higher junction temperatures. This capability can be expected to improve cooling efficiency, reduce cooling requirements, improve reliability, and increase current density.

Table 2.1: Comparison of SiC Polytypes with Silicon at 300 K [Neudeck, 2000; Shur 2006].

Property	**Si**	**4H-SiC**	**6H-SiC**	**3C-SiC**
Bandgap (eV)	1.1	3.28	3.08	2.35
Relative dielectric constant	11.9	9.76	9.66	9.72
Breakdown field $N_D = 10^{17}$ cm^{-3} (MV/cm)	0.6	//c-axis: 3.0	// c-axis: 3.2 | c-axis: > 1	> 1.5
Thermal conductivity (W/cm-K)	1.5	3 - 5	3 - 5	3 - 5
Intrinsic carrier concentration (cm^{-3})	10^{10}	~ 10^{-7}	~ 10^{-5}	~ 10
Electron mobility @ $N_D = 10^{16}$ cm^{-3} (cm^2/V-s)	1200	//c-axis: 800 | c-axis: 800	//c-axis: 60 | c-axis: 400	750
Hole mobility @ $N_A = 10^{16}$ cm^{-3} (cm^2/V-s)	420	115	90	40
Saturated electron velocity (10^7 cm/s)	1.0	2	2	2.5
Donor dopants & Shallowest ionization Energy (meV)	P: 45 As: 54	N: 45 P: 80	N: 85 P: 80	N: 50
Acceptor dopants & Shallowest ionization Energy (meV)	B: 45	Al: 200 B: 300	Al: 200 B: 300	Al: 270
1998 commercial wafer diameter (cm)	30	5	5	None

The high breakdown field of SiC allows higher voltage operation or reduced blocking layer thickness. Devices with thinner blocking layers have lower conduction losses and improved thermal characteristics. The high breakdown field also offers the possibility of extending the fast-switching, lower-loss performance of Schottky rectifiers and MOSFETs to much higher voltages and power levels [Neudeck, 2000].

2.2.3 Defect in SiC

One of the major problems with SiC wafers is the existence of "micropipes," which are large Burgers vector screw dislocations with a small pinhole [Othani, 2008]. They penetrate the entire crystal along the *c*-axis and cause critical flaws in SiC devices. Figure 2.9 shows an atomic force microscope (AFM) image of the (0001) Si surface of 6H-SiC, where a spiral step ending at a micropipe is visible [Feng, 2004]. Several possible causes exist for the formation of micropipes, and they are categorized into three groups [Othani, 2008]: (1) thermodynamic, (2) kinetic, and (3) technological causes. For example, the thermodynamic causes include thermoelastic stress due to non-uniform heating, while the kinetic causes are related to the nucleation process and growth surface morphology. In all of these cases, one must also consider the technological aspects, such as the seed surface preparation and contamination of the growth system. Recent advances in the physical vapor technique (PVT) growth technique have made possible a highly-controlled growth process for SiC bulk crystals and enabled us to achieve reproducible crystal growth under optimized growth conditions, which has led to a continuous reduction in the micropipe density over the past several years. In 2007, demonstration of extremely low micropipe densities (less than 1 cm^{-2} or even zero) over

100 mm diameter SiC wafers has been reported by Cree [www.Cree.com]. This would be expected to lead to the enhancement in the yield and productivity of SiC power devices and thus reducing their costs.

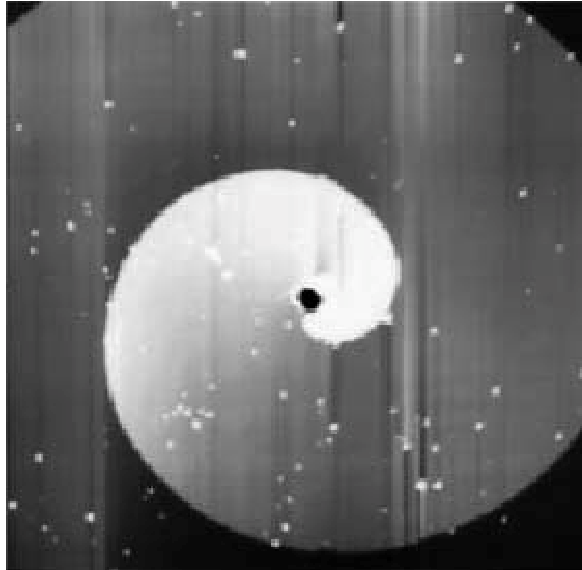

Fig. 2.9: AFM image (40 μm × 40 μm) of a growth spiral due to a micropipe on the 6H-SiC (0001)Si surface [Feng, 2004].

2.3 High-κ Dielectrics

2.3.1 Introduction

SiO_2 present several important features that have allowed it to be used as gate dielectric material for decades. Firstly, amorphous SiO_2 can be thermally grown on silicon with excellent control in thickness and uniformity, and forms a very stable interface with Si substrate. Secondly, SiO_2 presents excellent thermal and chemical

stability, which mean that as a device operated in a changing environment, its properties will remain constant and hence its reliability will be enhanced. The third one, band gap of SiO_2 is quite large (about 9 eV), which can provide excellent electrical isolation between the gate of the device and the channel. All of these superior properties allowed SiO_2 to be scaled down to a few nanometers [Houssa, 2004].

However, even SiO_2 has become almost an ideal gate dielectric for several decades, the continue scaling of MOS devices will present problems in the future. Wong and Iwai [2006] has summarized the limitation of this SiO_2 as follow:

(1) Physical thickness limitation

Theoretically, to have a SiO_2 bulk behavior (e.g. energy gap of about 8.9 eV), the SiO_2 layer must consists of at least two rows of neighbor oxygen atoms. Therefore, according to Fig. 2.10, "7 Å thick" is the ultimate theoretical limit of SiO_2. If the oxide thinner than 7 Å, it will cause the overlapping of the Si-rich interfacial regions then it would makes the dielectric film becomes conductive and result in a very large leakage current.

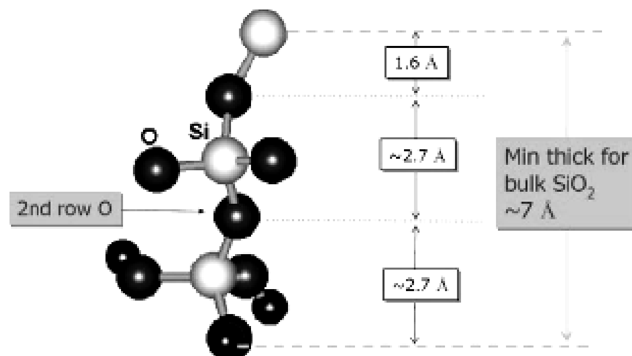

Fig. 2.10: Bonding structure of SiO_2 indicating the minimum thickness of the bulk oxide is about 7 Å [Wong and Iwai, 2006].

As the SiO_2 is thinned, quantum mechanical tunneling current becomes more significant [Wallace and Wilk, 2002]. Since the current from this kind of transport is exponentially dependent on the dielectric thickness, leakage currents through the gate oxide have increased dramatically as the gate oxide thickness has scaled sown.

(2) Reliability limitation

Another problem of scaling SiO_2 is reliability or life time. During operation of MOSFETs in integrated circuits, charge carriers flow through the device, resulting in the generation of defects in the SiO_2 gate layer and at the Si/SiO_2 interface. When the critical density of defect is reached, breakdown of the gate layer occurs, resulting in the failure of the device. These trends of increasing reliability issues with thinning gate dielectrics at some point will limit the scalability of silicon dioxide.

(3) Technological limitation

In the nanometer thick dielectric film, the interface layer is so thin (compared with the total oxide width) that any non-uniformity in chemical composition and even surface roughness fluctuations will cause the device characteristic to fluctuate. The thickness and uniformity requirement for gate dielectric film should be subjected to the most stringent control. Thinner oxide also cannot be fabricated in mass production since both the physical and the electrical characteristics would have wider statistical spreads.

Based on the discussion above, one possible solution to the leakage current and reliability issues created by scaling SiO_2 is the use of a higher permittivity dielectric in place of SiO_2, known as high- κ dielectric.

2.3.2 High-κ Dielectrics Properties

The term high-κ dielectric refers to a material with a high dielectric constant (κ) as compared to SiO_2 (κ = 3.9) [Toriumi and Kita, 2007]. The implementation of high-κ gate dielectrics is one of several strategies developed to allow further miniaturization of electronic components, according to Moore's Law [Intel website, 2009]. Recall that the traditional approach of scaling the gate dielectric in MOS capacitor has been reducing SiO_2 thickness (d_{SiO_2}) to increase oxide capacitance (C_{ox}):

$$C_{ox} = \frac{k_{SiO_2} e_o A}{d_{SiO_2}} \tag{2.2}$$

where κ is the dielectric constant (relative permittivity) of the SiO_2 and ε_o is the permittivity of free space (=8.85 x 10^{-3} pF/μm) and A is the area of capacitor. But Now that leakage currents due direct tunneling have reached unacceptably high levels, the more recent high-κ approach is to increase the physical thickness of the film (d_{ox}) to reduce the tunneling currents, yet at the same time obtain higher values of gate

capacitance by using a dielectric material with a higher dielectric constant ($\kappa_{high\text{-}k}$) relative to SiO_2 [Kawamoto, 2002],

$$C_{high-k} = \frac{k_{high-k} e_o A}{d_{high-k}} \tag{2.3}$$

where $k_{high\text{-}k}$ and $d_{high\text{-}k}$ are the dielectric constant and thickness of the high-κ material, respectively.

The expression of C can be written in term of effective oxide thickness (EOT). EOT is defined as the thickness of the SiO_2 layer that would be required to have the same capacitance as the high-κ material [Wallace and Wilk, 2002]. According to Eq. 2.2 and 2.3, EOT is given by

$$EOT = d_{SiO_2} = \left(\frac{k_{SiO_2}}{k_{high-k}} \right) t_{high-k} \tag{2.4}$$

For example, by using ZrO_2 as gate dielectric (κ≈ 20), the EOT would be 1 nm. This means that we can use a 5.1 nm thick ZrO_2 layer, in order to have a capacitance equivalent to a 1 nm thick of SiO_2 layer.