$Al_{0.15}Ga_{0.85}N$/GaN Heterostructure Field Effect Transistors (HFET) Device Structure Optimization and Thermal Effects

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Abstract

$Al_{0.15}Ga_{0.85}N$/GaN heterostructure field effect transistors (HFETs) was simulated by using ISETCAD software with varying substrate type, gate length and source drain resistances. The device output characterristics for drain current and voltage with various gate biases were studied. A maximum drain current of 0.18 mA/µm was obtained with a knee voltage of approximately 3 V at V_G =1 V using GaN substrate. A maximum extrinsic transconductance of 68 mS/mm was obtained at V_{DS} =10 V and device performance was limited by the source drain contact resistance. We investigated the device output drain current at various voltage characteristic in two thermal cases (isothermal and non-isothermal). The device performance can be improved by optimizing the substrate type which led to the reduction of contact resistance and the enhancement of transconductance.

1. Introduction

AlGaN/GaN heterostructure field effect transistors (HFETs) have recently attracted intense attention as promising candidates for high-voltage, high-power, and high temperature microwave applications [1-4]. The high peak electron velocity, high–saturation velocity and high breakdown electric field in nitride-based material are the advantageous parameters for the above applications.

These attractive material parameters will be even more exploited in the future when the gate length is ultimately reduced. For the moment, the minimum device size is limited by the breakdown electric field of the material. In addition to these material parameters, the superior transport properties of two dimensional electron gas (2DEG) in nitride heterostructures are also attractive (4-10). The promising device performance of nitride HFETs for high power applications is greatly ascribed to the very high 2DEG densities in excess of 10^{13} cm^{-2}, which are larger than those in GaAs based HFETs by about one order of magnitude.

In nitride heterostructures with wurtzite crystal structures in the (0001) orientation, there exist strong polarization affects which is piezoelectric (PE) polarization (11-14) and spontaneous polarization (15). These results in a large amount of polarization emerging at the AlGaN/GaN heterointerface which depends on the Al composition and the lattice strain at the heterointerface. The polarization values strongly influence the potential profile and the electron density in the heterostructure (16-20). Therefore, understanding of the effects of the polarization on the transport properties of 2DEG is indispensable for the understanding of the properties of nitride HFETs and further improving the device performance.

Our calculation is based on the theory developed by Shur and colleagues [21]. This theory shows that a very high sheet electron density ($n_s > 2 \times 10^{13}$ cm^{-3}) could not be attributed to the pure 2D-electron gas at the $Al_{0.15}Ga_{0.85}N$–GaN heterointerface. The high n_s value is achieved by doping a thin GaN layer at the heterointerface.

However, at higher doping level of the GaN channel, a significant fraction of electrons remain in delocalized states in the vicinity of the AlGaN-GaN heterointerface.

Three major contributions determine the sheet electron density near the AlGaN-GaN heterointerface: (1) the contribution from the electrons induced by the doped AlGaN barrier; (2) the contribution from the dopants in the GaN channel; (3) the contribution from the electrons generated by the piezoelectric effect (piezoelectric doping). When the sheet electron density in AlGaN-GaN heterostructures with doped GaN channel exceeds the critical value $n_{2Dmax} \sim 1 \times 10^{13}$ cm^{-3} the electron spill from the state near the heterointerface and occupy the delocalized states in the channel leading to a reduction of the electrons mobility. This reduction can be explained by a more pronounced ionized impurity scattering when electrons occupy a much wider doped region near the heterointerface.

In this work, both electrical properties and device performance of AlGaN/GaN HFETs are presented. Our work based on the theoretical and experimental work done by N.Maeda and N.Kobayashi [22]. The performance of these devices has been limited by self-heating and other problems associated with the large defect densities. Thus, accurate modeling of self heating effects in GaN/AlGaN HFETs and device structure optimization for better thermal management becomes important in our simulation work and the results obtained. In addition, we present the results of temperature rise in GaN/AlGaN HFETs characterized by different geometry, layered structure, doping density and substrate type. The simulation of self-heating effects in various AlGaN/GaN layered structures on different substrates will help to determine the parameters of the device structure that are optimum for thermal management.

2. Device simulation parameters and models used

Device simulation parameters of the optimized HFET geometry and doping profile are reported in Fig. 1 and Table 1. The simulation was performed by means of the 2-D device analysis program of ISE TCAD software [23] package which solves Poisson's and carrier continuity equations, with electron and hole-current densities given by the drift-diffusion model. The other models used in our simulations were: hydro (e Temperature), mobility (h High Field Saturation) (e High Field saturation), Carrier Temperature Drive, Effective Intrinsic Density (No Band Gap Narrowing). Our simulation solves the carrier (electron) temperature equations coupled with Poisson's and carrier continuity equations. Thermal contact was introduced to simulate the non-isothermal case in our HFET structure.

Figure 1 shows the basic design of an $Al_{0.15}Ga_{0.85}N$ /GaN HFETs where we introduced a doped channel design which allowed us to significantly increase the sheet electron density n_s near the $Al_{0.15}Ga_{0.85}N$/GaN heterointerface. 1µm thickness of undoped GaN is assumed to grow on two different substrates (sapphire and GaN) with 2µm thickness, followed by the 50 nm n-GaN channel doped layer and 30nm $n\text{-}Al_{0.15}Ga_{0.85}N$ layer.

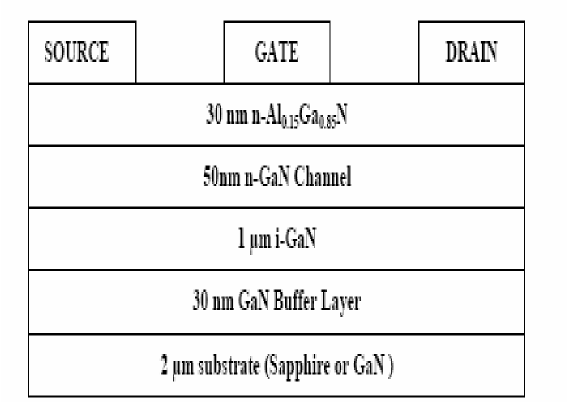

Fig. 1: The schematic of the AlGaN/GaN simulated HFETs structure.

Table 1: The parameters used in our simulation device.

Gate Length	**0.5 µm**
Channel Length	**4.0 µm**
Channel Thickness	**50nm**
Substrate Thickness	**2.0 µm**
Channel Doping(N_d)	**$5e^{17}$ cm^{-3},n-type**
AlGaN Doping	**$4.5e^{17}$ cm^{-3},n-type**
Source and Drain Length	**1 µm for each**
Source –Drain Contact resistance	**1 ohm-µm**
Source- Gate spacing	**0.75 µm**
Source - Drain spacing	**2.0 µm**
Gate Schottky Contact Barrier	**1eV**

3. Simulation results and discussion

Large currents and large voltages, which are required for high–power applications of AlGaN/GaN HFETs cause strong self-heating affecting power dissipation. Growing AlGaN/GaN epilayer structures on high thermal conductivity substrate decreases the self –heating effects in AlGaN/GaN HFETs.

Figures 2 and 3 show the drain current (DC) versus drain voltage characteristics of AlGaN/GaN HFETs on sapphire and GaN substrate respectively.

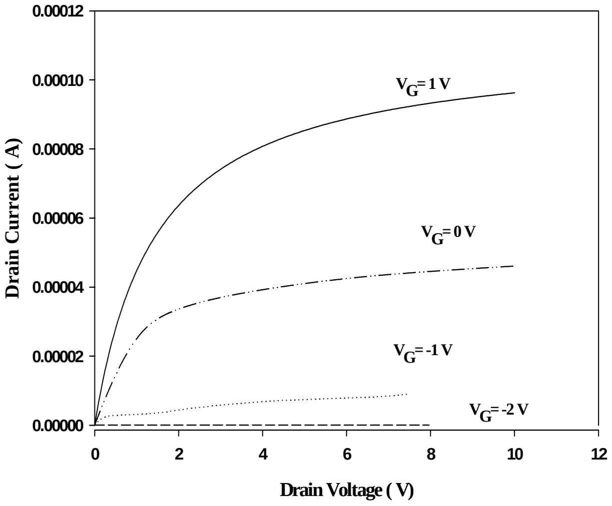

Fig .2 : Drain current versus drain voltage at different gate biases voltage for AlGaN/GaN HFETs on sapphire substrate.

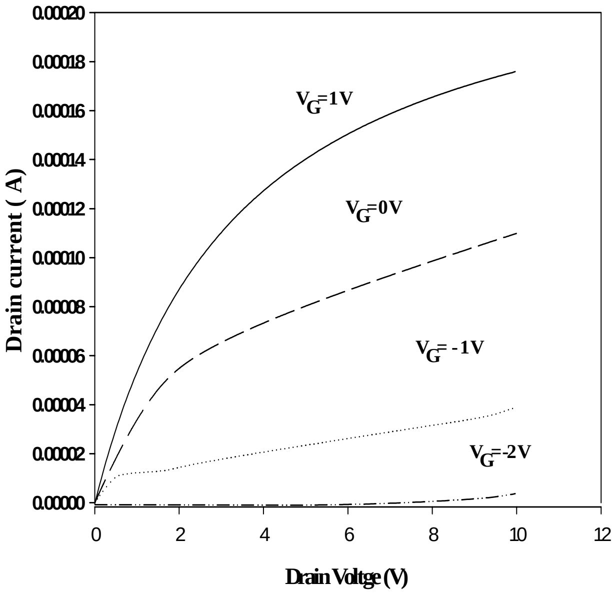

Fig. 3 : Drain current versus drain voltage at different gate biases voltage for AlGaN/GaN HFETs on GaN substrate.

It is observed that the maximum DC drain saturation current in AlGaN /GaN HFETs on GaN substrate was greater than in similar devices on sapphire substrate and this is attributed primarily to an effective heat sinking through a GaN substrate, which has a high thermal conductivity. From Fig. 2 we observed that, at a higher gate voltage ($V_G = 1$ V) the maximum drain current is about 0.09 mA; it falls rapidly with decreasing gate voltage, and reduces to about 0 mA at a gate voltage of - 2 V.

The I–V characteristics of the simulated HFETs on a GaN substrate exhibit a maximum drain current around 0.18 mA, at a gate bias voltage (V_G =1) and it falls rapidly with decreasing gate voltage, and reduces to about 0 mA at a gate voltage of - 2 V. As mentioned before, the difference in the saturation drain current at high gate bias voltage could be attributed to the higher effective heat sinking through a GaN substrate, which has a higher thermal conductivity.

It is known that at high temperatures, leakage current starts to dominate the drain current as gate voltage becomes more and more negative. Also, the electron mobility decreases with increase in temperature due to scatterings. Figure 4 shows the reduction of the drain current at each value of the gate bias in the case of non-isothermal process in AlGaN/GaN HFETs as we activated the electron temperature and lattice temperature effects in our device. The saturation current reduction is caused by the degradation of the electron mobility due to increased electron–phonon scattering. The GaN/substrate interface acts as thermal insulator that keeps the heat in the active channel and creates hot spots.

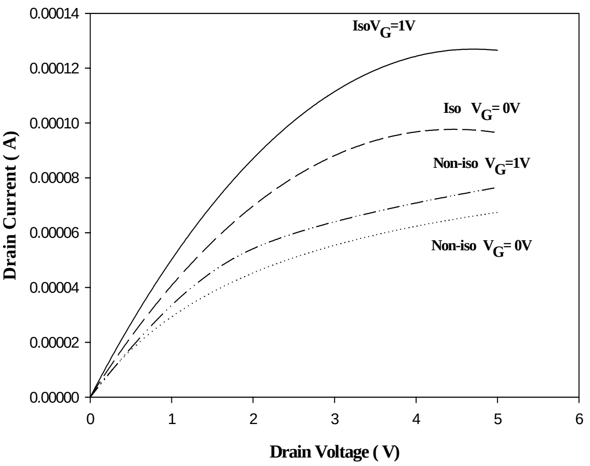

Fig. 4 : Drain current versus drain voltage at different gate biases voltage for AlGaN/GaN HFETs on GaN substrate in isothermal and non isothermal case.

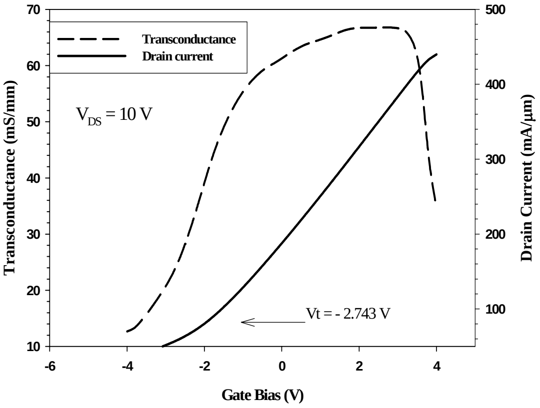

Fig. 5: The transconductance and source–drain current dependence on the gate bias for AlGaN/GaN HFETs on GaN substrate with 0.5 µm gate and 2µm source –drain spacing.

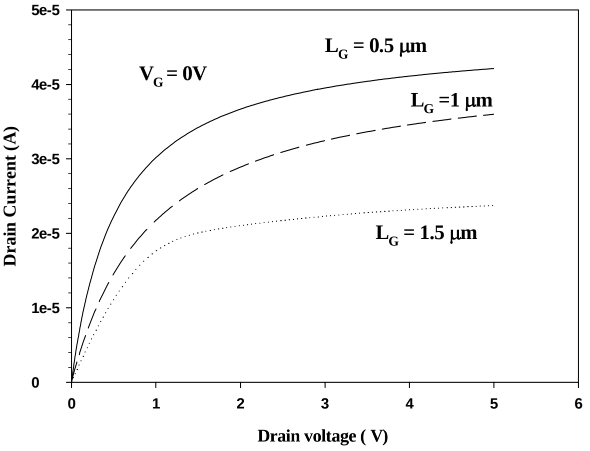

Fig. 6: Drain current versus drain voltage of AlGaN/ GaN HFET on sapphire substrate with varying gate length.

Higher temperatures may lead to mobility degradation and negative differential resistance. The transconductance and source–drain current of a AlGaN/GaN HFETs on GaN substrate versus gate bias voltage are shown in Fig. 5. The maximum transconductance (g_m) of 67 mS/mm was obtained at gate bias of (V_G = 2 V) and at V_{DS} = 10 V. The pinch-off voltage obtained is -2.743 V.

Figure 6 shows that with an increase in gate length, there are decreases in drain current which is attributed to suppression of the leakage current and increase in gate resistance.In addition, it is important to reduce gate length and specific contact resistivity simultaneously for improving microwave gain of HFETs and to achieve high speed operation. For HFETs transistors the time constant of the RC-circuit, where R represents the gate resistance and C the gate capacitance, should be as low as possible. The value of the capacitance is essentially determined by the gate length of the device, therefore the gate resistance has to be kept low while simultaneously reducing the gate length.

Figure 7 shows the drain current decreasing with increasing source drain resistance. It is observed that the drain current saturation maximum value is determined by the source-drain ohmic contact.

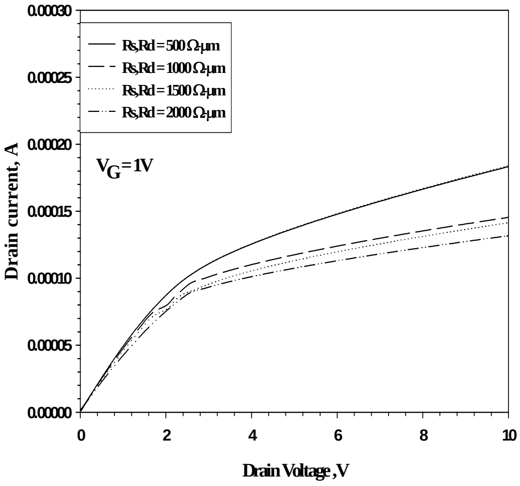

Fig. 7 : Drain current versus drain voltage of AlGaN/ GaN HFET on GaN substrate at various source and drain resistance.

4. Conclusion

AlGaN/GaN heterostructure field effect transistors HFETs were simulated and optimized through the ISE TCAD simulation software. The transistors exhibit good pinch-off characteristics with a threshold voltage of about -2.7 V and a saturation current density of 0.18 mA/µm on GaN substrate at room temperature. A peak transconductance of 67 mS/mm was obtained with GaN substrate. A reduction of saturation drain current was observed in HFETs on sapphire substrate compared to that obtained on GaN substrate due to effective heat sinking through a GaN substrate which has a high thermal conductivity than that of the sapphire substrate. We observed that gate leakage, self-heating process, drain-source resistance and gate length contact had effective changes in the transistor drain saturation current and transistor performance. More optimization for our transistor parameters and structure will probably enhance the device performance.

Acknowledgments

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