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COMPREHENSIVE REPORT

Project Title: **Computational Methods in FlipChip Assembly**

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Duration of Project: 1 September 2001 – 31 August 2002

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1.0 Introduction

1.1 Project Description

Flip chip technology, in the book edited by Lau (Lau, 1995) is defined as placing a chip to the substrate by flipping over the chip so that the I/O area of the chip is facing the substrate. By flipping over the chip, the interconnection between the chip and the substrate are achieved by conductive "bumps" placed directly in between the die surface and the substrate. Therefore, the whole chip surface can be utilized for active interconnections and at the same time, eliminates the need for wire bonding.

An internet source, (FlipChips Dot Com, 2001) indicates that flip chip interconnection has been introduced since the early sixties by IBM for use in their mainframe computers and IBM has continued to use flip chip up to the present day. The same source also acknowledges the role played by Delco Electronics in helping to develop flip chip for automotive applications in the seventies. These early developments together with the advantages of flip chip packaging technology which offers smaller chip size, higher I/O density with area array, better electrical performance and lowest cost interconnection for high volume automated production results in flip chip packaging being considered as the preferred choice over other conventional wafer level packaging technology (Meilhon et al., 2003).

There are essentially three basic elements in the solder flip chip interconnect systems (Fig. 1.1). These include the chip, the solder bump, and the substrate. The solder bumps in a flip chip interconnect system has three functions. First, the solder joint forms the electrical connection between the chip and the substrate. Second the solder joint also serve as a path for heat dissipation from the chip.

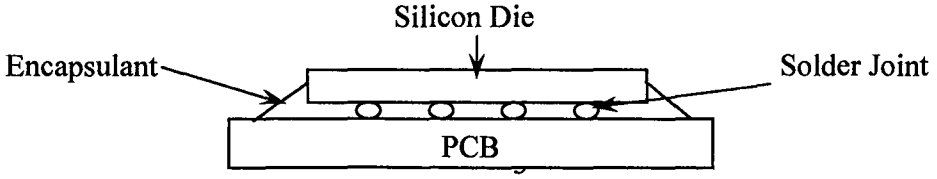


Fig. 1.1 Schematic of a solder flip chip interconnect system (Pang, 2001a)

Lastly, the solder joint provides the structural link between the chip and the substrate. The structural integrity of the solder joint affects both the electrical and thermal performances of the flip chip interconnect system. Degradation in the structural integrity can be a reliability concern.

Another reliability concern is the thermo-mechanical behaviour of the solder joint. Thermal mismatch deformations due to the different coefficient of thermal expansion (CTE) between different materials used in the package can cause mechanical stresses in the solder joint. This will eventually cause crack growth and leads to failure in the package.

The effect of temperature cycling on the reliability of microelectronic packages has been the subject of many studies. Because of the difference in the thermal expansion of the multiple materials involved in the construction of a typical package, temperature variations create a mismatch ultimately resulting in solder joint stress. Repeated application of this stress eventually causes solder joint failure, a mechanism commonly known as low cycle fatigue.

To minimize development costs and maximize reliability performance, advanced analysis is a necessity during the design and development phase of a microelectronic package. Computer simulation such as finite element analysis can provide a very detailed description of solder stress/strain distribution and history under a variety of loading conditions, and is a powerful tool for performing parametric studies and design optimization. However, analyst is typically interested in the cycles to failure that a package design configuration and cyclic loading

condition will cause. This requires the utilization of a life prediction methodology in which data typically provided by a finite element solution can be translated into cycles to solder joint failure.

Advances in the electronic industry leave in its wake a trail of reliability problems. The integrity of ball and bump solder joints is one of the major reliability concerns in modern microelectronic packages. A wide variety of literature is scanned for work done in addressing the reliability issues in microelectronic packages, particularly on the solder joint interconnect system.

Many investigators have studied the low-cycle fatigue life of solder bumps under accelerated thermal cycling test (e.g. Popelar et al. (2000), Darveaux (2000), Zahn (2000a), Zahn (2000b), Wiese et al. (2001), Lau et al. (2002), Schubert et al. (2002), Dutta et al. (2002), & Schubert et al. (2003). It is true that many package configurations studied by these researchers roughly have the same build-up and each of the case studies utilizes a fatigue life prediction methodology not much different from one another. Even solder fatigue lives predicted fall within a certain common range of a few hundred cycles to a few thousand cycles. However, despite all these work, not a single analysis approach and results obtained for a case study can be directly used for another case study. There will be too many irregularities that must be accounted for in order to compare any two case studies. Hence, even if fatigue life prediction methodology using plastic work is not new, different case study with different package configuration and different thermal cycle profile warrants the need for a simulation to be carried out in order to determine its solder fatigue life.

The objective of this work will be to predict the low-cycle fatigue life of a flip chip package subjected to two different accelerated temperature cycling test conditions. Temperature fluctuations caused by either power transients or environmental changes, along with the resulting

thermal expansion mismatch between the various package materials, results in time and temperature dependent creep deformation of solder. This deformation accumulates with repeated cycling and ultimately causes solder joint cracking and interconnect failure. Due to the thermal mismatch in thermal expansion, plastic strain is generated during temperature cycling and the solder structures accommodate most of the plastic strain. Since plastic strain is a dominant parameter that influences low-cycle fatigue, it is used as a basis for evaluation of solder joint structural integrity. An extensively published and correlated solder joint fatigue life prediction methodology based on viscoplastic finite element simulation was incorporated by which finite element simulation results were translated into estimated cycles to failure. Due to availability, the program ANSYS^{TM} was used to run the finite element simulations.

1.2 Project Activities

The activities carried out in this project can be summarized as follows

Stage 1: Modeling solder bump flip chip package

A detailed model of flip chip package was simulated based on based on viscoplastic finite element. Due to availability, the program ANSYS^{TM} was used to run this finite element simulations.

Stage 2: Development of solder bump fatigue model

A simplified and detailed models of solder bump fatigue was developed. An extensively published and correlated solder joint fatigue life prediction methodology based on viscoplastic finite element simulation was incorporated by which finite element simulation results were translated into estimated cycles to failure.

Stage 3: Derivation of algorithm for constitutive model for solder bump

The algorithm for constitutive model for solder bump was derived based on Anand's constitutive relations for rate-dependent viscoplasticity model and Darveaux constitutive relations. These constitutive relations were used to describe the deformation behaviour of solder joints.

Stage 4: Prediction of solder joint fatigue life

Based on non-linear Finite Element Analysis, simulations were carried out to calculate the plastic work per unit volume (or viscoplastic strain energy density). Another analysis based on the combination of a linear finite element analysis and imposed strain on the solder joints plus a non-linear analysis, was carried out to calculate assembly stiffness and to calculate strain energy density.

Stage 5: Parametric study on solder joint fatigue life

Package parametric analysis using the Artificial Neural Network (ANN) was used as a tool to predict other data points in the simulation results. This reduces the number of simulations required for parametric analysis.

Stage 6: Parametric optimization for fatigue life prediction

Once the effects of every package dimensions on the solder fatigue life have been established, the solder fatigue life can be appropriately adjusted to a higher fatigue life or a lower fatigue life by increasing or decreasing a chosen package dimension. Genetic Algorithm (GA) is used to optimize a combination of package dimensions that can provide a particular determined solder fatigue life.

The various stages of the work and their results are reported in the theses produced from this research. Several excerpts of the reports are available in the Appendix A.

1.3 Project Benefits

Through this research, the numerical analysis of solder bump flip chip package in electronic packaging material has been developed. To minimize development costs and

maximize reliability performance, advanced analysis is a necessity during the design and development phase of a microelectronic package. Computer simulation such as finite element analysis can provide a very detailed description of solder stress/strain distribution and history under a variety of loading conditions, and it is a powerful tool for performing parametric studies and design optimization. This will help the engineers in developing the electronic package requirement and the performance of the package can be predicted.

1.4 Project Duration

The project started in September 2001 and was completed in August 2002, which is for duration of one year.

1.5 Approved Grant Amount

The total amount approved by INTEL for this project is RM 41,200.00.

1.6 Project Cost

The total amount spent for this project was RM 41,200.0.

2 Project Contribution/Achievement

Thesis and Publications

The contribution of the research in terms of theses and publications are as follows:

Thesis:

1. MSc Thesis entitled: Solder Joint Reliability of Flip Chip BGA Packages – Lee Kor Oon (Mac, 2004).

Journal Papers:

1. I.A.Azid, Lee Kor Oon, Ong Kang Eu, K.N. Seetharamu, G.A.Quadir "Applications Of Artificial Neural Network For Fatigue Life Prediction", Key Engineering Materials, Volume 297-300 (2005), pp 96-101

2. KO Lee, KE Ong, KN Seetharamu, I.A.Azid, GA Quadir and TJ Goh,"Application of Artificial Intelligence for the Determination of Package Parameters for a desired Solder Joint Fatigue Life", Microelectronics International, Vol. 23, No. 2, 2006

3 Conclusion

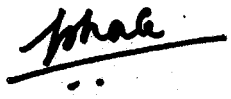
In this project, three-dimensional finite element analysis has been applied to determine the time-dependent solder joint fatigue response of a package under accelerated temperature cycling conditions. Due to the difference in the thermal expansion of the various materials involved in the construction of a typical package, temperature variations create a mismatch in package expansion which ultimately results in solder joint stress. Repeated application of this stress eventually causes solder joint failure, a mechanism commonly known as low cycle fatigue.

The solder structures accommodate the bulk of the plastic strain that is generated during accelerated temperature cycle. Since plastic strain is a dominant parameter that influences low-cycle fatigue, it is used as a basis for evaluation of solder joint structural integrity. An extensively published and correlated solder joint fatigue life prediction methodology was incorporated by which finite element simulation results were translated into estimated cycles to failure. The analysis methodologies as implemented in the ANSYS^{TM} finite element simulation software tool and the corresponding results for the solder joint fatigue life, is also discussed. Artificial Neural Network (ANN) has been used to consolidate the parametric studies and then the evaluation of parameters to give a particular fatigue life is achieved by the use of Genetic Algorithm (GA).

4 Acknowledgement

We would like to convey our sincere thanks to INTEL Technology Sdn. Bhd. for the offer of the grant and the generous support in using their model for flip chip package that has enabled this research to be carried out and completed successfully.

Report prepared by:



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APPENDIX A

Extract from MSc Thesis entitled: Solder Joint Reliability of Flip Chip BGA Packages – Lee Kor Oon (Mac, 2004).

CHAPTER 2
METHODOLOGY

2.1 Solder-bumped Flip Chip Package

A typical flip chip package measuring 14×14mm, with 256 solder balls (16×16 full ball matrix), 0.80mm pitch and attached to a 50×50mm board is analyzed. There are 2 dies in the package. The top die measured 9×9mm and the bottom die measured 12×12mm. The package outline drawing is shown in Fig. 2.1.

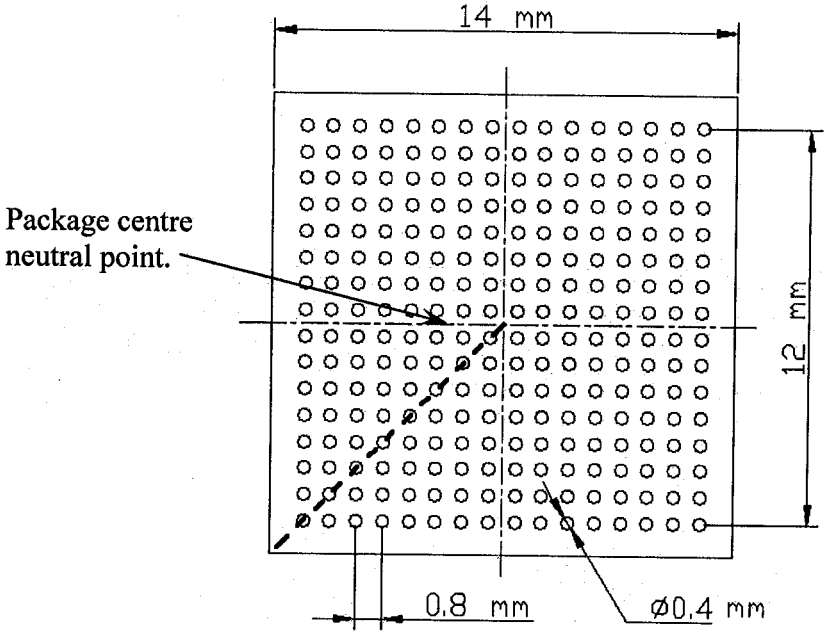


Fig. 2.1. Package outline drawing (Intel).

The basic structure of the solder-bumped flip chip package is shown in Fig. 2.2. More detailed layer dimensions of the package substrate and printed circuit board are shown in Figs. 2.3 and 2.4. Graphical details of the solder ball along with the package substrate pad and the printed circuit board pad are shown in Fig. 2.5. The stack-up layer dimensional information of the flip chip package is given in Table 2.1.

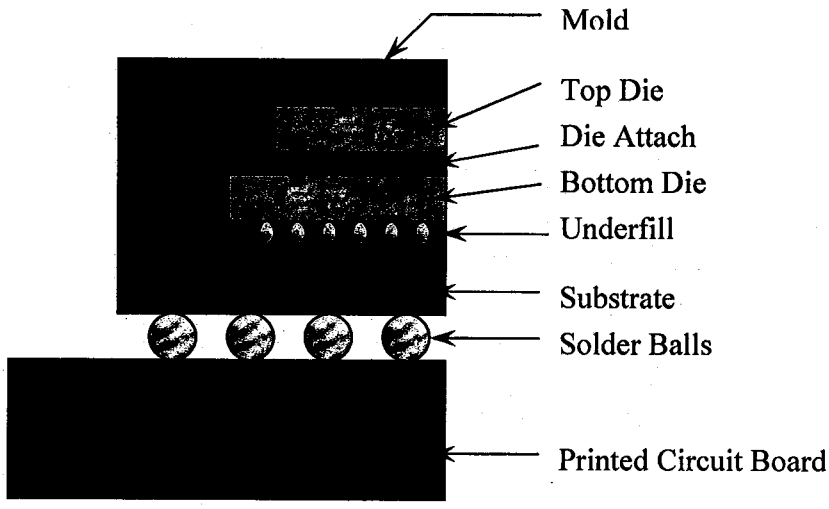


Fig. 2.2. Basic structure of a flip chip package (Intel).

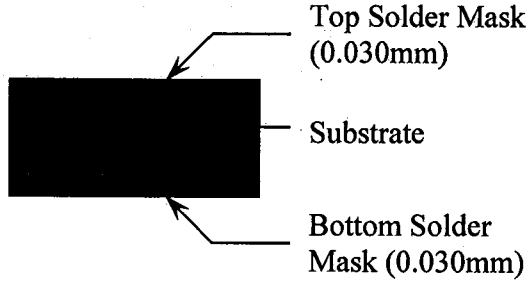


Fig. 2.3. Layer dimensions of package Substrate (Intel).

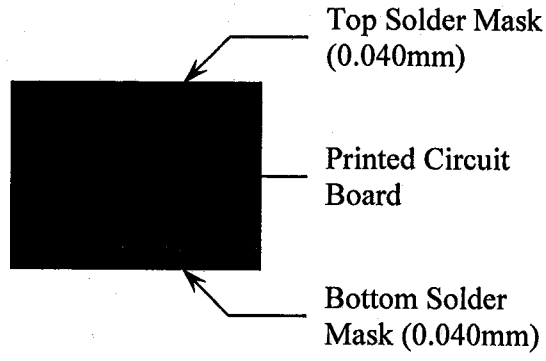


Fig. 2.4. Layer dimensions of printed circuit board (Intel).

As shown in Fig. 2.2, the basic structural layer layout of the typical flip chip package consists of the top die which is attached to the bottom die through the die attach layer. The bottom die is attached to the substrate through the underfill layer. Solder balls form the

interconnection between the package substrate and the printed circuit board. The mold encompasses the top and bottom dies.

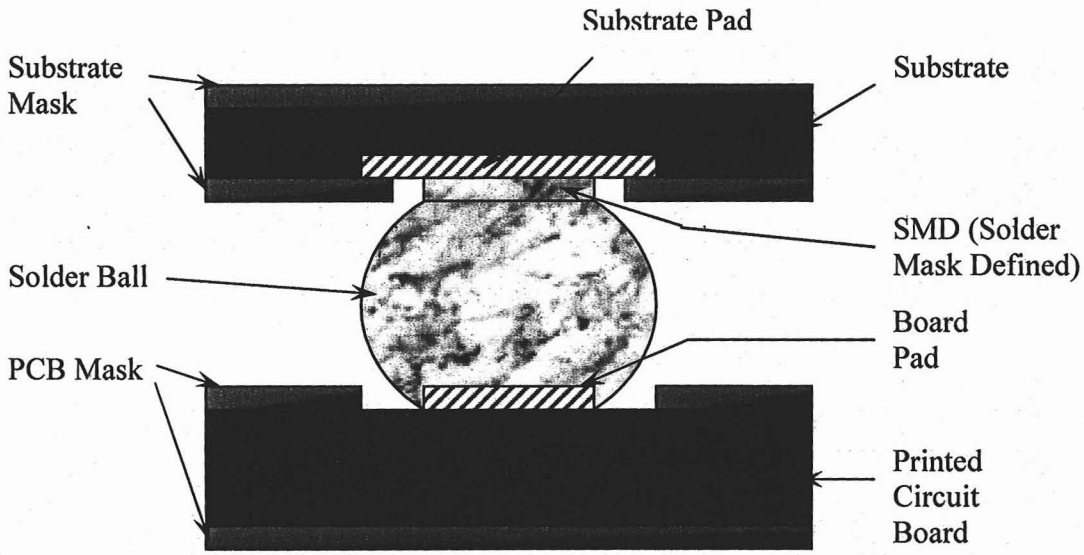


Fig. 2.5. **Graphical details of the solder ball (Intel).**

Table 2.1. **Stack-up layer dimensions of the package (Intel).**

Package Attribute		Dimension (mm)
Top Die	Thickness	0.100
	Size	9×9
Die Attach	Thickness	0.030
Bottom Die	Thickness	0.130
	Size	12×12
Underfill	Thickness	0.090
Mold	Thickness	0.540
Substrate	Thickness	0.168
	Size	14×14
Substrate Mask	Thickness	0.030
	Mask Opening Diameter	0.3254
Substrate Pad	Thickness	0.027
	Diameter	0.1881
SMD	Thickness	0.030
Solder Ball	Height	0.300
	Pitch	0.800
	Diameter	0.400
Printed Circuit Board	Thickness	1.570

	Size	50×50
PCB Mask	Thickness	0.040
	Mask Opening Diameter	0.500
Board Pad	Thickness	0.027
	Diameter	0.300

Table 2.1 shows the dimensions of the typical flip chip package used in the analysis. The top die has a thickness of 0.100 mm and the size of the die is 9×9 mm square. Underneath the top die is the die attach with a layer thickness of 0.030 mm. The top die and die attach is placed above the bottom die which has a thickness of 0.130 mm with a die size of 12×12 mm square. Beneath the bottom die is a 0.090 mm thick layer of underfill which connects the bottom die to the package substrate. The mold encompasses the top and bottom dies as shown in Fig. 2.2 with a thickness of 0.540 mm from the substrate. The package substrate surfaces have a 0.030 mm thick substrate mask. Other details at the solder ball joint interfaces include a 0.027 mm thick substrate pad with a diameter of 0.1881 mm and a 0.027 mm thick board pad with a diameter of 0.300 mm. The solder ball itself has a standoff height of 0.300 mm, a pitch of 0.800 mm and a diameter of 0.400 mm. The printed circuit board is a 50×50 mm square board with a thickness of 1.570 mm. The printed circuit board surfaces also have PCB masks of 0.040 mm thick.

2.2 Solder Ball Fatigue Models

Viscoplastic finite-element simulations methodologies are utilized to predict the stress level and accumulated strain energy density per thermal cycle within the critical solder ball of a package. Two models with different levels of package details are used for the simulations. The first model is a simplified version of the flip chip package where a few layer details are omitted from the simulation model. The second model is a full model with more layer details incorporated into the simulation model. Omission of a few layer details at the interface of the model is carried out in order to determine if model simplification can produce results similar to a

more complex model. For the simplified model only the most necessary basic components of the package are drawn and many small details at the solder ball interfaces are neglected, with a possible view of obtaining results with much less effort. Due to the complex physics that encompass this type of non-linear transient finite element analysis, only half of a diagonal slice of the package was modeled in order to facilitate reasonable model run times. The utilization of a half diagonal slice assures that a worst-case situation is simulated where the perimeter solder ball is the farthest bump from the package centre neutral point shown in Fig. 2.1. The half diagonal slice representing the finite element model is shown by the diagonal bold print dashed line in Fig. 2.1.

The half diagonal slice model goes through the thickness of the overall package assembly, taking into account all major components and a full set of halved solder joints. Utilization of a slice model necessitates the consideration of boundary constraints that has to be imposed on the slice model, which has to appropriately represent the actual boundary conditions by which the full package assembly is subjected to. The symmetrical diagonal plane remains planar and constant in the y-direction throughout the analysis. The opposite side of the diagonal symmetric plane is neither a free surface nor a true symmetry plane. A reasonable compromise is to couple the y-displacements of the nodes on the slice plane. The effect of this constraint is that the slice plane is free to move in the y-direction, but that the surface is required to remain planar. Boundary constraints applied to a typical slice model are shown in Fig. 2.6. For all models presented in this work, the printed circuit board length is truncated at a distance after the package length. For a diagonal slice model, the ball pitch is the hypotenuse (1.1314mm) of the true ball pitch (0.80mm). The y-dimension or width of the slice model is one-half the solder ball pitch (0.5657mm).

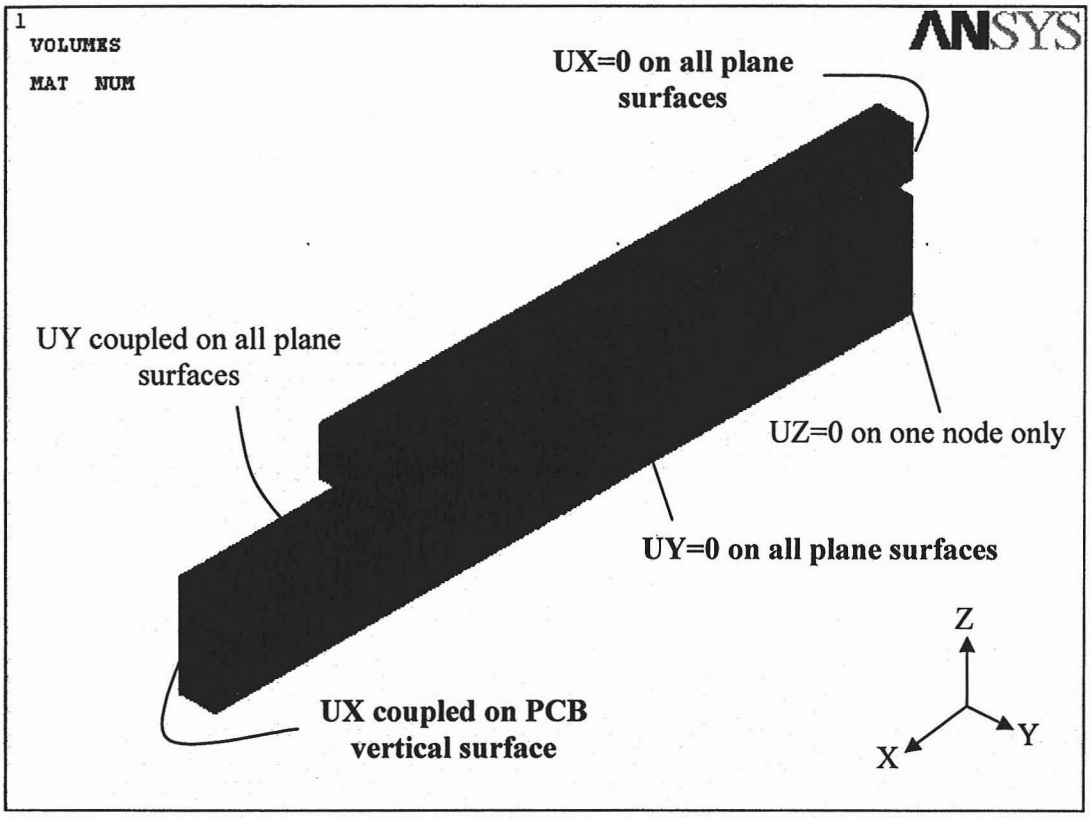


Fig. 2.6. Boundary constraints applied to a typical slice model (Zahn, 2000a).

2.2.1 Simplified Flip Chip Model

A simplified flip chip model is used for the first part of the simulation. The layer configuration of the model is shown in Fig. 2.2. By comparing Fig. 2.2 with Figs. 2.3 through 2.5, a few details of the flip chip package assembly are omitted from this model. The solder mask layers on the substrate and on the printed circuit board are not included in this model. The substrate pads and the board pads are not included as well. The solder mask defined (SMD) layer on top of the solder balls is also omitted from the model. This configuration simplifies

considerably the finite element model at the solder ball joints and hence reduces the modeling and computational time required.

Based on Table 2.1, a three dimensional model of the flip chip package is drawn using the commercial software ANSYS^{TM} 7.0. The half diagonal slice finite element model and the resulting mesh are shown in Figs. 2.7 and 2.8 respectively. The close-up details at one of the solder ball joint and its resulting mesh are shown in Figs. 2.9 and 2.10 respectively.

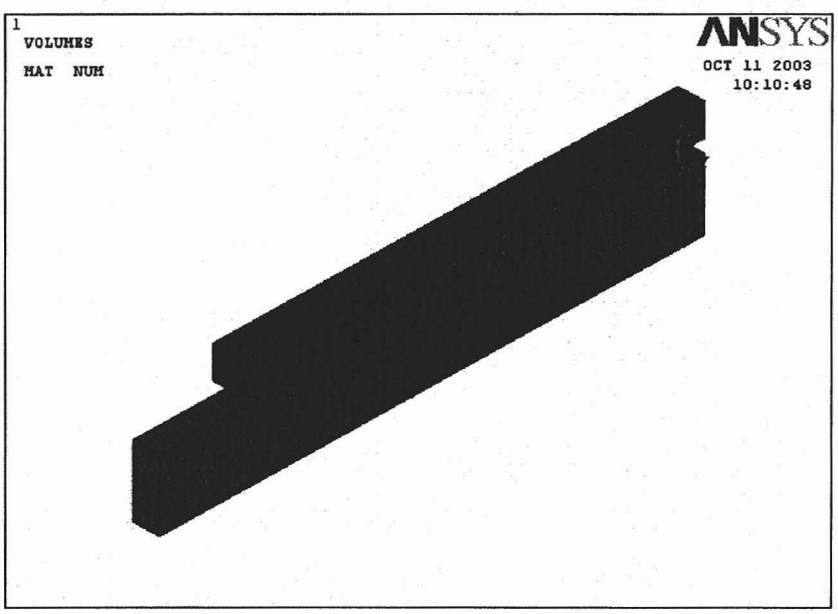


Fig. 2.7. Simplified diagonal slice model of the flip chip package.

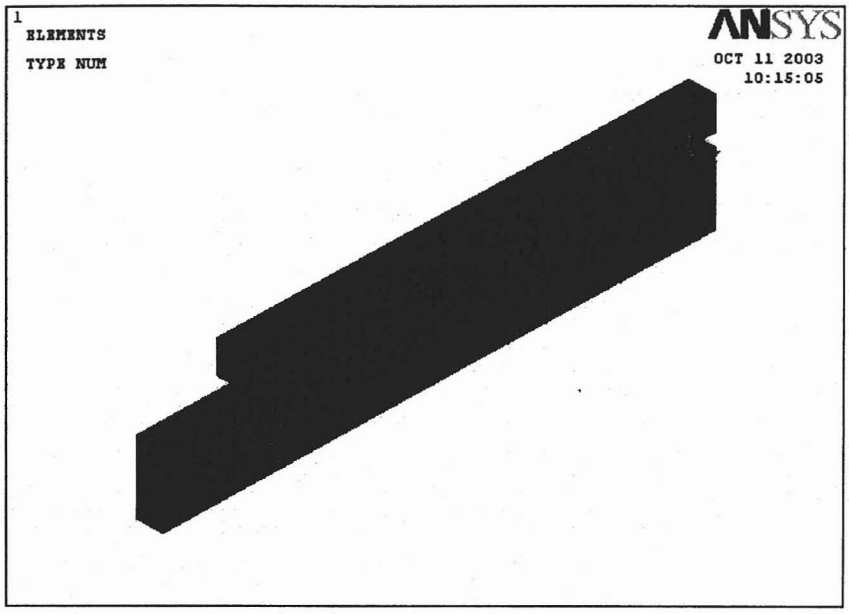


Fig. 2.8. Meshed simplified slice model of the flip chip package.

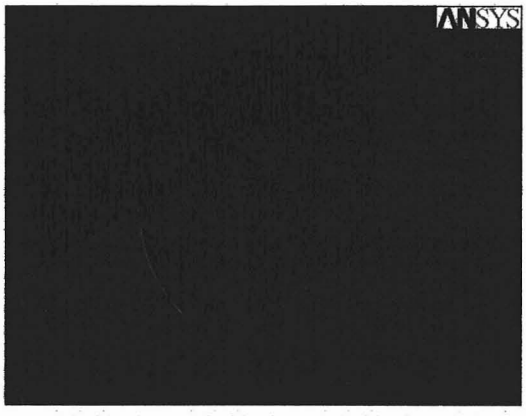


Fig. 2.9. Close-up details of a solder ball joint.

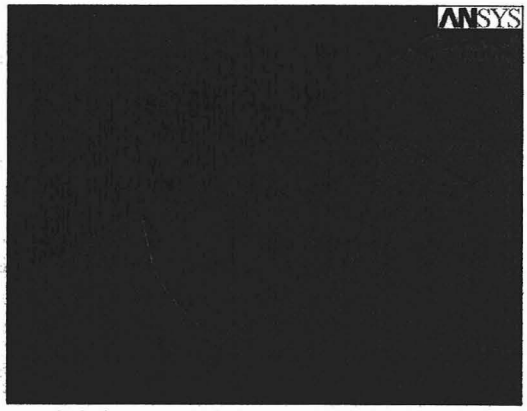


Fig. 2.10. The resulting mesh of a solder ball joint.

The entire model utilized a mapped or structured finite element mesh with 5506 elements and 7652 nodes. Typical solution run times are about 1.15 hours to 1.3 hours depending on the accelerated temperature cycling test condition applied.

2.2.2 Detailed Flip Chip Model

For the second part of the simulation, a more detailed flip chip model is used for simulation. As shown in Fig. 2.5, the SMD layer on top of each solder ball joints is included in the model. The substrate pads and the board pads along with the solder mask layers on the substrate and printed circuit board are included in the model. Based on Table 2.1 and Figs. 2.2 through 2.5, a three dimensional model of the flip chip package is drawn in ANSYS™ 7.0. The half diagonal slice finite element model and the resulting mesh are shown in Figs. 2.11 and 2.12 respectively. The close-up details at one of the solder ball joints and its resulting mesh are shown in Figs. 2.13 and 2.14 respectively

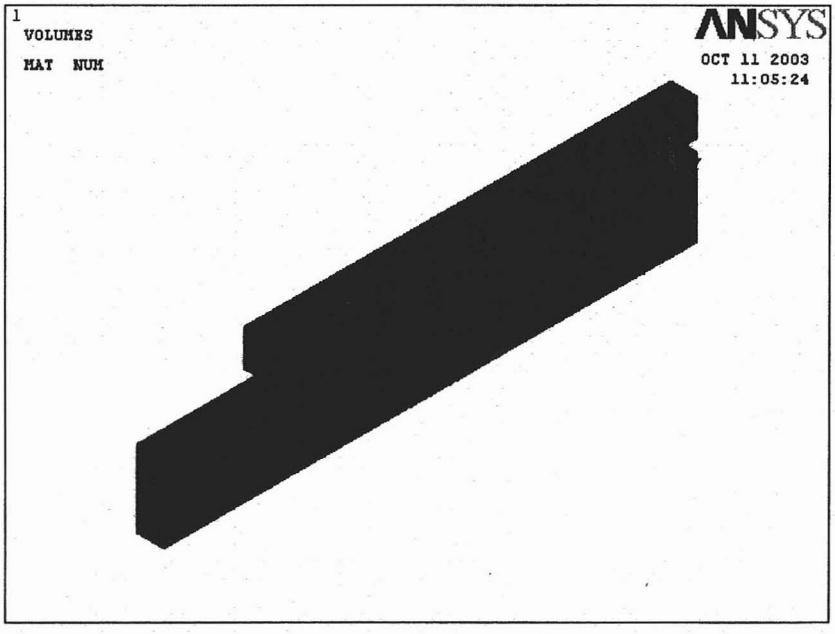


Fig. 2.11. Detailed diagonal slice model of the flip chip package.

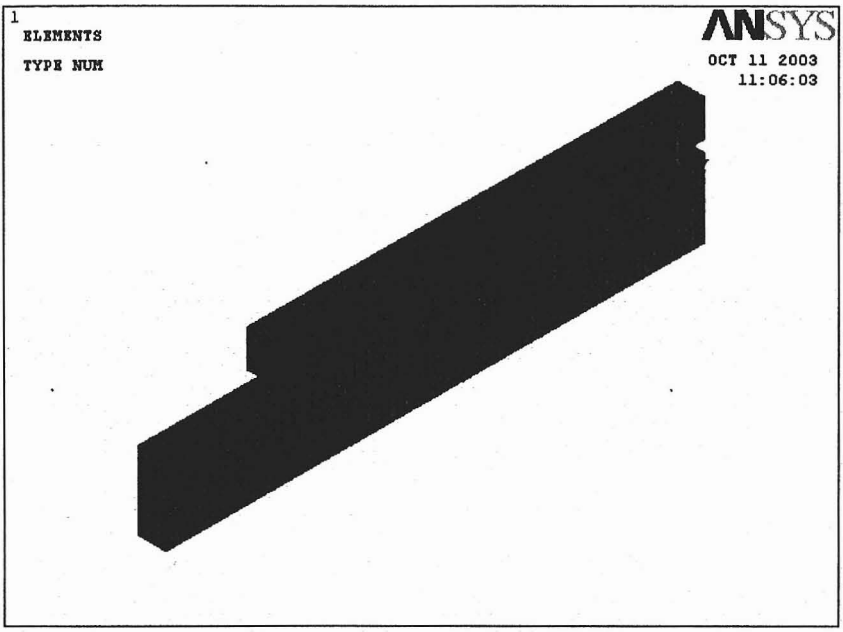


Fig. 2.12. Meshed detailed slice model of the flip chip package.

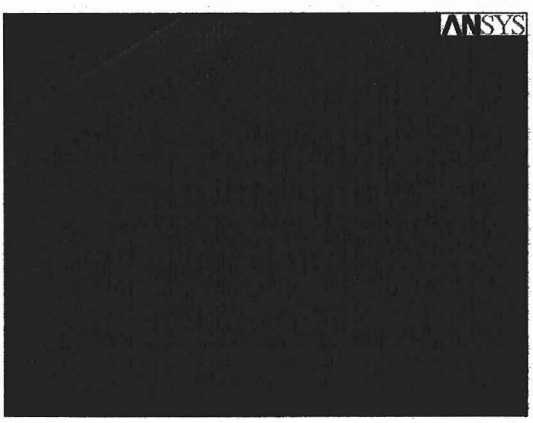


Fig. 2.13. Close-up details of a solder ball joint for the detailed model.

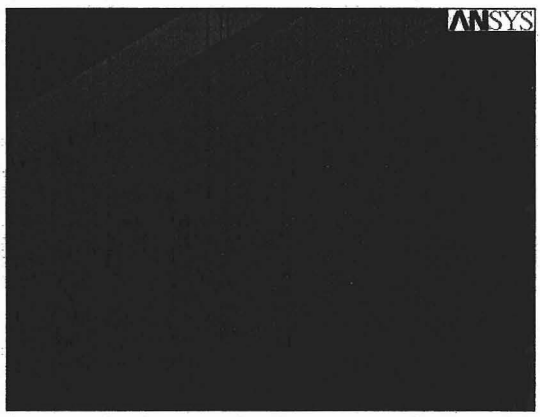


Fig. 2.14. The resulting mesh of a solder ball joint for the detailed model.

The entire model utilized a mapped or structured finite element mesh with 6920 elements and 9308 nodes. Typical solution run times are about 1.25 hours to 1.42 hours depending on the accelerated temperature cycling test condition applied.

2.3 Material Properties and Modified Anand Constants

Tables 2.2 through 2.8 show the material properties incorporated in the finite element models. As seen from the tables, most of the properties used in the analysis are dependent only on temperature.

Table 2.2. Die material properties (Intel).

Temp. (K)	Young's Modulus (MPa)
213	131000
233	131000
273	130000
293	130000
323	130000
373	129000
500	129000

Temp. (K)	CTE (1/K)
200	2.36E-6
250	2.63E-6
293	2.81E-6
325	2.89E-6
350	2.98E-6
425	3.3E-6
450	3.5E-6
500	3.61E-6

Poisson's Ratio
0.279

Table 2.3. Die attach/underfill material properties (Intel).

Young's Modulus (MPa)	CTE (1/K)	Poisson's Ratio
$-268349 + 4631.4T - 32.27T^2 + 0.117T^3 - 0.0002T^4 + 2\times10^{-7}T^5 - 1\times10^{-10}T^6$	$-0.028 + 0.0005T - 4\times10^{-6}T^2 + 1\times10^{-8}T^3 - 3\times10^{-11}T^4 + 3\times10^{-14}T^5 - 1\times10^{-17}T^6$	0.3

Table 2.4. Mold material properties (Intel).

Temp. (K)	Young's Modulus (MPa)
233	21300
273	19900
298	19000

Temp. (K)	CTE (1/K)
223	1.545E-5
410	5.020E-5
435.5	3.901E-5

Poisson's Ratio
0.3

323	18100	573	4.192E-5	
373	16100			
423	2200			
498	600			

Table 2.5. Substrate material properties (Intel).

Young's Modulus (MPa)	Shear Modulus (MPa)	CTE (1/K)	Poisson's Ratio
29664 – 39.455T (X,Y) 7800 (Z)	1520 (X,Y) 152 (Z)	1.6×10^{-5} (X,Y) 6×10^{-5} (Z)	0.39 (X,Y,Z)

Table 2.6. Solder ball material properties (Intel).

Young's Modulus (MPa)	CTE (1/K)	Poisson's Ratio
75827 – 151.64T	$2\times10^{-5} + 2\times10^{-8}$T	0.35

Table 2.7. Printed circuit board material properties (Intel).

Young's Modulus (MPa)	Shear Modulus (MPa)	CTE (1/K)	Poisson's Ratio
29664 – 39.455T (X,Y) 7800 (Z)	1520 (X,Y) 152 (Z)	1.6×10^{-5} (X,Y) 6×10^{-5} (Z)	0.39 (X,Y,Z)

Table 2.8. Substrate mask/PCB mask material properties (Intel).

Young's Modulus (MPa)	CTE (1/K)	Poisson's Ratio
4137	30×10^{-6}	0.40

T is material properties temperature in Kelvin

2.3.1 Anand's constitutive model and Darveaux's constitutive model

Anand (1982) presented a constitutive model to describe the deformation of metals at elevated temperature. Anand's model is described by equations (1) to (4).

$$\frac{d\varepsilon_p}{dt} = A\exp\left(-\frac{Q}{kT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \tag{1}$$

$$\frac{ds}{dt} = \left[h_o\left(|B|\right)^{a'}\frac{B}{|B|}\right]\frac{d\varepsilon_p}{dt} \tag{2}$$

$$B = 1 - \frac{s}{s^*} \tag{3}$$

$$s^* = s\hat{}\left[\frac{d\varepsilon_p / dt}{A}\exp\left(\frac{Q}{kT}\right)\right]^n \tag{4}$$

where $\frac{d\varepsilon_p}{dt}$ is the effective inelastic deformation rate

s is the initial value of deformation resistance

Q/k is the activation energy/Boltzmann's constant

A is the pre-exponential factor

ξ is the multiplier of stress

m is the strain rate sensitivity of stress

h_o is the hardening constant

$s\hat{}$ is the coefficient for deformation resistance saturation value

n is the strain rate sensitivity of saturation value

a' is the strain rate sensitivity of hardening

Anand's constitutive relations are proposed for rate-dependent viscoplasticity model. Plasticity is defined by the propensity of a material to undergo permanent deformation under

load. Viscoplasticity is defined when creep is taken into consideration with plasticity. Anand's model however does not consider rate-independent plasticity.

Darveaux (2000) has through his work presented his constitutive relations that describe the deformation behaviour of solder joints through equations (5) to (9) as shown below. Steady state creep of solder is expressed by the relationship of

$$\frac{d\varepsilon_s}{dt} = C_{ss}[\sinh(\alpha\sigma)]^n \exp\left(-\frac{Q_a}{kT}\right) \tag{5}$$

where $\frac{d\varepsilon_s}{dt}$ is the steady state strain rate, k is the Boltzmann's constant, T is the absolute temperature, σ is the applied stress, Q_a is the apparent activation energy, n is the stress exponent, α prescribes the stress level at which the power law dependence breaks down, and C_{ss} is a constant.

Transient creep at constant stress and temperature can be described by

$$\varepsilon_c = \frac{d\varepsilon_s}{dt}t + \varepsilon_T\left(1-\exp\left(-B\frac{d\varepsilon_s}{dt}t\right)\right) \tag{6}$$

where ε_c is the creep strain, $\frac{d\varepsilon_s}{dt}$ is the steady state creep rate, ε_T is the transient creep strain, and B is the transient creep coefficient.

The instantaneous creep rate is given by

$$\frac{d\varepsilon_c}{dt} = \frac{d\varepsilon_s}{dt}\left(1 + \varepsilon_T B \exp\left(-B\frac{d\varepsilon_s}{dt}t\right)\right) \tag{7}$$

where $\frac{d\varepsilon_s}{dt}$ is the steady state creep rate.

There is also a time-independent plastic strain component to the deformation at high stresses when $\tau/G > 10^{-3}$.

$$\varepsilon_p = C_p\left(\frac{\sigma}{G}\right)^{m_p} \tag{8}$$

where ε_p is the time-independent plastic strain, G is the shear modulus, and C_p and m_p are constants. This component is not considered in Anand's model. The total inelastic strain is given by the sum of creep strain and plastic strain

$$\varepsilon_{in} = \varepsilon_c + \varepsilon_p \tag{9}$$

where ε_{in} is the total inelastic strain.

As mentioned earlier, equation (8) is the time-independent plastic strain which has not been taken into consideration by Anand's model as Anand's model is only meant for a rate-dependent plasticity approach. Darveaux's model however incorporates both the time-independent plasticity as well as the time-dependent phenomenon. Due to this reason, Darveaux's model is adopted. However, Darveaux has also noted that many commercial finite element analysis softwares do not have his proposed constitutive relations incorporated.

ANSYS™ for example has viscoplastic elements as a standard option but utilizes Anand's constitutive model. Therefore, in order to include time-independent plasticity, Darveaux utilized an iterative process to determine the Anand constants that provide results which is comparable to results obtained by Darveaux's model. By doing this, Darveaux has modified the constants in Anand's constitutive relation to account for both time-dependent and time-independent phenomenon. These modified Anand constants are given in Table 2.9. Using ANSYS™ as the finite element analysis tool, the Anand plasticity data table is activated for the solder ball material and the constants listed in Table 2.9 are incorporated into the simulation. Solder ball materials are meshed in ANSYS™ using the VISCO107 elements, whereas all other package materials are meshed using SOLID45 elements.

Table 2.9. Darveaux modified Anand constants (Darveaux, 2000).

Constant	Parameter	Value	Definition
C1	S_o (MPa)	12.41	Initial Value of Deformation Resistance
C2	Q/R (1/Kelvin)	9400	Activation Energy/Boltzmann's Constant
C3	A (1/sec)	4.0E+06	Pre-Exponential Factor
C4	ξ (dimensionless)	1.5	Multiplier of Stress
C5	m (dimensionless)	0.303	Strain Rate Sensitivity of Stress
C6	h_o (MPa)	1378.95	Hardening Constant
C7	s (MPa)	13.79	Coefficient of Deformation Resistance Saturation Value
C8	n (dimensionless)	0.07	Deformation Resistance Value
C9	a (dimensionless)	1.3	Strain Rate Sensitivity of Hardening

2.4 Solder Joint Fatigue Life Prediction Methodology

Darveaux (2000) utilized two different methodologies to calculate the strain energy density accumulation in solder joints. The first method was based on non-linear Finite Element

Analysis. Simulations were carried out with a slice model as well as with a quarter symmetry model to calculate the plastic work per unit volume (or viscoplastic strain energy density). The second method was a combination of a linear finite element analysis to calculate assembly stiffness and imposed strain on the solder joints plus a non-linear analysis to calculate strain energy density.

Besides that, Darveaux had also carried out a series of tests using ceramic chip carriers and eutectic ball grid array joints with 8 thermal cycle conditions. Crack length measurements were carried out for all the tests involved and the measured crack growth data are correlated with the calculated inelastic strain energy density. The crack growth data were fit into the equations for crack initiation "N_o" and crack propagation rate "da/dN" as shown in equations (10) and (11).

$$N_o = K1(\Delta W_{ave})^{K2} \tag{10}$$

$$\frac{da}{dN} = K3(\Delta W_{ave})^{K4} \tag{11}$$

"ΔW_{ave}" is the element volumetric average of the stabilized change in plastic work within the controlled eutectic solder element thickness. *K1*, *K2*, *K3*, and *K4* are crack growth correlation constants.

By measuring the crack growth rate of actual solder joints under a series of tests and thermal cycle conditions, Darveaux (2000) was able to correlate the measured crack growth data with calculated inelastic strain energy density per cycle in the solder. Using the crack growth data, Darveaux was able to establish the four crack growth correlation constants (K1 through K4) in equations (10) and (11).

However, precautions must be taken as the methodology is sensitive to the finite element modeling procedure. Care must be taken in controlling the element thickness at the interface between the eutectic solder and substrate pad. Element volumetric averaging must also be used since the calculated strain energy density increases as element size in the solder joint decreases. This procedure reduces singularity issues whereby the sensitivity of the finite element meshing affects the plastic work simulation results.

Darveaux (2000) provided crack growth correlation constants for fifteen different configurations using ANSYS that include the type of finite element model used, the simulation method involved, the time step scheme of the simulations and the thickness of element layers in averaging. Since the models used in this work are slice models that utilizes ANSYS for non-linear finite element analysis, there are only two configurations given by Darveaux that fits these criteria. The only difference between the two configurations is the choice of a fine or course time step scheme. Both configurations require that the element interface thickness is at 0.0254 mm (1 mil). In the present work, a fine time step scheme is chosen and the only set of crack growth correlation constants that fit into all the above mentioned criteria are shown in Table 2.10.

Table 2.10. Darveaux K1 through K4 crack growth correlation constants.

Constant	Value
K1	22400 cycles/psi
K2	-1.52
K3	5.86×10^{-7} in/cycle/psi
K4	0.98

With the crack growth correlation constants in Table 2.10 and the calculated strain energy density obtained by ANSYS simulation, the characteristic solder joint fatigue life "α_w" can then

be calculated by summing the cycles to crack initiation with the number of cycles it takes for the crack to propagate across the entire solder joint diameter "a" as shown in equation (12). "α_w" is defined as the characteristic life at which 63.2% of the population (sample) in a test has failed and "α_w" is a deterministic function. However, "α_w" can further be used to find out the cumulative distribution of failures by calculating cycles to first failure and the failure free life of a certain sample size (Darveaux, 2000).

$$\alpha_w = N_o + \frac{a}{da/dN} \tag{12}$$

Zahn (2000a) has also noted that material intermetallic layers normally present at the solder pad/solder ball interfaces have mechanical influences on the fatigue life of the solder joints. These effects are not directly included in the finite element models. However, since Darveaux derived his fatigue life prediction methodology using actual measurement data of solder joints, which are presumed to have similar intermetallic structures, their influence can be assumed to have been indirectly taken into consideration in the predicted results.

2.5 Temperature Cycling Tests: B-Test and X-Test

Two temperature cycle profile known as B-test and X-test are used for the simulations. Each test has distinctively different profile and temperature ranges. The B-test is a standard temperature cycling procedure documented in the JEDEC standard JESD22-A104-B. JEDEC (Joint Electronic Device Executive Council) is an organization that prepares and publishes test standards designed to serve the public interest. The X-test is an industry standard provided by Intel Technology Sdn. Bhd.

For both the simplified and the detail model, two simulations are carried out, namely the B-test and the X-test. The temperature cycle profiles for a B-test and an X-test are shown in Figs. 2.15 and 2.16 respectively. As seen from Figs. 2.15 and 2.16, the B-test is more stringent where package assembly is subjected to higher temperature range. In the B-test, the package assembly is also being subjected to a maintained highest and lowest temperature loading for a period of time. In comparison, the X-test has a relatively more relaxed temperature cycling range where the extremes of the temperature range are lower than that of the B-test. The package assembly is also not subjected to a maintained temperature loading at the highest and lowest temperature in the X-test.

The microelectronic industry selectively applied different test conditions to simulate the different types of environment in which the final product with the flip chip package is being targeted for used.

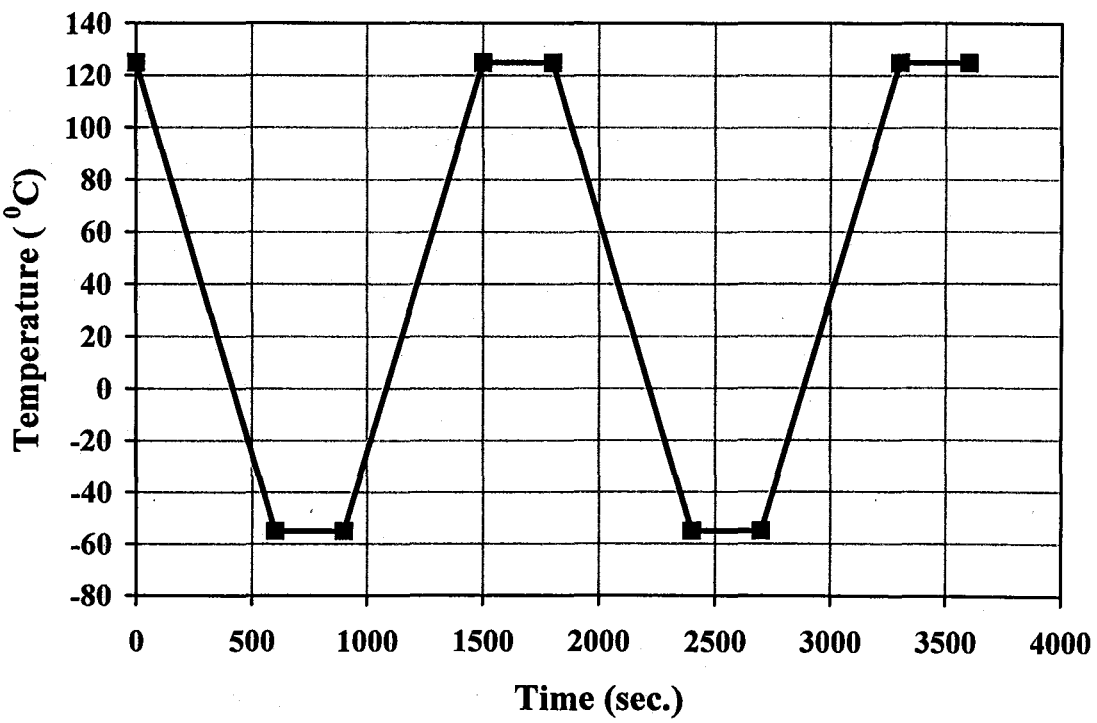


Fig. 2.15.

Temperature cycling test B.

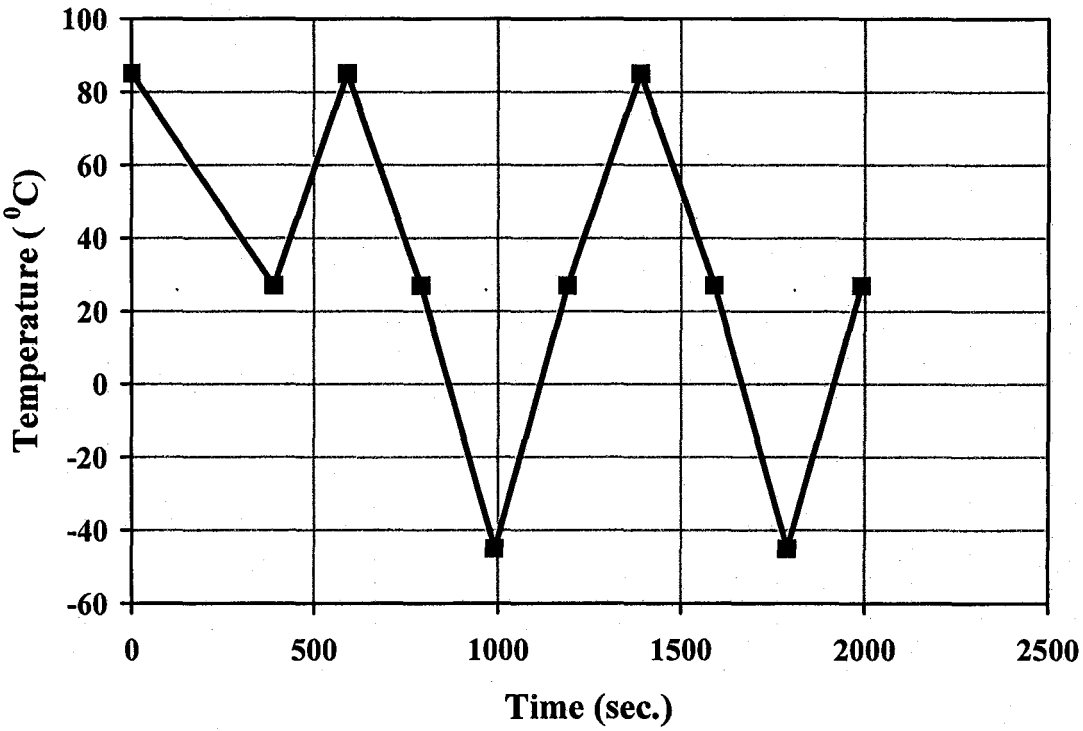


Fig. 2.16. Temperature cycling test X.

2.6 ANSYS^{TM} Solution Methodology

Three dimensional non-linear finite element modeling is used to calculate the strain energy density accumulation in solder joints. ANSYS^{TM} is used to model the three-dimensional finite element diagonal slice model of the flip chip package. The solder material is modeled as a viscoplastic solid, the printed circuit boards as orthotropic linear elastic solids, and the rest of the materials as linear elastic solids. The printed circuit boards are modeled as orthotropic solids because many different layers of materials exist within the PCBs. Due to this reason, PCB can no longer be considered as isotropic material as the material properties is no longer independent of direction. PCBs may have different elastic constants (Young's modulus, Poisson's ratio, and shear modulus) in the three principle directions.

The goal of the simulations is to calculate the plastic work per unit volume or viscoplastic strain energy density accumulated per thermal cycle. Two thermal cycles were simulated in order to establish a stable stress-strain hysteresis loop. Through experience and observation of other publications that incorporate Darveaux's methodology, Zahn (2000a) has indicated in his work that the difference in life prediction by a two thermal cycle's simulation and a three thermal cycle's simulation is less than 5%. However, by simulating only two thermal cycles instead of three thermal cycles, 30-35% of simulation run times can be reduced. The plastic work accumulated during the last cycle was used for all crack growth correlations.

Once the diagonal slice model has been completed and appropriately meshed as shown in Figs. 2.9 and 2.13, the boundary constraints as shown in Fig. 2.6 are applied to the model. Having done this, the following ANSYS™ solution setup commands, as shown in Zahn (2000a) are used to initiate the simulation.

```
!SET SOLUTION OPTIONS
/solu                   !enter solution processor
eqslv,pcg,1.0e-08       !set solver and tolerance
antype, static, new     !set analysis type
nlgeom, on              !set large def and strain
nropt,auto,,off         !set Newton-raphson solution
outres,all,last         !write data to .rst file
```

Variables such as temperature and time used in the thermal cycle can be set in ANSYS™ using variable names and equations. The analysis will use one substep for every 10 degrees K of temperature change in a thermal ramp load step as suggested by Darveaux (2000) and as calculated by the variable "rmpstp". Once the solution setup is complete and the solution variables are set, the commands to initiate the two thermal cycles for each test conditions can be entered.

For the B-test, the ANSYS™ zero strain reference temperature is set to the high temperature "hitmp" of the thermal cycle sequence. Each thermal cycle in the B-test consists of four load steps (ramp low, dwell low, ramp high, and dwell high). Thus a complete B-test

simulation of two thermal cycles consists of eight load steps. For the X-test, the reference temperature is set as the assembly temperature. In the X-test, the first load step ramps low from the assembly temperature to the room temperature. Then the following four load steps (ramp high, ramp low, ramp low, ramp high) define the first thermal cycle. Therefore, a complete X-test simulation of two thermal cycles consists of nine load steps.

The following sequence of ANSYS™ commands indicates the setting of thermal cycle variables and the setting of the zero strain reference temperature in the B-Test. The commands required for the first thermal cycle and the second thermal cycle are included as well.

B-Test:

```
!SET THERMAL CYCLE VARIABLES
hitmp = 125+273              !set high cycle temperature (K)
hirmp = 10*60                !set low-high ramp time (sec)
hidwl = 5*60                 !set high dwell time (sec)

lotmp = -55+273              !set low cycle temp (K)
lormp = 10*60                !set high-low ramp time (sec)
lodwl = 5*60                 !set low dwell time (sec)
delta = hitmp-lotmp          !calculate delta temperature
rmpstp = delta/10            !calculate ramp substeps

tref,hitmp                   !set zero strain temp

!RAMP LOW (LOAD STEP 1)
autots,off                   !turn off auto time step
nsubstp,rmpstp               !set substeps
bf,all,temp,lotmp            !apply temp to all nodes
kbc,0                        !linearly ramp loads
time,lormp                   !set time
lswrite,1                    !write load step file 1

!DWELL LOW (LOAD STEP 2)
autots,on                    !turn on auto time step
nsubstp,10,100,1             !set substeps
bf,all,temp,lotmp            !apply temp to all nodes
kbc,1                        !maintain loads
time,lormp+lodwl             !set time
lswrite,2                    !write load step file 2

!RAMP HIGH (LOAD STEP 3)
```

```
autots,off                          !turn off auto time step
nsubstp,rmpstp                      !set substeps
bf,all,temp,hitmp                   !apply temp to all nodes
kbc,0                               !linearly ramp loads
time,lormp+lodwl+hirmp              !set time
lswrite,3                           !write load step file 3

!DWELL HIGH (LOAD STEP 4)
autots,on                           !turn on auto time step
nsubstp,10,100,1                    !set substeps
bf,all,temp,hitmp                   !apply temp to all nodes
kbc,1                               !maintain loads
time,lormp+lodwl+hirmp+hidwl        !set time
lswrite,4                           !write load step file 4
```

To continue with second thermal cycle, the above ANSYS™ command groups for load steps 1 through 4 are repeated. However, the t-value indicating time in the ANSYS™ "time,t" command for load steps 5 through 8 must be adjusted appropriately. This can be done by adding a multiplier in front of each of the time constants for load steps 5 through 8 respectively as follows:

```
time,2*lormp+lodwl+hirmp+hidwl          !LS5
time,2*lormp+2*lodwl+hirmp+hidwl        !LS6
time,2*lormp+2*lodwl+2*hirmp+hidwl      !LS7
time,2*lormp+2*lodwl+2*hirmp+2*hidwl    !LS8
```

To execute the eight load steps written to the ANSYS™ load step files, the following command is used to solve all the eight load steps.

```
lssolve,1,8,1                       !solve all load step files
```

X-Test:

```
!SET THERMAL CYCLE VARIABLES
```

```
asstmp = 85+273         !set assembly temp (K)
hitmp = 85+273          !set high cycle temp (K)
rotmp = 27+273          !set room temp (K)
lotmp = -45+273         !set low cycle temp (K)

assrmp = 390     !set assembly temp to room temp ramp time (sec)
rohirmp = 200    !set room-high temp ramp time (sec)
hirormp = 200    !set high-room temp ramp time (sec)
rolormp = 200    !set room-low temp ramp time (sec)
lorormp = 200    !set low-room temp ramp time (sec)

deltaa = asstmp-rotmp       !calc delta temp A
rmpstpa = deltaa/10         !calc ramp substeps A
deltab = hitmp-rotmp        !calc delta temp B
rmpstpb = deltab/10         !calc ramp substeps B
deltac = rotmp-lotmp        !calc delta temp C
rmpstpc = deltac/10         !calc ramp substeps C

tref,asstmp                 !set zero strain temp

!RAMP LOW (LOAD STEP 1)
autots,off
nsubstp,rmpstpa
bf,all,temp,rotmp
kbc,0
time,assrmp
lswrite,1

!RAMP HIGH (LOAD STEP 2)
autots,off
nsubstp,rmpstpb
bf,all,temp,hitmp
kbc,0
time,asstmp+rohirmp
lswrite,2

!RAMP LOW (LOAD STEP 3)
autots,off
nsubstp,rmpstpb
bf,all,temp,rotmp
kbc,0
time,assrmp+rohirmp+hirormp
lswrite,3

!RAMP LOW (LOAD STEP 4)
autots,off
nsubstp,rmpstpc
bf,all,temp,lotmp
kbc,0
time,assrmp+rohirmp+hirormp+rolormp
lswrite,4
```

```
!RAMP HIGH (LOAD STEP 5)
autots,off
nsubstp,rmpstpc
bf,all,temp,rotmp
kbc,0
time,assrmp+rohirmp+hirormp+rolormp+lorormp
lswrite,5
```

To continue with the second thermal cycle, the above ANSYS™ command groups for load steps 2 through 5 are repeated. However, the t-value indicating time in the ANSYS™ "time,t" command for load steps 6 through 9 must be adjusted accordingly. This can be done by adding a multiplier in front of each of the time constants for load steps 6 through 9 respectively as follows:

```
time,assrmp+2*rohirmp+hirormp+rolormp+lorormp          !LS6
time,assrmp+2*rohirmp+2*hirormp+rolormp+lorormp        !LS7
time,assrmp+2*rohirmp+2*hirormp+2*rolormp+lorormp      !LS8
time,assrmp+2*rohirmp+2*hirormp+2*rolormp+2*lorormp    !LS9
```

To execute the nine load steps written to the ANSYS™ load step files, the following command is used.

```
lssolve,1,9,1                !solve all load step files
```

Once the two thermal cycles (eight load steps for B-test and nine load steps for X-test) have completed execution, it is necessary to obtain the ΔW_{ave} for the worst-case solder joint. The worst-case solder joint can be identified by plotting the nodal plastic work of the solder ball materials at the end of the last load step. Once the worst-case solder joint has been identified, only the 0.0254mm (1 mil) thick layer of solder ball material elements at the joint interface are selected using the ANSYS™ ESEL (element select) command. Once the 0.0254 mm thick layer of solder ball material elements which make up the solder joint have been selected within

ANSYS™, the below sequence of ANSYS™ commands are then used to calculate ΔW_{ave}. The set of commands below are for a B-test. An X-test uses the same commands below with the exception of that of the first line for each cycle.

```
!CALC AVG PLASTIC WORK FOR CYCLE 1
set,4,last,1          !for X-test, use the command: set,5,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
wavg1=sumplwk/sumvolu

!CALC AVG PLASTIC WORK FOR CYCLE 2
set,8,last,1          !for X-test, use the command: set,9,last,1
etable,vtable,volu
etable,vsetable,nl,plwk
smult,pwtable,vtable,vsetable
ssum
*get,sumplwk,ssum,,item,pwtable
*get,sumvolu,ssum,,item,vtable
wavg2=sumplwk/sumvolu

!CALC DELTA AVG PLASTIC WORK
dwavg=wavg2-wavg1
```

Since Darveaux provides crack growth correlation constants in English units, it is important to remember to convert the simulated ΔW_{ave} (ANSYS™ constant "dwavg") from units of MPa to units of psi. Also, the solder joint diameter should be converted from units of mm to units of inches. These values can then be substituted into equations (10) through (12) to obtain cycles to crack initiation, crack propagation rate, and solder joint characteristic fatigue life respectively.

2.7 Summary

A non-linear finite element analysis approach will be utilized to predict the fatigue life of solder joints. ANSYS™ will be used as the finite element simulation software tool. A general approach in the prediction of solder joint fatigue life is shown in Fig. 2.17. As seen from Fig. 2.17, a typical slice model of the package assembly is first created in ANSYS™. The slice model will be used in the finite element simulations and subjected to two temperature cycling profiles. The strain energy density accumulated per cycle can then be determined in the post processing of each simulation. Based on the type of analysis carried out and also the model used in the simulation, four crack growth correlation constants can be determined (Darveaux, 2000). Using the crack growth correlation constants and the strain energy density calculated, the number of cycles to crack initiation can be calculated. Also by using the crack growth correlation constants and the number of cycles to crack initiation, the crack growth rate per thermal cycle can be determined. Finally, the characteristic solder joint fatigue life can be calculated using the number of cycles to crack initiation, the crack propagation rate and the joint diameter at the interface of the solder ball. Artificial Neural Network (ANN) and Genetic Algorithm (GA) will then be used for parametric study and optimization.

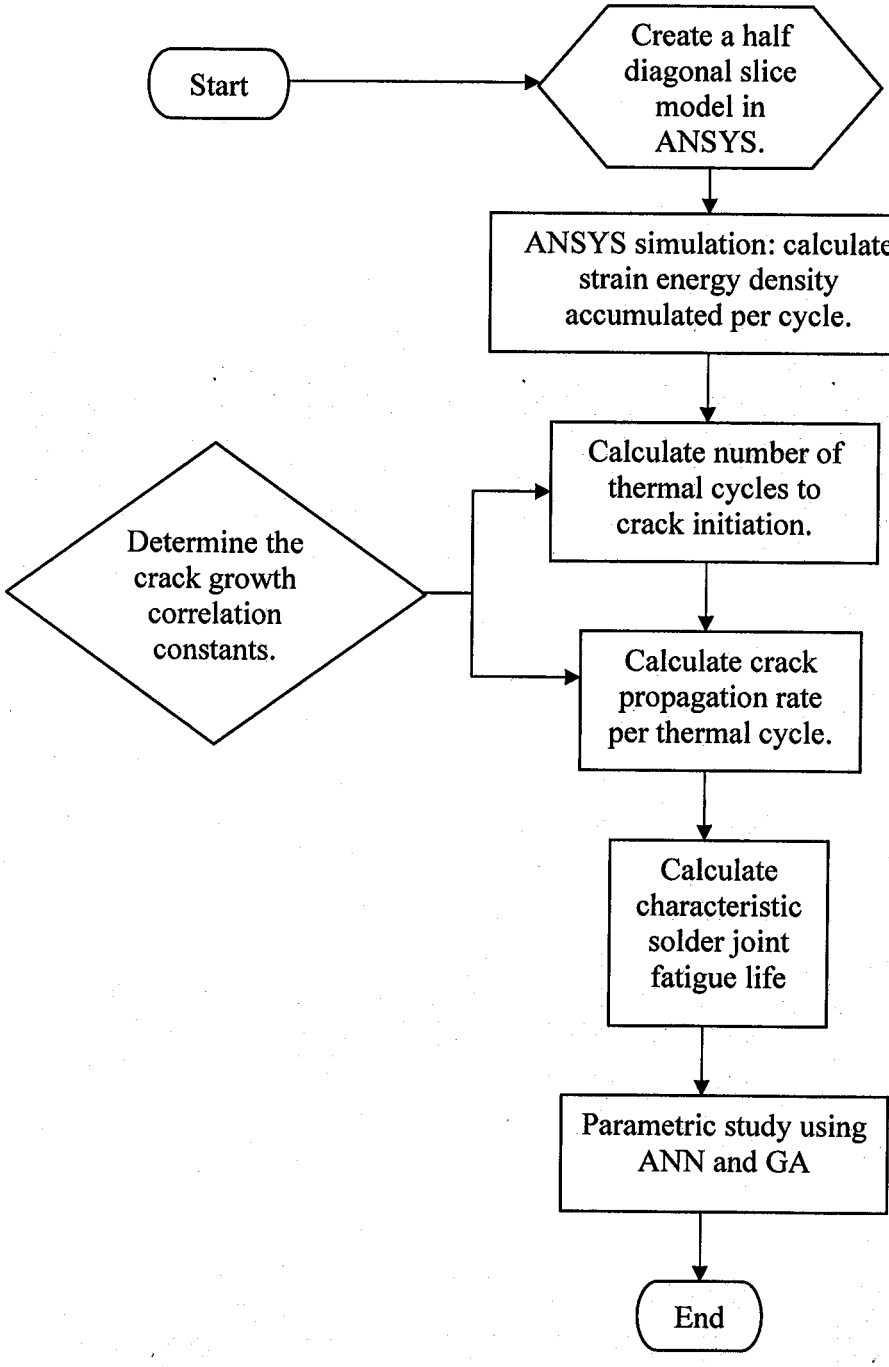


Fig. 2.17 Solder joint fatigue life prediction method.

CHAPTER 3
RESULTS AND DISCUSSION

3.1 Results

Two diagonal slice models are created to study the effect of model simplification on the solder ball joint fatigue life. The first model is the simplified flip chip slice model shown in Fig. 2.7 and the second model is the detailed flip chip model shown in Fig. 2.11. Both slice models are subjected to two different test conditions, namely a B-test condition and an X-test condition. The interest of each simulation is to study the fatigue life of the solder joint interfaces, both at the ball/substrate interface and at the ball/board interface. Results shown subsequently will be listed as follows:

i) Simplified Model: B-Test (3 view angle of worst-case solder ball)

ii) Simplified Model: X-Test (3 view angle of worst-case solder ball)

iii) Detailed Model: B-Test (3 view angle of worst-case solder ball)

iv) Detailed Model: X-Test (3 view angle of worst-case solder ball)

Graphical plots of nodal solution will concentrate on the von Mises stress distribution of the worst-case solder ball joint and the corresponding solder joint plastic work. Since the interest of this work is to study the stresses at the solder ball joint interfaces, only plots of von Mises nodal stress distribution at the worst case solder balls are selected to be displayed. Von Mises equation as defined in ANSYS 7.0 Documentation, is a measure of shear strain in a material. The equivalent strain for the elastic, plastic, creep and thermal strains are computed in postprocessing using the von Mises equation. Therefore, von Mises stress is chosen because this stress is

directly related to the distortion energy and is appropriate for material undergoing plastic deformation.

Section 3.2 will highlight the results obtained for the simplified slice model and subsequently, section 3.3 will highlight the results obtained for the detailed slice model. For each section, results for B-test will be shown first followed by results of X-test. All figures shown in the two sections are nodal solution plots of the worst-case solder joint which are at the eighth solder ball from the package centre.

3.2 Simplified Flip Chip Model

3.2.1 B-Test

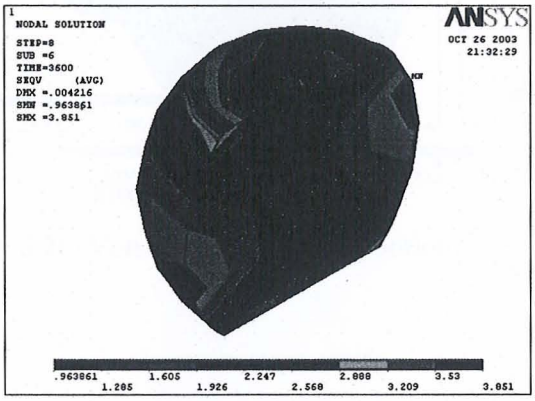


Fig. 3.1a. Von Mises stress distribution.

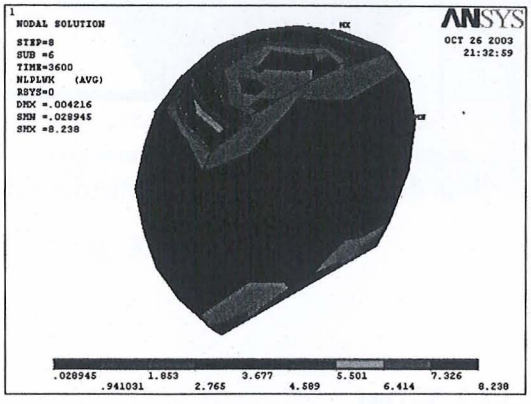


Fig. 3.1b. Plastic work

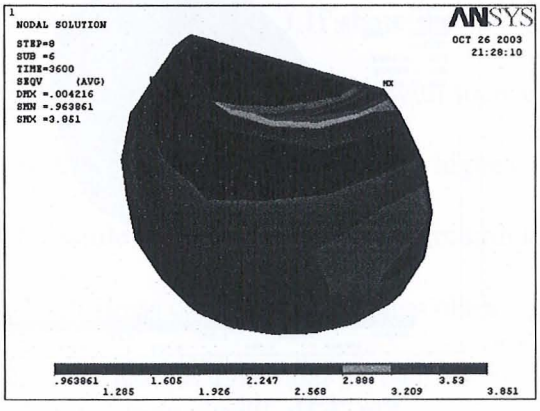


Fig. 3.1c. Von Mises stress distribution.

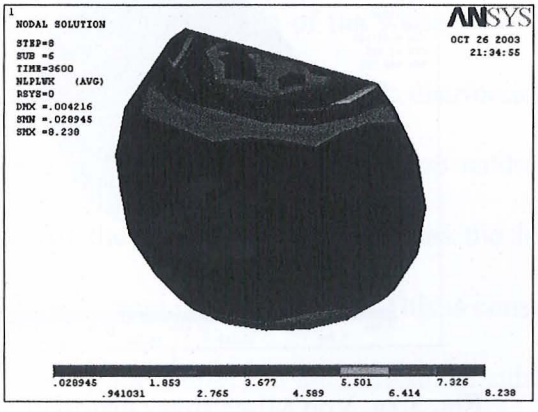


Fig. 3.1d. Plastic work

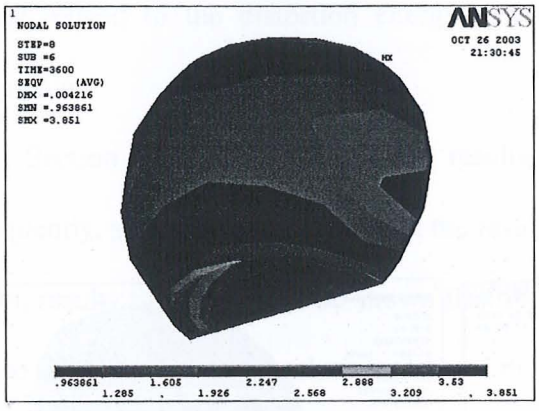


Fig. 3.1e. Von Mises stress distribution.

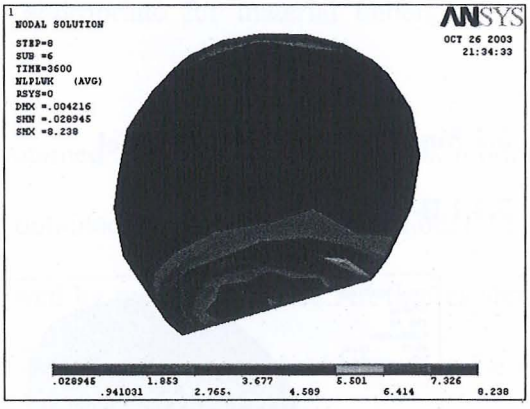


Fig. 3.1f. Plastic work

3.2.2 X-Test

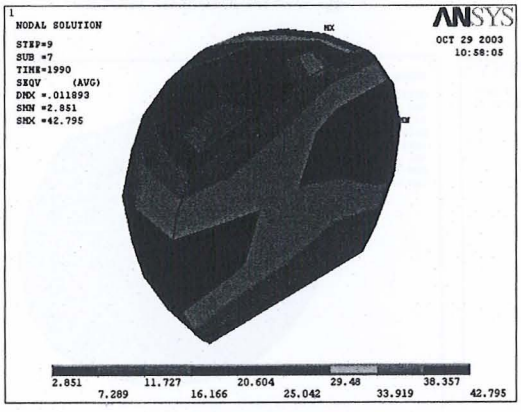


Fig. 3.2a. Von Mises stress distribution.

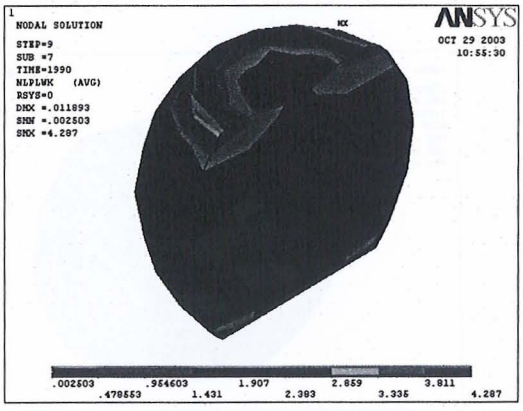
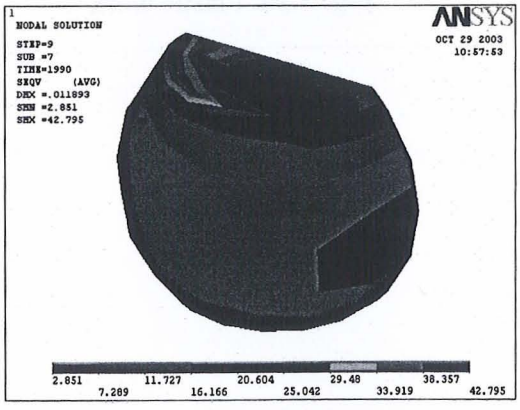


Fig. 3.2b. Plastic work



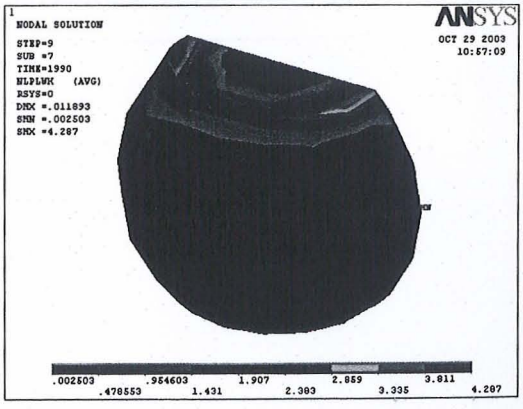


Fig. 3.2c. Von Mises stress distribution.

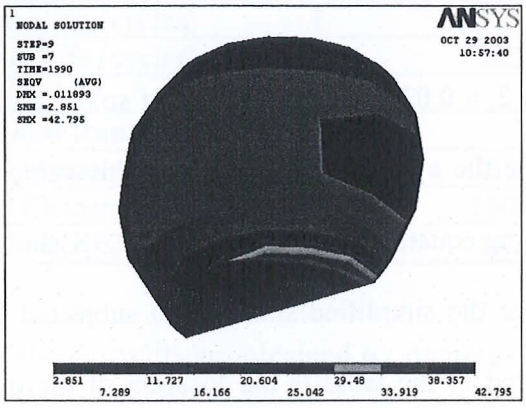


Fig. 3.2d. Plastic work

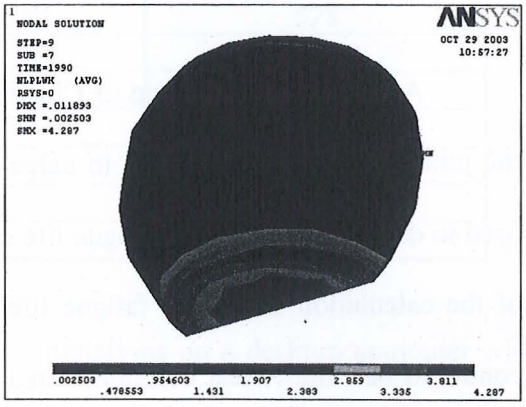


Fig. 3.2e. Von Mises stress distribution.

Fig. 3.2f. Plastic work

3.2.3 Simulation Results

Figs. 3.1a through 3.1f show the von Mises stress distribution of the worst-case solder joint at three different view angles with their corresponding solder plastic work distribution for the B-test. As seen from the figures, highest stress occurs at the edge of the top solder ball interface while the area around the circumference of the solder ball diameter has the lowest stress. High stress concentration is also observed at the bottom solder interface. This is consistent with the fact that the top solder surface and the bottom solder surface is attached to the substrate and printed circuit board respectively. Therefore, differing expansion of package components due to thermal mismatch of the various package materials will cause high stress concentration at the solder ball interfaces. The solder plastic work distribution also indicates that high stress concentration area also has high plastic work done.

Figs. 3.2a through 3.2f also show similar von Mises stress distribution of the worst-case solder joint at three different view angles with their respective solder plastic work distribution for

the X-test. Similar trends as discussed in the previous paragraph are also observed from the figures.

As indicated at the end of Chapter 2, a 0.0254mm thick layer of solder ball elements at the joint interfaces are selected to calculate the averaged plastic work. This value will then be used to determine the solder fatigue life using equations (10) to (12). Table 3.1 shows the results of the calculation for solder fatigue life for the simplified slice model subjected to the B-test condition and the X-test condition. Included in the table is the location of the diagonal slice model failure ball (from the model centre). Also included is the viscoplastic strain energy density which is substituted into Equations (10) and (11) to calculate cycles to crack initiation and crack propagation rate respectively. The solder joint diameter, cycles for the crack to propagate across this diameter, and the characteristic solder joint fatigue life (63.2% population failure) are also provided in Table 3.1.

Table 3.1. Results for simplified flip chip model.

Data Description	B-Test (-55°C to 125°C)	X-Test (-45°C to 85°C)
Ball/Substrate Solder Joint		
Failure Joint (From Centre)	8	8
Delta Plastic Work/Cycle (MPa)	1.0620	0.4506
Delta Plastic Work/Cycle (psi)	154.02	65.35
Crack Initiation (cycles)	11	39
Crack Growth Rate (mm/cycle)	0.2073E-02	0.8950E-03
Solder Joint Diameter (mm)	0.30	0.30
Crack Propagation (cycles)	145	335
Characteristic Life (cycles)	156	374
Ball/Board Solder Joint		
Failure Joint (From Centre)	8	8
Delta Plastic Work/Cycle (MPa)	0.8159	0.2587
Delta Plastic Work/Cycle (psi)	118.34	37.51
Crack Initiation (cycles)	16	91

Crack Growth Rate (mm/cycle)	0.1601E-02	0.5190E-03
Solder Joint Diameter (mm)	0.30	0.30
Crack Propagation (cycles)	187	578
Characteristic Life (cycles)	203	669
Model Size and Run Time Info.		
Total Model Nodes	7652	7652
Total Model Elements	5506	5506
CPU Run Time (Hrs)	1.02	0.88

The above results are obtained by running the simulations on a desktop computer with these specifications: (Pentium III Processor 1.0 GHz, 1 Gbyte RAM, Windows NT Professional operating system).

3.3 Detailed Flip Chip Model

3.3.1 B-Test

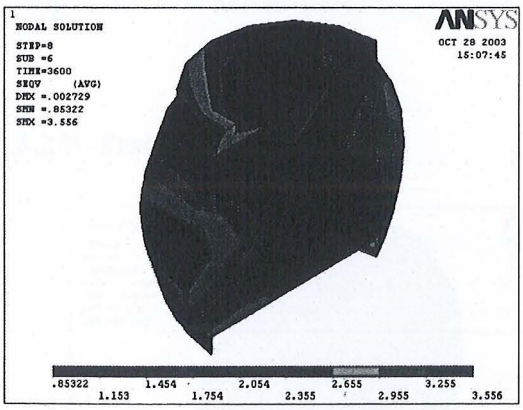


Fig. 3.3a. Von Mises stress distribution.

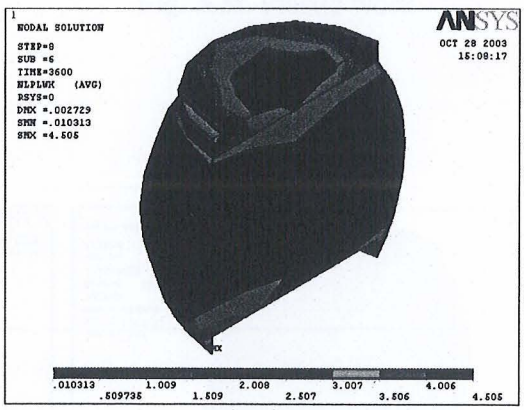


Fig. 3.3b. Plastic work

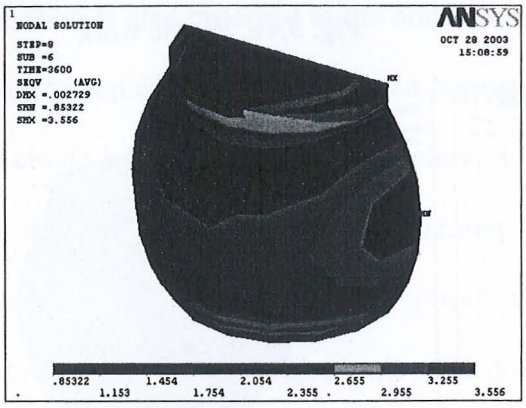


Fig. 3.3c. Von Mises stress distribution.

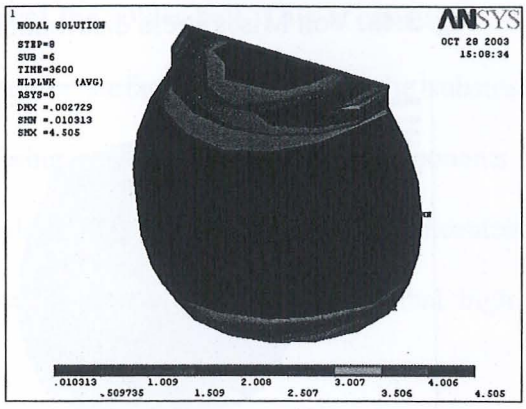


Fig. 3.3d. Plastic work

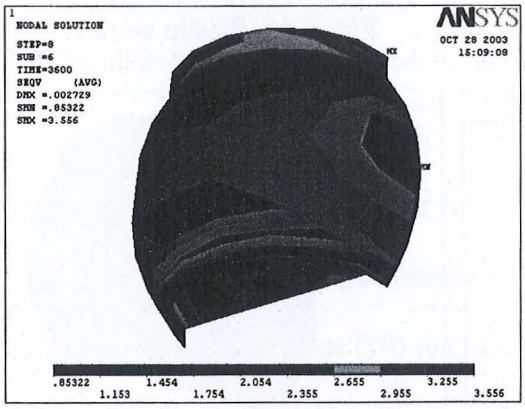


Fig. 3.3e. Von Mises stress distribution.

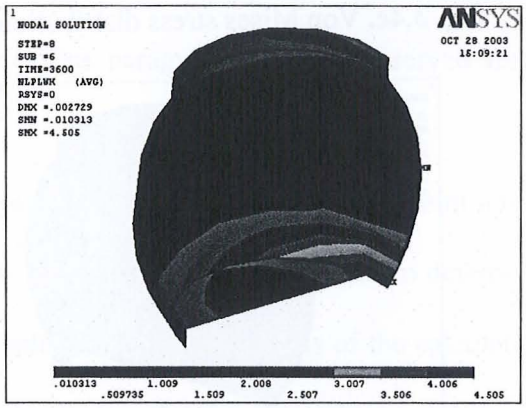
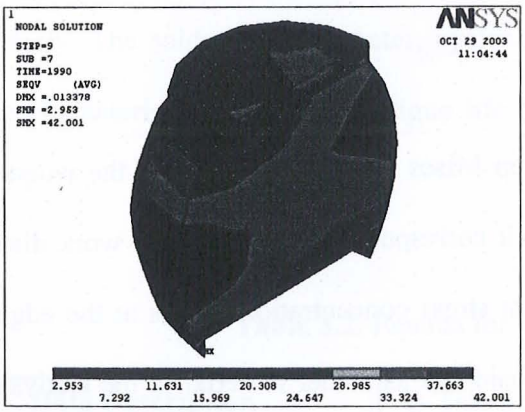


Fig. 3.3f. Plastic work

3.3.2 X-Test



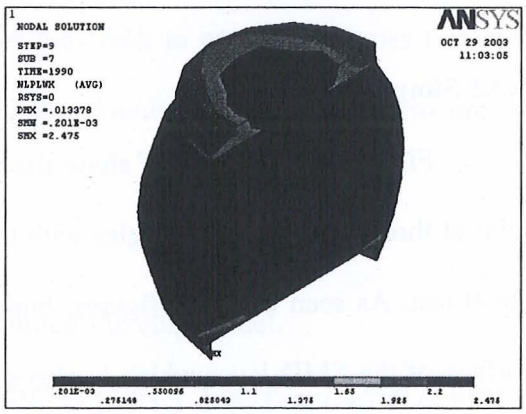


Fig. 3.4a. Von Mises stress distribution.

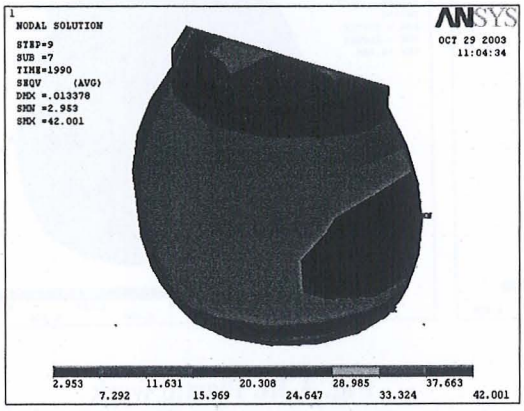


Fig. 3.4b. Plastic work

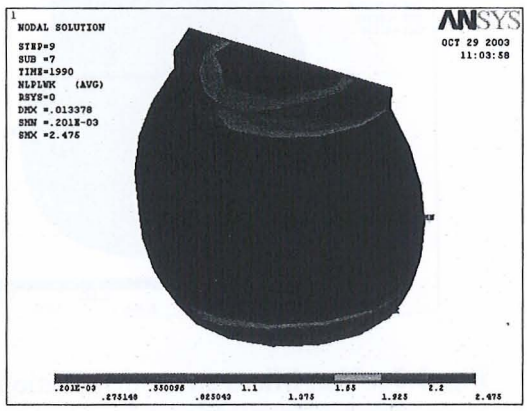


Fig. 3.4c. Von Mises stress distribution.

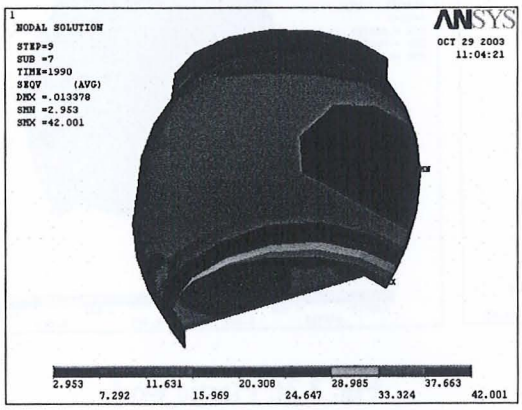


Fig. 3.4d. Plastic work

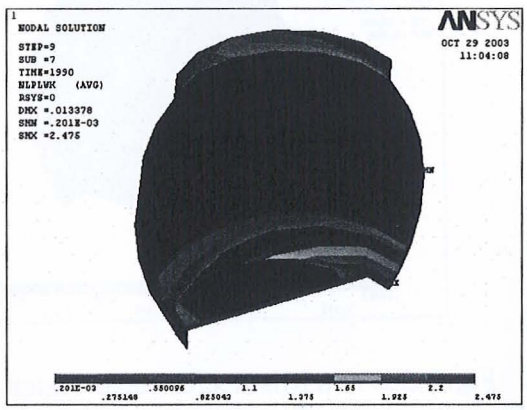


Fig. 3.4e. Von Mises stress distribution.

Fig. 3.4f. Plastic work

3.3.3 Simulation Results

Figs. 3.3a through 3.3f show the von Mises stress distribution of the worst-case solder joint at three different view angles with their corresponding solder plastic work distribution for the B-test. As seen from the figures, highest stress concentration occurs at the edge of the top surface of the SMD layer which is also considered as solder material in the analysis. The area around the circumference of the solder ball diameter also shows the lowest stress. High stress

concentration is also observed at the bottom edge of the solder ball. This is consistent with the fact that the top SMD surface and the bottom solder surface is attached to the substrate and printed circuit board respectively. Therefore, differing expansion of package components due to thermal mismatch of the various package materials will also cause high stress concentration at the solder ball interfaces. The solder plastic work distribution also indicates that high stress concentration area also has high plastic work done.

Figs. 3.4a through 3.4f also show similar von Mises stress distribution of the worst-case solder joint at three different view angles with their respective solder plastic work distribution for the X-test. Similar trends as discussed in the previous paragraph are also observed from the figures.

As indicated earlier, a 0.0254mm thick layer of solder ball elements at the joint interfaces are selected to calculate the averaged plastic work. This value will then be used to determine the solder fatigue life using equations (10) to (12). Table 3.2 shows the results of the calculation for solder fatigue life for the detailed slice model subjected to the B-test condition and the X-test condition. Included in the table is the location of the diagonal slice model failure ball (from the model centre). Also included is the viscoplastic strain energy density which is substituted into Equations (10) and (11) to calculate cycles to crack initiation and crack propagation rate respectively. The solder joint diameter, cycles for the crack to propagate across this diameter, and the characteristic solder joint fatigue life (63.2% population failure) are also provided in Table 3.2.

Table 3.2. Results for detailed flip chip model.

Data Description	B-Test (-55°C to 125°C)	X-Test (-45°C to 85°C)

Ball/Substrate Solder Joint		
Failure Joint (From Centre)	8	8
Delta Plastic Work/Cycle (MPa)	0.5407	0.1600
Delta Plastic Work/Cycle (psi)	78.42	23.21
Crack Initiation (cycles)	30	188
Crack Growth Rate (mm/cycle)	1.07E-03	0.324E-03
Solder Joint Diameter (mm)	0.30	0.30
Crack Propagation (cycles)	280	925
Characteristic Life (cycles)	310	1113
Ball/Board Solder Joint		
Failure Joint (From Centre)	8	8
Delta Plastic Work/Cycle (MPa)	0.3051	0.09119
Delta Plastic Work/Cycle (psi)	44.25	13.23
Crack Initiation (cycles)	71	442
Crack Growth Rate (mm/cycle)	0.6110E-03	0.1870E-03
Solder Joint Diameter (mm)	0.30	0.30
Crack Propagation (cycles)	491	1605
Characteristic Life (cycles)	562	2047
Model Size and Run Time Info.		
Total Model Nodes	9308	9308
Total Model Elements	6920	6920
CPU Run Time (Hrs)	1.58	1.38

The above results are obtained by running the simulations on a desktop computer with these specifications: (Pentium III Processor 1.0 GHz, 1 Gbyte RAM, Windows NT Professional operating system).

3.4 Discussion

Four simulations are done using two package diagonal slice models. Two of the simulations are carried out using the simplified flip chip model while the other two simulations are carried out using the detailed flip chip model. Tables 3.1 and 3.2 indicate the detailed simulation results for the two flip chip models.

Results of the stress distribution and plastic work distribution as shown in the figures in section 3.2 and section 3.3 are rarely seen in published literature as most of them are interested in the final solder joint fatigue life. Therefore comparison of solder stress distribution

with the literature is not a feasible option. However a general comparison of the solder fatigue life with published results can still be adopted to determine whether if the characteristic solder fatigue life calculated is acceptable.

In the overall comparison between the simplified flip chip model and the detailed flip chip model, the simplified models have a relatively shorter fatigue life compared to the detailed models. This indicates that no simplification should be done on the actual model, as this will only cause premature failure of the flip chip package. The results also show that small details at the solder joint interfaces are important to maintain the structural integrity of the flip chip package and hence, should be included in any simulation models used. From the four simulations carried out, inclusion of all the package layer details results in a doubled package fatigue life for the B-test and a tripled package fatigue life for the X-test. Therefore this also establishes that model simplification is not an option for this type of analysis.

Since model simplification has been ruled out, only results of solder life from the detailed model will be used for comparison with other published results. The present work as indicated in Table 3.2 shows that for the joint at the ball/substrate interface, solder life is 310 cycles for the B-test and 1113 cycles for the X-test. Results observed from Zahn (2000a), shows 8 different package configurations with different temperature cycles applied, producing solder lives at the ball/substrate interface that range from 287 cycles to 1130 cycles. Table 3.2 in the present work also shows that for the joint at the ball/board interface, solder life is 562 cycles for the B-test and 2047 cycles for the X-test. Similar comparison with Zahn (2000a) shows a solder life range for the ball/board interface to be from 690 cycles to 1536 cycles. Keeping in mind that none of the package configurations used by Zahn are similar to the present flip chip configuration adopted for this work and the temperature cycle profile used by Zahn is also different from the present B-test and X-test adopted, differences in the comparison of solder lives are expected. However, the ranges of solder joint life obtained in the present work are still within the generally acceptable range.

In all four simulations evaluated, the solder joint at the package substrate fails first while the fatigue life at the ball/board interface has almost double the life expectancy of that at the ball/substrate interfaces. The first failure ball at both solder ball joint interfaces for all simulations occurs at the eighth solder ball, which is the last solder ball from the package centre, at the diagonal edge of the package.

The next chapter will discuss about the package parametric study and the use of ANN and GA for optimization.

CHAPTER 4
PARAMETRIC STUDY AND OPTIMIZATION

4.1 Parametric Study

In the previous chapter, a comparison is made between the simplified flip chip model and the detailed flip chip model. From the results obtained, it is recommended that all simulations should be carried out using the detailed flip chip model. Keeping this in mind, the detailed flip chip model used in Chapter 3 is taken as the standard case model for a parametric study using the X-test condition.

For the parametric study, six package dimensions will be involved. The six package dimensions involved are the board thickness, the substrate thickness, the bottom die size, the solder ball standoff height, the top solder mask opening diameter and the bottom die thickness. A study will be carried out to look at the effect of each package dimension on the overall package fatigue life. The values of these parameters will be varied in a range so that the original values of each package dimension as in the standard case model fall in between the chosen ranges for each parameter. This is carried out in order to determine what the effect of increasing or decreasing a package dimension will have on the characteristic solder ball fatigue life. Values for the chosen ranges of the package dimensions should not deviate too much from the original model in the control case and they should also be physically possible to model (i.e. no intersection in between any two materials). For example, the bottom die size should not be smaller than the top die size and it should also be smaller than the package substrate size. Increments are chosen in a way that an additional five simulations can be done in between the specified ranges for each parameter.

The chosen ranges for each parameter and their respective increments are shown subsequently:

a) 1.17 mm ≤ **Board thickness** ≤ 2.17 mm with 0.2 mm increments

b) 0.108 mm ≤ **Substrate thickness** ≤ 0.208 mm with 0.02 mm increments

c) 5.6570 mm ≤ **Bottom die size** ≤ 8.4855 mm with 0.5657 mm increments

d) 0.27 mm ≤ **Solder ball standoff height** ≤ 0.32 mm with 0.01 mm increments

e) 0.3154 mm ≤ **Top solder mask opening diameter** ≤ 0.3654 mm with 0.01 mm increments

f) 0.11 mm ≤ **Bottom die thickness** ≤ 0.16 mm with 0.01 mm increments

All together, an additional 30 simulations are carried out for the parametric study. A summary of the simulated results is shown in Table 4.1.

Table 4.1. X-Test Parametric Study

X-Test parametric study (Detailed Flip Chip Model)								
Simulation No.	Parameters						Life Cycles	
	Board Thickness	Substrate Thickness	Bottom Die Size	Solder Ball Height	Solder Mask Opening	Bottom Die Thickness	Ball/ Substrate Interface	Ball/ Board Interface
1	**1.17**	0.168	7.9198	0.3	0.3254	0.13	1807	3666
2	**1.37**	0.168	7.9198	0.3	0.3254	0.13	1380	2634

3	**1.77**	0.168	7.9198	0.3	0.3254	0.13	938	1687
4	**1.97**	0.168	7.9198	0.3	0.3254	0.13	818	1448
5	**2.17**	0.168	7.9198	0.3	0.3254	0.13	732	1282
6	1.57	**0.108**	7.9198	0.3	0.3254	0.13	786	1542
7	1.57	**0.128**	7.9198	0.3	0.3254	0.13	884	1695
8	1.57	**0.148**	7.9198	0.3	0.3254	0.13	993	1864
9	1.57	**0.188**	7.9198	0.3	0.3254	0.13	1246	2251
10	1.57	**0.208**	7.9198	0.3	0.3254	0.13	1391	2469
11	1.57	0.168	**5.6570**	0.3	0.3254	0.13	4080	8075
12	1.57	0.168	**6.2227**	0.3	0.3254	0.13	3071	5832
13	1.57	0.168	**6.7884**	0.3	0.3254	0.13	2309	4238
14	1.57	0.168	**7.3541**	0.3	0.3254	0.13	1657	2984
15	1.57	0.168	**8.4855**	0.3	0.3254	0.13	786	1555
16	1.57	0.168	7.9198	**0.27**	0.3254	0.13	989	1856
17	1.57	0.168	7.9198	**0.28**	0.3254	0.13	1030	1916
18	1.57	0.168	7.9198	**0.29**	0.3254	0.13	1072	1981
19	1.57	0.168	7.9198	**0.31**	0.3254	0.13	1155	2121
20	1.57	0.168	7.9198	**0.32**	0.3254	0.13	1197	2196
21	1.57	0.168	7.9198	0.3	**0.3154**	0.13	1098	2048
22	1.57	0.168	7.9198	0.3	**0.3354**	0.13	1113	2050
23	1.57	0.168	7.9198	0.3	**0.3454**	0.13	1105	2052
24	1.57	0.168	7.9198	0.3	**0.3554**	0.13	1092	2054
25	1.57	0.168	7.9198	0.3	**0.3654**	0.13	1074	2056
26	1.57	0.168	7.9198	0.3	0.3254	**0.11**	1317	2456
27	1.57	0.168	7.9198	0.3	0.3254	**0.12**	1206	2232
28	1.57	0.168	7.9198	0.3	0.3254	**0.14**	1036	1897
29	1.57	0.168	7.9198	0.3	0.3254	**0.15**	970	1771
30	1.57	0.168	7.9198	0.3	0.3254	**0.16**	913	1663

* *The highlighted rows indicate the original package dimensions as in the standard case model. This serves to show where the original package dimensions fit in the data above and how each parameter is varied with respect to their original value.*

Figs. 4.1 through 4.6 display the summarized results from Table 4.1 in graphical plots.

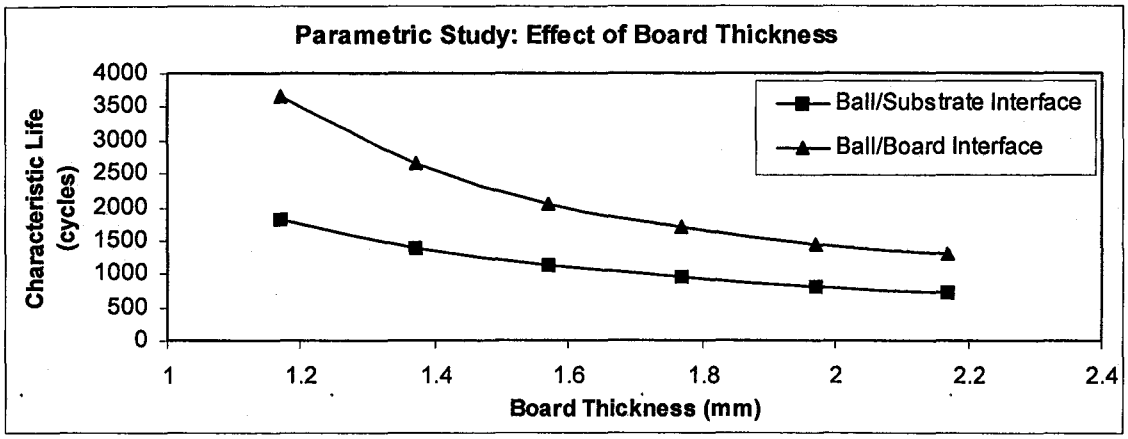


Fig. 4.1. Effect of board thickness on solder fatigue life.

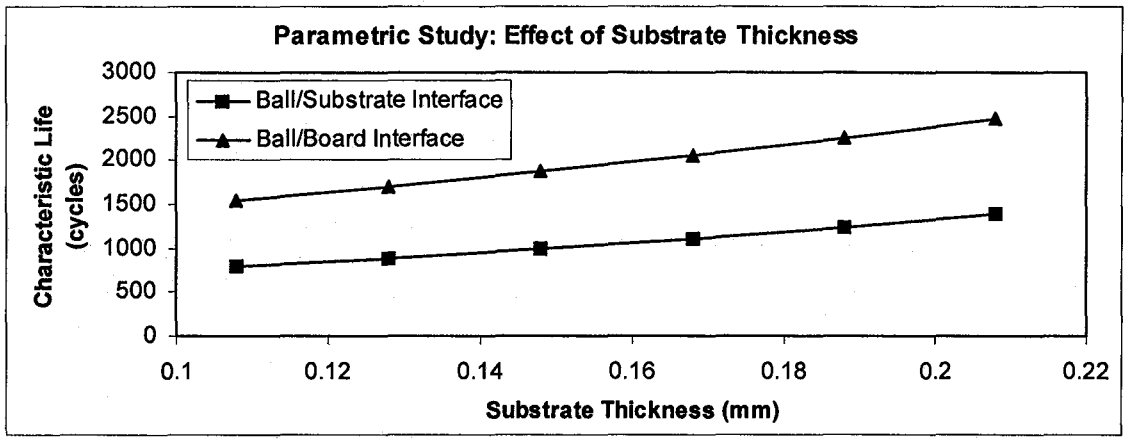


Fig. 4.2. Effect of substrate thickness on solder fatigue life.

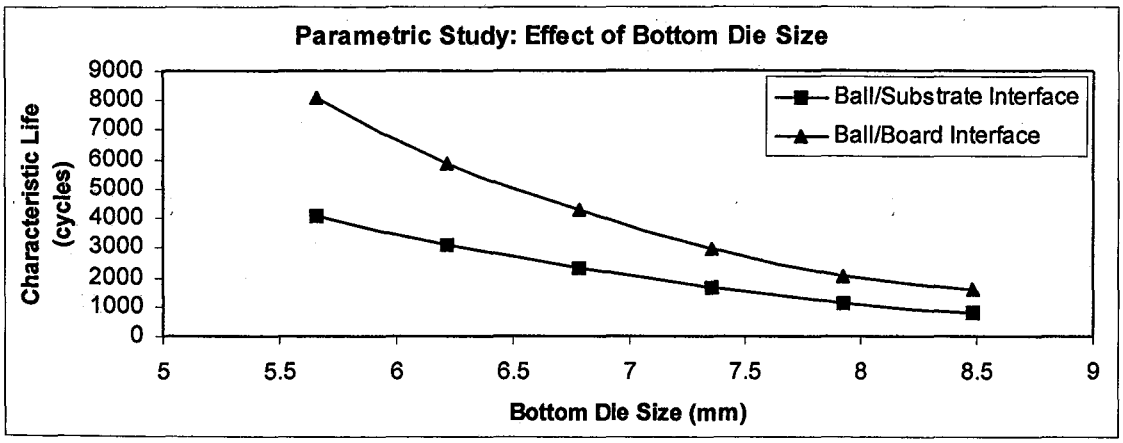


Fig. 4.3. Effect of bottom die size on solder fatigue life.

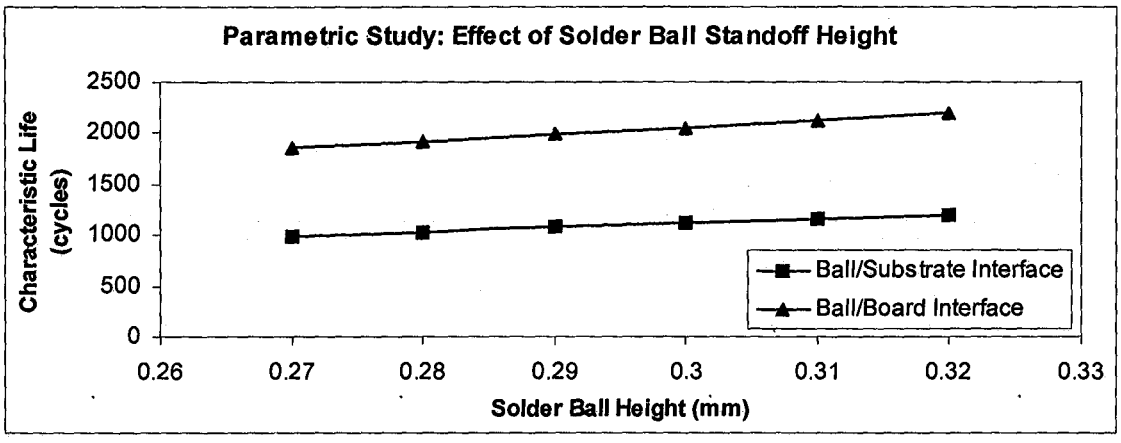


Fig. 4.4. Effect of solder ball standoff height on solder fatigue life.

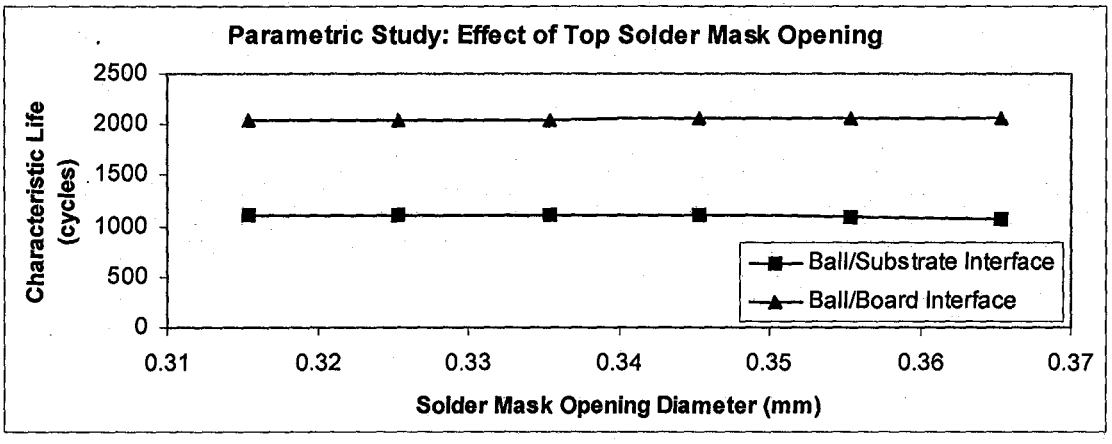


Fig. 4.5. Effect of top solder mask opening on solder fatigue life.

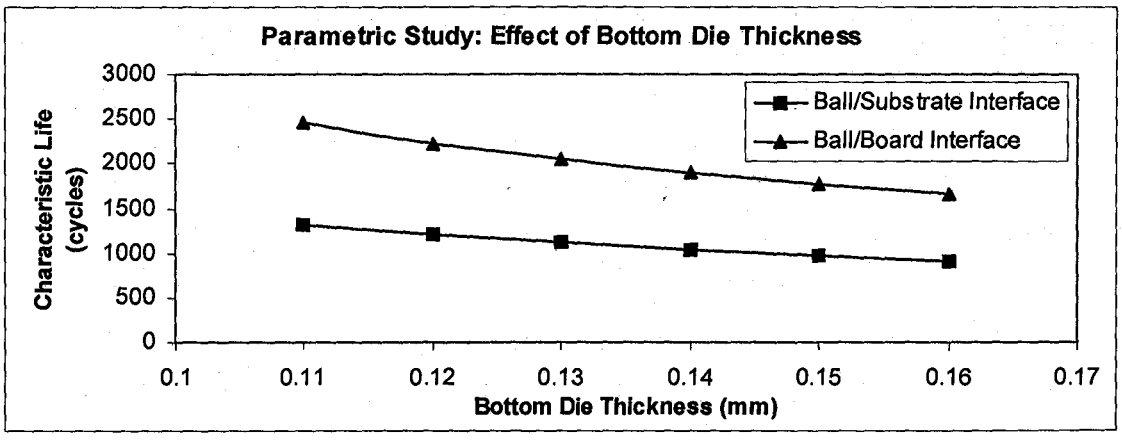


Fig. 4.6. Effect of bottom die thickness on solder fatigue life.

Fig. 4.7 combines all the data shown in Figs. 4.1 through 4.6 for the solder ball/substrate interface to make a comparison between all the six parameters studied. From Fig. 4.7, the bottom die size has the greatest effect on the solder fatigue life as the increments taken for this parameter is the largest among the six package dimensions. Take note that due to the difference in the data increments of each parameter studied, Fig. 4.7 should not be considered as a measurement of how much effect a certain parameter has on the solder fatigue life.

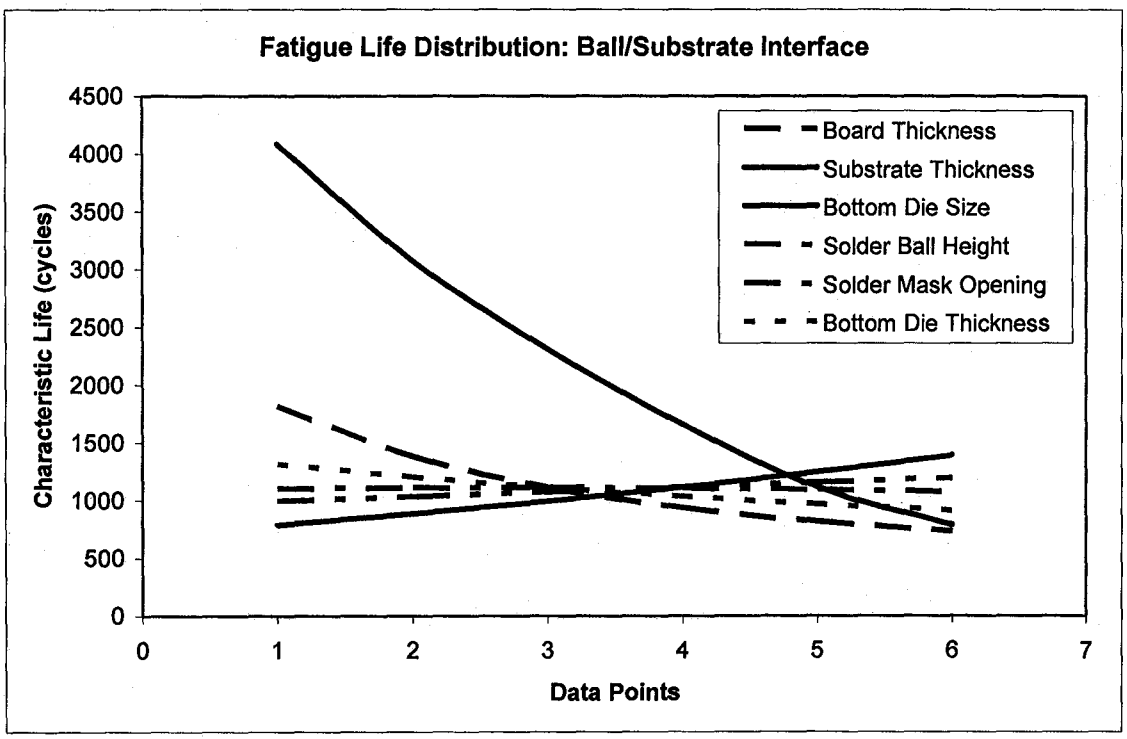


Fig. 4.7. Effect of package dimensions on the solder fatigue life.

As seen from Fig. 4.7, the board thickness, the bottom die size and the bottom die thickness show a decreasing trend with increasing parameter values. The top solder mask opening is almost constant for all data points. On the other hand, the substrate thickness and the solder ball height show an increasing trend with increasing parameter values.

Fig. 4.8 also shows the comparison of all six package parameters and their effect on the characteristic fatigue life at the solder ball/board interface.

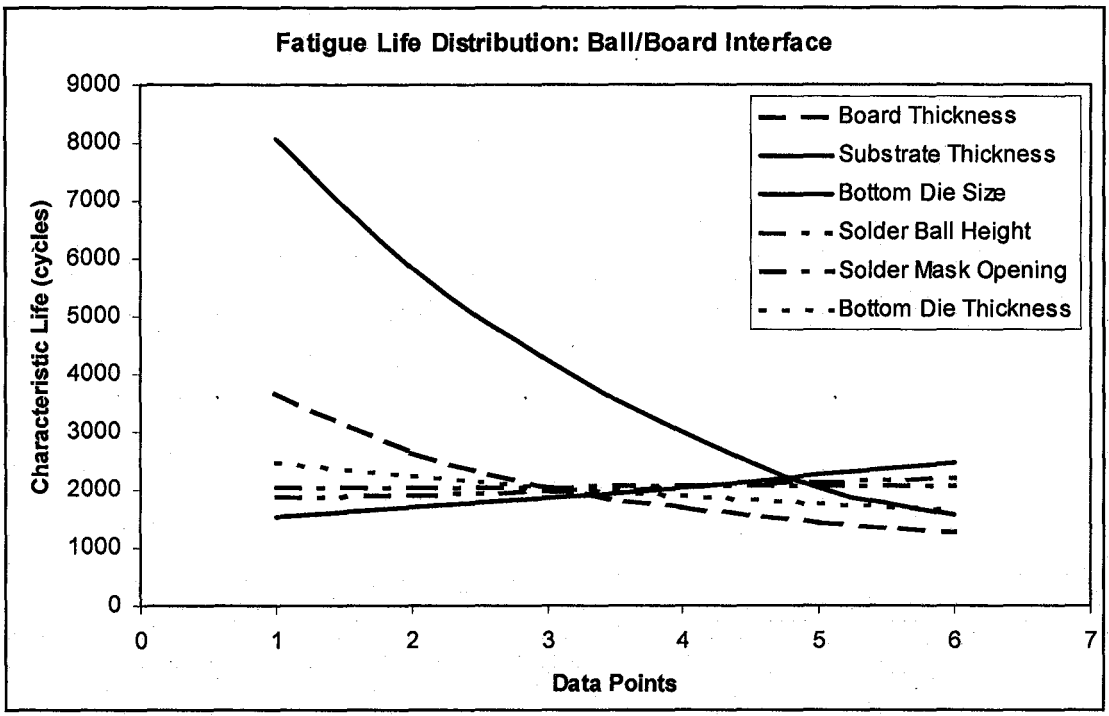


Fig. 4.8. Effect of package dimensions on solder fatigue life.

As seen from Fig. 4.8, the fatigue life distribution for the ball/board interface shows an almost similar trend with the fatigue life distribution of the ball/substrate interface. The only difference is the values of the fatigue life, which approximately double those at the ball/substrate interface.

4.2 Application of Artificial Neural Network for Fatigue Life Prediction

In the first chapter, the Artificial Neural Network (ANN) is introduced as a tool to predict other data points within a known set of data. A total of six package dimensions are involved in the parametric study. Each dimension has six ANSYS^{TM} simulated data points including the data for the control case model. From the existing six data points, ANN is used to further predict additional data points in between each of the original six ANSYS^{TM} simulated data points. Keeping in mind that there are two solder ball interfaces to consider, 2 sets of data will be used

to train the network for each package dimension, one for the ball/substrate interface and another for the ball/board interface.

Table 4.2 indicates the data points ranges used for the ANN predictions as compared to the data point ranges used in the ANSYS simulations.

Table 4.2. Data points for ANSYS and ANN.

Package Parameter	ANSYS Simulations		ANN Predictions	
	Data range (mm)	Increment (mm)	Data range (mm)	Increment (mm)
Board thickness	1.17 to 2.17	0.2	1.22 to 2.12	0.05
Substrate thickness	0.108 to 0.208	0.02	0.113 to 0.203	0.005
Bottom die size	5.6570 to 8.4855	0.5657	5.798 to 8.344	0.141425
Solder ball height	0.27 to 0.32	0.01	0.2725 to 0.3175	0.0025
Solder mask opening	0.3154 to 0.3654	0.01	0.3179 to 0.3629	0.0025
Bottom die thickness	0.11 to 0.16	0.01	0.1125 to 0.1575	0.0025

4.2.1 Prediction for the Parameter 'Board Thickness'

Table 4.3 shows the predicted values of the characteristic fatigue life for the parameter 'Board Thickness' at both solder ball joint interfaces. The following figures depict the data in Table 4.3 in graphical plots with Fig. 4.9a showing the effect of board thickness at the ball/substrate interface and Fig. 4.9b showing the effect of board thickness at the ball/board interface. Both figures show a good conformance between the ANSYS simulated results and the ANN predicted results.

Table 4.3. Data for ANSYS simulations and ANN predictions (Board Thickness).

ANSYS Simulations			ANN Predictions		
Board Thickness (mm)	Characteristic Life (cycles)		Board Thickness (mm)	Characteristic Life (cycles)	
	Ball/Substrate Interface	Ball/Board Interface		Ball/Substrate Interface	Ball/Board Interface
1.17	1807	3666	-	-	-
-	-	-	1.22	1696	3364
-	-	-	1.27	1585	3089
-	-	-	1.32	1478	2846
1.37	1380	2634	1.37	1380	2634
-	-	-	1.42	1295	2452
-	-	-	1.47	1225	2296
-	-	-	1.52	1166	2162
1.57	1113	2047	1.57	1113	2047
-	-	-	1.62	1064	1946
-	-	-	1.67	1019	1855
-	-	-	1.72	976	1769
1.77	938	1687	1.77	938	1687
-	-	-	1.82	910	1607
-	-	-	1.87	873	1534
-	-	-	1.92	845	1478
1.97	818	1448	1.97	818	1448
-	-	-	2.02	793	1427
-	-	-	2.07	770	1382
-	-	-	2.12	749	1327
2.17	732	1282	-	-	-

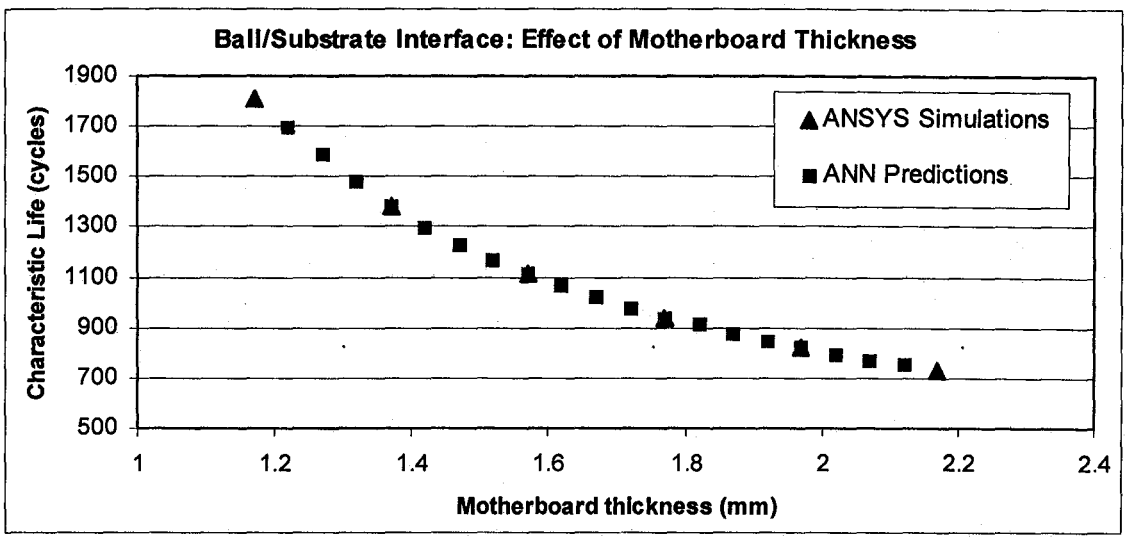


Fig. 4.9a. ANN Predictions for Ball/Substrate Interface

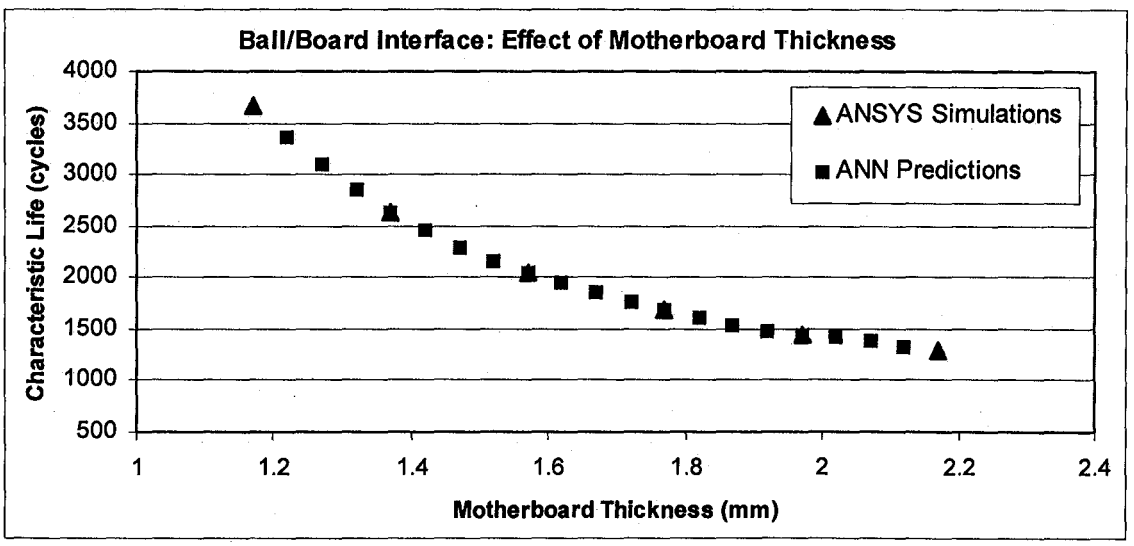


Fig. 4.9b. ANN Predictions for Ball/Board Interface

4.2.2 Prediction for the Parameter 'Substrate Thickness'

Table 4.4 shows the predicted values of the characteristic fatigue life for the parameter 'Substrate Thickness' at both solder ball joint interfaces. Fig. 4.10a shows the effect of substrate thickness at the ball/substrate interface and Fig. 4.10b shows the effect of substrate thickness at the ball/board interface. Both figures show a good agreement between the ANSYS simulated results and the ANN predicted results.

Table 4.4. Data for ANSYS simulations and ANN predictions (Substrate Thickness).

ANSYS Simulations			ANN Predictions		
Substrate Thickness (mm)	Characteristic Life (cycles)		Substrate Thickness (mm)	Characteristic Life (cycles)	
	Ball/Substrate Interface	Ball/Board Interface		Ball/Substrate Interface	Ball/Board Interface
0.108	786	1542	-	-	-
-	-	-	0.113	810	1578
-	-	-	0.118	834	1616
-	-	-	0.123	858	1655
0.128	884	1695	0.128	884	1695
-	-	-	0.133	910	1735
-	-	-	0.138	937	1777
-	-	-	0.143	964	1819
0.148	993	1864	0.148	993	1863
-	-	-	0.153	1022	1907
-	-	-	0.158	1051	1953
-	-	-	0.163	1082	2000
0.168	1113	2047	0.168	1113	2048
-	-	-	0.173	1145	2097

-	-	-	0.178	1178	2147
-	-	-	0.183	1211	2198
0.188	1246	2251	0.188	1245	2250
-	-	-	0.193	1281	2304
-	-	-	0.198	1316	2358
-	-	-	0.203	1353	2413
0.208	1391	2469	-	-	-

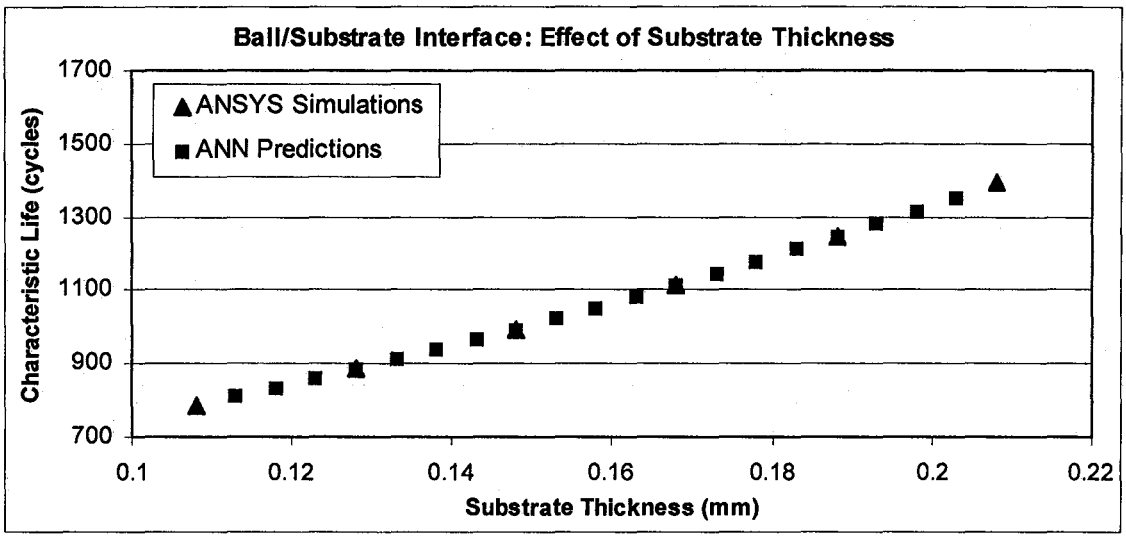


Fig. 4.10a. ANN Predictions for Ball/Substrate Interface

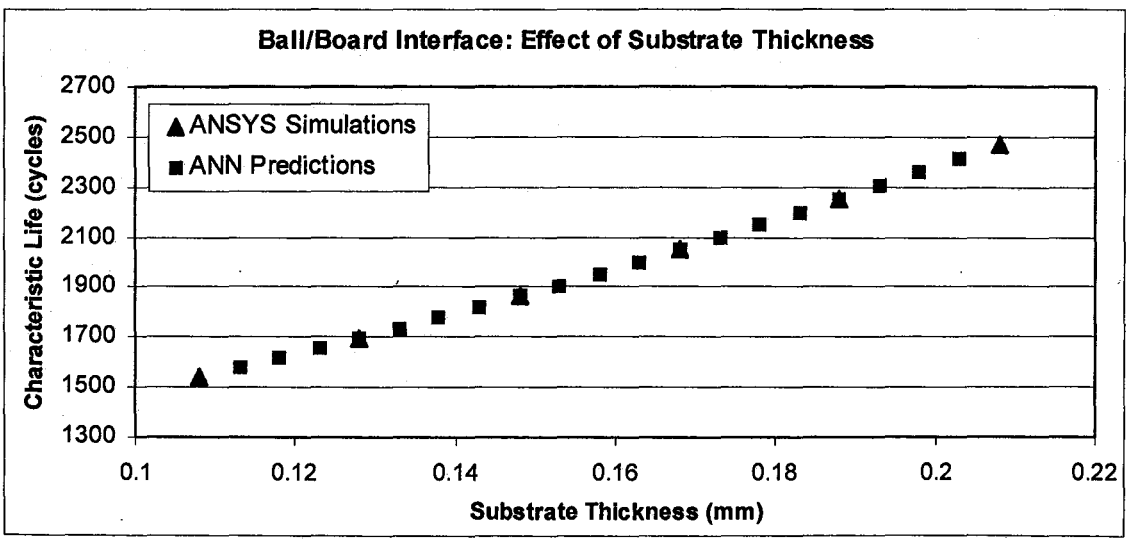


Fig. 4.10b. ANN Predictions for Ball/Board Interface

4.2.3 Prediction for the Parameter 'Bottom Die Size'

Table 4.5 shows the predicted values of the characteristic fatigue life for the parameter 'Bottom Die Size' at both solder ball joint interfaces. Fig. 4.11a shows the effect of substrate thickness at the ball/substrate interface and Fig. 4.11b shows the effect of bottom die size at the ball/board interface. Both figures show a good agreement between the ANSYS simulated results and the ANN predicted results.

Table 4.5. Data for ANSYS simulations and ANN predictions (Bottom Die Size).

ANSYS Simulations			ANN Predictions		
Bottom Die Size (mm)	Characteristic Life (cycles)		Bottom Die Size (mm)	Characteristic Life (cycles)	
	Ball/Substrate Interface	Ball/Board Interface		Ball/Substrate Interface	Ball/Board Interface
5.6570	4080	8075	-	-	-
-	-	-	5.7980	3891	7460
-	-	-	5.9400	3647	6875
-	-	-	6.0810	3362	6331
6.2227	3071	5832	6.2230	3071	5833
-	-	-	6.3640	2817	5381
-	-	-	6.5060	2617	4969

-	-	-	6.6470	2457	4592
6.7884	2309	4238	6.7880	2309	4239
-	-	-	6.9300	2156	3905
-	-	-	7.0710	1994	3584
-	-	-	7.2130	1825	3277
7.3541	1657	2984	7.3540	1657	2985
-	-	-	7.4960	1497	2711
-	-	-	7.6370	1352	2462
-	-	-	7.7780	1224	2240
7.9198	1113	2047	7.9200	1113	2049
-	-	-	8.0610	1017	1886
-	-	-	8.2030	932	1752
-	-	-	8.3440	856	1643
8.4855	786	1555	-	-	-

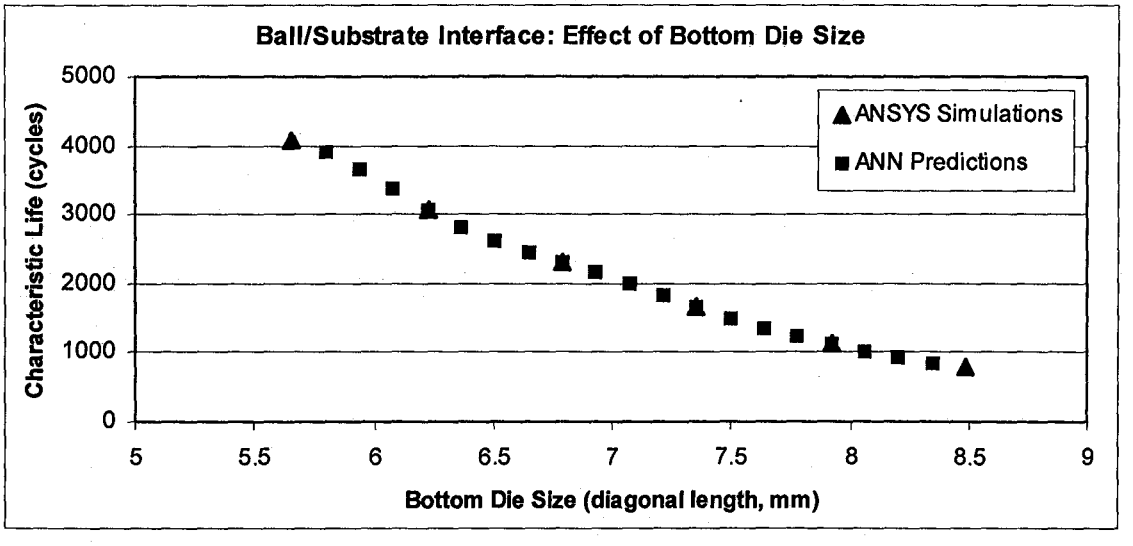


Fig. 4.11a. ANN Predictions for Ball/Substrate Interface

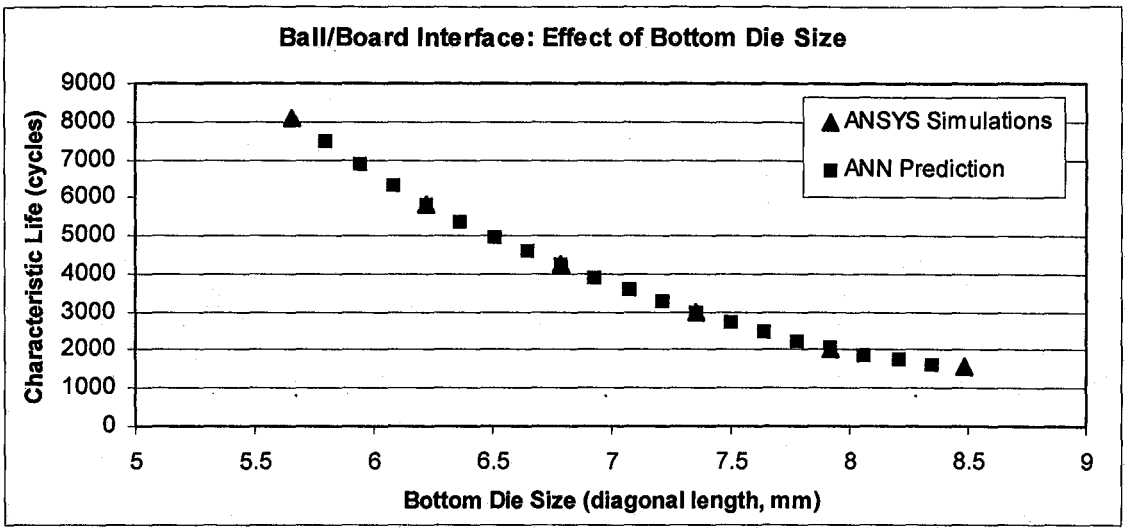


Fig. 4.11b. ANN Predictions for Ball/Board Interface

4.2.4 Prediction for the Parameter 'Solder Ball Standoff Height'

Table 4.6 shows the predicted values of the characteristic fatigue life for the parameter 'Bottom Die Size' at both solder ball joint interfaces. Fig. 4.12a shows the effect of substrate thickness at the ball/substrate interface and Fig. 4.12b shows the effect of bottom die size at the ball/board interface. Both figures show a good agreement between the ANSYS simulated results and the ANN predicted results.

Table 4.6. Data for ANSYS simulations and ANN predictions (Solder Ball Height).

ANSYS Simulations	ANN Predictions

Solder Ball Height (mm)	Characteristic Life (cycles)		Solder Ball Height (mm)	Characteristic Life (cycles)	
	Ball/Substrate Interface	Ball/Board Interface		Ball/Substrate Interface	Ball/Board Interface
0.27	989	1856	-	-	-
-	-	-	0.2725	999	1871
-	-	-	0.275	1009	1886
-	-	-	0.2775	1020	1901
0.28	1030	1916	0.28	1030	1916
-	-	-	0.2825	1040	1932
-	-	-	0.285	1051	1948
-	-	-	0.2875	1061	1964
0.29	1072	1981	0.29	1071	1980
-	-	-	0.2925	1082	1997
-	-	-	0.295	1092	2013
-	-	-	0.2975	1103	2031
0.3	1113	2047	0.3	1113	2048
-	-	-	0.3025	1123	2065
-	-	-	0.305	1134	2083
-	-	-	0.3075	1144	2101
0.31	1155	2121	0.31	1155	2120
-	-	-	0.3125	1165	2139
-	-	-	0.315	1176	2158
-	-	-	0.3175	1186	2177
0.32	1197	2196	-	-	-

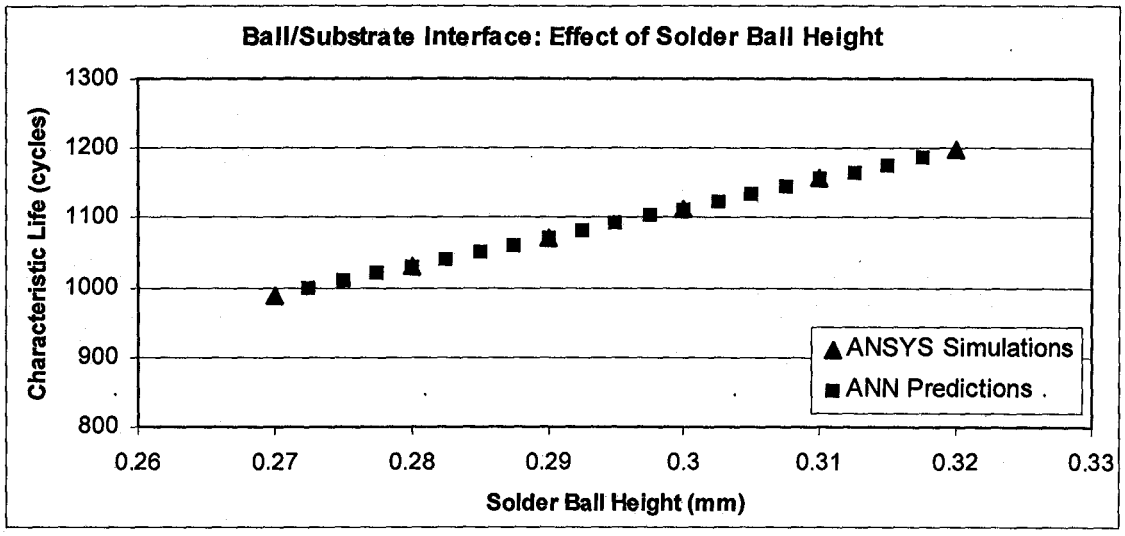


Fig. 4.12a. ANN Predictions for Ball/Substrate Interface

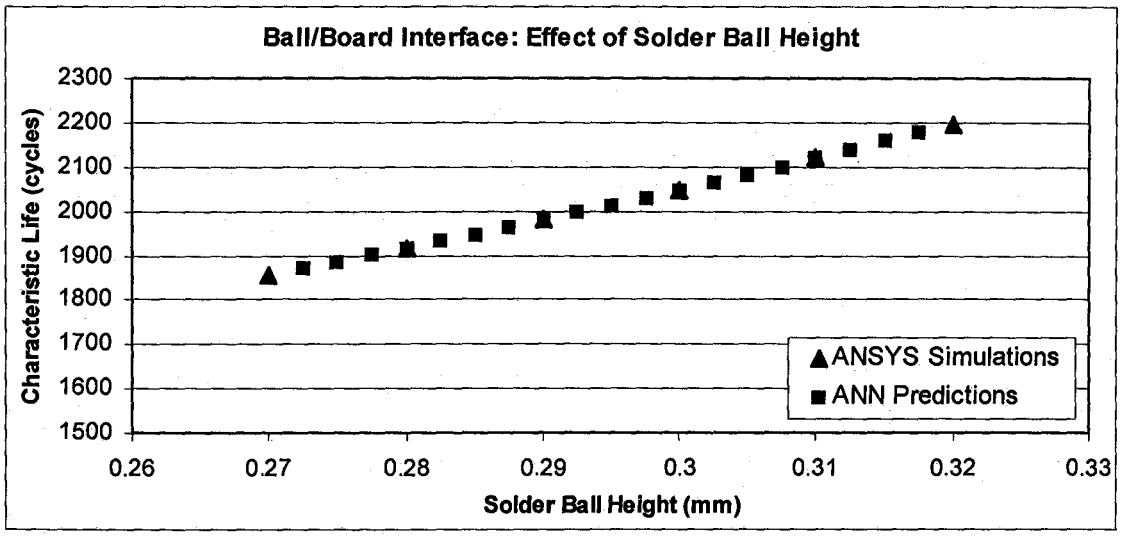


Fig. 4.12b. ANN Predictions for Ball/Board Interface

4.2.5 Prediction for the Parameter 'Solder Mask Opening'

Table 4.7 shows the predicted values of the characteristic fatigue life for the parameter 'Solder Mask Opening' at both solder ball joint interfaces. The following figures depict the data in Table 4.7 in graphical plots with Fig. 4.13a showing the effect of board thickness at the ball/substrate interface and Fig. 4.13b showing the effect of board thickness at the ball/board interface. Both figures show a good conformance between the ANSYS simulated results and the ANN results.

Table 4.7. Data for ANSYS simulations and ANN predictions (Solder Mask Opening).

ANSYS Simulations			ANN Predictions		
Solder Mask Opening (mm)	Characteristic Life (cycles)		Solder mask Opening (mm)	Characteristic Life (cycles)	
	Ball/Substrate Interface	Ball/Board Interface		Ball/Substrate Interface	Ball/Board Interface
0.3154	1098	2048	-	-	-
-	-	-	0.3179	1104	2047
-	-	-	0.3204	1107	2047
-	-	-	0.3229	1111	2048
0.3254	1113	2047	0.3254	1113	2048
-	-	-	0.3279	1114	2048
-	-	-	0.3304	1115	2049
-	-	-	0.3329	1115	2049
0.3354	1113	2050	0.3354	1115	2049
-	-	-	0.3379	1114	2050
-	-	-	0.3404	1112	2050
-	-	-	0.3429	1109	2051
0.3454	1105	2052	0.3454	1106	2051
-	-	-	0.3479	1102	2052

-	-	-	0.3504	1099	2052
-	-	-	0.3529	1095	2053
0.3554	1092	2054	0.3554	1090	2054
-	-	-	0.3579	1086	2054
-	-	-	0.3604	1082	2055
-	-	-	0.3629	1078	2056
0.3654	1074	2056	-	-	-

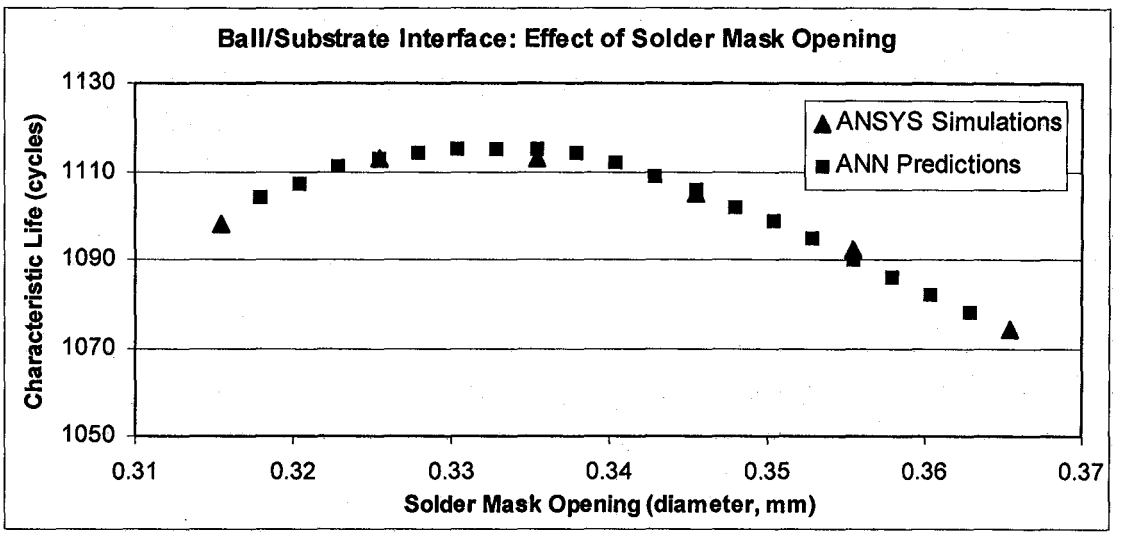


Fig. 4.13a. ANN Predictions for Ball/Substrate Interface

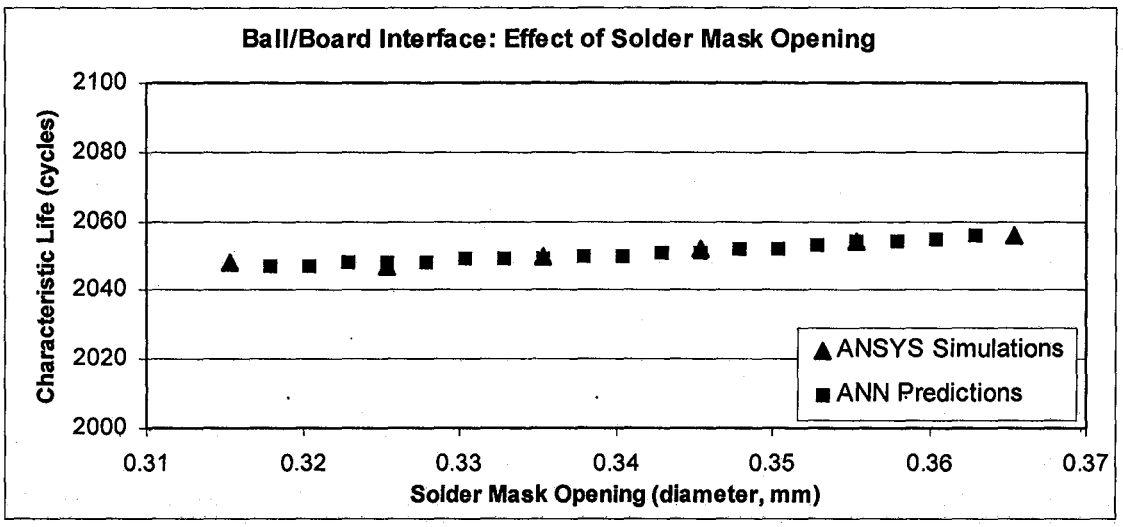


Fig. 4.13b. ANN Predictions for Ball/Board Interface

4.2.6 Prediction for the parameter 'Bottom Die Thickness'

Table 4.8 shows the predicted values of the characteristic fatigue life for the parameter 'Bottom Die Thickness' at both solder ball joint interfaces. The following figures depict the data in Table 4.8 in graphical plots with Fig. 4.14a showing the effect of board thickness at the ball/substrate interface and Fig. 4.14b showing the effect of board thickness at the ball/board interface. Both figures show a good conformance between the ANSYS simulated results and the ANN results.

Table 4.8. Data for ANSYS simulations and ANN predictions (Bottom Die Thickness).

ANSYS Simulations			ANN Predictions		
Bottom Die Thickness (mm)	Characteristic Life (cycles)		Bottom Die Thickness (mm)	Characteristic Life (cycles)	
	Ball/Substrate Interface	Ball/Board Interface		Ball/Substrate Interface	Ball/Board Interface
0.11	1317	2456	-	-	-
-	-	-	0.1125	1287	2397
-	-	-	0.115	1259	2339
-	-	-	0.1175	1232	2284
0.12	1206	2232	0.12	1206	2232
-	-	-	0.1225	1182	2182
-	-	-	0.125	1158	2135
-	-	-	0.1275	1135	2090
0.13	1113	2047	0.13	1113	2047
-	-	-	0.1325	1092	2007
-	-	-	0.135	1072	1968
-	-	-	0.1375	1053	1932
0.14	1036	1897	0.14	1035	1897
-	-	-	0.1425	1017	1863
-	-	-	0.145	1001	1831
-	-	-	0.1475	985	1801
0.15	970	1771	0.15	969	1771
-	-	-	0.1525	954	1743
-	-	-	0.155	940	1715
-	-	-	0.1575	927	1689
0.16	913	1663	-	-	-

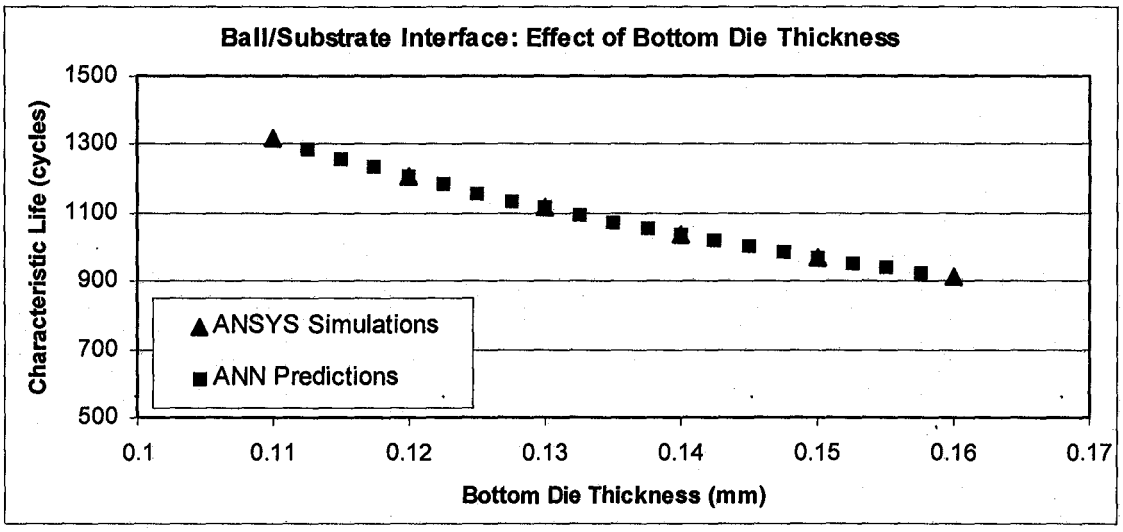


Fig. 4.14a. ANN Predictions for Ball/Substrate Interface

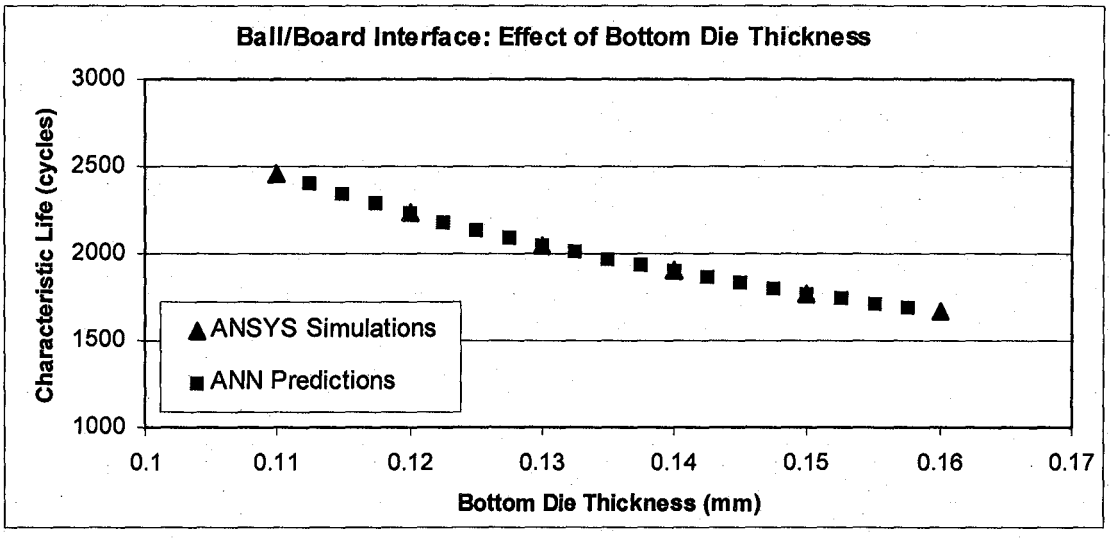


Fig. 4.14b. ANN Predictions for Ball/Board Interface

4.2.7 Discussion

Looking back at Figs. 4.9 through 4.14 in the previous section, it is easily perceived that the fatigue life predictions are easily anticipated due to the almost linear plots in most of the graphs. This is also supported by the fact that most of the plots in Figs. 4.9 through 4.14 are showing either an increasing trend or a decreasing trend except for Fig. 4.13a. In fact one can easily fit these curves to different equations and use the equations for life prediction within the specified ranges. These factors raise the important question of the practicality of using ANN for fatigue life predictions, when a simple line plot of the six ANSYS simulated data can give a fairly accurate prediction for all the other data points. This issue will be addressed in the following discussion.

All the plots in Figs. 4.9 through 4.14 only involve one changing parameter, with the other five parameters fixed at the same value as in the standard case model. It is true that in such scenario, the fatigue life predictions can be easily carried out with a simple line plot. However, such a method will become impossible if more than one package dimension is changing or if the plots become more complicated. This necessitates the use of ANN for a more versatile prediction, as the ANN can take care of all the difficulties mentioned above.

4.3 Verification of ANN Predictions

As a comparison and also as a verification that ANN predicted fatigue lives agree well with ANSYS simulated fatigue lives, three sets of six parameter values not plotted in any graphs in the previous section are used for fatigue life prediction. Three sets of package dimensions as shown in Table 4.9 are chosen for verification. First ANN uses the existing data for training and

to predict the fatigue lives of the mentioned sets of package dimensions shown in Table 4.9. Then ANSYS is used to remodel new finite element models based on the three chosen sets of package dimensions. For each set of package dimensions chosen, an ANSYS simulation is run to predict the fatigue life. This value is then compared with the value obtained through ANN.

Table 4.9 displays the chosen set of parameter values and their respective fatigue lives predicted both by ANN and ANSYS. As can be seen from Table 4.9, the fatigue lives predicted by both ANN and ANSYS are very close to each other, within a 100 cycles difference.

Table 4.9. Fatigue life comparison.

*Parameters (mm)	ANN Predicted Fatigue Life		ANSYS Simulated Fatigue Life	
	Ball/Substrate Interface (cycles)	Ball/Board Interface (cycles)	Ball/Substrate Interface (cycles)	Ball/Board Interface (cycles)
Set 1				
b = 1.42 st = 0.175 ds = 7.3541 bh = 0.295 mo = 0.3404 dt = 0.125	2016.6	3913.4	2068	3871
Set 2				
b = 1.85 st = 0.133 ds = 6.7884 bh = 0.276 mo = 0.3504 dt = 0.146	1294	2485.8	1313	2398
Set 3				
b = 1.61 st = 0.154 ds = 7.3541 bh = 0.313 mo = 0.3304 dt = 0.152	1309.7	2393.3	1362	2357

* *b = board;* *bh = ball height;*

st = substrate thickness; *mo = mask opening;*
ds = die size; *dt = die thickness;*

4.4 Parametric Optimization with ANN and GA

The parametric study carried out in section 4.1 of this chapter studies the effect of 6 package dimensions on the overall package solder life. By knowing how certain package dimension changes with the solder fatigue life, parametric optimization can be achieved by selectively reducing or increasing certain package dimensions accordingly so that solder fatigue life can be maximized. From results shown in Figs. 4.1 through 4.6, it can be deduced that solder fatigue life can be optimized by reducing the thickness of the PCB board, increasing the thickness of the substrate, reducing the size of the bottom die, increasing the height of the solder ball standoff height and also by reducing the bottom die thickness.

Besides the parametric study carried out, ANN and GA can also be used to predict possible package dimensions for a limited fatigue life cycle range. For this purpose, a program is executed with ANN and GA. In addition to that, a few lines of programming commands enable GA to selectively collect the combination set of package dimension values that fall within the user specified fatigue life cycle range. By collecting these data, a rough idea of the variation of package parameter values that gives a limited range of solder fatigue life can be determined.

Consider the case of the detailed flip chip model used for an X-test simulation in Chapter 3. The fatigue life at the ball/substrate interface is 1113 cycles whereas the fatigue life at the ball/board interface is 2047 cycles. In the case when the need to increase or decrease the solder fatigue life arises, the above methodology can be utilized to predict and to be decided upon, which package parameter should be changed in order to meet the new requirements. The

following data in Table 4.10 list the possible combination of package parameter values for a given solder fatigue life constraint of between 1000 to 1100 cycles.

Table 4.10. Parametric Data for Ball/Substrate Interface

Combination No.	Board Thickness	Substrate Thickness	Bottom Die Size	Ball Height	Mask Opening	Die Thickness	Life Cycle (1000-1100)
5	1.817	0.197	7.751	0.279	0.320	0.118	1081
9	1.462	0.197	8.371	0.304	0.342	0.121	1019
11	1.684	0.154	7.946	0.307	0.328	0.112	1063
25	1.865	0.192	7.456	0.281	0.332	0.118	1040
42	1.211	0.127	8.460	0.277	0.316	0.159	1063
84	1.652	0.167	7.932	0.314	0.332	0.133	1060
86	1.978	0.201	7.378	0.311	0.344	0.129	1096
100	1.821	0.141	7.167	0.288	0.335	0.140	1017
112	1.774	0.148	7.508	0.293	0.342	0.116	1010
124	1.947	0.201	7.102	0.274	0.329	0.120	1030
136	1.978	0.201	7.290	0.313	0.346	0.151	1079
325	1.477	0.199	8.380	0.313	0.321	0.140	1079
359	1.558	0.135	7.604	0.273	0.316	0.130	1016
516	1.517	0.167	8.468	0.307	0.332	0.112	1069
611	1.516	0.155	8.328	0.306	0.343	0.114	1058
3019	1.841	0.194	7.796	0.306	0.330	0.151	1029
3776	2.096	0.157	6.525	0.315	0.363	0.128	1009
4054	2.046	0.176	7.178	0.291	0.323	0.113	1098
4582	1.638	0.126	7.795	0.317	0.337	0.113	1093
6723	1.657	0.157	7.797	0.318	0.324	0.136	1080
8966	1.640	0.204	8.316	0.316	0.325	0.126	1027
9208	2.157	0.152	6.162	0.277	0.341	0.144	1038

The results shown are some of the possible combinations of package parameters that give a solder life cycle in between 1000 to 1100 cycles at the ball/substrate. It will be up to the user to decide upon which package dimension to change after considering the data in Table 4.10. Other combination of package dimensions for a given solder life cycle ranges at the ball/substrate interface are given in Appendix A. Appendix B also list down all the possible combination of package dimensions for different life cycle ranges at the ball/board interface.

Through the data shown in Table 4.10, Appendix A and Appendix B, solder fatigue life can be maximized. The data generated and displayed in Tables 4.10, Appendix A and Appendix B are based on very loose constraints on the package parameters. Therefore, changes in the package parameters shown are very random to make any trend out of them. By introducing more

constraints on the package dimensions, the randomized changes can be reduced and the methodology employed can therefore produce more useful data.

CHAPTER 5

CONCLUSIONS

5.1 Overall Conclusions

A finite element analysis based methodology for estimating the characteristic fatigue life of a solder joint interconnect under accelerated temperature cycling has been applied to predict the reliability performance of a flip chip package. The method uses the ANSYS^{TM} finite element analysis tool along with Anand's viscoplastic constitutive law. Darveaux's crack growth rate model was applied to calculate solder joint characteristic life using simulated viscoplastic strain energy density results at the package substrate and printed circuit board solder joints.

Two package configurations were evaluated with the above methodology, with the first being a simplified flip chip model and the second being a detailed flip chip model. Each of these configurations was subjected to two accelerated temperature cycling test, namely the B-test and the X-test. Simulation results indicate that for the simplified flip chip model, the characteristic life results for the X-test are 59-70% greater than the results for the B-test. For the detailed flip chip model, the characteristic life results for the X-test are 72-73% greater than the results for the B-test. Generally, the results also indicate that the solder joint at the corner end of the package tends to fail first. The characteristic lives of solder joint at the package ball/board interface are 24-46% higher than the characteristic lives of solder joint at the package ball/substrate interface. This means that the interface between the solder ball and substrate will fail first before the interface between the solder ball and the board.

In addition to the above results, a parametric study has been carried out to determine the effect of six package parameters on the package characteristic life. The six parameters involved are the board thickness, the substrate thickness, the bottom die size, the solder ball standoff

height, the solder mask opening diameter and the bottom die thickness. Results indicate that a higher solder joint reliability can be achieved with thinner board, thicker substrate, smaller die size, higher solder ball standoff, and thinner die. Effect of the solder mask opening for the models studied is relatively insignificant. Overall comparison indicates that the die size has the most profound effect on the solder joint characteristic life.

With the above results, ANN has been utilized to predict additional solder joint characteristic life for package configurations not simulated earlier in the parametric study. Results obtained show a good match between ANN predictions and simulated results. Further verification of ANN predictions by re-simulating the package configurations with ANSYS™ indicate results of characteristic lives that are less than a hundred cycles in difference. It has also been demonstrated that by consolidating the existing data, GA can be used as a tool to predict possible package dimensional values for a given constraints on the solder joint characteristic life.

5.2 Suggestions for Future Work

- Numerous methodologies exist to convert finite element simulation results (i.e. viscoplastic strain energy density) to cycles to failure under accelerated temperature cycling conditions. However, all these methodologies assume the utilization of eutectic solder materials. Life prediction methodologies for high temperature solder of future non-lead based interconnect materials, are almost non-existent due to their low volume use in today's microelectronics packaging industry. Since the packaging industry is striving towards a lead-free packaging environment, it is timely that some work be carried out with regard to this.

- Results obtained through these methodologies lack general applicability. There are many different types of packages in the microelectronics industry. From the past work done, many similarities can be derived from different package analysis, yet the results obtained from one type of package analysis cannot be fully utilized by the same analysis of a different package. Therefore, it would be more useful if an analysis of a generalized scheme of microelectronic packages be carried out so that the findings can be used by different types of microelectronic packages.

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RECOMMENDED READING MATERIALS

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