INVESTIGATION OF LOW DIELECTRIC CONSTANT (K) FILMS FOR DEEP SUB-MICRON CMOS APPLICATION

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UNIVERSITI SAINS MALAYSIA
KAMPUS KEJURUTERAAN
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Laporan Akhir Projek Penyelidikan Jangka Pendek

Investigation of Low Dielectric Constant (k) Films for Deep Sub-Micron CMOS Application

by
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LAPORAN AKHIR PROJEK PENYELIDIKAN JANGKA *PENDEK*

FINAL REPORT OF SHORT TERM RESEARCH PROJECT

Sila kemukakan laporan akhir ini melalui Jawatankuasa Penyelidikan di Pusat Pengajian dan Dekan/Pengarah/Ketua Jabatan kepada Pejabat Pelantar Penyelidikan

1. **Nama Ketua Penyelidik:** *Name of Research Leader* Ir. Cheong Kuan Yew

   ☐ Profesor Madya/ *Assoc. Prof.* ☑ Dr./ *Dr.* ☐ Encik/Puan/Cik *Mr/Mrs/Ms*

2. **Pusat Tanggungjawab (PTJ):** *School/Department*

   School of Materials & Mineral Resources Engineering

3. **Nama Penyelidik Bersama:** *Name of Co-Researcher*

   Assoc. Prof. Dr. Luay Bakir Hussain

4. **Tajuk Projek:** *Title of Project*

   OLD TITLE: Development of localized-selective-stress etch-stop layer (ESL) for a new CMOS integration scheme

   NEW TITLE: Investigation of low dielectric constant (k) films for deep sub-micron CMOS application.

5. **Ringkasan Penilaian/***Summary of Assessment*:	Tidak Mencukupi *Inadequate*		Boleh Diterima *Acceptable*	Sangat Baik *Very Good*	
	1	2	3	4	5
i) **Pencapaian objektif projek:** *Achievement of project objectives*	☐	☐	☐	☑	☐
ii) **Kualiti output:** *Quality of outputs*	☐	☐	☑	☐	☐
iii) **Kualiti impak:** *Quality of impacts*	☐	☐	☑	☐	☐
iv) **Pemindahan teknologi/potensi pengkomersialan:** *Technology transfer/commercialization potential*	☐	☑	☐	☐	☐
v) **Kualiti dan usahasama :** *Quality and intensity of collaboration*	☐	☐	☐	☐	☑
vi) **Penilaian kepentingan secara keseluruhan:** *Overall assessment of benefits*	☐	☐	☑	☐	☐

6. **Abstrak Penyelidikan**
(Perlu disediakan di antara 100 - 200 perkataan di dalam **Bahasa Malaysia dan juga Bahasa Inggeris**. Abstrak ini akan dimuatkan dalam Laporan Tahunan Bahagian Penyelidikan & Inovasi sebagai satu cara untuk menyampaikan dapatan projek tuan/puan kepada pihak Universiti & masyarakat luar).

Abstract of Research
(An abstract of between 100 and 200 words must be prepared in Bahasa Malaysia and in English).
This abstract will be included in the Annual Report of the Research and Innovation Section at a later date as a means of presenting the project findings of the researcher/s to the University and the community at large)

Please refer to Appendix A

7. **Sila sediakan laporan teknikal lengkap yang menerangkan keseluruhan projek ini.**
[Sila gunakan kertas berasingan]
Applicant are required to prepare a Comprehensive Technical Report explaning the project.
(This report must be appended separately)

A Comprehensive Technical Report is appended separately.

Senaraikan kata kunci yang mencerminkan penyelidikan anda:
List the key words that reflects your research:

Bahasa Malaysia	*Bahasa Inggeris*
Pengendapan Sol-gel	Sol-gel deposition
Pemalar dieletrik rendah	Low dielectric constant
Filem nipis	Thin filem

8. **Output dan Faedah Projek**
Output and Benefits of Project

(a) * **Penerbitan Jurnal**
Publication of Journals
(Sila nyatakan jenis, tajuk, pengarang/editor, tahun terbitan dan di mana telah diterbit/diserahkan)
(State type, title, author/editor, publication year and where it has been published/submitted)

1. K.Y. Cheong and F.A. Jasni, "Effects of Precursor Aging and Post-Deposition Treatment Time on Photo-assisted Sol-gel Derived Low-Dielectric Constant SiO_2 Thin Film on Si," ***Microelectronics Journal*** (Elsevier), vol. 38, pp. 227-230, 2007.

2. W.C. Ee and K. Y. Cheong, "Effects of Annealing Temperature on Low Dielectric Constant SiO_2 Thin Films Derived from Sol-gel Tetraethylorthosilicate and Methyltriethoxysilane Source," ***Microelectronics Journal*** (Elsevier) – under review.

(b) **Faedah-faedah lain seperti perkembangan produk, pengkomersialan produk/pendaftaran paten atau impak kepada dasar dan masyarakat.**
State other benefits such as product development, product commercialisation/patent registration or impact on source and society.

The formulation used to produce the low-k thin film may be employed in future generation of microelectronic devices. This enables a better performance device to be made and eventually quality of life of man-kind can be improved.

* Sila berikan salinan/*Kindly provide copies*

(c) **Latihan Sumber Manusia**
Training in Human Resources

i) Pelajar Sarjana: Not Applicable
Graduates Students
(Perincikan nama, ijazah dan status)
(Provide names, degrees and status)

ii) Lain-lain:
Others

Undergraduate (Final Year Project) – 2 students
- 2005/2006: Ms Farah Anis binti Jasni
- 2006/2007: Mr Ee Woei Chang

Research Assistant – 1 student
- July 2006 – Oct 2006: Ms Khor Siew Cheng

9. **Peralatan yang Telah Dibeli:**
Equipment that has been purchased

No equipment is purchased under this grant.

IR. DR. CHEONG KUAN YEW
Pensyarah
P.P. Kejuruteraan Bahan & Sumber Mineral
Kampus Kejuruteraan
Universiti Sains Malaysia

Tandatangan Penyelidik
Signature of Researcher

22 June 2007

Tarikh
Date

Komen Jawatankuasa Penyelidikan Pusat Pengajian/Pusat
Comments by the Research Committees of Schools/Centres

Dari laporan projek didapati, kemajuan dan hasil yang diperolehi telah mencapai objektif.

Dua kertas akademik telah dihasilkan dan diterbit dalam jurnal antarabangsa.

2-7-2007

TANDATANGAN PENGERUSI
JAWATANKUASA PENYELIDIKAN
PUSAT PENGAJIAN/PUSAT
Signature of Chairman
[Research Committee of School/Centre]

Tarikh
Date

Appendix A

English Abstract:

Silica (SiO_2) thin film on Si with low dielectric constant (k) properties has been systematically prepared and investigated. Two types of this low-k material have been deposited on Si via sol-gel spin-on coating. Tetraethylorthosilicate (TEOS) was used as a precursor to produce the first type of film. The effects of precursor aging (0, 2, 4, and 6 days) and post-deposition treatment time (0, 1, 2, 3 h) on photo-assisted condition have been investigated. The other type of film was derived from a mixture of TEOS and methyltriethoxysilane (MTES). Different molar ratio of TEOS/MTES (1:1, 2:1 4:1 and 6:1) and post deposition annealing condition (300-500°C for 30 minutes in argon) have been investigated. The physical properties of the dielectric film was characterized using Filmetric, fourier transform infrared spectroscopy, X-ray diffraction, atomic force microscope (AFM), and scanning electron microscope; while the electrical properties were investigated by conductive AFM and a semiconductor parameter analyzer. The best film derived from TEOS alone was using longest aging time of precursor with longest photo exposure time. Using a mixture of TEOS:MTES=4:1, the derived film with the lowest leakage current and k value (1.93) was annealed at 500°C.

Malay Abstract:

Filem nipis silika (SiO_2) yang berpemalar dieletrik rendah endap di atas Si tlah disediakan dan dikaji dengan sistematik. Dua jenis film nipis telah disediakan menggunkan pemutaran sol-gel. Tetraethylorthosilicate (TEOS) telah digunakan sebagai prapenanda untuk film jenis pertama. Kesan masa penuaan (0, 2, 4, dan 6 hari) dan rawatan pasca pengendapan (0, 1, 2, 3 jam) ke atas keadaan rawatan foto telah dikaji. Film nipis lagi satu telah disediakan dengan campuran TEOS dan methyltriethoxysilane (MTES). Nisbah molar TEOS/MTES (1:1, 2:1 4:1 dan 6:1) dan suhu rawatan pasca pengendapan (300-500°C, 30 min. di argon) telah dikaji. Sifat fizikal film telah dicirikan dengan *Filmetric, fourier transform infrared spectroscopy, X-ray diffraction, atomic force microscope (AFM)*, dan *scanning electron microscope*; manakala sifat elektrik telah dikajikan dengan *conductive AFM* dan semiconductor parameter analyzer. Film yang paling bagus disediakan dengan TEOS sahaja ialah daripada prapenanda dan rawatan foto yang palingg lama. Dengan menggunakan prapenanda campuran (4:1) telah menghasilkan film berarus bocor paling rendah dan nilai k (1.93) bila dirawat pada 500°C.

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Effects of precursor aging and post-deposition treatment time on photo-assisted sol–gel derived low-dielectric constant SiO_2 thin film on Si

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Abstract

In this paper, we have reported the results of sol–gel derived low dielectric constant SiO_2 treated with UV light as a function of precursor aging time and post-deposition UV exposure time. Filmetrics, Fourier-transform infrared, and scanning electron microscope were employed to characterize the films. Precursor aged for the longest time (4 days) has demonstrated the lowest refractive index, which can be related to reduction of dynamic dielectric constant (k_e). However, when the UV exposure time increased, the k_e value also increased. These observations have been explained in the text.

Keywords: Sol-gel; Low-dielectric constant thin film; Fourier-transform infrared

1. Introduction

The evolution of integrated circuit (IC) devices is governed by Moore's law. It is achieved largely through die shirks. As the semiconductor node moves from 0.25 μm to lower values, a critical point is reached where the reduction in signal propagation delay (or *RC* delay, where *R* and *C* refer to resistance and capacitance, respectively) due to a shorter path is offset by a higher resistance of metal trace and an increased effect of the inter and intra-layers of insulating dielectrics [1]. As such, the conventional thermal growth and chemical vapor deposited SiO_2 with dielectric constant (k) of 3.9 is not able to meet the requirement as inter and intra-layers of insulating di-electrics. This *RC* delay can be reduced by lowering the capacitance, *C*, value, whereby a lower k material is used [1].

Many polymers have been considered as low-k materials, however, they are having poor thermal stability and mechanical strength [2,3]. Comparatively, sol–gel derived silica has demonstrated a better property but their k values are not as low as their polymer counterparts [4,5]. In this project, SiO_2 thin film with k value lower than the convention thermal and chemical vapor deposited SiO_2 will be deposited on silicon (Si) by sol–gel spin-on-coating and post-deposition treatment under UV light at various times. The morphology and chemical structures of the films will be studied.

2. Experimental procedures

Tetraethyl orthosilicate (TEOS), deionized water (DI), ethanol, and HCl were used to prepare a crystal clear precursor for the sol–gel derived SiO_2 thin films. Firstly, a mixture of 12.4 mol ratio of DI:TEOS was prepared under stirring condition. An appropriate amount of ethanol was added to the mixture and then followed by a few drops of HCl to control pH of the precursor. The precursor was stirred for 90 min so that hydrolysis could be initiated. The product was then divided into four equal amounts and stored in four different beakers. The beakers were labeled as A, B, C, and D; indicating the aging time for the precursor before deposition. The aging time for A, B, C, and D were 0, 2, 4, and 6 days, respectively. After underwent an appropriate aging, the precursor was ready to be applied on a RCA-cleaned Si (1 0 0) wafer. A spinner

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was used to perform the spin-on-coating process with a speed and time of 4000 rpm and 45 s, respectively. After spinning, the sample was inserted in a chamber with UV wavelength of 250 nm for the post-deposition treatment. The samples were exposed at the same wavelength for different durations. After the treatment the samples were sent for characterization. The thickness and optical properties of the films were examined by a Filmetrics system. The chemical structure of the films was characterized using a Fourier-transform infrared (FTIR). Scanning electron microscopy (SEM, SUPRA-35VP) was utilized to investigate the morphology of the films.

3. Results and discussion

Sample D that has been aged for 6 days has fully transformed into gel form. Therefore, it could not be used in the subsequent process. Fig. 1 shows the result of oxide thickness as a function of UV exposure time for the three types of samples (A, B, and C). As UV exposure time increases, the oxide thickness decreases but the changes are small. This indicates that densification of the gel to solid state occurs as UV exposure time increases. In contrast, oxide thickness significantly increases as the aging time of the precursor increases from 0 to 4 days. This is probably due to the increase of polymerization of the precursor as the aging time increases and attribute to a more viscous precursor.

Fig. 2 presents the refractive index (n) of the thin film as a function of UV exposure time. All of the samples revealed n value lower than the conventional thermal and chemical vapor deposited SiO_2 films ($n = 1.46$). This indicates that the sol–gel derived SiO_2 film in this work probably has a larger porosity or larger chemical structures. This may imply that the dielectric constant (k) of the thin film is also relatively smaller than the SiO_2 film prepared by conventional methods. As UV exposure time increases, n value also demonstrated an increasing trend. Contrary, the n value decreases dramatically as the aging time of the precursor increases. Since the polymerization may initiate after a period of aging, the chemical structures could become larger than non-aged precursor. This suggests that the reduction of n value is most probably attributed to the change of chemical structures that may induce pores in the film.

The dynamic dielectric constant (k_e) of these films has been investigated at UV-visible range using a Filmetrics system at wavelength of 632.8 nm. The squared of the n value obtained from this wavelength provides the k_e value (Fig. 3) as shown in Eq. (1). The trend of k_e as a function of UV exposure time and precursor aging time are similar to Fig. 2.

$$k_e = n^2. \tag{1}$$

Fig. 4 reveals the FTIR spectra for the SiO_2 thin film prepared from precursor aged for 4 days and treated under

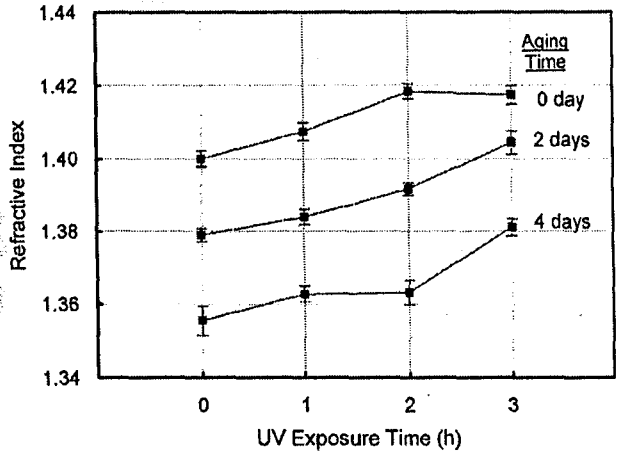

Fig. 2. Refractive index as a function of UV exposure time for samples prepared from precursor aged at different period.

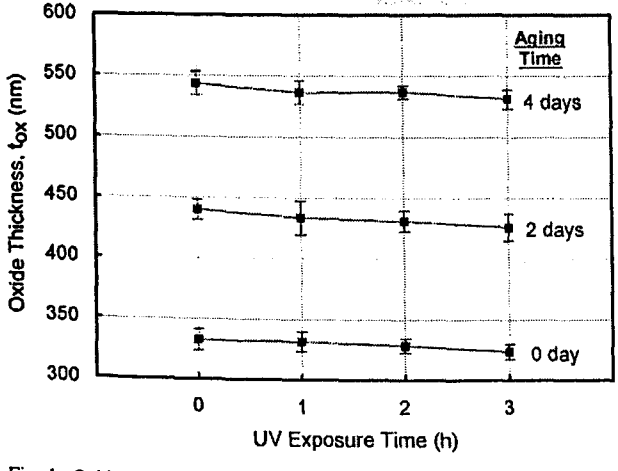

Fig. 1. Oxide thickness as a function of UV exposure time for samples prepared from precursor aged at different period.

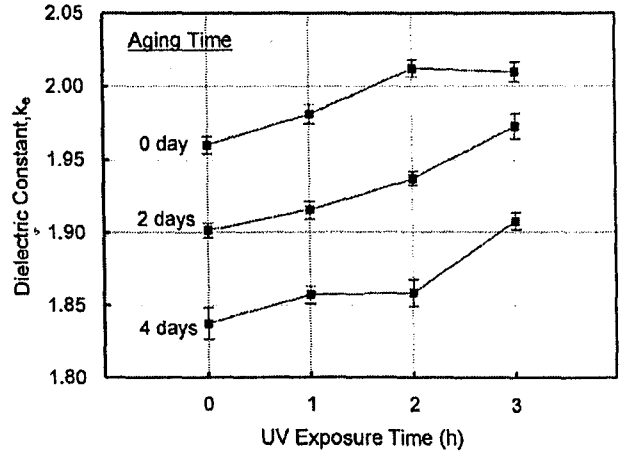

Fig. 3. Dynamic dielectric constant as a function of UV exposure time for samples prepared from precursor aged at different period.

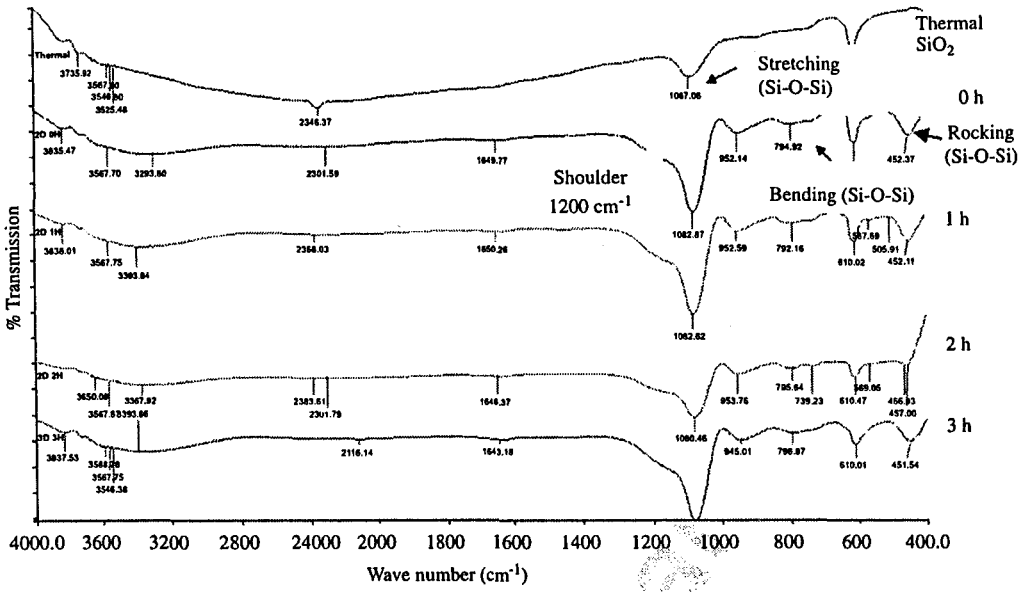

Fig. 4. A comparison of FTIR spectra for samples prepared from precursor aged for 4 days treated at different UV exposure time and thermal SiO_2 sample.

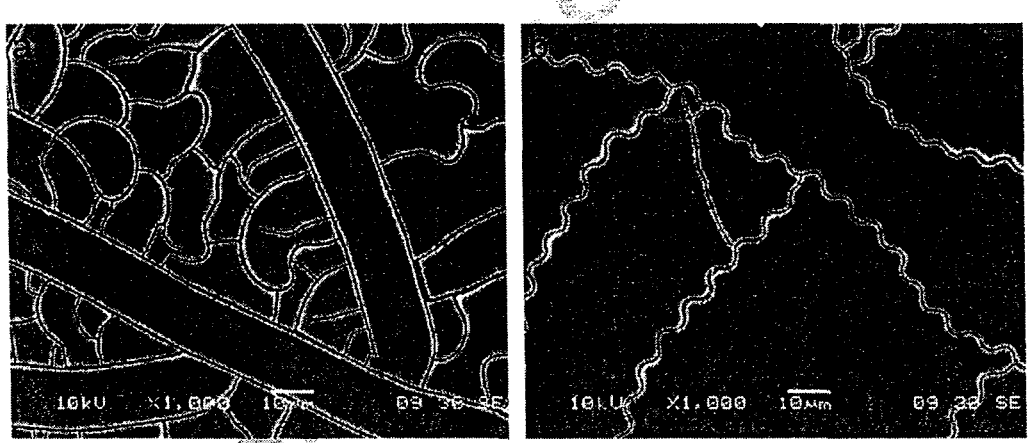

Fig. 5. SEM micrographs of samples prepared from precursor aged for 4 days and treated at (a) 0 and (b) 3 h of UV light.

UV light at different durations. These spectra are also compared with a spectrum obtained from a conventional thermal SiO_2 thin film. From the spectra, individual peaks with wave numbers have been included. Peaks representing SiO_2 structures and the mode of the structures have also been included for comparison. Besides having stretching mode of Si–O–Si, rocking (454 cm^{-1}) and bending (739 cm^{-1}) modes of Si–O–Si were also observed in the sol–gel derived SiO_2 films. A shoulder at 1200 cm^{-1} is also being observed in all the spectra of the investigated films. This shoulder indicates an increase of stretch in Si–O–Si of this films if compared with the conventional SiO_2 film [6]. Some reports also suggested that the appearance of this shoulder may attribute to the decrease of refractive index (n) [6]. This conclusion is in agreement with the observation obtained in this work. In general, the shape of the FTIR spectra of the remaining two samples (aged at 0 and 2 days) are almost similar to Fig. 4.

Fig. 5(a) and (b) compares the SEM micrographs of the sol–gel derived SiO_2 films prepared from precursor aged for 4 days. The non-UV treated film (Fig. 5(a)) shows a random microcrack on the film surface. After the UV treatment, the cracks have been reduced significantly. The actual reason for this reduction has yet been investigated. The most probable explanation of this observation may be due to the breaking of huge chemical structures derived

from the long aging time of the precursor. After this breaking process, UV may also be introduced to enhance the drying process of the film.

4. Conclusions

The effect of precursor aging time and of post-deposition UV exposure time of sol–gel derived low dielectric constant SiO_2 have been investigated and reported in this paper. Optical properties, chemical structures, and film morphology have been studied. Samples prepared from precursor aged for the longest time revealed the lowest dynamic dielectric constant. This constant was increased when UV exposure time increased. These observations have been explained in the text.

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Effects of Annealing Temperature on Low Dielectric Constant SiO_2 Thin Films Derived from Sol-gel Tetraethylorthosilicate and Methyltriethoxysilane Source

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Abstract

The results of low dielectric constant (k) SiO_2 films derived from sol-gel spin-on coating process using a combination of tetraethylorthosilicate (TEOS) and methyltriethoxysilane (MTES) (mole ratio of TEOS:MTES = 4:1) have been reported. The effects of post deposition annealing temperature (300 to 500 °C for 30 min in argon ambient) on the physical, chemical, and electrical properties of the oxide have been systematically investigated. Filmetric system, Fourier transform infrared spectroscope, x-ray diffraction system, atomic force microscope, and field-emission scanning electron microscope with energy dispersive x-ray have been employed for physical and chemical analyses. Electrical property of the oxide, in terms of leakage current through the oxide, has also been investigated. The oxide annealed at 500 °C produced the lowest dielectric constant value (k=2.3) and the lowest leakage current with no obvious oxide breakdown. The explanation of this observation has been discussed.

1. Introduction

The growth of integrated circuit technology is primarily based on the ability of minimum feature size in the circuits to continue shrink down to deep submicron region. Smaller devices give higher packing density as well as higher operating speeds. However, with a higher device speed, there is an almost inevitable need to reduce RC delay in multilevel interconnections; where R and C are resistance and capacitance, respectively. This RC delay can either be reduced by lowering R value of metal interconnect, whereby aluminum is replaced by copper, and/or C value of interlayer dielectric (ILD), whereby a conventional oxide is replaced by a lower k material [1,2].

A variety of low k materials have been reported, such as non-fluorinated polymers, organic polymer, and silica (SiO_2) [2,3]. Among these materials, low-k SiO_2 has demonstrated a more structural and thermal stable film than others [2]. Many techniques have been used to produce SiO_2-based low k materials. Sol-gel spin-on coating is appeared to be a more extendible method as it is able to fill various aspect ratio of interconnects and produce porous structures that can further lower the k value (1.3-2.5) [2-5]. Although a lower k value of sol-gel derived SiO_2 films can be produced from inorganic Si source, such as tetraethylorthosilicate (TEOS), a few issues need to be addressed. One of the issues is the absorption of moisture on SiO_2 surface due to presence of hydrophilic (Si-OH or Si-OCH_3) groups. This may cause the films to crack and properties to deteriorate with time. In order to solve this problem, organic solution, such as methyltriethoxysilane (MTES), has been added into the TEOS precursor [5-7]. Yu *et al.* have reported that by using a combination of this solutions with mole ratio ranging from TEOS:MTES = 2.0:1 to 0.25:1 and by varying the annealing temperature of the film from 300 to 450 °C, physical and electrical properties of the SiO_2 film

could be improved [5,6]. In this paper, we are reporting the physical, chemical, and electrical results of sol-gel derived SiO_2 thin films from a combination of a higher TEOS:MTES ratio (4:1). The effect of annealing temperature (300-500 °C) on the properties of the films has also been systematically investigated.

2. Experiment

Two types of sol have been prepared in order to produce a silica sol. Sol A consisted of a mixture of TEOS (Fluka), ethanol (J. T. Baker) and deionized (DI) water, and an appropriate amount of HCl (J. T. Baker) as a catalyst. Sol B was contenting a mixture of MTES (Fluka) as an organic precursor, ethanol, DI water, and NH_4OH (J. T. Baker) as a base catalyst. Both sols, with a mole ratio of so; A: sol B = 4:1were mixed together and allowed to hydrolyze for 24 h. After that, the solution was applied on a pre-cleaned Si (100) substrate placed on a spin coater. The sol-gel spinning process was conducted at a speed of 3000 rpm for 30 s. Subsequently after the spinning, the as-deposited film was soaked into a mixture of hexamethyldisilazane (HMDS) (Merck) and toluene (BDH) solution; so that surface modification was initiated. After this process, the film was then heat-treated independently at 300, 400 and 500 °C in argon-flow ambient for 30 min. After the heat treatment, the samples were sent for physical characterization. For electrical characterization, a layer of aluminum was evaporated onto the film and then patterned into area (A) of 9.98×10^{-4} cm^2. The subsequent process of fabricating it into metal-oxide-semiconductor (MOS) test structure has been described elsewhere [8].

The oxide thickness (t_{ox}) and refractive index (n) of the films were examined by a Filmetrics system. From the n value, density of the oxide, ρ, can be determined using the following relationship [9]:

$$\rho = (n - 1)/0.202 \quad (1).$$

By knowing ρ value, porosity (Π) and dielectric constant (k) of the oxide can be deduced from the following equations [7]:

$$\Pi = 1 - \rho/\rho_s \quad (2)$$

and

$$k = 1 + 6.33(n - 1) \quad (3)$$

where ρ_s is the density of a thermally grown conventional SiO_2 film (2.27 g/cm^3). Chemical structure of the oxide was characterized at room temperature using a Fourier transform infrared spectrometer (FT-IR) (Perkin Elmer). X-ray diffractometer (XRD) (PANalytical X'pert Pro MRD 3040) was used to investigate structure, phase, preferred crystal orientation, and crystallite size of the oxide. Energy dispersive x-ray analyzer (EDX) (JSM-6460LV) together with field emission scanning electron microscope (FESEM) was employed to study the morphology and chemical element of the oxide. Surface roughness of the oxide was characterized by an atomic force microscope (AFM) (Nano Navi SII). The electrical behavior of the oxides, in terms of leakage current through the oxide, has been evaluated using current-voltage (I-V) measurement (KEITHLEY 238 High Current Source Measurement Unit). The obtained I-V measurement was then transformed into current density (J)-electric field (E) plot. The J value was calculated by J = I/A and E is approximated by $E \cong V/t_{ox}$.

3. Results and Discussion

Figure 1 shows the results of oxide thickness (t_{ox}) and refractive index (n) as a function of annealing temperature. The t_{ox} is in the range of 110 to 160 nm for all the samples. The effect of annealing temperature has great influence on n value of the oxide. It can be seen that n value is decreased with an increase of annealing

temperature [10]. Figure 2 presents the calculated percentage of porosity (Π%) and dielectric constant (k) values of the oxide as a function of the annealing temperature. When anneal temperature increases from 300 °C to 500 °C, Π% value increases from 19.07 % to 54.19 %, while k value decreases from 4.5 to 2.3. This observation may be attributed to the increase of open void appears in the oxide, which contributed to the lowering of k value as the annealing temperature is increased.

Figure 3 shows the transmittance mode of FT-IR spectra of the oxides annealed at different temperatures. The strongest peak located at around 1060 cm^{-1} is attributed to a stretching of Si–O–Si bond. A shoulder of this peak is extended to wave number of approximately 1100 to 1200 cm^{-1} depending on the annealing temperature. This shoulder refers to a longitudinal optical (LO) vibration of Si–O–Si linkage. The appearance of this LO shoulder is due to optical scattering effect of porous sample [6]. This is an indirect method to deduce the porosity appears in a sample and it will be elaborate further in the subsequent paragraph. There are another two peaks revealed at around 800 cm^{-1} and 460 cm^{-1}. These are contributed by bending of O–Si–O and Si–O–Si bonds. The presence of the bending O–Si–O bond is caused by hydrolysis process occurred in the oxide. Meanwhile, the previous mentioned stretching Si–O–Si bonds is attributed to the condensation process of the oxide; which involves hydroxyls group and subsequently initiated the formation of inorganic polymer of Si–O–Si bond. These are the transmittance peaks related to SiO_2. Besides, peaks associated with Si substrate and incomplete or contamination of organic substances have been detected at location around 610 cm^{-1} (Si–Si bond) and >2300 cm^{-1} (2340 cm^{-1}, 3400 cm^{-1}, and 3600 cm^{-1} are related to Si–CH_3, Si–H, and stretching of O–H, respectively). As the

annealing temperature increases, the later peak is reduced until it could not be detected [11].

The shift of transmittance peak located around 1060 cm^{-1} as a function of annealing temperature is shown in Fig. 4. The shift of the position is also accompanied by the change of full-width at half-maximum (FWHM) of the peak. When the annealing temperature increases from 300 to 400 °C, the peak of Si–O–Si stretching bond is shifted to a higher value; which is closer to its theoretical value of 1080 cm^{-1}. However, there is a reduction in the FWHM of the peak. Hence, we may conclude that a densification of the film is obtained as the stretching of Si–O–Si bond is less in oxide annealed at 400 °C if compared with oxide annealed at 300 °C [12]. However, when the annealing temperature is further increased to 500 °C, the position of the peak is shifted to a lower wave number; which is further away from 1080 cm^{-1}. At the same time, the FWHM value of the particular peak is increased. This indicates that the stretching of Si–O–Si bond is increased if compared with the oxide annealed at 400 °C. During this bond stretching process, it may generate vacancy of oxygen atom. This vacancy may be treated as a donor like trap (Si^{+}). The deficiency of oxygen has been proven by EDX results (Fig. 5) obtained from FESEM investigation under a full area of 10,000X magnification (the micrographs are not shown). It can be observed that the weight percentage and atomic percentage of oxygen is decreased when the oxide is annealed at 500 °C.

The XRD patterns for samples annealed at different temperatures are showed in Fig. 6. The result is matched with phase and structure of SiO_2 using a JCPDS file number = 5-0490. There are two obvious peaks at 44.35° and 68.99°, associated with

SiO_2 (200) and (203), respectively, in all samples. As the annealing temperature increases, the later orientation of SiO_2 is reduced.

Topography of oxide surface has been altered as the annealing temperature increases. Quantitatively, root-mean-square (RMS) roughness and n-point mean height (R_z) of the investigated surfaces have been extracted and their results are presented in Fig. 7. The value of RMS roughness and R_z are increased with the increase of annealing temperature. The surface of the film becomes rougher as the annealing temperature increases may attribute to grain growth process [13].

Figure 8 presents the J-E plot of oxides annealed at different temperatures. When annealing temperature increases, at a specific E, the J value is reduced. This indicates that leakage current has been reduced. The oxide breakdown field of the investigated oxide has been extracted from the J-E plots. This field refers to an instantaneous increase of J value at a particular electric field. It is obvious that oxide annealed at 400 and 300 °C have demonstrated a sharp increase of J at approximately 3.8 and 2.3 MV/cm, while there is no significant increase in oxide annealed at 500 °C.

The increment of breakdown field and reduction of leakage current at higher annealing temperature may be attributed to the increase of surface roughness as what has been revealed in Fig. 7. As the surface becomes rougher, the probability of a region with thicker oxide is high. The thicker oxide may restrict the movement of charge passing through the oxide. Therefore, a lower leakage current is detected. Besides surface roughness, deficiency of oxygen in oxide annealed at 500 °C may act as a donor-like trap for the injected electron. As the electron being injected from Si into the

oxide, majority of the electron is captured and neutralized in the trap. This is not happening in samples annealed at 300 and 400 °C. Therefore, the leakage current is much lower than those oxides. From the electrical results, it could be concluded that the oxide structure is strong as it is becoming more difficult to electrically break the oxide, even though the percentage of porosity in the oxide is increasing with the increase of annealing temperature (Fig. 2)

4. Conclusion

Low dielectric constant (k = 2.3) SiO_2 thin films were fabricated using sol-gel process with a combination of tetraethylorthosilicate and methyltriethoxysilane. The post deposition annealing temperature has a great effect on the physical, chemical, and electrical properties of the films. With increasing annealing temperature, percentage of porosity has been increased while the dielectric constant and refractive index of the oxide have been decreased. The high value of oxide surface roughness and appeared of donor-like trap in the oxide was main caused of the low leakage current detected in oxide annealed at higher temperature.

Acknowledgment

The authors would like to acknowledge the financial support provided by Universiti Sains Malaysia through USM Short Term Research Grant (6035150).

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Figure Caption

Fig. 1: The oxide thickness and refractive index as a function of annealing temperature.

Fig. 2: The calculated percentage of porosity and dielectric constant of SiO_2 films annealed at different temperatures.

Fig. 3: Transmittance mode FTIR spectra of the investigated oxides annealed at different temperatures.

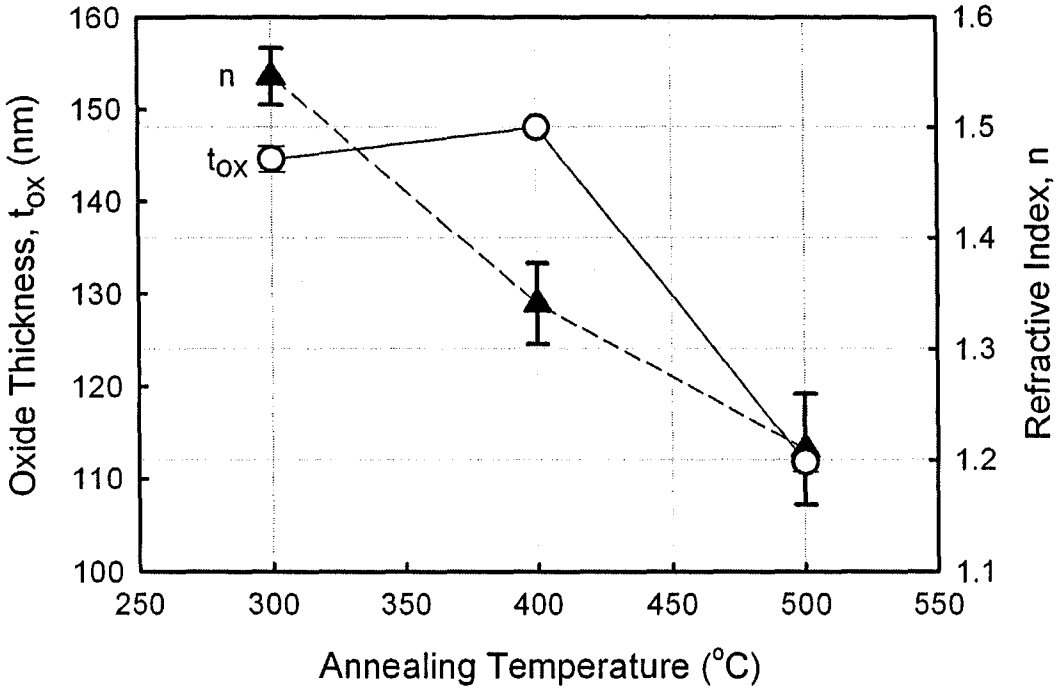
Fig. 4: Wave number and full-width at half-maximum (FWHM) of Si-O-Si stretching bond as a function of annealing temperature.

Fig. 5: Weight percentage and atomic percentage of oxygen element detected in oxides annealed at different temperatures. The percentages were deduced from an area of 10,000X magnification.

Fig. 6: Pattern of XRD as a function of annealing temperature.

Fig. 7: A comparison between root-mean-square (RMS) roughness and n-point mean height (R_z) as a function of annealing temperature.

Fig. 8: Current density–electric field characteristics of oxides annealed at different temperatures.



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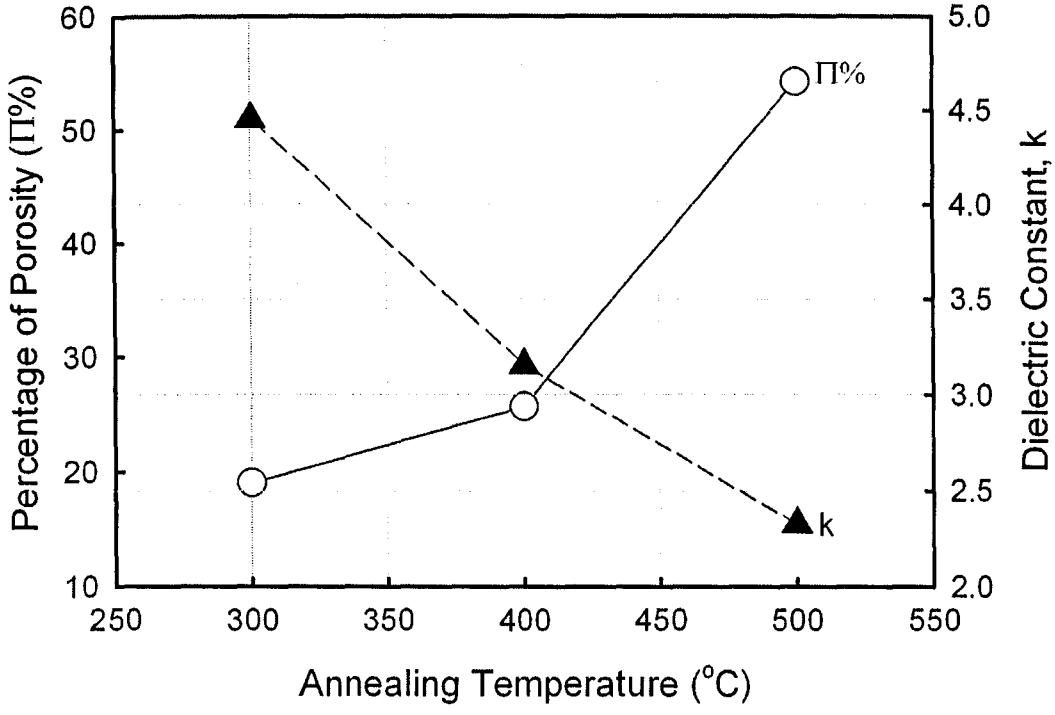

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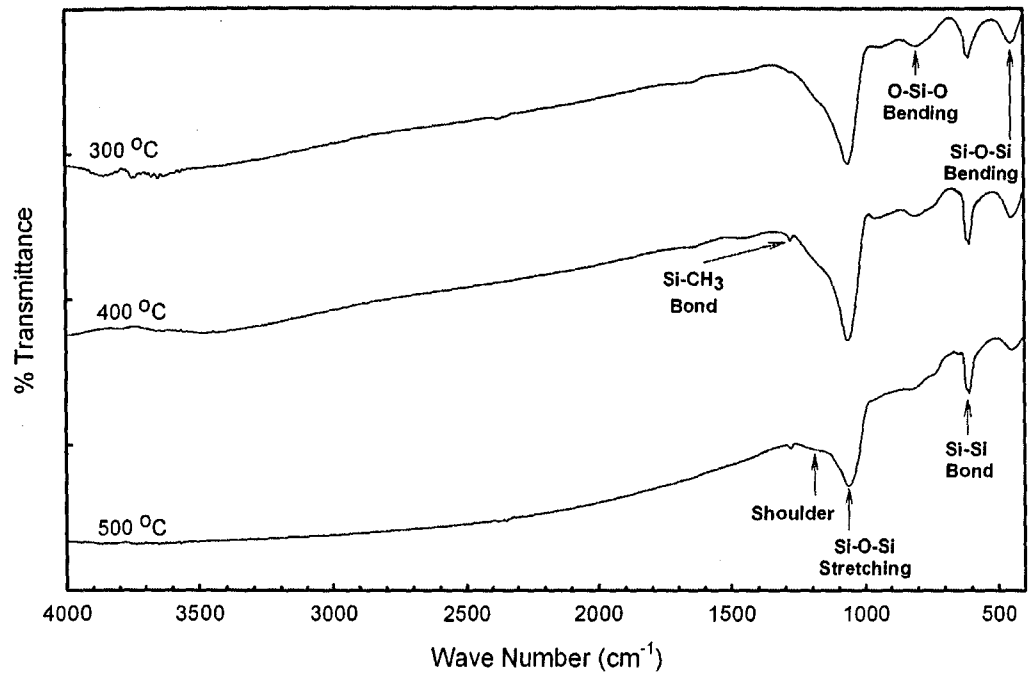

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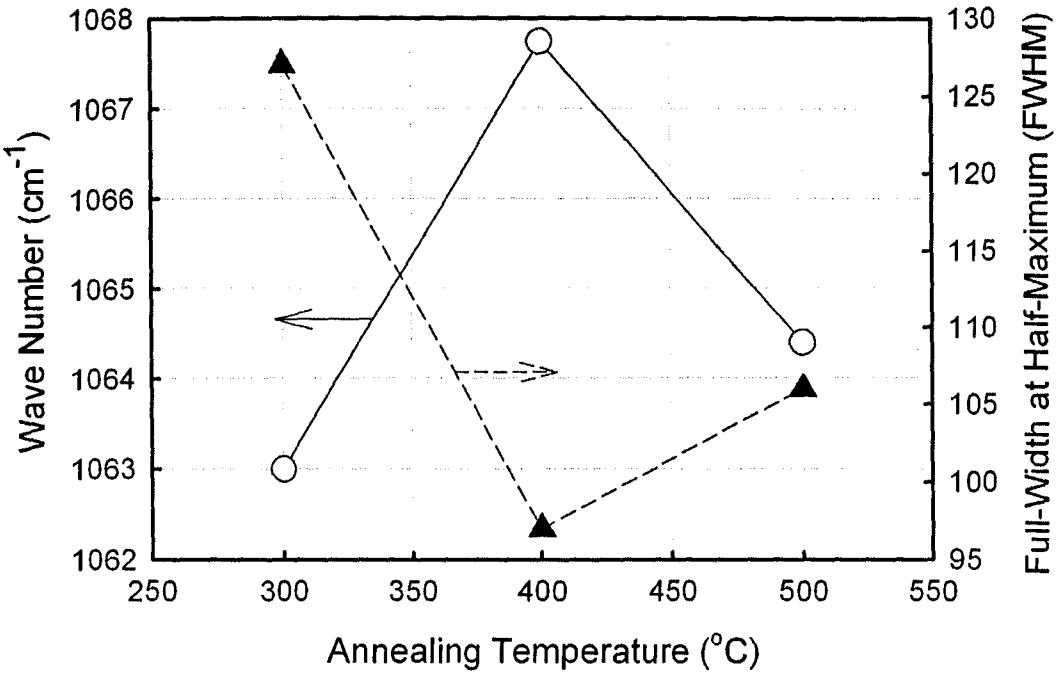

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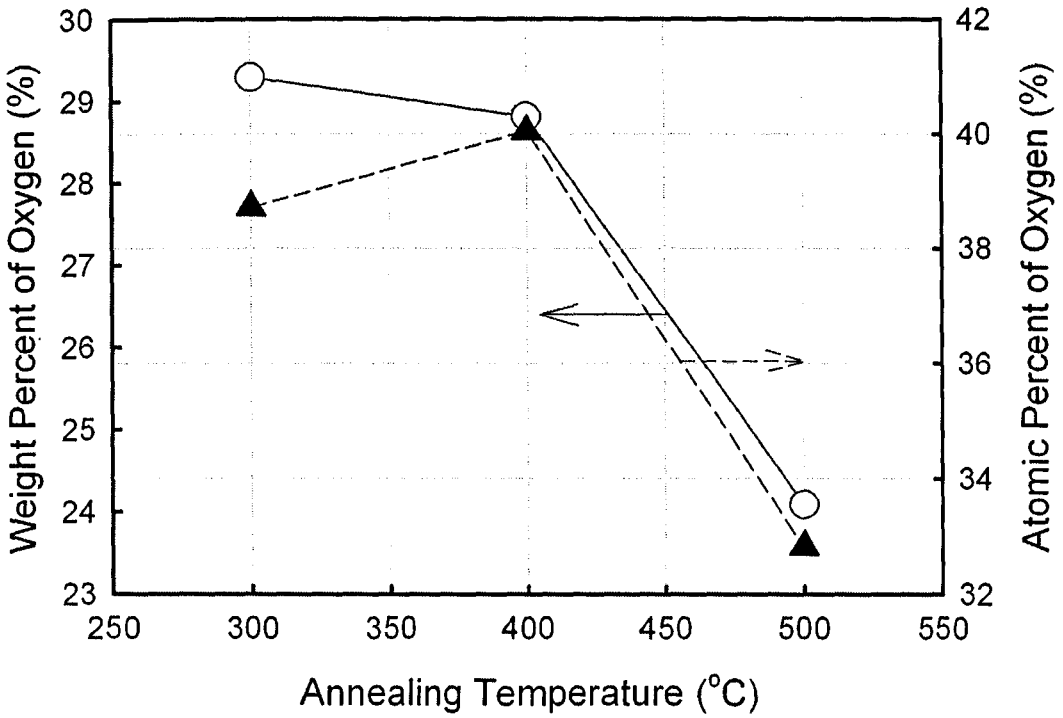

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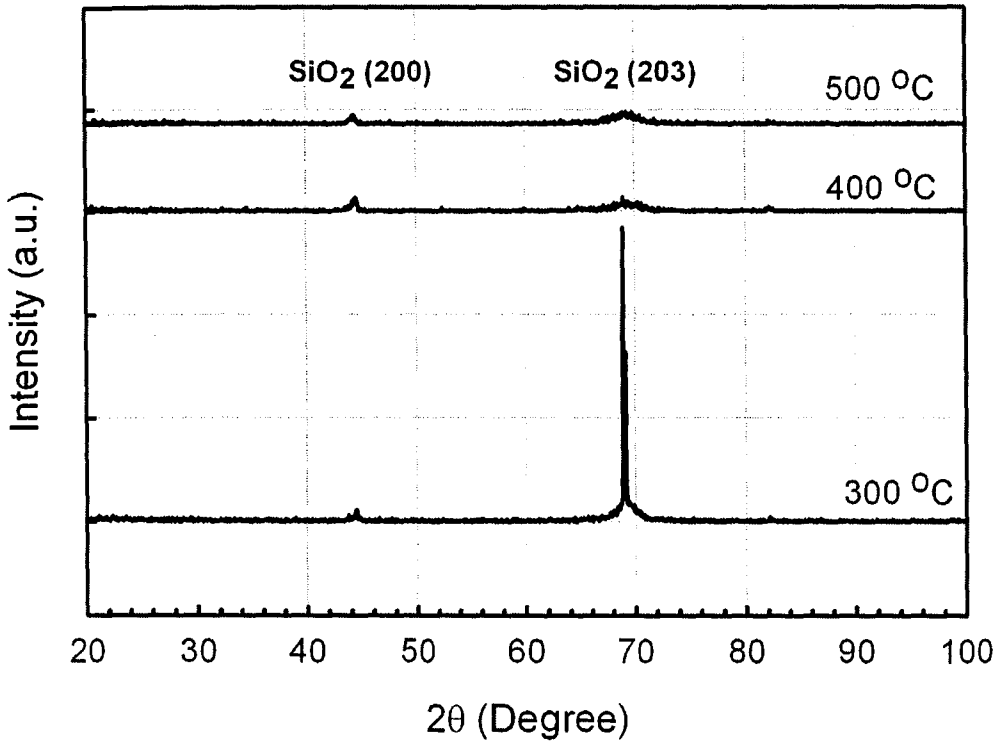

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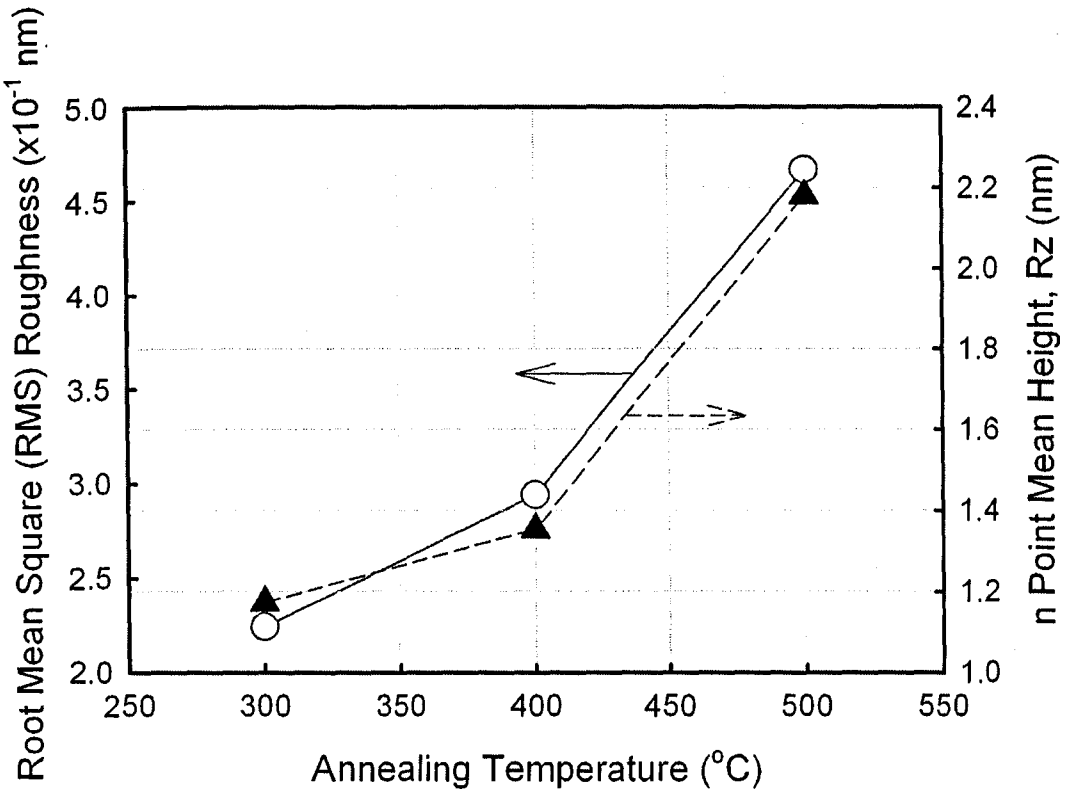

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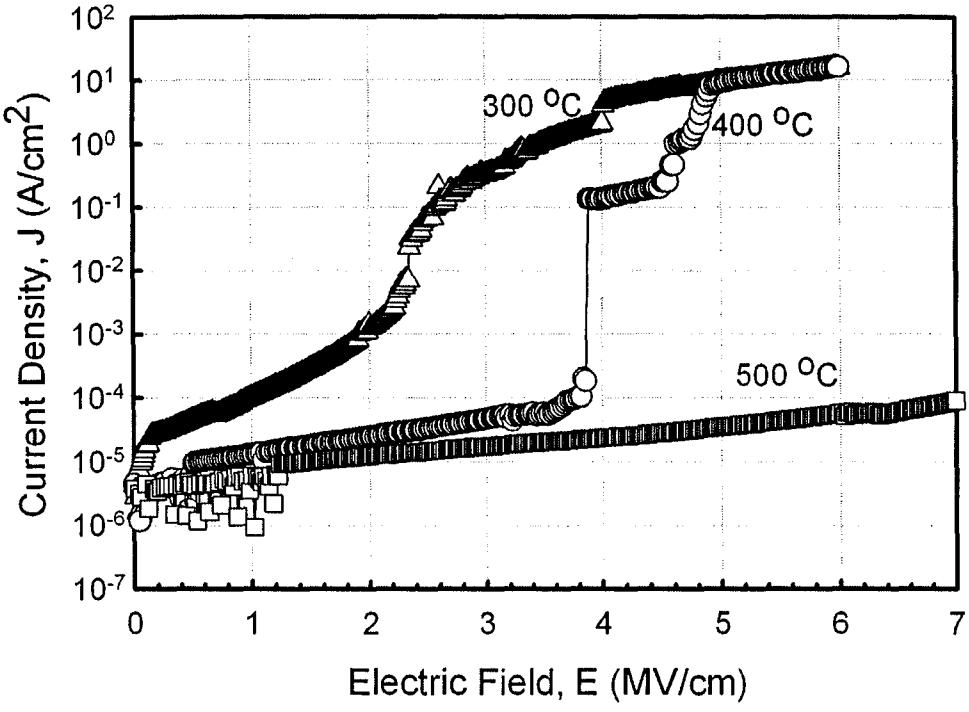

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DEVELOPMENT OF LOCALIZED SELECTIVE-STRESS ETCH-STOP-LAYER (ESL) FOR A NEW CMOS INTEGRATION SCHEME (OLD TITLE)

INVESTIGATION OF LOW DIELECTRIC CONSTANT (k) FILMS FOR DEEP SUB-MICRON CMOS APPLICATION (NEW TITLE)

A Research Report
Submitted to

Research Creativity and Management Office
Universiti Sains Malaysia

by

Ir. Dr. Cheong Kuan Yew (Principle Researcher)
Assoc. Prof. Dr. Luay Bakir Hussain

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Research Assistant – 1 student

- July 2006 – Oct 2006: Ms Khor Siew Cheng

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IR. DR. CHEONG KUAN YEW
ASSOC. PROF. DR. LUAY BAKIR HUSSAIN

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ABSTRACT

Silica (SiO_2) thin film on Si with low dielectric constant (k) properties has been systematically prepared and investigated. Two types of this low-k material have been deposited on Si via sol-gel spin-on coating. Tetraethylorthosilicate (TEOS) was used as a precursor to produce the first type of film. The effects of precursor aging (0, 2, 4, and 6 days) and post-deposition treatment time (0, 1, 2, 3 h) on photo-assisted condition have been investigated. The other type of film was derived from a mixture of TEOS and methyltriethoxysilane (MTES). Different molar ratio of TEOS/MTES (1:1, 2:1 4:1 and 6:1) and post deposition annealing condition (300-500°C for 30 minutes in argon) have been investigated. The physical properties of the dielectric film was characterized using Filmetric, fourier transform infrared spectroscopy, X-ray diffraction, atomic force microscope (AFM), and scanning electron microscope; while the electrical properties were investigated by conductive AFM and a semiconductor parameter analyzer. The best film derived from TEOS alone was using longest aging time of precursor with longest photo exposure time. Using a mixture of TEOS:MTES=4:1, the derived film with the lowest leakage current and k value (1.93) was annealed at 500°C.

ABSTRAK

Filem nipis silika (SiO_2) yang berpemalar dieletrik rendah endap di atas Si tlah disediakan dan dikaji dengan sistematik. Dua jenis film nipis telah disediakan menggunkan pemutaran sol-gel. Tetraethylorthosilicate (TEOS) telah digunakan sebagai prapenanda untuk film jenis pertama. Kesan masa penuaan (0, 2, 4, dan 6 hari) dan rawatan pasca pengendapan (0, 1, 2, 3 jam) ke atas keadaan rawatan foto telah dikaji. Film nipis lagi satu telah disediakan dengan campuran TEOS dan methyltriethoxysilane (MTES). Nisbah molar TEOS/MTES (1:1, 2:1 4:1 dan 6:1) dan suhu rawatan pasca pengendapan (300-500°C, 30 min. di argon) telah dikaji. Sifat fizikal film telah dicirikan dengan *Filmetric, fourier transform infrared spectroscopy, X-ray diffraction, atomic force microscope (AFM)*, dan *scanning electron microscope*; manakala sifat elektrik telah dikajikan dengan *conductive AFM* dan semiconductor parameter analyzer. Film yang paling bagus disediakan dengan TEOS sahaja ialah daripada prapenanda dan rawatan foto yang palingg lama. Dengan menggunakan prapenanda campuran (4:1) telah menghasilkan film berarus bocor paling rendah dan nilai k (1.93) bila dirawat pada 500°C.

CHAPTER 1: INTRODUCTION

1.1 Introduction

The semiconductor industry is continuing its quest to create ever more powerful microprocessor and memory chips by ultra large-scale integration (ULSI) through the continue reduction of the minimum size of device features. Along with this goes a corresponding increase in device density on the chip, which in turn results in an increase in the number of wiring levels and a reduction in the wiring pitch [Yu *et al.*, 2004]. As device sizes continue to shrink down to the deep submicron region, they require a multilevel interconnection architecture to minimize the time delay due to parasitic resistance (R) and capacitance (C). The gain in device speed at the gate level is offset by the propagation delay at the metal interconnects because of the increased RC time constant. Therefore, the device interconnection network becomes a limiting factor in determining chip performance metrics such as device speed, cross talk, and power consumption of ULSI circuits [Sze, 2002].

Reducing the RC time constant of ULSI circuits requires interconnect materials with low resistivity and interlayer films with low capacitance. Note that

$$C = k\varepsilon_0 A / d \quad , \tag{1.1}$$

where ε_i is the free space permittivity,

A is the area of dielectric layer,

d is the thickness of the dielectric film, and

k is relative dielectric constant.

Regarding the low capacitance issue, it is not easy to lower the parasitic capacitance by increasing thickness of the interlayer dielectric (which makes gap filling more difficult) or decreasing wiring height and area (which result in the increase of interconnect resistance). Therefore, materials with low dielectric constant (low k) are required. The dielectric permittivity is equal to the product of k and ε_o, where k and ε_o are the relative dielectric constant and permittivity of free space [Sze, 2002].

Copper, is already replacing aluminum to take advantage of its lower resistivity. The next step will be the substitution of silicon dioxide with insulating films having lower dielectric constants as the interlayer dielectric for on-chip interconnections [Manjari *et al.*, 2002]. In order to improve circuit performance, new materials with lower dielectric constant than conventional SiO_2 (k = 4.0) are needed. By doping it with fluorine to produce fluorinated silica glass, this is lowered to 3.5. Another approach is to make a porous dielectric. The pores lead to a smaller average dielectric constant, since air has a dielectric constant of roughly 1.0. Among porous materials, porous silica films are more promising, because they usually have good mechanical strength and thermal stability and most importantly, they are compatible with the silicon wafer and related materials used in existing integrated circuit (IC) technology [Yu *et al.*, 2004]. For porous materials used as Inter-layer Dielectric (ILD), the porosity and pore size are critical. Higher porosity in the films can lower the dielectric constant, but normally it has also negative impact on other crucial properties of the films such as mechanical and

thermal properties. Consequently, porosity should be no higher than needed to achieve the desired dielectric goals. Pore dimensions being much smaller than the feature size of the devices are desirable to minimize film defects and reduce the risk of short circuits. Therefore, it is necessary to characterize the nature of the porosity to guide the synthetic efforts and to correlate a variety of electrical and mechanical properties

The spin-on option appears to be more extendible because it can produce porous materials leading to ultra low-k dielectrics ($k \leq 2.0$) that cannot be obtained by PECVD deposition. More importantly, the microstructure of the spin-on dielectrics, such as the porosity, pore size and pore interconnectivity, can be controlled precisely. One of the methods to fabricate spin-on films is by sol-gel technique [Yu *et al.*, 2004]. Oxides formed by the sol-gel process are of considerable technological interest for a variety of reasons: the technique is

1) inexpensive.
2) simple.
3) requires a relatively short annealing time.

Perhaps more importantly, the sol-gel process allows the use of multi component systems; one may tailor the electronic properties of the oxide by varying its chemical composition (Warren *et al.*, 1991).

Sol-gel derived silica films willl provide low dielectric constant but still caused

some problem. The thin films get deteriorated with time due to the absorption of moisture from the surroundings by the hydrophilic (Si–OH or Si–OCH_3) groups present on the surface. Hence, for long-term applications, the thin films need to have water repellent. Several co-precursors for example methyltrimethoxysilane (MTMS), methyltriethoxysilane (MTES) and dimethylchlorosilane (DMCS) can be used for this purpose [Rao & Kalesh, 2003].

Hydroxyl and silanol groups in the final product are harmful to dielectrics because they are readily absorbing moisture from the atmosphere. The absorbed moisture may increase the dielectric constant of the silica films and cause via hole poisoning and other integration problems. Thus, surface modification for example trimethylchlorosilicate (TMCS) and hexamethyldisilazane (HMDS) is necessary to reduce the silanol groups and keep the dielectric constant of the films low [Yu *et al.*, 2004].

Many sol gel method using different precursor have been done to produce low dielectric constant SiO_2 material. The most popular precursors being used are inorganic tetraethyl orthosilicate (TEOS) and organic methyltriethoxysilane (MTES) [Yu *et al.*, 2004]. The incorporation of organic precursor makes it easier to get crack-free films with thickness $\geq 1\,\mu m$. The ratio of TEOS and MTES (2.0, 1.5, 1.0, 0.5 and 0.25) also has a great influence on the structural and dielectric properties of the films [Yu *et al.*, 2004]. The annealing temperature (300, 400 and 450 °C) also affects the structural and

dielectric properties of the films. With increasing annealing temperature, porosity in the film increased, dielectric constant of the films decreased. [Yu *et al.*, 2004].

1.2 Research Objective

Two types of low-k dielectric SiO2 thin film have been systematically investigated. There are derived from (1) tetraethylorthosilicate (TEOS) and (2) mixture of TEOS and methyltriothoxysilane (MTES). The objectives of the first type of TEOS derived low-k SiO_2 films are:

1. To investigate the effects of precursor aging time on photo-assisted sol-gel derived low-dielectric constant sio_2 thin film on Si
2. To investigate the effects of post-deposition treatment time on photo-assisted sol-gel derived low-dielectric constant sio_2 thin film on Si

The objectives of the second type of TEOS/MTES derived low-k SiO_2 films are:

1. To fabricate low dielectric constant (k) porous silica thin films using sol-gel spin on coating technique with different ratio of tetraethylorthosilicate (TEOS) and methyltriothoxysilane (MTES) as precursors.
2. To study the effect of post-deposition annealing temperature on the properties of the thin films.

1.3 Research Scope

Research scope is:

a) Obtain the thickness and refractive index of SiO_2 thin films using Filmetrics.

b) Analyze the chemical structures present using Fourier Transform Infrared Spectroscopy (FTIR).

c) Analyze the SiO_2 thin films surface roughness using Atomic Force Microscope (AFM) and lateral propagation of the breakdown event at a nanometer scale from electrical considerations using CAFM.

d) Analyze the microstructure, grain and pore using scanning electron microscope (SEM) and determine the element presence using energy dispersive X-ray analysis (EDX).

e) Measure the properties electrical using semiconductor parameter analyzer (SPA).

f) Analyze on structures, phases, preferred crystal orientations and structural parameters crystallite size and crystallinity using X-ray Diffraction (XRD).

1.4 Report Structure

This report will be dividing to five main chapters. Introduction research project and objective will be presented at chapter 1. Chapter 2 discuss about literature review. Chapter 3 shows the experiment procedure and research result and discussion will be discussed at chapter 4. The last chapter is about conclusion and suggestion for the further study.

CHAPTER 2: LITERATURE REVIEW

2.1 CMOS Device

2.1.1 CMOS Device Introduction

Complementary metal-oxide-semiconductor (CMOS) is a major class of integrated circuits. CMOS are used in logic and memory chips, and they dominate the IC market.

Figure 2.1 shows the cross section of a simple CMOS structure. The need to reduce power consumption of the circuits for microprocessors and electronic components is one of the major driving forces for Complementary MOS (CMOS). In fact, currently only CMOS technology is used in advanced intergrated-circuit manufacturing due to the low power-dissipation requirement [Sze, 2002].

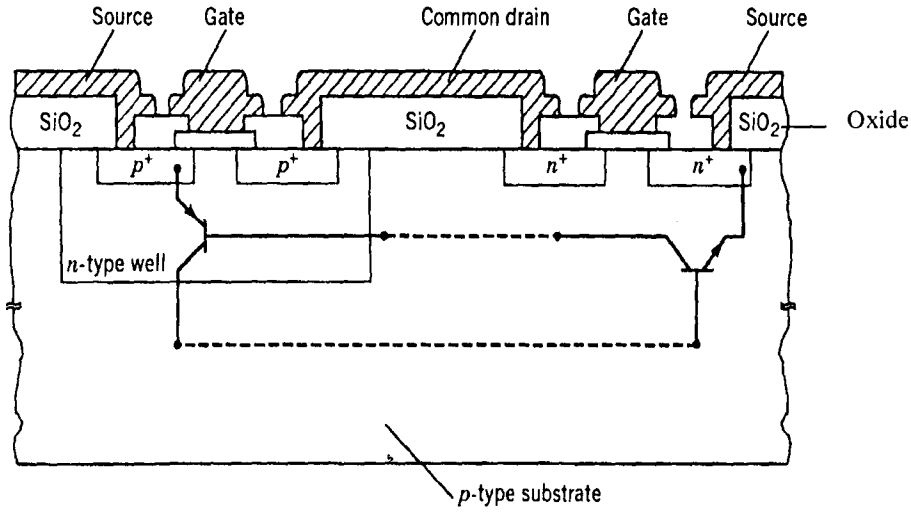

Figure 2.1: A metal gate CMOS transistor [Ghandhi, 1994].

2.1.2 CMOS Development History

In 1960, Bell Labs developed the technique of Epitaxial Deposition whereby a single crystal layer of material is deposited on a crystalline substrate. Epitaxial deposition is widely used in bipolar and sub-micron CMOS fabrication. Kahng at Bell Labs fabricates the first MOSFET at the same year. In 1961, Fairchild and Texas Instruments both introduce first commercial ICs. In 1963, Radio Corporation of America (RCA) produced the first PMOS IC. In 1963, Frank Wanlass at Fairchild Semiconductor originated and published the idea of complementary-MOS (CMOS). It occurred to Wanlass that a complementary circuit of NMOS and PMOS would draw very little current [Jones, 2000].

2.1.3 CMOS Roadmap

In the past 30 years with the success story of scaling each technology generation became smaller according to Moore's law, which predicted a decrease in feature sizes by a factor of 0.7 every three years. This made the chips faster by 15–30 % per year and reduced power consumption. It is argued that scaling may face a new situation. The area is still reduced, but performance is difficult to improve and costs may increase [Risch 2006].

The three main limiting factors for performance increase are indicated in Fig. 2.2. The three factors are:

1) source drain leakage,

2) gate leakage,

3) junction leakage.

This showed that the gate leakage stops SiO_2 scaling. Source drain leakage reduction needs higher channel doping and shallower junctions. However, this increases junction capacitance, junction leakage, gate induced drain currents, reduces carrier mobility and increases parasitic resistance [Risch, 2006].

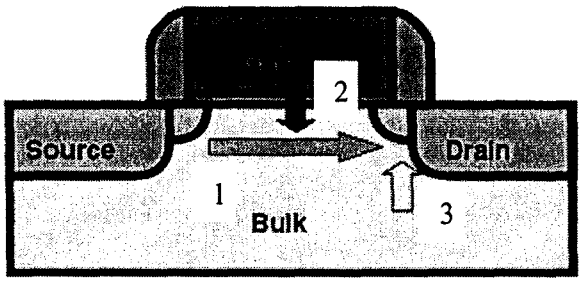

Figure 2.2: Device scaling limits of bulk devices: source, drain, gate and junction leakage currents [Risch 2006].

2.2 Low Dielectric Constant

2.2.1 Introduction of Dielectric

The relative dielectric constant of a material under given conditions is a measure of the extent to which it concentrates electrostatic lines of flux. It is the ratio of the amount of stored electrical energy when a potential is applied, relative to the permittivity of a vacuum. It is also called relative permittivity [Ruzyllo, 2003].

The dielectric constant is represented as k. It is defined as

$$k = \frac{\varepsilon_s}{\varepsilon_o} \tag{2.1}$$

where ε_s = static permittivity of the material

ε_0= vacuum permittivity

Vacuum permittivity is derived from *Maxwell's* equations by relating the electric field intensity E to the electric flux density D. In vacuum (free space), the permittivity ε is just ε_0, so the dielectric constant is 1.

The dielectric constant, k, is a parameter defining ability of material to store charge. Consequently, it also defines capacitance, C. Capacitor comprising of a layer of dielectric sandwiched between two metal plates. In Fig. 2.3 defines area of the capacitor contact (A) [Ruzyllo, 2003].

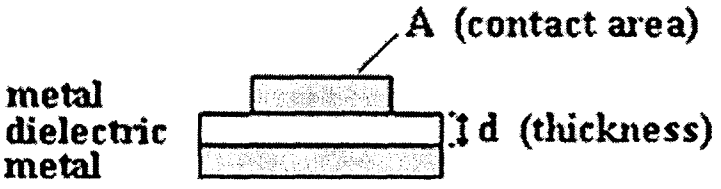

Figure 2.3: The values of dielectric being dependent on specimen thickness and Geometry [Ruzyllo, 2003].

Regnier et al., [1996] reported the silicon dioxide thin films prepared by plasma-enhanced chemical vapour deposition (PECVD) using an oxygen plasma and a mixture of 5 % silane in argon injected in the after glow. According to the obtained result, the electrical insulation is improved and reaches values typical of good insulators. A resistivity higher than 10^{15} Ω cm, a dielectric constant of 4.2 is obtained. The

dielectric constant values measured for thermally grown SiO_2 used as reference which showed 4.0. A dielectric that holds a lot of promise is SiO_2 based xerogel, which is a porous material having a dielectric constant k in the range of 1.3-2.5, compared to k = 4 for thermally grown SiO_2 [Manjari et al., 2002].

2.2.2 RC Delays in Interconnects

The circuit speed is limited by the total interconnect *"RC"* delay and the power dissipation is mainly limited by the total effective capacitances of the interconnect load. To reduce wasted power and improve speed, the parasitic capacitances and resistances in interconnects need to be reduced significantly. The gain in device speed at the gate level is offset by the propagation delay at the metal interconnects because of the increased RC time constant, as shown in Fig. 2.4 [May & Sze, 2002].

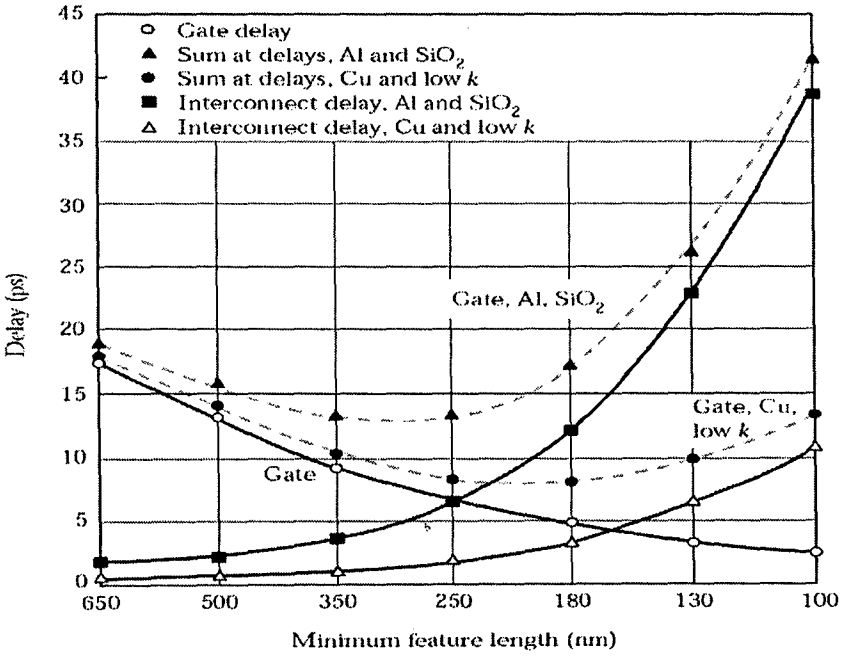

Figure 2.4: Calculated gate and interconnect delay versus technology generation [May & Sze, 2002].

The resistance of the interconnect line is [Wilson et al, 1993]:

$$R = \frac{pl}{wt_m} \tag{2.3}$$

where p = metal resistivity

l = length of the interconnect

w = width of the interconnect

t_m = metal thickness

To first order of the capacitance of an interconnect line with a metal plate above and below the line is given by [Wilson et al, 1993]:

$$C = \frac{\varepsilon_o lw}{d} \tag{2.4}$$

where ε_o = dielectric constant

l = interconnect length

w = metal width

d = thickness of ILD

The two main approaches for improving interconnect speed and power dissipation are [Vasudev, 1996]:

(i) Use of low dielectric materials for interlevel dielectric layers (ILDs).

(ii) Use of Cu as a plug-fill and conductor, replacing the conventional Al-alloy/ W-plug interconnect system in use today.

2.2.3 Low Dielectric Constant Materials

The properties of the interlayer dielectric film and how it formed have to meet the following requirements [May & Sze, 2002]:

i. low dielectric constant
ii. low residual stress
iii. high planarization capability
iv. high capability for gap filling
v. low deposition temperature
vi. simplicity of process
vii. ease of integration

A substantial number of low-k materials have been synthesized for the interlayer dielectric in ULSI circuits. Some of the promising low-k materials are shown in Table 2.1. These materials can be either inorganic or organic [May & Sze, 2002].

Table 2.1: Low-k materials [May & Sze, 2002].

Criteria	Materials	Dielectric Constant
Low-k materials	Polyimide	2.7-2.9
	SiLK(aromatic hydrocarbon polymer)	2.7
	PAE[poly(arylene ethers)]	2.6
	Fluorinated amorphous carbon	2.1
	TEOS / MTES	1.73-2.25
	Xerogels (porous silica)	1.1-2.0

2.2.4 Properties of Low Dielectric Constant Materials

Many sol-gel methods using different precursor have been done to produce low dielectric constant SiO_2 thin film. Different precursor and catalyst will affected thin film properties. Table 2.2 shows the various properties of SiO_2 thin film which produced by different precursor and catalyst.

Table 2.2: Properties of silicon dioxide thin films.

Properties	TEOS/ MTES	TEOS	Pure Silica Zeolite (PSZ) MEL	TEOS/ MPS + TEOS/ MTES	TEOS + HF as catalyst	TEOS and surface modification with TMCS
Thickness (nm)		300-490	-	910 (3 coating)	490	550
Dielectric Constant, k	1.98-2.25	1.9-2.5	1.5-2.4	1.8-2.8	1.65-2.6	2.45
Refractive Index, n_e	1.05-1.22	1.4-1.46	-	-	1.1-1.3	1.26
Fixed Oxide Charge ($1/cm^2$)	-	$8x10^{10}$ - $1x10^{11}$	-	-	-	-
Interface State Density (cm^2eV)	-	10^{11} - $5x10^{11}$	-	-	-	-
Mobile Ion Charge ($1/cm^2$)	-	$1x10^{11}$ - $1.5x10^{11}$	-	-	-	-
Resistivity (Ωcm)	-	10^{12}	-	-	-	-
Breakdown	-	$>10^6$	-	-	-	-

Field Strength (V/cm)						
Rrms (nm)	-	-	5.6	-	-	-
Ra (nm)	-	-	3.41	-	-	-
Density (kg/cm^3)	-	-	-	-	-	1.29
Leakage Current Density (Acm^{-2})	-	-	-	-	$9x10^{-6}$-$1.3x10^{-8}$	-
Porosity (%)	47.90-87.46	-	-	-	-	43.2
Reference	[Yu *et al.*, 2004]	[Manjari *et al.*, 2002]	[Li *et al.*, 2005]	[Seraji *et al.*, 2000]	[He *et al.*, 2006]	[Hong *et al.*, 1997]

Yu *et al.*, [2004] report the preliminary results on organic modified silica materials derived from sol-gel method. Yu *et al.*, [2004] used inorganic tetraethylorthosilicate (TEOS) and organic methyltriethoxysilane (MTES) as precursor. The incorporation of organic precursor makes it easier to get crack free films. The ratio of TEOS and MTES also has great influence on the structural and dielectric properties of the films [Yu *et al.*, 2004]. The refractive index and porosity of the films with different ratio of TEOS and MTES are shown in Fig. 2.5.

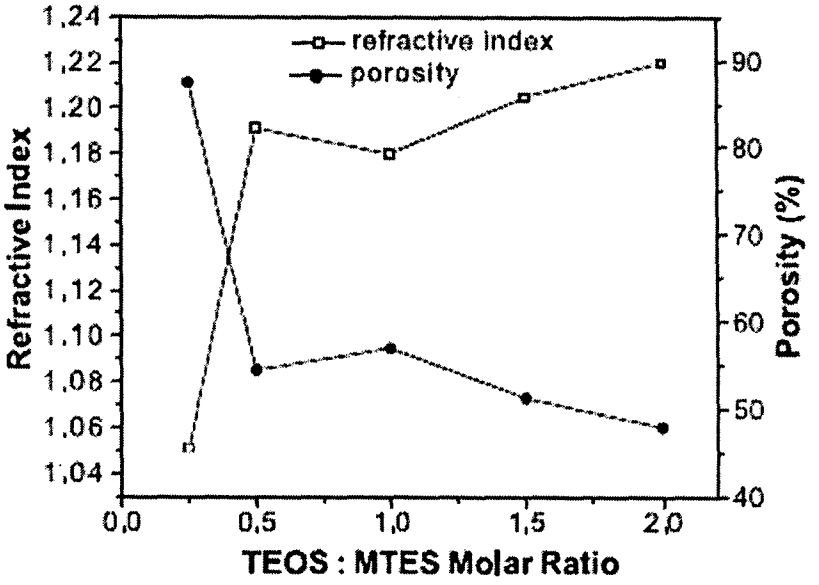

Figure 2.5: The refractive index and porosity of the films with different ratio [Yu *et al.*, 2004].

The dependence of dielectric constant of the films on the MTES concentration is shown in Table 2.3. The experiment dielectric measurements showed that the dielectric constant of the films decreased with increasing MTES due to the increase of the porosity.

Table 2.3: The dependence of dielectric constant of films on TEOS/MTES ratio [Yu *et al.*, 2004].

TEOS/MTES	2	1.5	1	0.5	0.25
Dielectric Constant	2.25	2.15	2.11	1.73	1.98

Manjari *et al.*, [2002] prepared silica xerogels by the sol-gel method following a two-step acid base catalyst process. The precursor TEOS is hydrolyzed by reacting with water and ethanol as the solvent. The hydrolysis reaction is accelerated by HCl which is the acid catalyst. After hydrolysis, the TEOS underwent condensation, which is accelerated by a base catalyst. Passivating properties of xerogel films through current-voltage (I-V) and capacitance-voltage (C-V) measurement is calculated. The value of the fixed oxide charge density, interface density, mobile ion charge and others properties have been calculated as shown at Table 2.3. A typical C-V plot is shown in Fig. 2.6, which displays well-marked accumulation, depletion, and inversion characteristics. The dielectric constants of the films were calculated and were found to be in the range 1.9-2.5 [Manjari *et al.*, 2002].

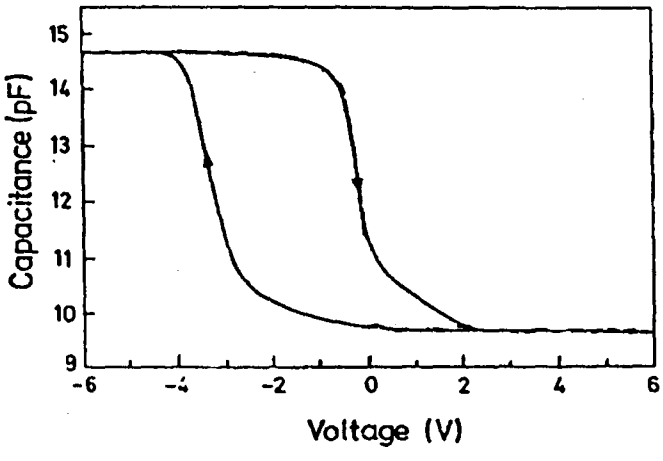

Figure 2.6: C-V characteristics of Al-xerogel-ρSi metal-insulator-semiconductor device [Manjari *et al.*, 2002].

Li *et al.*, [2005] explore pure-silica-zeolite (PSZ) MEL as a new option for low-k dielectric films. The surface roughness measured by AFM shown at Fig. 2.7. The results show surface roughness of the PSZ MEL film with is 5.6 nm [Li *et al.*, 2005].

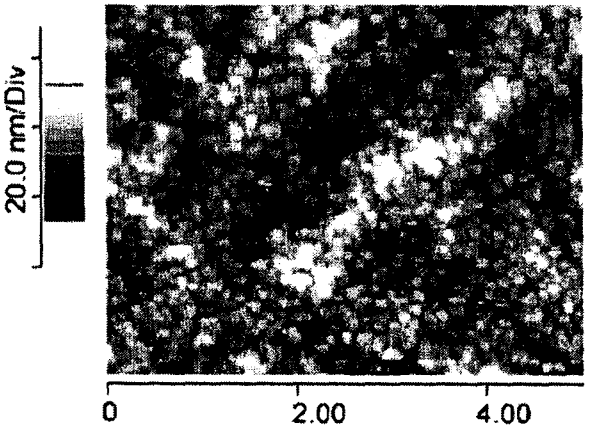

Figure 2.7: AFM images of calcined PSZ MEL spin-on films. All the measurements were carried out on a 5 μm-5 μm area [Li *et al.*, 2005].

A multiple step sol-gel process was developed to produce a mesoporous silica-based gel reported by Seraji *et al.*, [2000]. Two types of organic-inorganic hybrid sols were prepared. Sol A consisting of linear oligomers, which would form a dense matrix. Sol A was prepared by mixing common sol-gel precursor TEOS and methacryloxypropyltrimethoxysilane (MPS) in a molar ratio of 95:5 with HCl as a catalyst. Another sol consisting of highly branched clusters was made by mixing TEOS and methyltriethoxysilane (MTES) in a molar ratio of 1:1 with NH_4OH as a catalyst. It was found that the film thickness decreased as the heat treatment temperature increased. Fig. 2.8 showed SEM micrograph of a cross section of a sample with two coatings, treated at 450 °C and illustrating the thickness and uniformity of the film. SEM analyses

indicated that the films were uniform and crack-free, and the films adhered very well to the substrates [Seraji *et al.*, 2000].

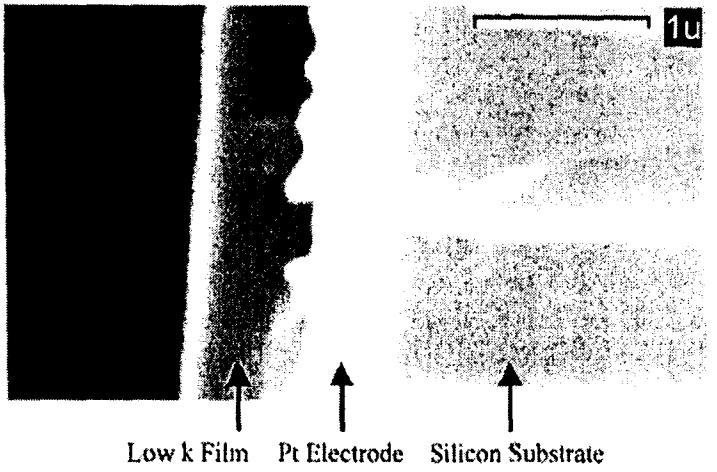

Figure 2.8: SEM micrograph of cross section of sol-gel film [Seraji *et al.*, 2000].

He et al., [2006] we firstly introduced fluorine ion into porous silica films by sol–gel method, in which hydrofluoric acid (HF) was used as catalyst instead of hydrochloric acid. The annealing results in the k value of films decreasing significantly. This is because that the associated hydroxyls in films are reduced obviously due to the annealing shown in Fig. 2.9. With increasing annealing temperature, the dielectric constant of the film decreases continuously, and reaches the lowest value of 1.65.

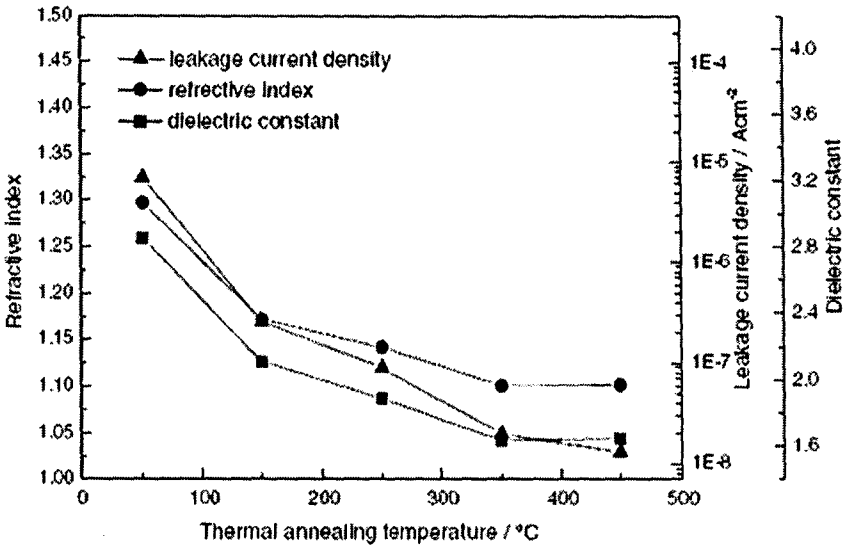

Figure 2.9: The dielectric constant, refractive index, porosity and the leakage current density of the nanoporous silica films as the function of annealing temperature [He et al., 2006].

Hong et al., [1997] reported that SiO_2 xerogel thin film with a low dielectric constant prepared by a two-step acid-base catalyst procedure and surface modification with trimethylchlorosilane (TMCS). In the first step, TEOS, ethanol, water and HCl were mixed at room temperature for 4 h (stock solution). In the second step, base-catalyst (0.5 M NH_4OH) was added to 10 ml of the stock solution. The measured dielectric constant was 2.45. This value is much lower than that of conventional SiO_2 film actually used in the fabrication of integrated circuits (IC). However, unmodified film shows a dielectric constant of 3.95, which is similar to that of conventional SiO_2 film. Table 2.4 summarizes the density, porosity, refractive index and measured dielectric constants of unmodified and modified films [Hong *et al.*, 1997].

Table 2.4: Characteristic data of SiO_2 xerogel [Hong *et al.*, 1997].

Ellipsometer	Modified film	Unmodified film
Density (g/cm^3)	1.29	1.93
Refractive index	1.26	1.39
Porosity (%)	43.2	15
Dielectric constant	2.45	3.95

2.2.5 Requirements of Low Dielectric Constant Materials

There are few general requirements for a low k material to be successfully integrated. They are [Shamiryan *et al.*, 2004]:

i) Hydrophobicity

ii) Mechanical stability

iii) Thermal stability

iv) Chemical and physical stability

v) Compatibility with other materials

vi) Reliability

2.3 Interlayer Dielectric (ILD)

2.3.1 Introduction of Interlayer Dielectric

A fully processed four layer multilevel metallization (MLM) interconnect cross

section is shown in Fig. 2.10. In Fig. 2.10 there are five layers of dielectric shown for the four layer metal structure. The first four are referred to as interlayer dielectric layers (ILDs) and serve to insulate the metal layers within the layer and from each other. The ILD separating the silicon from the first metal interconnect layer is referred to as ILD 0. The ILD separating the first layer of metal from the second is referred to as ILD 1. ILD 2 and ILD 3 then, are the dielectric layers between metal 2 and metal 3, and metal 3 and metal 4, respectively.

The final layer of dielectric is referred to as the passivating layer. The purpose of this layer is to provide physical and chemical protection to the underlying metal and device structure during the final assembly processes. Generally, this layer is composed of one or more layers of dielectric whose composition may act as mobile ion barriers or inhibit the diffusion of moisture and corrosive ions to metal surfaces [Wilson et al, 1993].

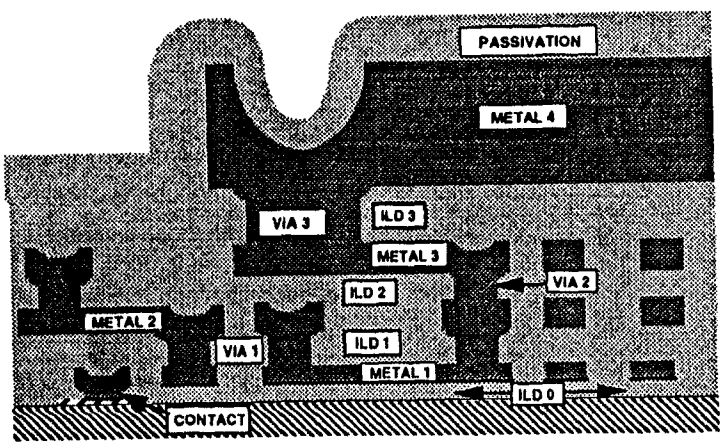

Figure 2.10: Schematic cross section of a four layer metal system [Wilson et al, 1993].

2.3.2 Deposition of Interlayer Dielectric

2.3.2.1 Sol-Gel Deposition Technique

The sol-gel process is a versatile solution process for making thin films. In general, the sol-gel process involves the transition of a system from a liquid "sol" (mostly colloidal) into a solid "gel" phase. Applying the sol-gel process, it is possible to fabricate materials in a wide variety of forms: ultra-fine or spherical shaped powders, thin film coatings, ceramic fibers, microporous inorganic membranes, monolithic ceramics and glasses, or extremely porous aerogel materials. The sol-gel process can be described by the hydrolysis and condensation reactions of the precursors [Yu *et al.*, 2004]:

Hydrolysis:

$$Si - OR + H_2O \rightarrow Si - OH + ROH \quad (2.5)$$

Water condensation:

$$Si - OH + HO - Si \rightarrow Si - O - Si + H_2O \quad (2.6)$$

Alcohol condensation:

$$Si - OR + HO - Si \rightarrow Si - O - Si + ROH \quad (2.7)$$

The alkoxide groups (OR) are replaced by hydroxyl groups (OH) in the hydrolysis reaction. The silanol groups are subsequently involved in the condensation reactions producing siloxane bonds (Si-O-Si). In practice, it is impossible that all the Si-OH bonds are transformed to Si-O-Si bonds. However, the remaining hydroxyl or

silanol groups in the final product are harmful to dielectrics because they are readily absorbing moisture from the atmosphere. The absorbed moisture may increase the dielectric constant of the silica films and cause via hole poisoning and other integration problems.

Thus, surface modification is necessary to reduce the silanol groups and keep the dielectric constant of the films low. The surface hydroxyls can be removed by thermal or chemical treatment of the samples. The sequence of surface dehydration is the initial removal of physically adsorbed water at low temperatures followed by the progressive removal of weakly hydrogen bonded hydroxyls, strongly hydrogen bonded hydroxyls and finally isolated hydroxyls [Yu *et al.*, 2004].

2.3.2.1.1 Type of Precursor

There are many different types of precursor that can be used. All should be soluble inorganic solvents and easily converted to the relevant oxide preferably by hydrolysis but alternatively by chemical reaction or oxidation decomposition. Several preparative methods are available dependant on the nature of the starting materials. There are different types precursor can be using as long as it will soluble like:

i. Salt

ii. Hydroxide

iii. Oxide

iv. Alkoxide

Probably the best starting materials for sol gel preparation are the class of materials known as alkoxides. All form alkoxides have the following general formula [Lisa, 1988]:

$$M(OR)_x \qquad (2.8)$$

where M = silicon

R = alkyl group

x = valence state of the silicon

For long-term applications, the sol-gel thin films need to have water repellent like hydrophobic property. Several co-precursors can be used for this purpose. Even though there are some reports on the tetramethoxysilane (TMOS) based hydrophobic aerogels but the TMOS is highly toxic and it is very expensive. Therefore, in the present studies TEOS precursor have been used to make hydrophobic silica thin film because TEOS is non-toxic and the cost is at least four times lower compared to the TMOS precursor [Rao & Kalesh, 2003].

2.3.2.1.2 Effect of Water: Alkoxide Ratio (R)

The ratio of water: alkoxide (R) determines the amount of co-solvent required, but this ratio also influences the reaction rate. Fig. 2.11 showed the phase diagram for

TEOS / Ethanol / Water [Brinker & Scherer, 1990].

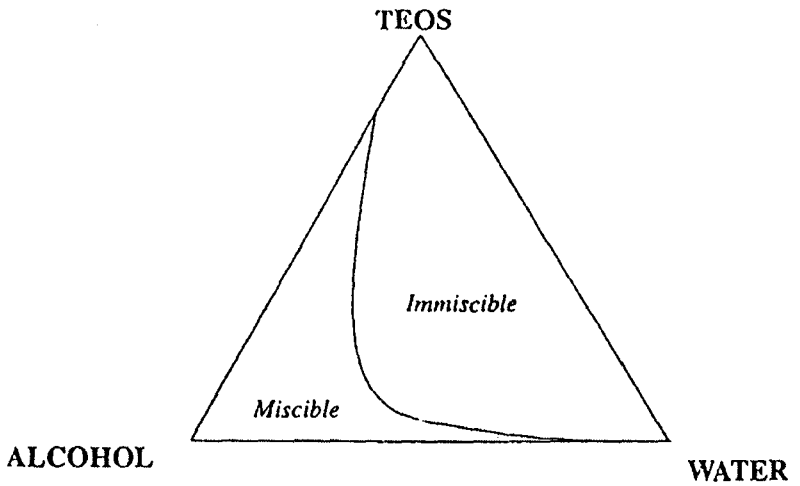

Figure 2.11: The phase diagram for TEOS / Ethanol / Water [Brinker & Scherer, 1990].

If the amount of water becomes very small, however, the hydrolysis rate slows down due to the reduced reactant concentration. Similarly, if very large amounts of water are used the other reactant (alkoxide) is effectively diluted [Brinker & Scherer, 1990].

Figure 2.12 plots the dependence of film thickness upon the volume percent of TEOS in the solution. The lines in the upper right with the open points represent films prepared with the H_2O / TEOS ratio equal to four. The TEOS content of each solution was varied here by increasing the H_2O / TEOS ratio. Thus, the dotted line extrapolation would represent the situation where the additional water simply dilutes the oxides present in the solution and the water influences the condensation of the oxide film

[Glaster & Pantano, 1984].

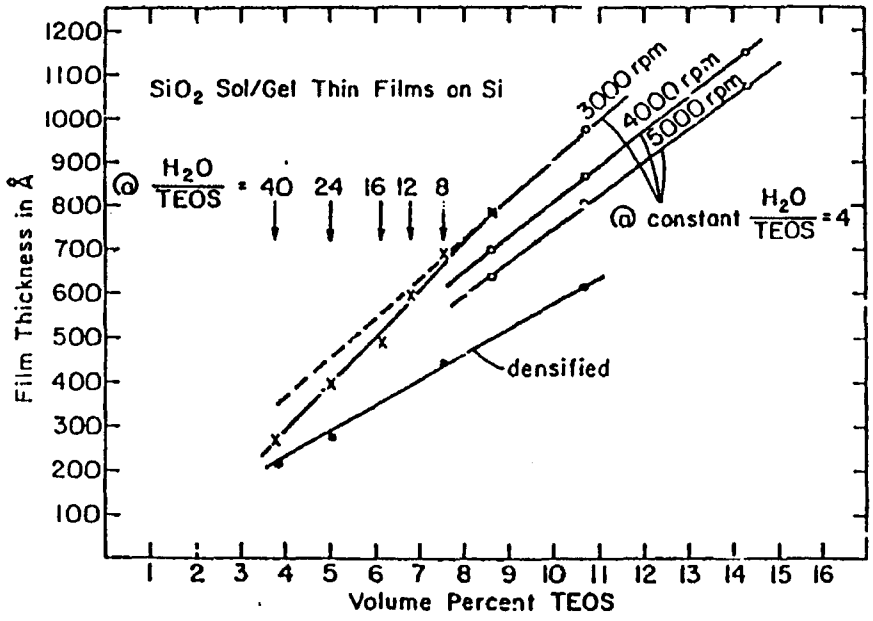

Figure 2.12: The dependence of film thickness upon the volume percentage of TEOS in ternary solutions of TEOS + H_2O + C_2H_5OH [Glaster & Pantano, 1984].

2.3.2.1.3 Sol-gel Spin On Coating

Spin coating has been used for several decades for the application of thin films. A typical process involves depositing a few drop of precursor onto the center of a substrate and then spinning the substrate at high speed (typically around 3000 rpm). Final film thickness and other properties will depend on the nature of the precursor (viscosity, drying rate, percent solids, surface tension, etc.) and the parameters chosen for the spin process. One of the most important factors in spin coating is repeatability. For sure repeat the spinning processes will thicker the layer (Klein, 1991). Fig. 2.13

shown the process flow chart fabricates thin film using spin-on coating.

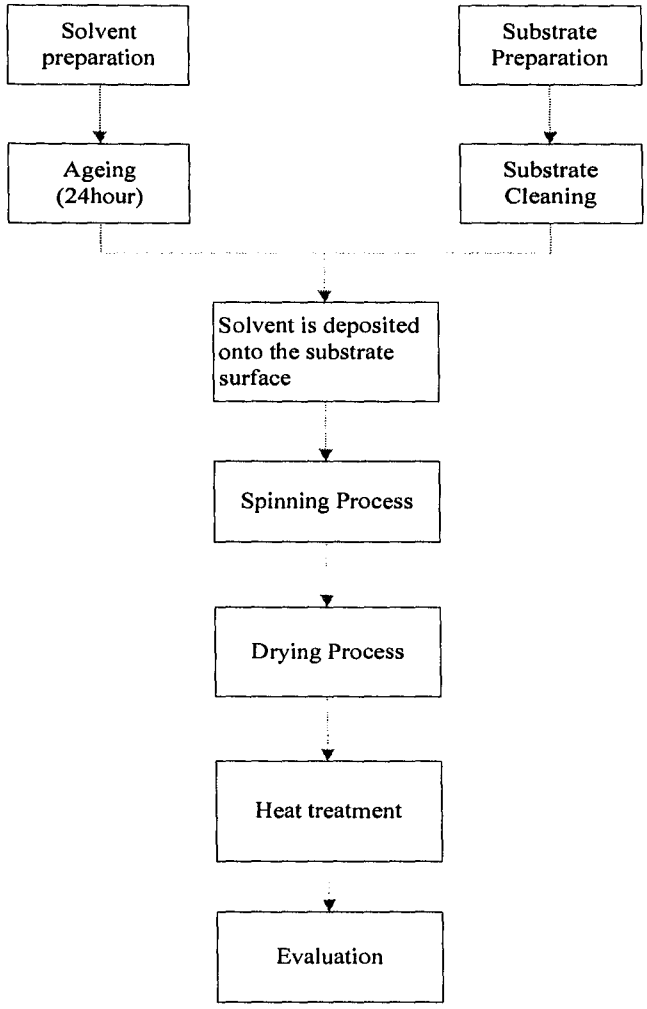

Figure 2.13: Process flow chart fabricate thin film using spin-on coating [Klein, 1991].

2.3.2.1.4 Surface Modification

In the surface modification, the Si-OH groups on the pore surface, which tend to absorb moisture, are terminated with stable methyl groups. Trimethylchlorosilicate (TMCS) has been widely used for this purpose. Hexamethyldisilazane (HMDS) has been used instead of TMCS for surface modification. Both TMCS and HMDS replace

the higher polar hydroxyl groups on the surface of the film with less polar methyl groups [Manjari *et al.*, 2002].

However, TMCS contains chloride and hydrochloride acid (HCI) generated during processing may corrode the metal lines. This is serious concern for xerogel films to be used as interlayer dielectric in very large scale integrated technology. On the other hand, HMDS does not contain any chlorine and is therefore better suited for this application [Manjari *et al.*, 2002].

The dielectric constant of the films underwent different surface modification is compared in Fig. 2.14. The dielectric constant reduced from 4.33 for no HMDS treated film to 3.07 for HMDS-treated film and further reduced to the ultralow k region of 1.89 for HMDS and air plus nitrogen dehydroxylated film. Therefore, the HMDS chemical modification and air plus nitrogen two-step annealing are very effective in dehydroxylation and lowering the dielectric constant of the silica films [Yu *et al.*, 2004].

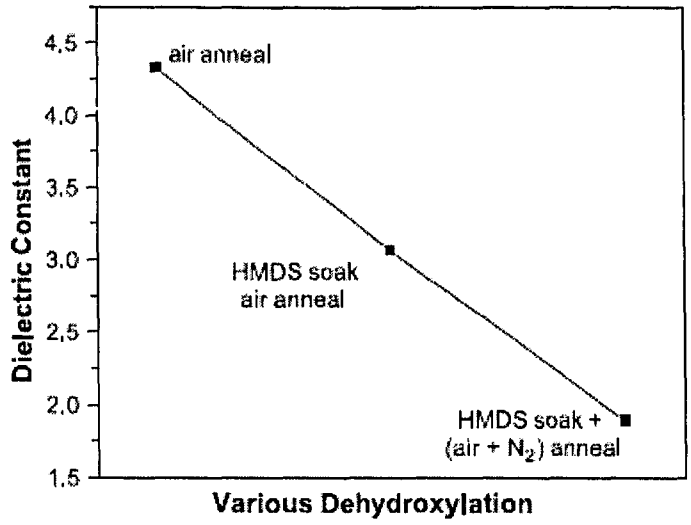

Figure 2.14: Dielectric constant of the films with different surface modifications [Yu *et al.*, 2004].

2.3.2.1.5 Annealing Process

Annealing is a heating process in which a wafer is heated to achieve a desired physical or chemical change with minimum material being added to or removed from the wafer surface [Hong, 2001]. Yu et al., [2004] report that the porosity of the films will increased with temperature. The refractive index, porosity and dielectric constant of the films annealed at different temperatures are tabulated in Table 2.5. The porosity of 300 °C film was found to be much lower and the dielectric constant of it was much higher than that of other two samples; whereas the properties of both 400 °C and 450 °C samples were more close. The changes of porosity and dielectric constant of the 400 °C and 450 °C film with respect to 300 °C film are shown in Fig. 2.15 (Yu *et al.*, 2004).

Table 2.5: Effect of thermal treated temperature on the properties of the films [Yu *et al.*, 2004].

Temperature (°C)	300	400	450
Refractive index	1.31	1.22	1.18
Porosity (%)	24.3	47.01	56.96
Dielectric constant	3.12	2.3	2.11

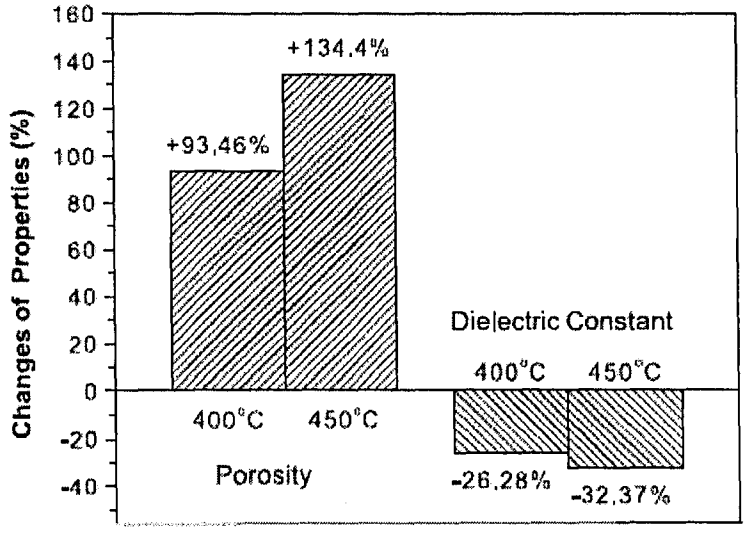

Figure 2.15: The changes of dielectric constant and porosity of the films with respect to the 300 °C film [Yu *et al.*, 2004].

The porosity increased about 93.46 % and 134.4 % and the dielectric constant decreased by 26.28 % and 32.37 % for 400 °C and 450 °C films, respectively, compared to that of 300 °C film. The higher porosity with increasing temperature results in lower dielectric constant of the films [Yu *et al.*, 2004]

2.3.2.1.6 Advantages of Sol-Gel Technique

There are several advantages of sol-gel processed oxides over thermal oxides [Weimer *et al.*, 1987]:

1) The composition and microstructure of the oxide may be precisely tailored and are independent of the composition of the substrate.
2) Sol-gel films may be deposited at room temperature on any substrate.
3) Film thickness can controlled by the deposition process
4) Multilayer films, consisting, e.g., of alternating layers of two different compositions, are easily to obtained by multiple spinning

2.4 Morphology Characterization of Film Layer

2.4.1 Film thickness

Oxide thickness will be an important parameter in process characterization and have many technique can use to measure the thickness. Perhaps the simplest method for determining the thickness of an oxide is to compare the color of the wafer with a reference color chart. Apart from that, thickness thin film also can be measure using thin film measurement system like filmetrics, elipsometrics, profilometer and etc [May & Sze, 2002].

2.4.2 Refractive Index

The definition of refractive index is:

Refractive index, n = Speed of light in a vacuum / Speed of light in the film (2.9)

For SiO_2, refractive index = 1.46. The refractive index is related to the wavelength of the light used for the measurement. A prism separates white light into a colorful light spectrum; this is because the refractive index of this prism material, quartz, is a function wavelength of the light. Light with different wavelengths has different refractive angles inward to and outward from the prism, giving the colorful spectrum of light [Hong, 2001].

The refractive index and refractive angle illustrated in Fig. 2.16 can be described by the equation of refraction:

$$n_1 \sin \theta_1 = n_2 \sin \theta_2 \quad (2.10)$$

Here n_1 is the refractive index of the first dielectric material, usually air with a dielectric index very close to 1. The incident angle is θ_1, n_2 is the refractive index of the second dielectric material, and θ_2 is the refractive angle. This equation can be used to measure the dielectric index by shining a laser beam into the dielectric material and measuring the refractive angle. However, it is impossible to measure the refractive index of a dielectric film by applying this equation when film thickness is too thin [Hong, 2001].

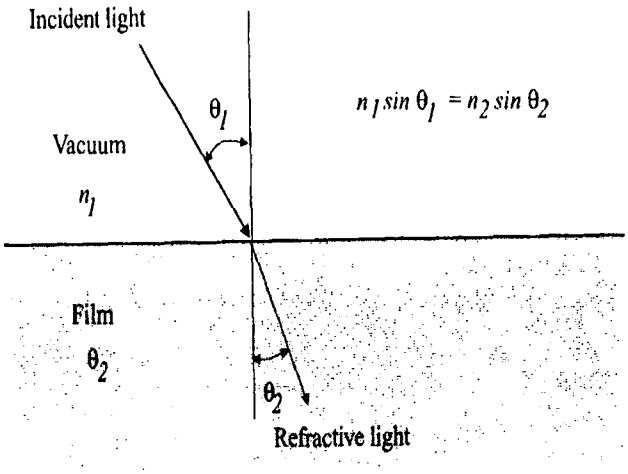

Figure 2.16: Refractive index and refractive angle [Hong, 2001].

For the silicon compound dielectric thin film, the refractive index measurement can give some useful information on the film's chemical composition and the physical conditions of the film. For the silicon- or nitrogen- rich oxide, the refractive index will be higher than the stoichiometric value of 1.46, but it will be lower than that value when it is oxygen rich [Hong, 2001].

The dependence refractive index of the silica films on annealing temperature are presented in Fig. 2.17. It is observed that the refractive index of the film annealed at 50 °C is 1.297. As the annealing temperature increases to 150 °C the refractive index decreases accordingly, which is from the evaporation of the physisorbed water. Because of the pyrolytic of organic ingredients in films, the refractive index goes on decreasing continuously and reached the lowest value of 1.101 at 350 °C [He *et al.*, 2006].

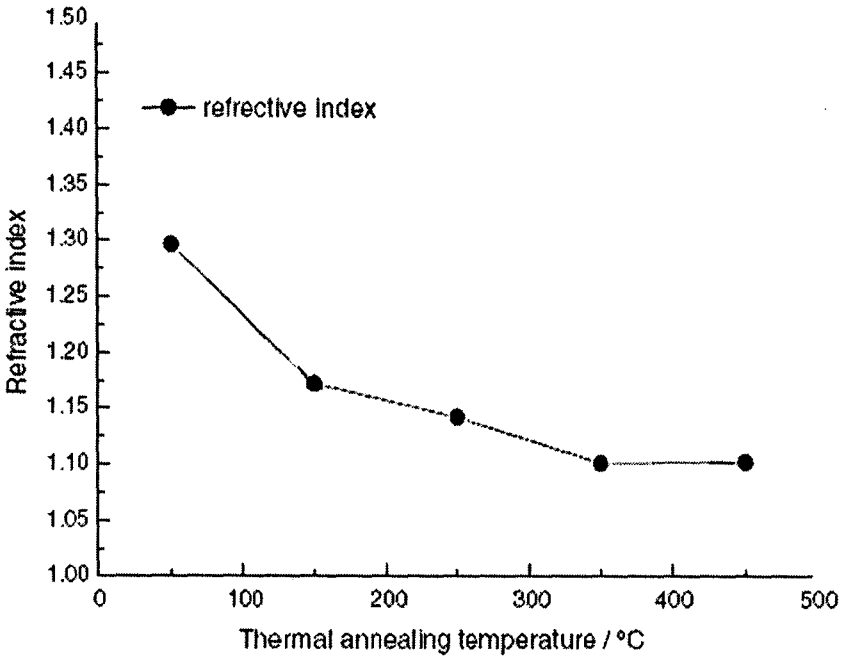

Figure 2.17: The refractive index of the nanoporous silica films as the function of annealing temperature [He *et al.*, 2006].

2.4.3 Qualitative and Quantitative Chemical Species Determination

Qualitative and quantitative chemical species determination at certain sample can be done using Fourier Transform Infrared Spectroscopy (FTIR). FTIR is most useful for identifying chemicals that are either organic or inorganic. It can be utilized to quantitative some components of an unknown mixture. It can be applied to the analysis of solids, liquids, and gasses. The term Fourier Transform Infrared Spectroscopy (FTIR) refers to a fairly recent development in the manner in which the data is collected and converted from an interference pattern to a spectrum. Today's FTIR instruments are computerized which makes them faster and more sensitive than the older dispersive instruments [Runyan & Shaffner, 1997].

The FTIR spectra of films heat-treated at different temperatures are shown in Fig. 2.18. The most intense absorption peak located at 1060 cm^{-1} is the transverse optical (TO) vibration of Si–O–Si linkage. The peak centered around 1100 cm^{-1} as a shoulder at the high frequency end of 1060 cm^{-1} peak assigns to the corresponding longitudinal optical (LO) vibration of Si–O–Si linkage. Yu et al., [2004] explained the appearance of the LO shoulder as scattering due to the porous nature of the samples. The peak located in 775 cm^{-1} is associated with symmetric stretching of Si–O–Si linkage.

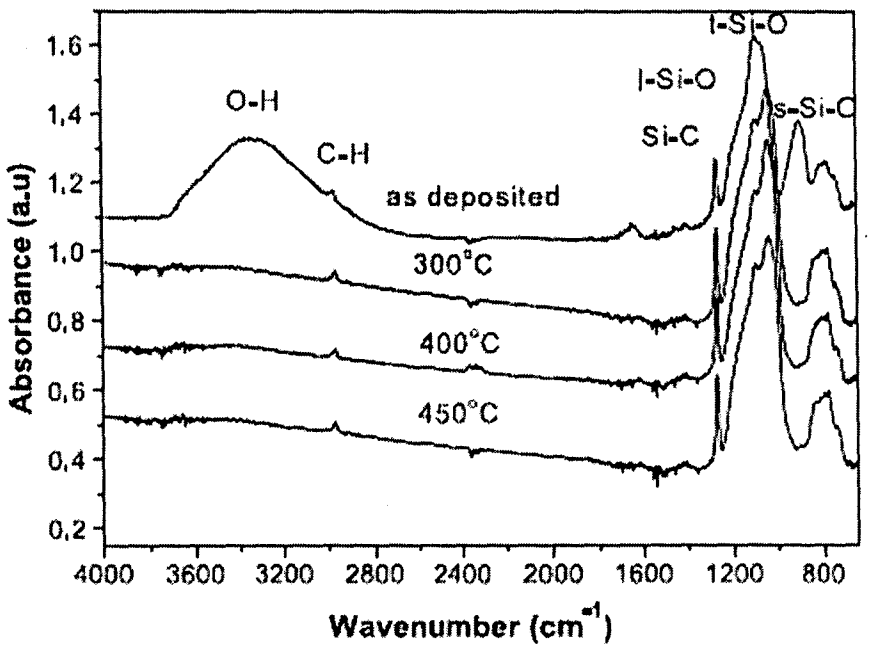

Figure 2.18: FTIR spectra of films annealed at different temperature [Yu *et al.*, 2004].

The broad peak between 3300 cm^{-1} and 3700 cm^{-1} corresponds to a stretching of –OH and physisorbed moisture on the surface in several modes. There was a very great –OH peak for the as-deposited film indicating the high content of the silanol groups.

With increasing temperature, the peak intensity around 3300 cm^{-1}– 3700 cm^{-1} decreased gradually, so more silanol groups were removed at higher temperature. Furthermore, the peak area around 1100 cm^{-1} was also increased with increasing annealing temperature, suggesting the porosity of the films increased [Yu *et al.*, 2004].

2.4.4 X-Ray Diffraction (XRD)

X-ray diffraction is a nondestructive technique for determining structural crystal defeats. It requires little sample preparation and gives structural information over entire semiconductor wafers. The XRD image is not magnified because no lenses are used. XRD give microscopic information through photographic enlargement of the topograph.

Consider a perfect crystal arranged to diffract monochromatic X-rays of wavelength λ from lattice planes spaced d. The X-rays are incident on the sample at an angle α, as shown in Fig. 2.19.

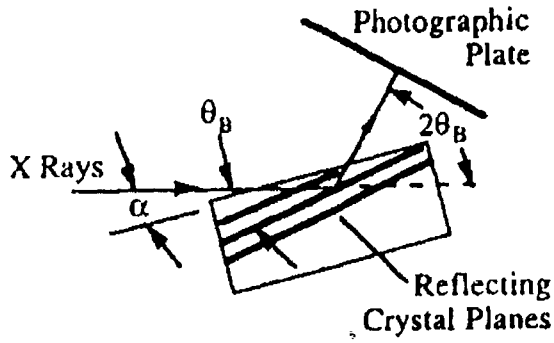

Figure 2.19: Berg-Barrett reflection topography.

The primary beam is absorbed by or transmitted through sample; only the diffracted beam is recorded on the film. The diffracted beam emerges at twice the Bragg angle θ_B defined by

$$\theta_B = \sin^{-1}(\lambda/2d) \qquad (2.11)$$

The diffracted X-ray are detected on a high-resolution, fine grained photographic plate or film held as close as possible to the sample without intercepting the incident beam.

2.4.5 Atomic Force Microscope (AFM)

Atomic force microscopy (AFM) operates by measuring the forces between a probe and the sample. These forces depend on the nature of the sample, the distance between the probe and the sample, the probe geometry, and sample surface contamination. AFM is suitable for conducting as well as insulating samples. The AFM principle is illustrated in Fig. 2.20.

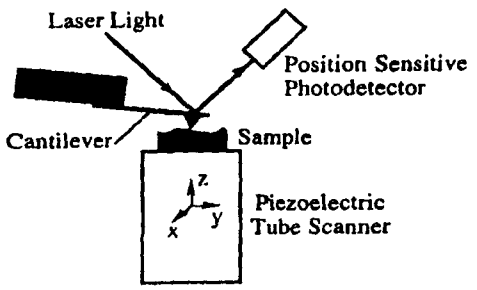

Figure 2.20: Schematic Illustration of an atomic force microscope.

2.4.6 Scanning Electron Microscope (SEM)

The scanning electron microscope (SEM) is a microscope that uses electrons rather than light to form an image. There are many advantages to using the SEM instead of a light microscope. The SEM has a large depth of field, which allows a large amount of the sample to be in focus at one time. The SEM also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. Preparation of the samples is relatively easy since most SEM only require the sample to be conductive. The combination of higher magnification, larger depth of focus, greater resolution, and ease of sample observation makes the SEM one of the most heavily used instruments in research areas today.

Figure 2.21 shown the microstructure of the silica aerogels was observed using scanning electron microscope (SEM). The silica aerogels was prepared using TEOS as precursor and MTES as co-precursor. Image of SEM indicate that the MTES modified aerogels have uniform particle and pore sizes [Rao & Kalesh, 2004].

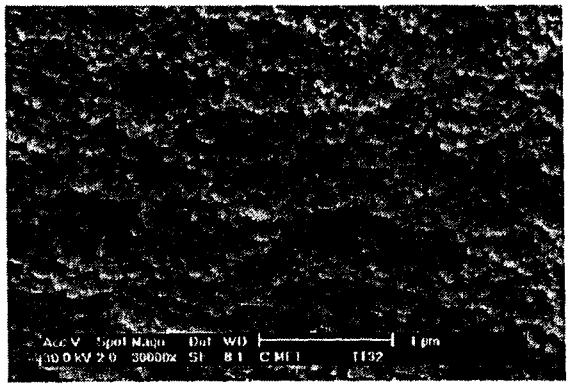

Figure 2.21: SEM microstructure of silica aerogels modified using the molar ratio of MTES / TEOS = 0.3 [Rao & Kalesh, 2004].

2.4.7 Electrical Properties

An electrical current flowing through a solid, and having units of charge per unit time per unit area (measured in the direction perpendicular to the flow direction). For electrons with number density, n_e flowing through a solid with velocity, v the resulting volume current J is given by:

$$J = -en_e v \tag{2.12}$$

where $-e$ is the charge on an electron. Experimentally, it is observed that the volume current is proportional to the applied electric field E,

$$J = \sigma E \tag{2.13}$$

where σ is conductivity

Yu et al., [2004] report that the leakage current of the silica films at 1 MV / cm was reduced with increasing temperature as shown at Fig. 2.22. The leakage current density at 1 MV / cm for the 300 °C film was as high as 8.4×10^{-3} A / cm^2, it reduced to 8.1×10^{-6} A / cm^2 for 400 °C film and 1.6×10^{-7} A / cm^2 for 450 °C film, respectively.

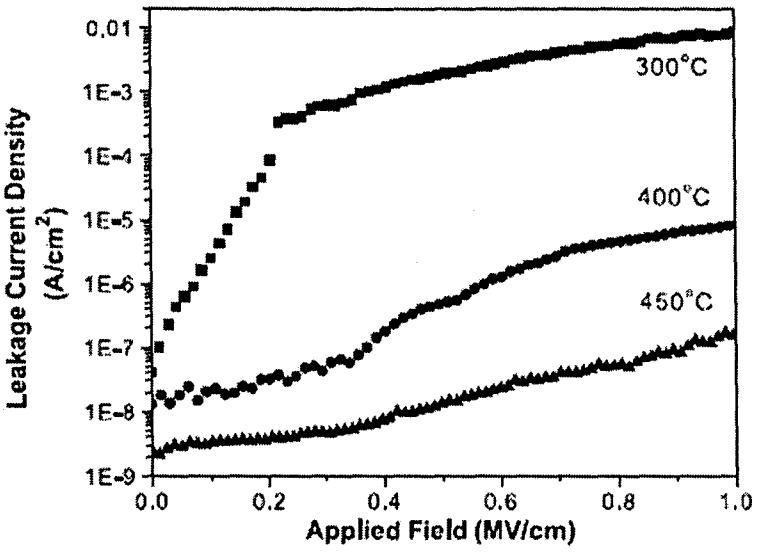

Figure 2.22: I–V property of different temperature treated films [Yu *et al.*, 2004].

CHAPTER 3: METHODOLOGY

3.1 Introduction

Fabrication SiO_2 thin film with silicon wafer as substrate was studied in this research. Silicon wafer use is n-type and (100) plane. The wafer cut to small piece using diamond cutter, the small piece is use as sample. To remove the organic and inorganic contamination from silicon wafers, procedure RCA (Radio Corporation of America) cleaning was introduced. The SiO_2 layer had been deposited at Si wafer using spin-on coating technique. The precursors used are (1) inorganic tetraethyl orthosilicate (TEOS) and (2) mixture of TEOS and organic methyltriethoxysilane (MTES). The incorporation of organic precursor makes it easier to get crack-free films with thickness 100 nm. The ratio of TEOS and MTES also has a great influence on the structural and dielectric properties of the films. Various surface modifications have been conducted to remove the silanol groups and their effects on film properties have been studied by advanced techniques.

3.2 Experimental Design

The experimental work was designed properly to fulfill the research objectives. The fabrication and characterization of the silicon dioxide sol-gel thin film was carried out in 2 phases. Phase 1 is about the sol-gel thin film fabrication and phase 2 is characterization process. There are as shown in Fig. 3.1 and Fig. 3.2.

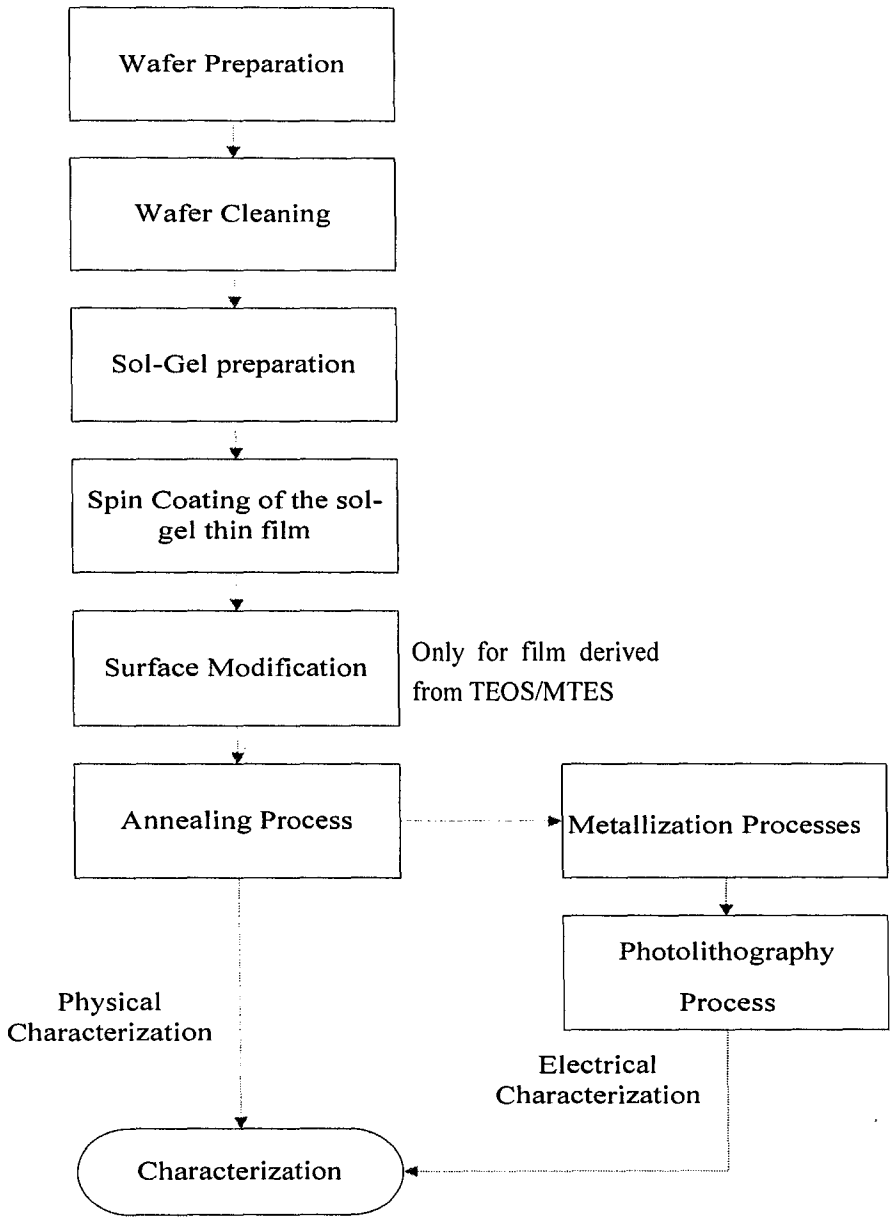

Figure 3.1: Flow chart of the fabrication process - phase 1 of the experiment.

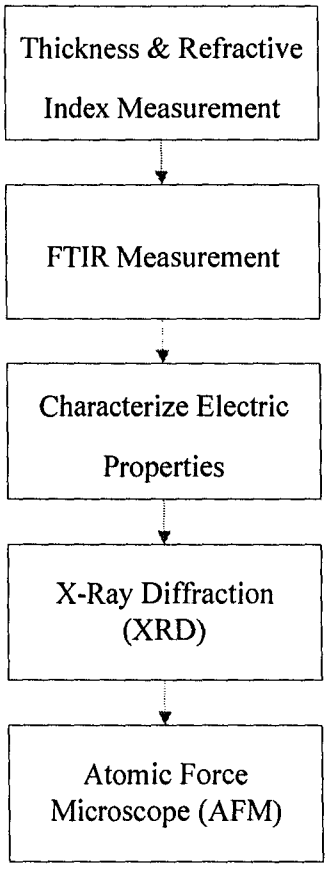

Figure 3.2: Flow chart of the characterization process - phase 2 of the experiment.

3.3 Phase 1: Fabrication Process

3.3.1 Wafer Preparation

N-type silicon wafer with diameter 2 inch and orientation (100) was used to prepare the sample. Generally wafer silicon using in this research have characteristic as below:

- Diameter : 2 Inch
- Type and dopant : N-Phosphorus
- Resistivity : 0.75-1.25 Ωcm
- Thickness : 275 ± 25 μm
- Processing method : Czochralski (CZ)
- Orientation : (100)

The wafer is cut to dimension 1 cm × 1 cm using diamond cutter. Wafer cutting step is as below:

- Place the wafer on a cutting board. Do not touch the Si wafer with your hands. Use tweezers to handle wafer.
- Place diamond cutter on the very edge of the Si wafer and press down firmly. The Si wafer should cleave easily.

3.3.2 Wafer Cleaning

Contaminants present on the surface of silicon wafers at the start of processing, or accumulated during processing, have to be removed at specific processing steps in order to obtain high performance and high reliability semiconductor devices. The RCA

clean is the industry standard for removing contaminants from wafers. Werner Kern developed the basic procedure in 1965 while working for RCA (Radio Corporation of America). Chemicals use for the RCA cleaning and their Physical and Chemical Properties are shown in Table 3.1. The standard RCA cleaning procedure has five major steps used sequentially:

1. Remove greasy impurities which may be residue from the photoresist.
2. Remove metallic contamination.
3. NH_4OH: H_2O2: H_2O = 1:1:5, 70-80°C for 10 min: Remove organic firms, desorption of trace metals.
4. Dissolve alkali ions and hydroxides of Al^{+3}, Fe^{+3}, Mg^{+2}.
5. Remove oxide and trace metals in oxide.

3.3.2.1 Chemical Reagents

1. Hydrogen Peroxide
2. Sulfuric acid
3. Ammonium Hydroxide
4. Hydrochloride Acid
5. Hydro fluoride Acid
6. Deionized water

Table 3.1: Chemicals use for the RCA cleaning and their physical and chemical properties.

Raw material	Hydrogen Peroxide	Sulfuric Acid	Ammonium Hydroxide	Hydrochloride Acid	Hydro Fluoride Acid
Chemical Formula	H_2O_2	H_2SO_4	NH_4OH	HCl	HF
Molecular Weight (g / mol)	34.01	98.08	35.05	36.46	20.01
Melting Point (°C)	-25	3	-72	-74	<-36
Boiling Point (°C)	108	280	36	85	108
Density (g / ml)	1.17	1.84	0.9	1.1-1.2	1.97
Physical Property	Clear, colorless liquid	Colorless to brown liquid	Clear, colorless solution	Colorless, fuming liquid	Colorless, fuming liquid
Chemical Property	Slight acrid odor	Odorless	Ammonia odor	Pungent odor of hydrogen chloride	Acrid odor, do not breathe fumes
Solubility	Infinitely soluble	Miscible in all proportions	Infinitely soluble	Infinite in water with slight evolution of heat	Infinitely soluble

3.3.2.2 Apparatus

1. Glass beaker 500 ml x 2
2. Fused silica beaker 250 ml x 2
3. Plastic beaker 250 ml x 2
4. Thermometer
5. Hot Plate
6. Retort & Clamp
7. Dryer
8. Volumetric cylinder 10 ml & 50 ml

3.3.2.3 Experimental procedure:

a) Remove greasy impurities

1. Fresh mixture of H_2SO_4 : H_2O_2 (4:1) is prepared by measuring the following reagents into fused silica beaker.
    a) 40 ml of H_2SO_4
    b) 10 ml of H_2O_2
2. Wafer are submerged in cold solution and the beaker is placed on hot plate and heat to 90 °C.
3. The solution is maintained at 90 °C for additional 10 min.
4. Wafers are removed from the beaker and rinsed immediately with DI water for more than 5 min.
5. The wafer is rinsed in ultrasonic bath for 3 min.

b) Remove metallic contamination

1. Wafers are submerged directly in a mixture of HF : H_2O. The solution is prepared by mixing 40 ml of DI water and 10 ml HF in a plastic beaker.
2. Wafers are allowed to remain in the solution for 1 min.
3. After that, the wafers are rinsed with DI water for 5 min or more to remove the HF solution.
4. The wafers are rinsed in ultrasonic bath for 3 min.

c) Remove organic firms, desorption of trace metals.

1. Fresh mixture of NH_4OH-H_2O_2-H_2O (0.5 :1 : 4) is prepared by measuring the following chemical reagent into a fused silica beaker.
   a) 7 ml of NH_4OH
   b) 14 ml of H_2O_2
   c) 50 ml of H_2O
2. The beaker is placed on the hot plate and heated up to 70 °C.
3. Still wet wafers are submerged in the hot solution.
4. The solution is maintained at 70 °C for 10 min.
5. The wafers are rinsed with DI water for more than 5 min.
6. The wafers are rinsed in ultrasonic bath for 3 min.

d) Dissolve alkali ions and hydroxides

1. Fresh mixture of HCl-H_2O_2-H_2O (1 : 1 : 4) is prepared by measuring the following chemical reagent into a fused silica beaker.

a) 10 ml of HCl

b) 10 ml of H_2O_2

c) 40 ml of H_2O

2. The beaker is placed on the hot plate and heated up to 70 °C.
3. Still wet wafers are submerged in the hot solution.
4. The solution is maintained at 70 °C for 10 mins.
5. The wafers are rinsed with DI water for more than 5 min.
6. The wafers are rinsed in ultrasonic bath for 3 min.

e) Remove oxide and trace metals in oxide.

1. Wafers are submerged directly in a mixture of HF : H_2O. The solution is prepared by mixing 2 ml of DI water and 98 ml HF in a plastic beaker.
2. Wafers are allowed to remain in the solution for only 10 s.
3. After that, the wafers are rinsed with DI water for only 20-30 s to remove the HF solution.
4. The wafers are rinsed in ultrasonic bath for 3 min.

3.3.3 Sol-Gel preparation

3.3.3.1 Chemical Reagent

1. Tetraethyl Orthosilane (TEOS)
2. Methyltriethoxysilane (MTES)
3. Hydrochloride Acid (HCl)

4. Ammonium Hydroxide (NH_4OH)
5. Ethanol
6. DI Water

3.3.3.2 Experimental procedure:

Experimental Procedure for TEOS derived SiO_2 film:

Tetraethyl orthosilicate (TEOS), deionized water (DI), ethanol, and HCl were used to prepare a crystal clear precursor for the sol-gel derived SiO_2 thin films. Firstly, a mixture of 12.4 mole ratio of DI:TEOS was prepared under stirring condition. An appropriate amount of ethanol was added to the mixture and then followed by a few drops of HCl to control pH of the precursor. The precursor was stirred for 90 min so that hydrolysis could be initiated. The product was then divided into four equal amounts and stored in four different beakers. The beakers were labeled as A, B, C, and D; indicating the aging time for the precursor before deposition. The aging time for A, B, C, and D were 0, 2, 4, and 6 days, respectively. After underwent an appropriate aging, the precursor was ready to be applied on a RCA-cleaned Si (100) wafer. A spinner was used to perform the spin-on-coating process with a speed and time of 4000 rpm and 45 s, respectively. After spinning, the sample was inserted in a chamber with UV wavelength of 250 nm for the post deposition treatment. The samples were exposed at the same wavelength for different durations. After the treatment the samples were sent for characterization.

Experimental Procedure for TEOS/MTES derived SiO_2 film:

1. The solution used to prepare the SiO_2 sol-gel thin film consisted of two types of sols.
2. Sol A consisted of tetraethorthosilane (TEOS), ethanol, and deionized water. Volume of solution A in 100 ml total solution shown in Table 3.2.
3. Sol B consisted of methyltriethoxysilane (MTES), ethanol, and deionized water. Volume of solution B in 100 ml total solution shown in Table 3.3.
4. A small amount of 1 M HCI acid was added to sol A and a small amount of 1 M NH_4OH was added to sol B.
5. Both sols were allowed to hydrolyze for about 24 hour before mixing them together with different ratios of sol A and sol B. Ratio of solution A and solution B are shown in Table 3.4..
6. Mix sol A and B according to the different ratios (1 : 1, 2 : 1, 4 : 1, 6 : 1).
7. The solution is ready for spin coating immediately.

Table 3.2: Volume of solution A in 100 ml total solution.

Moles Ratio H_2O / TEOS	H_2O / ml	TEOS / ml	Ethanol / ml
12	33	33.5	33.5

Table 3.3: Volume of solution B in 100 ml total solution.

Moles Ratio H_2O / MTES	H_2O / ml	MTES / ml	Ethanol / ml
12	33	33.5	33.5

Table 3.4: Ratio of solution A and solution B used to prepare sol-gel solution.

Ratio	1:1	2:1	4:1	6:1
Solution A (ml)	4	8	12	24
Solution B (ml)	4	4	4	4

3.3.4 Spin Coating of the sol-gel thin film

Spin Coating Process Description

1. Start up the spin coater and flow the Argon gas into the spin coater for few second.
2. The rotational speed and dwell time were set. Speed of rotation for the spin coater was set to 3000 rpm and dwell time was set to 15 s.
3. Switch on the vacuum and ensure that the vacuum is function. Vacuum is important in holding the substrate to avoid the substrate fly away when the spinning process.
4. The cleaned Si substrate was placed on the middle of the stage. The stage is connected to the vacuum pump hence it can hold the Si substrate.
5. The precursor was dropped on the substrate by using a dropper.
6. Start the spin coater by press the start button. The silica gel will spread uniformly on the substrate surface.
7. After the spin coater stop spinning and the "safe to remove coated part" appear on

the screen only the sample was removed from the spin coater.

8. The coated substrate need to be annealed immediately after spin coating to avoid further oxidation and contamination of the sample. If unavoidable, the coated sample need kept in the desiccators.

9. The processing step is repeated for different substrate. Flows chart of Spin Coating Process are shown in Fig. 3.3 and spin-on coating machine are shown in Fig.3.4.

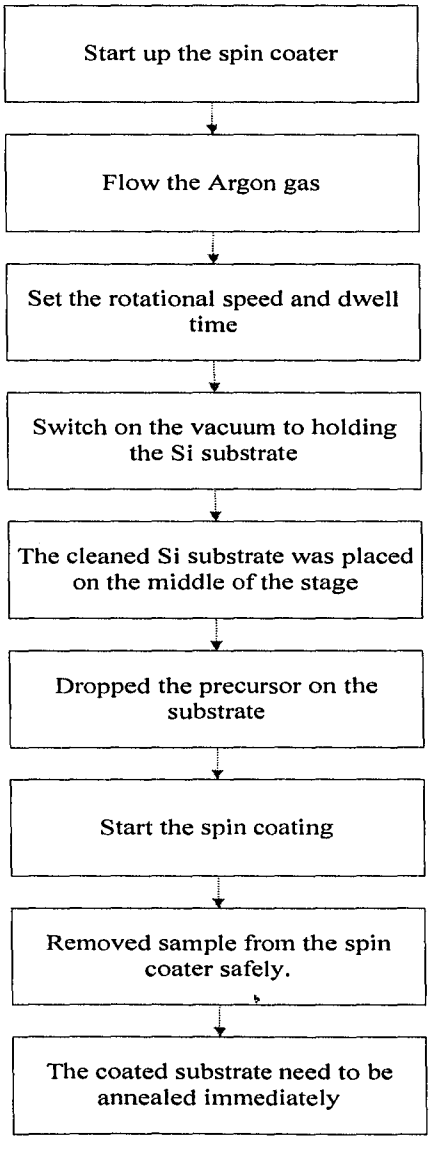

Figure 3.3: Process flow of Spin Coating Process.

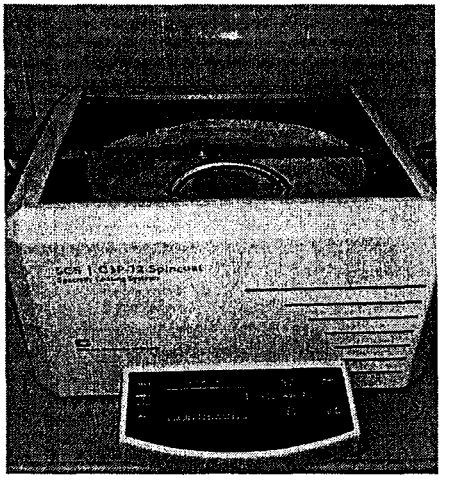

Figure 3.4: Spin Coat Machine 'SCS G3P-12 Spincoat'.

3.3.5 Surface Modification

Following spin coating, the as-deposited films were soaked into hexamethyldisilazane (HMDS) – toluene solution to conduct surface modification. The as-deposited films were soaked into the 10 % HMDS-toluene solution for 1h at room temperature. The following chemical reagent is measure into a fused silica beaker.

a) 2 ml of HMDS

b) 18 ml of toluene

The HMDS can replace –OH groups in the silica film by inert $-CH_3$ groups:

$$2Si - OH + (CH_3)_3 - Si - NH - Si - (CH_3)_3 \rightarrow 2Si - O - Si - (CH_3)_3 + NH_3 \qquad (3.1)$$

3.3.6 Annealing Process

The surface modified films should be annealed immediately to avoid the oxidation of the sample and contamination of the sample. The surface modified films were then dehydroxylation treated in argon gas using quartz tube furnace. In order to

investigate the effect of processing temperature on the properties of the films, the films were heat treated at 300 °C, 400 °C, and 500 °C for 30 min. Wait until furnace at set point temperature. Put the sample fixed on the quartz boat and slide boat slowly and gently into furnace using quartz rod. Make sure the boat is at middle of the quartz tube for uniform heating. The samples need to hold at that temperature for 30 min. After elapsed time, slide sample to edge of tube with quartz rod. Let sample cool for 10 min. When sample is cool, remove samples from furnace. Turn off heater. It is important that a small amount of gas flow while furnace is cooling, this is because as the furnace cools, air inside contracts drawing in air with dust. Over a short time this dust will contaminate the tube. Fig. 3.5 had shown the temperature profile for annealing.

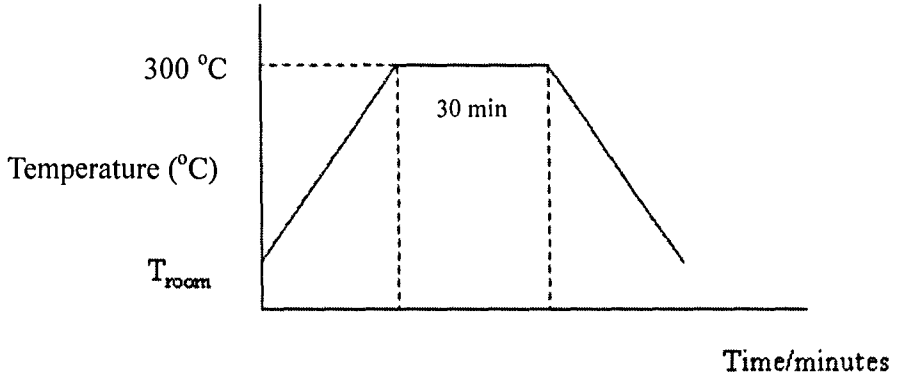

Figure 3.5: Temperature profile for annealing of the sample.

3.3.7 Metallization Process

In the metallization process, a layer of metal is deposited on the wafer surface to provide electrical contact to the devices. Metal can be deposited using several different methods- sputtering, evaporation or plating. Metallization process in this project is used

thermal evaporator system, metal using will be aluminums. The following steps make up the metallization process:

First remove the outside cover from the evaporator. Then remove the wafer holder. This is where the wafers will be during the evaporation process. The metal will be placed in a tungsten boat (tungsten has a relatively high melting point). Carefully load the wafers into the wafer holder. Place the cover back onto the evaporator. Installed tungsten boat between the two electrodes. When the chamber has been pumped down sufficiently, current is applied through the boat or filament to heat the aluminum inside to melt, the molecule which will travel in a line-of-sight path to the sample. Allow wafers to cool down for 15 min, and then remove the wafer holder. Use tweezers to remover the wafers. Structure semiconductors after metallization are shown in Fig. 3.6.

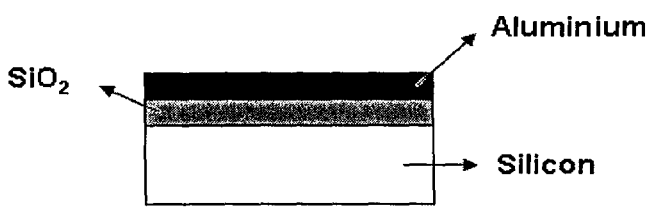

Figure 3.6: Schematic Illustration layer structure semiconductor after metallization.

This processes need to be done at high vacuum environment to secure from dirty particle or air particle that will effected the aluminum depositions at surface wafer. Always make sure the sample is clean to ensure there are no dirty particles in interlayer

structure capacitor. Dirty particle will affect the properties electricity capacitor.

3.3.8 Photolithography Process

Photolithography is a process analogous to developing film in a darkroom. The purpose of photolithography is to transfer images from a mask to the surface of photo resist layer on a wafer. Photo resist is a film used in photolithography that temporarily holds the pattern of a circuit path or microscopic element of a chip. The process flows for photolithography are shown at Fig. 3.7.

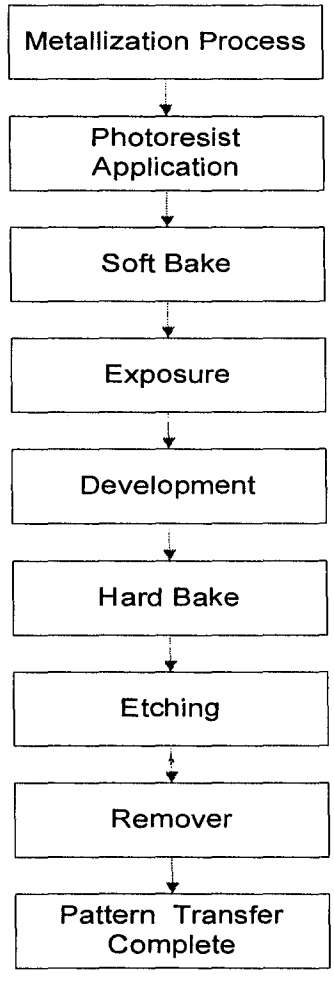

Figure 3.7: Process flow of Photolithography Process.

Using tweezers, place the wafer on the wafer chuck in the center of the photo resist spinner. After making sure the wafer is centered on the wafer chuck, press the button to lock on the vacuum line. The vacuum will secure the wafer to the chuck. Using an eye dropper, flood the wafer surface with primer. Wait ten seconds, letting the primer dwell on the wafer surface so that it will allow good adhesion between the photoresist and the wafer surface. Then, start spinning the wafer at 2700 rpm for 10 s. In a manner similar to applying the primer, an eye dropper is also used to place photoresist on the wafer. Apply the resist so that the whole wafer surface is covered. Spin the wafer at 2700 rpm for 10 s. Then, release the vacuum, and use tweezers to carefully remove the wafer. Pre-heat the Soft-Bake Oven to the temperature between 80-100 ^{o}C. Place the tin plate containing the wafer into the Soft-Bake Oven for 10 min. The purpose of the soft bake is to semi-harden the photoresist. The wafer is aligned with respect to the mask in an optical lithographic system, and the resist is exposed to UV light for 30-35 s. Exposure can affect the way that the resist image is finally produced and it is important that the exposure is kept within certain limits. Mask pattern and window area are shown in Fig. 3.8.

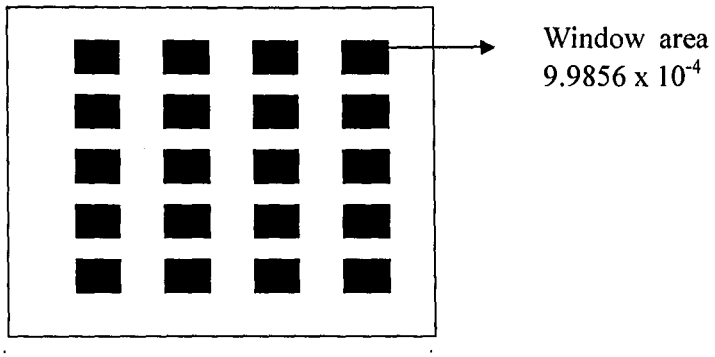

Figure 3.8: Schematic Illustration mask pattern.

The exposed areas are subsequently removed in the development process; the resist image will be identical to the opaque image on the mask. This is identifying as positive resist as shown in Fig. 3.9.

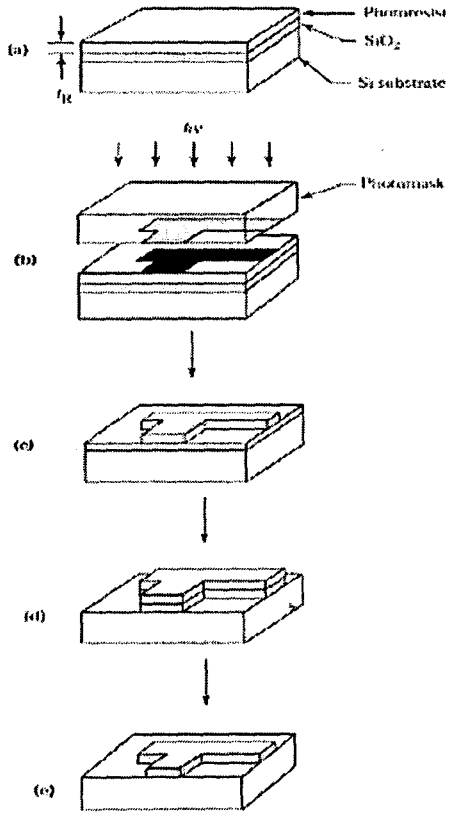

Figure 3.9: Details of the Photolithography pattern transfer process.

After the resist exposed to UV light, the exposed resist is dissolved in the developer. Make sure the development time is suitable and the wafer is then rinsed and dried. After development, inspect the wafers under a microscope, to see if the patterns are clear and well defined. If everything looks okay, the wafer is placed into the Hard Bake oven which should be preheated to between 120-130 °C to increase the adhesion of the resist to the substrate. After that, the sample is etch using aluminum etchant to remove the aluminum at area exposed to UV. Aluminum etchant concentrations are shown in Table 3.5.

Table 3.5: Aluminum etchant concentrations.

Chemicals	Percentage (%)
H_3PO_4	73
HNO_3	4
CH_3COOH	3.5
DI water	19.5

The remaining photoresist is remove using remover. The final sample is showed like figure 3.10.

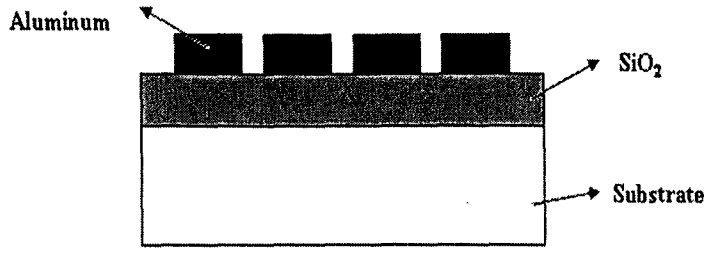

Figure 3.10: Schematic Illustration the final sample after photolithography process.

After that the sample is doing metallization at the sample back side to produce back contact. Back contacts have been produce using sputtering machine. Before metallization back contact, the sample back side need to be clean to avoid any oxide layer using mix solution 1 ml HF and 20 ml DI water. After that the sample clean with DI water to remove the acid solution.

3.4 Phase 2: Characterization

3.4.1 Thickness & Refractive Index Measurement

Perhaps the simplest method for determining the thickness of an oxide is to compare the color of the wafer with a reference color chart. When an oxide-coated wafer is illuminated with white light perpendicular to the surface, the light penetrates the oxide and is reflected by the underlying silicon wafer. Constructive interference leads to enhancement of a certain wavelength of reflected light, and the color of the wafer corresponds to the wavelength. Clearly, color chart comparisons are subjective

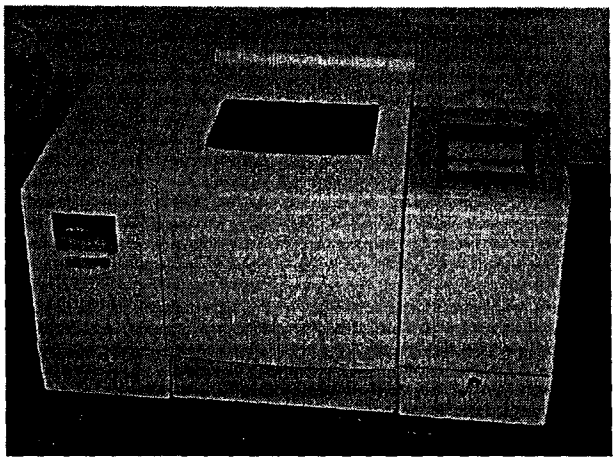

Figure 3.12: Schematic Illustration Fourier Transform Infrared Spectroscopy (FTIR) machine.

3.4.3 XRD Analysis

The purpose of this analysis is to identify the phase of material. Crystallographic and phase analysis were performed on x-ray diffraction by using monochromatic CuKα radiation. The detection angle was from 5 to 100 degree and the graph of counts as angle 2θ was recorded. Identification of crystallite phase was carried out by comparison of XRD patterns with JCPDS standards. In addition to monitoring the evolution of the microstructure and chemistry, XRD data was carried out to measure the crystallite size.

3.4.4 AFM Analysis

The sample topography is measured by scanning the tip, which contacts the surface, across the sample. The tip is brought into continuous contact with the sample and scanned across the sample surface. When the probe touches the surface, it is pulled toward the sample by capillary action. By scanning in either way, the local height of the

sample is measured. Three dimensional topographical maps of the surface are then constructed by plotting the local sample height versus horizontal probe tip position.

Conductive – AFM (C-AFM) used to analyze I-V curve. Before analysis the sample back side needs to clean with HF solution to remove oxide layer during annealing process. After that, sample need to deposited metal layer at back side to allow current flow. Machine used for AFM analysis are shown in Fig. 3.13.

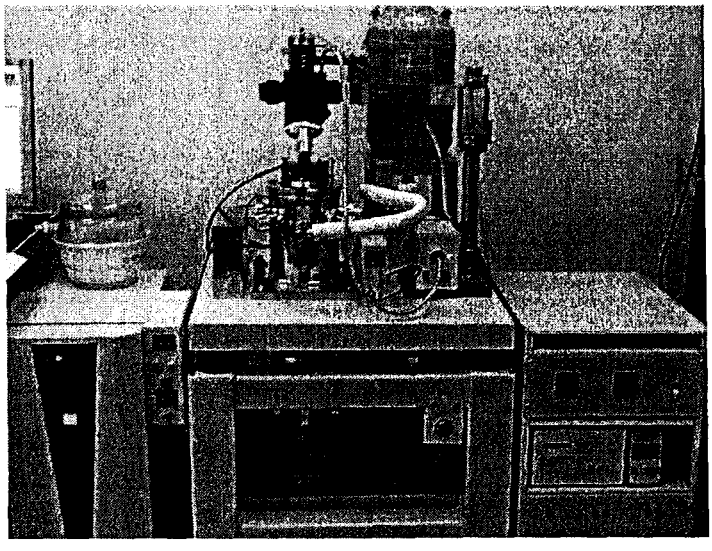

Figure 3.13: Schematic Atomic Force Microscope (AFM).

3.4.5 Characterize Electric Properties

Current-voltage measurement was done on the sample which is after photolithography process. Characterization electric current-voltage is important because the chart is to determine basic parameters of a device and to model its behavior in an electrical circuit.

Measurement capacitance-voltage was done using machine measurement model 'KEITHLEY 238 High Current Source Measurement Unit' and software using to analysis result obtain is Metrics ICS Software. Wafer is place on a plat with 2 terminal, input and output connect to the wafer and the plat. Output terminal connect at top surface sample and input terminal connect at opposite side.

CHAPTER 4: RESULT AND DISCUSSION

This chapter discussed the results obtained from oxide thickness and refractive index, Fourier transform infrared spectroscopy (FTIR), X-ray diffraction (XRD), atomic force microscopy (AFM), scanning electron microscopy (SEM), energy dispersive x-ray analysis (EDX), and current-voltage (I-V) measurements. Firstly, the results and discussion on TEOS-derived SiO_2 films will be presented and then follow by TEOS/MTES-derived SiO_2 films.

4.1 TEOS-derived SiO_2 film

Sample D that has been aged for 6 days has fully transformed into gel form. Therefore it could not be used in the subsequent process. Figure 4.1 shows the result of oxide thickness as a function of UV exposure time for the three types of samples (A, B, and C). As UV exposure time increases, the oxide thickness decreases but the changes is small. This indicates that densification of the gel to solid state occurs as UV exposure time increases. In contrast, oxide thickness significantly increases as the aging time of the precursor increases from 0 to 4 days. This is probably due to the increase of polymerization of the precursor as the aging time increases and attribute to a more viscous precursor.

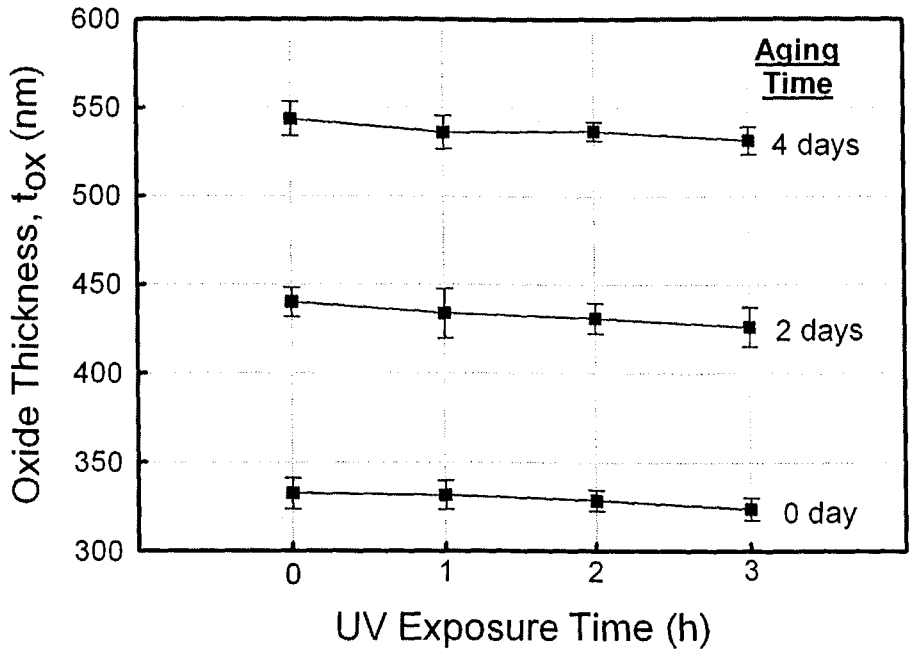

Figure 4.1. Oxide thickness as a function of UV exposure time for samples prepared from precursor aged at different period.

Figure 4.2 presents the refractive index (n) of the thin film as a function of UV exposure time. All of the samples revealed n value lower than the conventional thermal and chemical vapor deposited SiO_2 films (n = 1.46). This indicates that the sol-gel derived SiO_2 film in this work probably has a larger porosity or larger chemical structures. This may imply that the dielectric constant (k) of the thin film is also relatively smaller than the SiO_2 film prepared by conventional methods. As UV exposure time increases, n value also demonstrated an increasing trend. Contrary, the n value decreases dramatically as the aging time of the precursor increases. Since the

polymerization may initiate after a period of aging, the chemical structures could become larger than non-aged precursor. This suggests that the reduction of n value is most probably attributed to the change of chemical structures that may induce pores in the film.

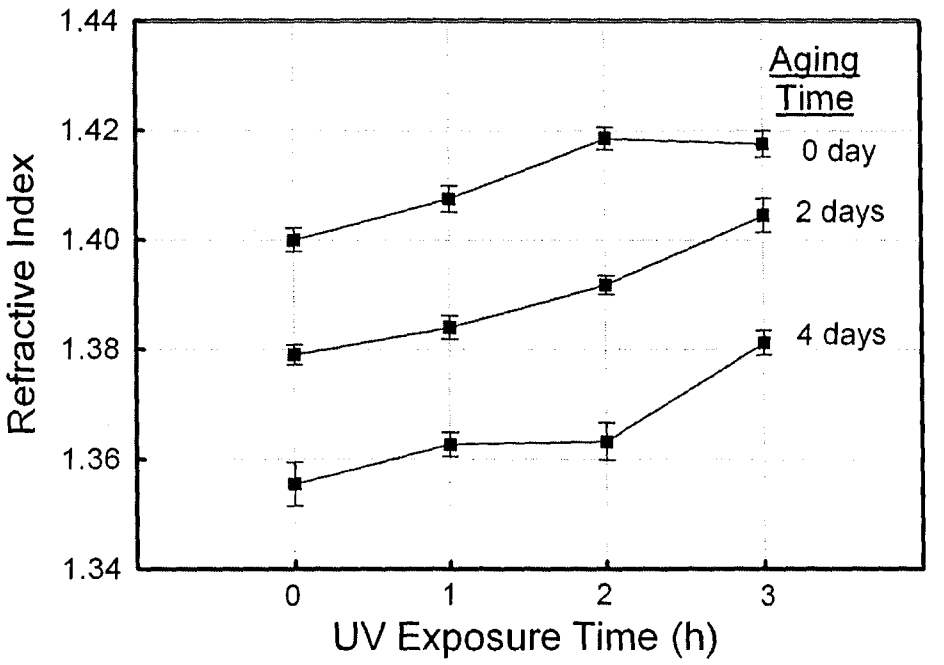

Figure 4.2. Refractive index as a function of UV exposure time for samples prepared from precursor aged at different period.

The dynamic dielectric constant (k_e) of these films has been investigated at UV-visible range using a Filmetrics system at wavelength of 632.8 nm. The squared of the n value obtained from this wavelength provides the k_e value (Fig. 4.3) as shown in Equation (1). The trend of k_e as a function of UV exposure time and precursor aging

time are similar to Fig. 4.2.

$$k_e = n^2 \qquad (4.1)$$

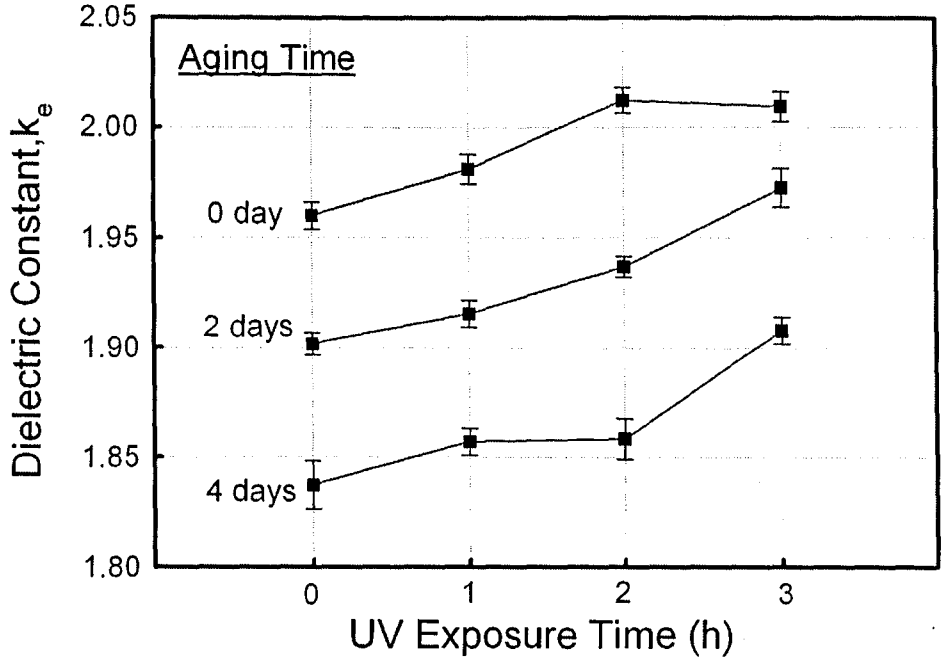

Figure 4.3. Dynamic dielectric constant as a function of UV exposure time for samples prepared from precursor aged at different period.

Figure 4.4 reveals the FTIR spectra for the SiO_2 thin film prepared from precursor aged for 4 days and treated under UV light at different durations. These spectra are also compared with a spectrum obtained from a conventional thermal SiO_2 thin film. From the spectra, individual peaks with wave numbers have been included. Peaks

representing SiO_2 structures and the mode of the structures have also been included for comparison. Besides having stretching mode of Si-O-Si, rocking (454 cm^{-1}) and bending (739 cm^{-1}) modes of Si-O-Si were also observed in the sol-gel derived SiO_2 films. A shoulder at 1200 cm^{-1} is also being observed in all the spectra of the investigated films. This shoulder indicates an increase of stretch in Si-O-Si of this films if compared with the conventional SiO_2 film (Lau, 1999). Some reports also suggested that the appearance of this shoulder may attribute to the decrease of refractive index (n) (Lau, 1999). This conclusion is in agreement with the observation obtained in this work. In general, the shape of the FTIR spectra of the remaining two samples (aged at 0 and 2 days) are almost similar to Fig. 4.4.

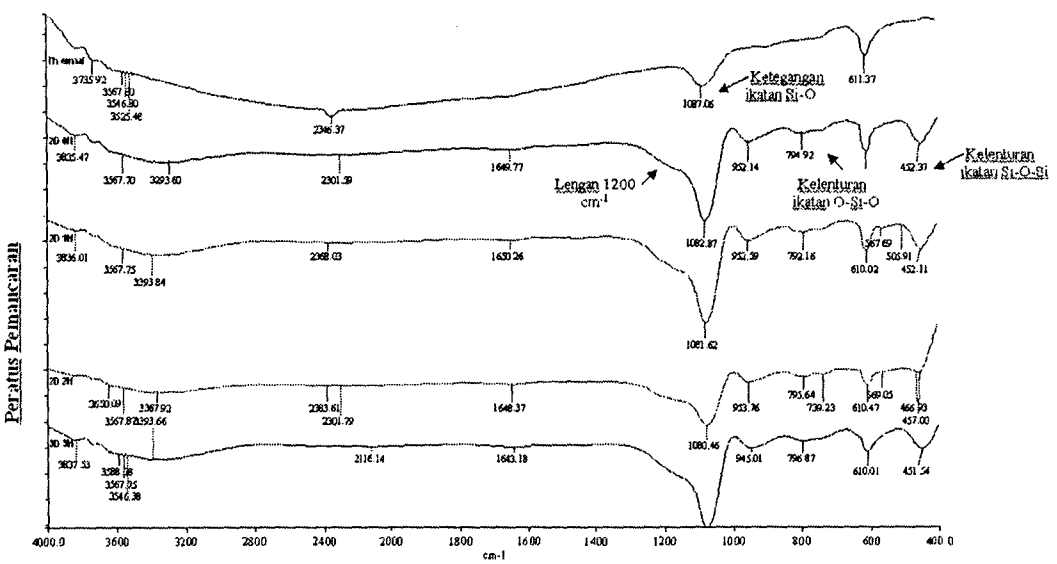

Figure 4.4. A comparison of FTIR spectra for samples prepared from precursor aged for 4 days treated at different UV exposure time and thermal SiO_2 sample.

Figure 4.5(a) and (b) compares the SEM micrographs of the sol-gel derived SiO_2 films prepared from precursor aged for 4 days. The non-UV treated film [Fig. 5(a)] shows a random micro-crack on the film surface. After the UV treatment, the cracks have been reduced significantly. The actual reason for this reduction has yet been investigated. The most probable explanation of this observation may due to the breaking of huge chemical structures derived from the long aging time of the precursor. After this breaking process, UV may also be introduced to enhance the drying process of the film.

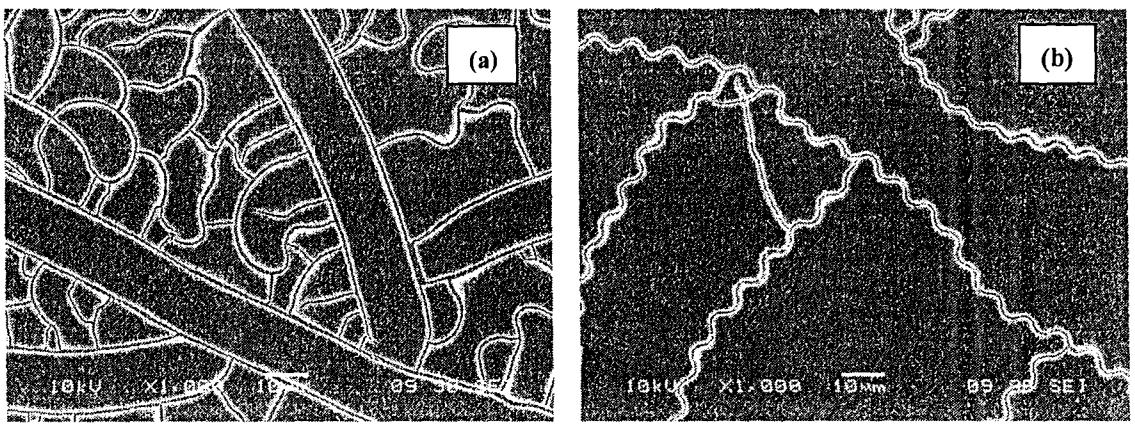

Figure 4.5. SEM micrographs of samples prepared from precursor aged for 4 days and treated at (a) 0 and (b) 3 h of UV light.

4.2 TEOS-derived SiO_2 film

Oxide Thickness and Refractive Index Measurements

Thickness of oxide layer was measured using a Filmetrics system. This system is also able to measure refractive index (n_e) of the oxide at a measured wavelength of 632.8 nm. The oxide thickness and refractive index measurements have been performed

for samples with TEOS/MTES ratio of 1:1, 2:1, 4:1 and 6:1 and heat treated at 300 °C, 400 °C, and 500 °C (Fig. 4.6). The oxide thicknesses of all the samples were in the range of 110 to 160 nm. Apart from using Filmetrics, a color chart has been using to verify the oxide thickness. The color chart was prepared based on thermally grown SiO_2 on Si. It was found that the SiO_2 thickness of 110 nm – 160 nm was appeared as dark violet to red violet and royal blue, light blue to metallic blue and metallic to very light yellow green. The results obtained from the color chart are in agreement with the one measured from Filmetrics.

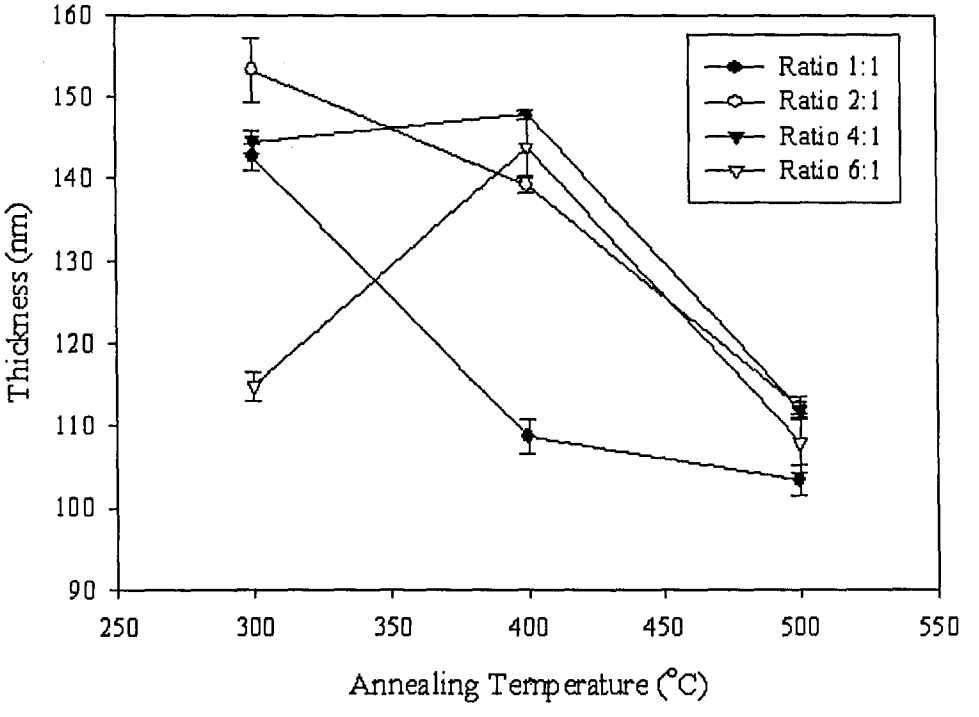

Figure 4.6: Oxide thickness measured result for sample with different TEOS/MTES ratios and annealing temperatures.

From the result of refractive index measurement (Fig. 4.7), it can be seen that the index value is decreased with an increase of annealing temperature. This is in agreement with the work reported by Warran et al., (1991). At annealing temperature of 300 °C, the refractive index of the sample with a ratio of 1:1 was 1.5994. The refractive index was then reduced to 1.1474 when the annealing temperature was increased to 500 °C.

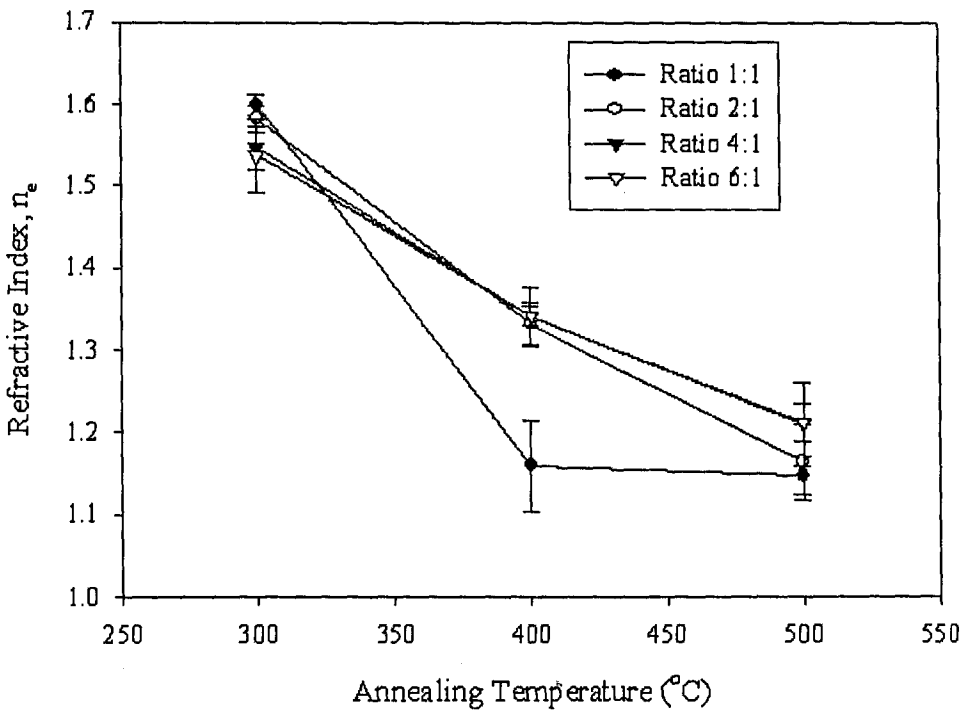

Figure 4.7: Refractive index of samples prepared by different TEOS/MTES ratios and heat treated at different temperatures.

According to Hong, (1997), refractive index of a film is strongly influenced by the density and porosity of the film and subsequently the dielectric constant of the film. From the refractive index measurement, value of density, porosity, and dielectric constant of the investigated films have been calculated. The film density has been calculated using Eq. (4.2) [Hong, 1997]:

$$\rho = \frac{n_e - 1}{0.202} \tag{4.2}$$

where ρ and η_e are the density and refractive index of the film.

The porosity of a film can be calculated by Eq. (4.3) [Hong, 1997]:

$$\text{Porosity} = 1 - \frac{\rho}{\rho_s} \tag{4.3}$$

where ρ_s is the reference density of a thermally grown conventional SiO_2 film with a value of 2.27 g / cm^3. The dielectric constant, k, of film is then transformed using Eq. (4.4) [Hong, 1997]:

$$k = 1 + 6.33\ (n_e - 1) \tag{4.4}$$

In the following sub-section, the calculation procedure of obtaining the density value has been provided.

Example of calculation:

The η_e of sample annealed at 500 °C with TEOS/MTES ratio of 1:1 is 1.1474

From Eq. (4.2), $\rho = \frac{n_e - 1}{0.202}$

$$= \frac{1.1474 - 1}{0.202}$$

$$= 0.7297 \text{ g / cm}^3$$

From Eq. (4.3), Porosity $= 1 - \frac{\rho}{\rho_s}$

$$= 1 - \frac{0.7297}{2.27}$$

$$= 0.678$$

From Eq. (4.4), $k = 1 + 6.33 (n_e - 1)$

$$= 1 + 6.33 (1.1474 - 1)$$

$$= 1.933$$

Figure 4.8 presents the result of porosity as a function of annealing temperature and TEOS/MTES ratio. In general, there is an increase of percentage of porosity in the film, for all of the TEOS/MTES ratios, as the annealing temperature is increased. Yu et al., (2004) has reported that the porosity of a film is increased with an increase of annealing temperature. At 300 °C, the porosity of the sample with a ratio of 1:1 was approximately 30.7 %. While the percentage of porosity of the film has been increased to 67.8 % after the film has been annealed at 500 °C. The increment of porosity was approximately 37.1 %. The presence of high percentage of porosity does not weaken the mechanical structure of SiO_2. This aspect will be indirectly proven in the electrical

measurement that will be provided in the subsequent paragraphs.

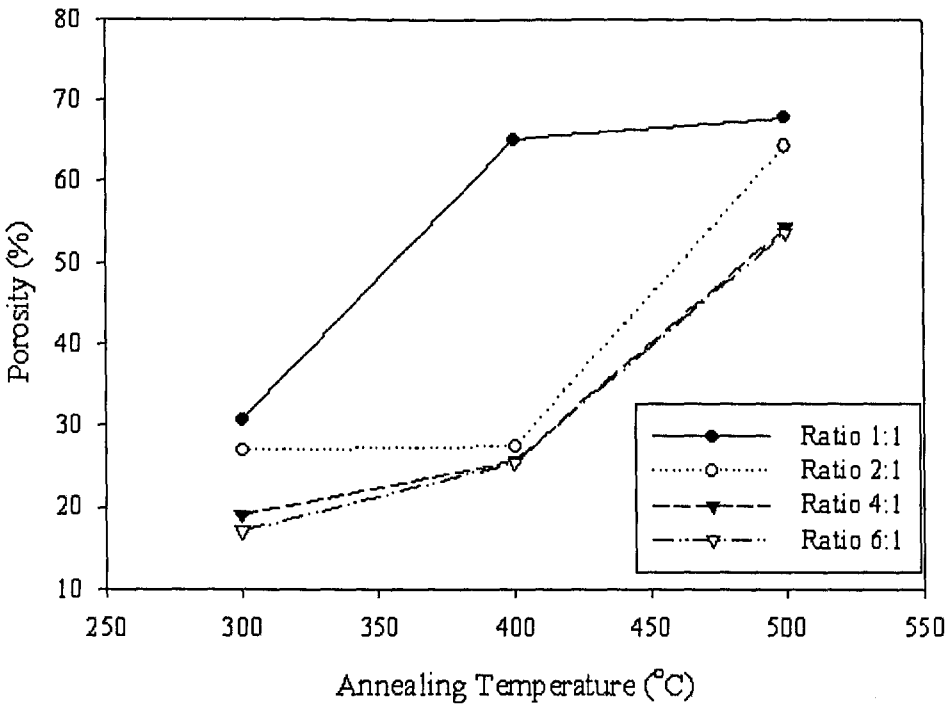

Figure 4.8: The calculated percentage of porosity for SiO_2 films prepared by different TEOS/MTES ratios and annealing temperatures.

According to the results demonstrated in Fig. 4.8, by varying the TEOS/MTES ratio, the percentages of porosity available in the films is also varies significantly. It can be observed that the porosity of the films increased with an increase of MTES concentration (or the reduction of TEOS concentration). The main reason for this phenomenon may be attributed to the different mechanism of hydrolysis as the ratio changes [Yu et al., 2004]. According to the work done by Brinker et al., (1990), acid catalysis produces long chain and less branched polymers in hydrolysis stage. During

condensation stage, due to the low reaction rate, the film has sufficient time to cross-link and form a dense gel. Therefore, pore volume and pore size in the formed film is low. On the other hand, in a base catalysis process, it may produce highly branched polymers during hydrolysis stage. Hence, in the condensation rate is fast, and the growth tends to form spherically expanding clusters (particles). Therefore, the formed film has higher porosity compared with a film produced using an acid catalyze. In this work, the TEOS was catalyzed by an acid catalyze while the MTES was catalyzed by base substance; thus, a composite structure with highly porous clusters embedded into a dense matrix was formed. The MTES that was catalyzed by base can be regarded as a pore generator in the broadest sense. Hence, as the molar fraction of MTES increases, the amount of porous cluster is also increases and resulting in an increase in porosity.

The calculated dielectric constant, k, as a function of annealing temperature and TEOS/MTES ration is presented in Fig. 4.9. In general, the k value reduces as the annealing temperature increases. The dielectric constant of sample prepared by TEOS/MTES ratio of 1:1 and heat treated at 300 °C was 4.79. A significant reduction of the k value (1.93) is observed as the annealing temperature is increased to 500 °C. As the annealing temperature increases, the percentage of porosity in the film is also increased. There would be a large amount of air trapped (k_{air} = 1.0) inside the pore. This may attribute to the lowering of k value.

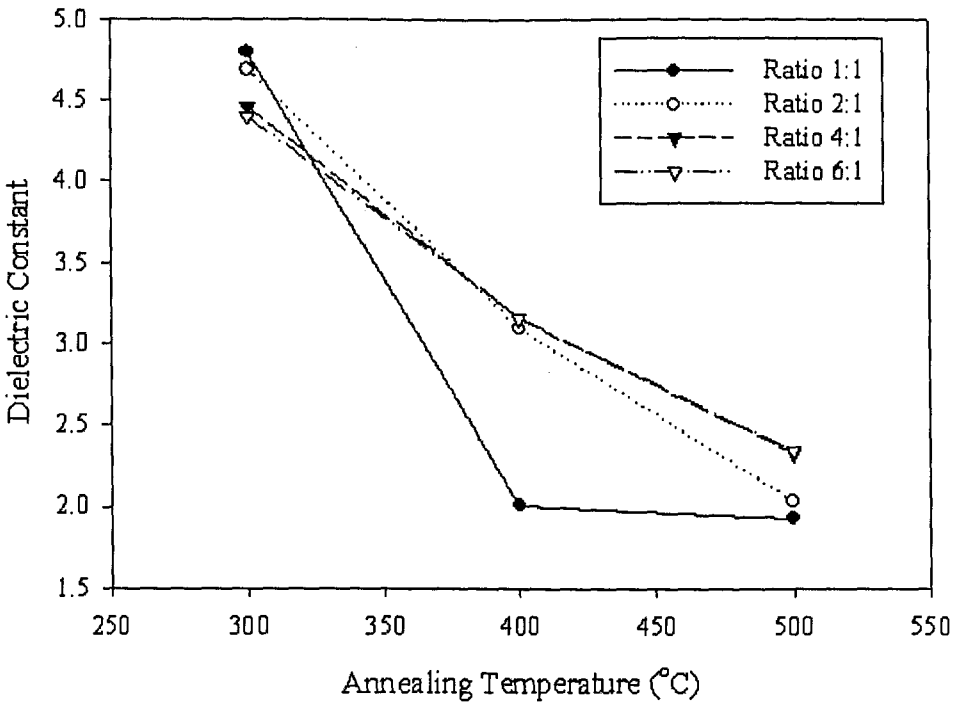

Figure 4.9: The calculated dielectric constant as a function of annealing temperature and TEOS/MTES ratio.

4.3 Characterization of Fourier Transform Infrared Spectroscopy (FTIR)

Sample with TEOS/MTES ratio of 4:1and heat treated at 300 °C, 400 °C, and 500 °C were independently investigated using a FTIR system (Fig. 4.10). FTIR is used to determine qualitative and quantitative chemical species and bonding of a film. From the spectra obtained in Fig. 4.5, there are 3 strong infrared transmittance peaks at around 1060 cm^{-1}, 800 cm^{-1} and 460 cm^{-1}. These peaks are strongly associated with Si-O bonds available in a silicon dioxide film. The peak around 1060 cm^{-1} peak is the strongest and it is attributed to a Si-O stretching bond. For thermal SiO_2, this peak is located at 1080 cm^{-1} [Lau, 1999]. The shift of this peak as a function of annealing temperature is shown

in Fig. 4.11. The shift of the position is also accompanied by the change of full-width at half-maximum (FWHM) of the peak (Fig. 4.12). When the annealing temperature increases from 300 to 400 °C, the peak of Si-O-Si stretching bond is shifted to a higher value; which is closer to 1080 cm^{-1}. However, there is a reduction in the FWHM of the peak. Hence, we may conclude that a densification of the film is obtained as the stretching of Si-O-Si bond is less in sample annealing at 400 °C if compared with 300 °C [Dimitrov et al., 2000]. However, when the annealing temperature is further increased to 500 °C, the position of the peak is shifted to a lower wave number; which is further to 1080 cm^{-1}. At the same time, the FWHM value of the particular peak is increased. This indicates that the stretching of Si-O-Si bond increases if compared with the sample annealed at 400 °C. During this bond stretching process, it may generate vacancy of oxygen atom. This vacancy may be treated as a donor like trap (Si^{+}).

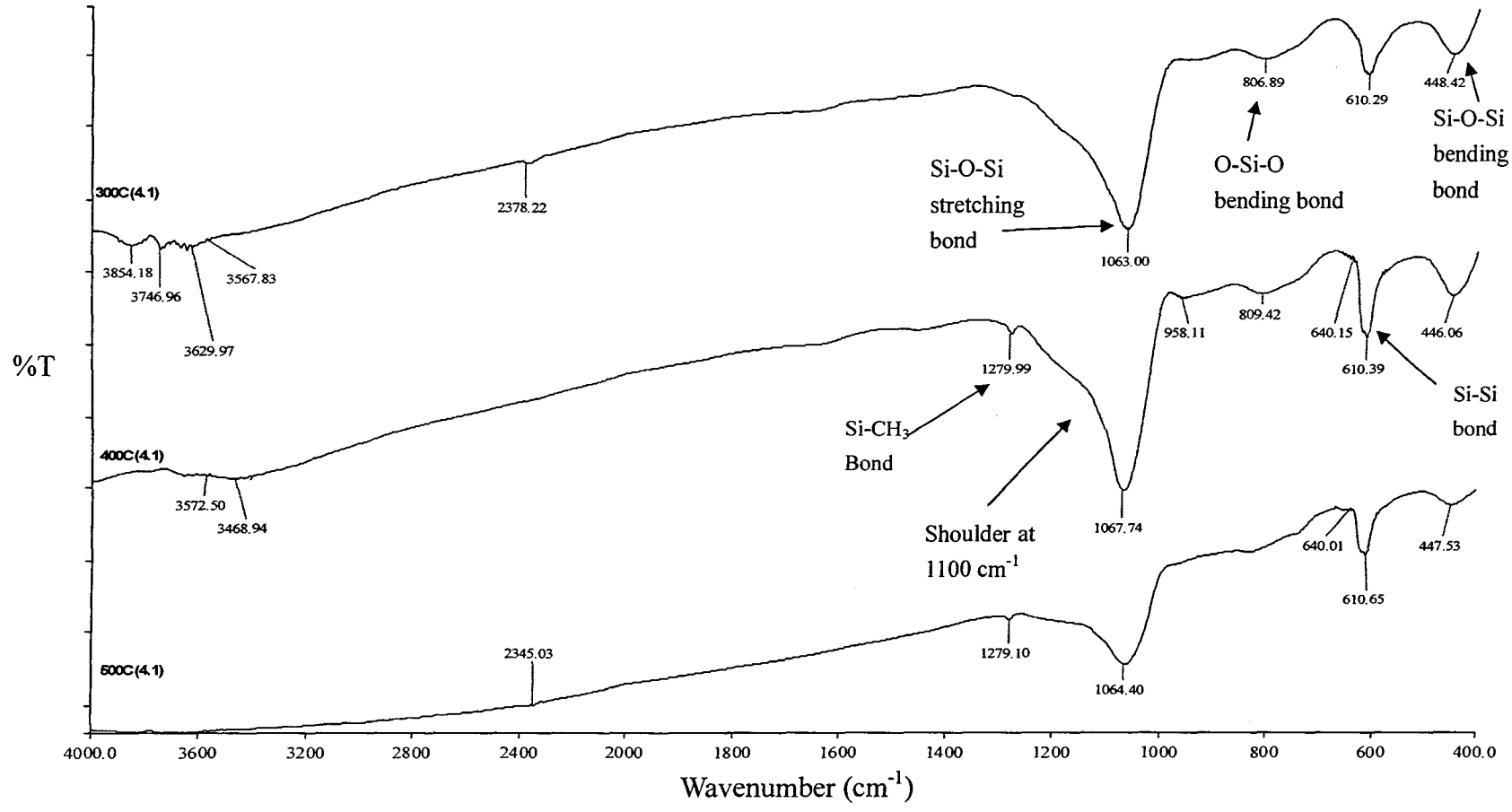

Figure 4.10: FTIR spectra of film prepared by TEOS/MTES ratio of 4:1 and heat treated at different temperatures.

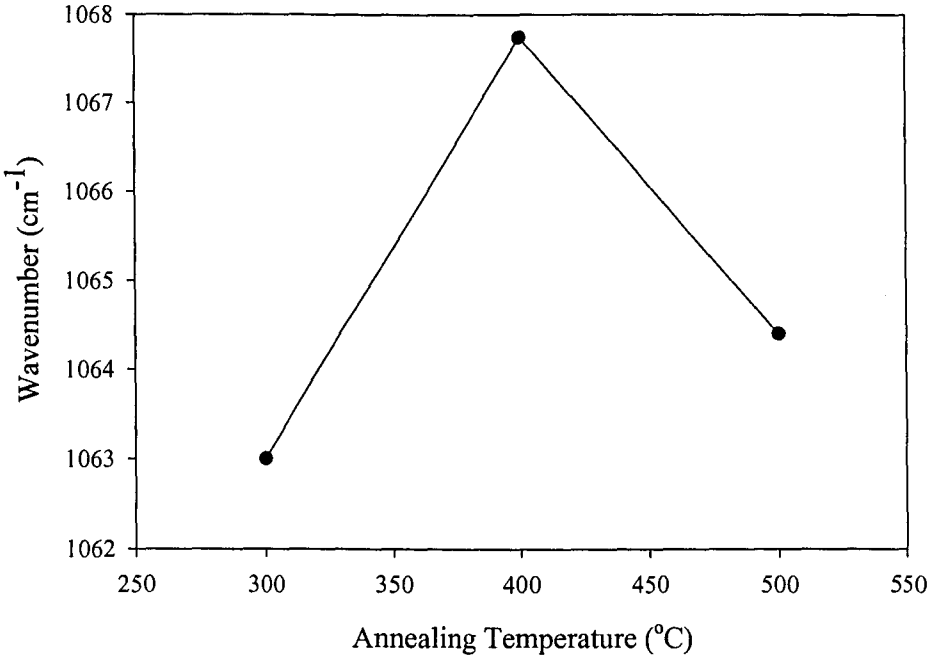

Figure 4.11: Location of peak due to Si-O-Si stretching bond as a function of annealing temperature.

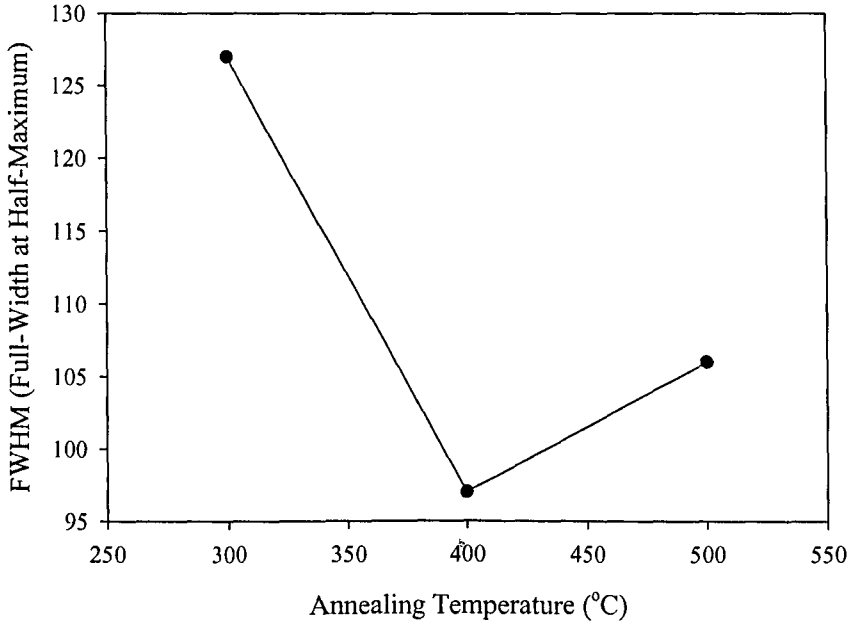

Figure 4.12: FWHM value of the transmittance peak of Si-O-Si stretching bond as a function of annealing temperature.

From the transmittance spectra shown in Fig. 4.10, a shoulder is detected around 1100 to 1200 cm^{-1}. This shoulder is corresponding to the longitudinal optical (LO) vibration of Si–O–Si linkage. The appearance of this LO shoulder is due to the optical scattering effect of porous sample [Yu et al., 2004].

Besides the transmittance peak located around 1060 cm^{-1}, there are additional two peaks associated with Si-O bonds. The peaks located at around 800 cm^{-1} and 460 cm^{-1} are attributed to bending of O-Si-O and Si-O-Si bonds [Lau, 1999]. The presence of bending bonding O-Si-O is caused by hydrolysis process from the sample. Meanwhile, the previous mentioned stretching bonding of Si-O-Si is attributed to the condensation process; which involving the hydroxyls group and subsequently initial the formation of inorganic polymer containing of Si-O-Si bond. Besides transmittance peaks related to SiO_2, peaks associated with Si substrate and incomplete or contamination of organic substances have been detected at location around 610 cm^{-1} (Si-Si bond) and >2300 cm^{-1} (2340 cm^{-1}, 3400 cm^{-1} and 3600 cm^{-1} is related to $Si-CH_3$, Si-H, and stretching of O-H, respectively) [Kim, 1997 and Lau, 1999]. As the annealing temperature increases, the later peak is reduced until it was not detected in sample treated at 500 °C.

4.3 Characterization of X-Ray Diffraction (XRD)

The x-ray diffractor graph of sample prepared by TEOS/MTES ratio of 4:1 and annealed at 300, 400 and 500 °C is showed in Fig. 4.13. The result is matched with

phase and structure of SiO_2 using a JCPDS file for SiO_2 (file number = 5-0490). There are two obvious peaks at 44.35° and 68.99° detected in sample annealed at 300 °C. These peaks are associated with SiO_2 with (200) and (203) orientations. As the annealing temperature increases, the later orientation of SiO_2 is reduced and eventually disappeared.

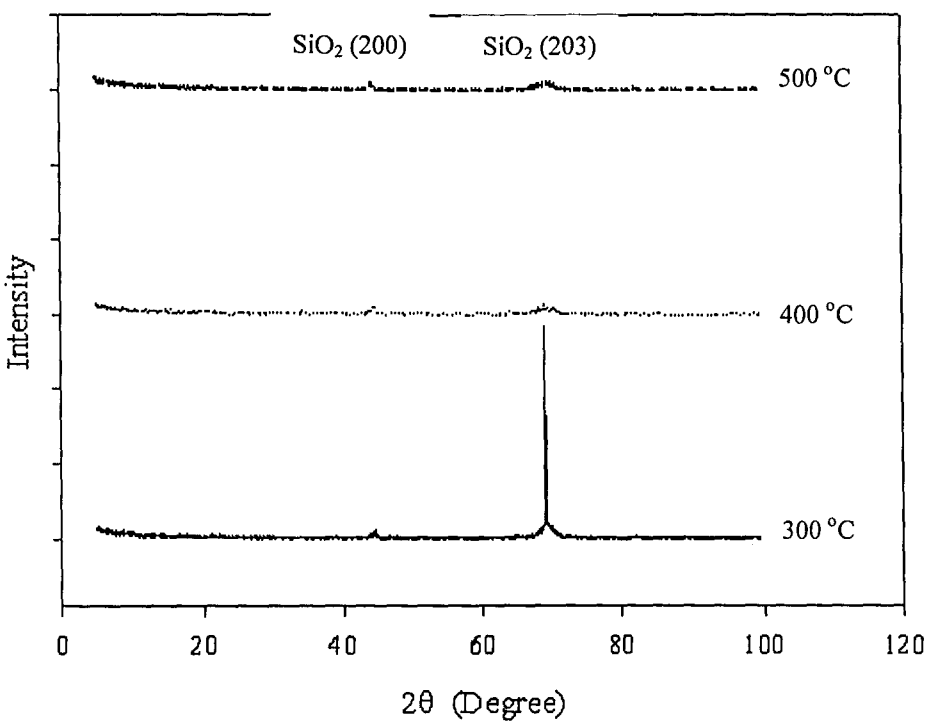

Figure 4.13: Pattern of XRD measured in sample prepared by TEOS/MTES ratio of 4:1 and anneal at 300 °C, 400 °C and 500 °C.

The crystallite size of SiO_2, for the film, at a particular orientation can be estimated using Scherrer equation [Eq. (4.5)].

$$L_{hkl} = \frac{k\lambda}{\beta_{hkl}\cos\theta_{hkl}} \tag{4.5}$$

where k is Scherrer constant, λ is wavelength of x-ray radiation, θ_{hkl} is Bragg angle, and β_{hkl} is half intensity width measure in radian. In this work the crystallite size at (2000 orientation has been estimated. The intensity of the peak at (200) is shown in Fig 4.9. It can be observed that the intensity increases from 300 to 400 °C and beyond that annealing temperature, the intensity is reduced. Figure 4.15 shows the effect of annealing temperature on the crystallite size. The trend of crystallite size as a function of annealing temperature is the same as the one revealed in Fig. 4.13. The crystallite size increases as the annealing temperature increased from 300 to 400 °C and further increase of temperature he size is reduced significantly. It has been reported that when the annealing temperature is higher than a critical value, the grain or crystallite size drops down rapidly and vice versa and the annealing temperature is lower than the critical value [He *at el.*, 2005]. When the annealing temperature is lower than the critical value, the density of nucleation is low. This may promote the growth of crystallite or grain size [He *et al.*, 2005].

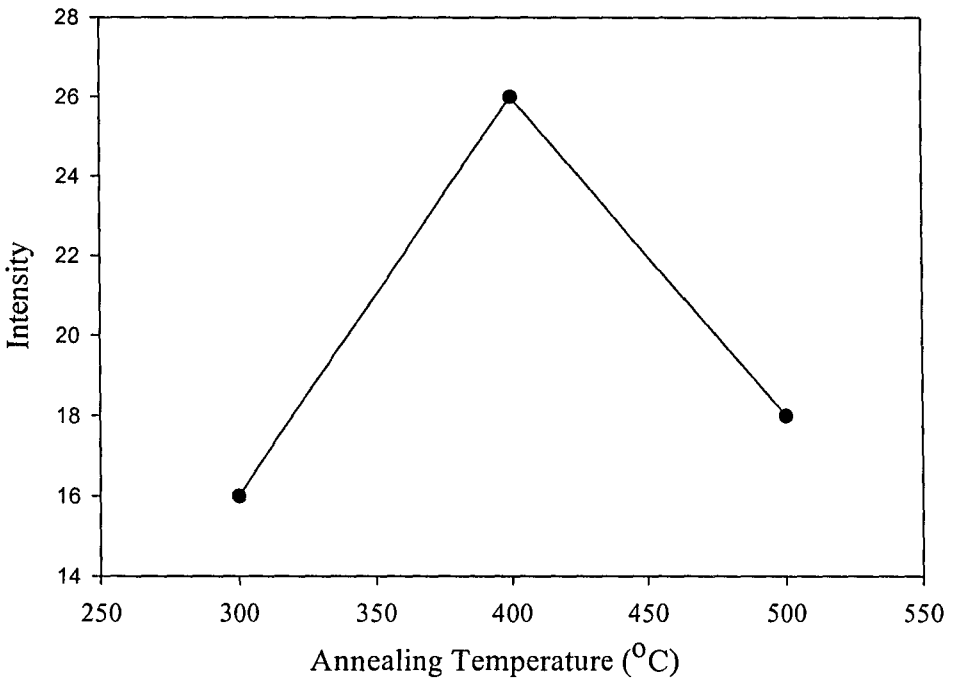

Figure 4.14: Effect of annealing temperature on intensity for SiO_2 with orientation (200).

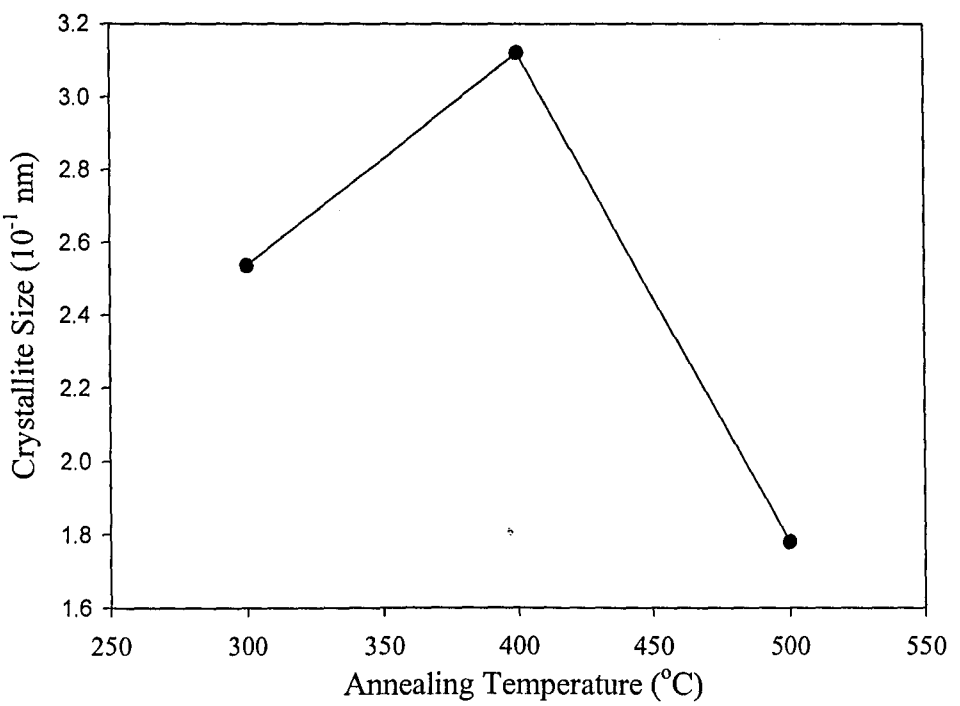

Figure 4.15: Effect of annealing temperature on the crystallite size.

When the annealing temperature of the film is higher than the critical value, there are two possible mechanisms that may cause the decrease in crystallite size. One is the oxygen deficiency in the SiO_2 thin films. When the annealing temperature is beyond the critical value, the concentration of oxygen is super-saturated and attributed to an oxygen deficit in the oxide layer. As a result, a high density of planar defect (grain boundaries) appears in the film and it restricts the grain growth process [He *et al.*, 2005]. Hence, a smaller crystallite size is observed. This explanation is in agreement with the wave number shift of transmittance peak around 1060 cm^{-1} for sample annealed at 500 °C (Fig. 4.14). The other mechanism that may attribute to the reduction of crystallite size as temperature is beyond a critical value is the high nucleation density. The nucleation of complex oxide requires a sufficient energy to overcome chemical-reaction barrier. This may be possible with higher annealing temperature. During this high annealing process, clustering of stable crystallite is initiated and this combination of clusters acts as nucleation sites for the growing of thin film. Since the high annealing temperature promotes the clustering, a higher density of nuclei is obtained and this high density of nuclei restricts the further growth of grain or crystallite size [He *et al.*, 2005]. The subsequent sub-section shows the procedure of calculating the crystallite size.

Example of calculation:

The sample is annealed at 500 °C and prepared by TEOS/MTES ratio of 4:1.

From Fig 4.14, $k = 0.9$

$\lambda = 1.54$

$\theta_{hkl} = 0.8400$

$\beta_{hkl} = 44.34 / 2 = 22.17^{o}$

From Eq. (4.5), $L_{hkl} = \dfrac{k\lambda}{\beta_{hkl} \cos\theta_{hkl}}$

$$= \frac{0.9(1.54x10^{-10})}{0.84(\cos 22.17)}$$

$$= 1.78 \text{ x}10^{-10} \text{ m}$$

The study of phase and orientation changes in SiO_2 prepared by different ratio of TEOS / MTES heat treated at 400 °C is showed in Fig. 4.16. It has been reveal that the SiO_2 (200) oriented peak at 44.35° is independent of TEOS/MTES ratio. However, the other peak related to SiO_2 (031) is the ratio dependence. This peak increases as the concentration of TEOS increases (or the MTES decreases). This is because TEOS is the source of Si-O. If the concentration of TEOS reduces, this may affect the formation of the Si-O-Si structure.

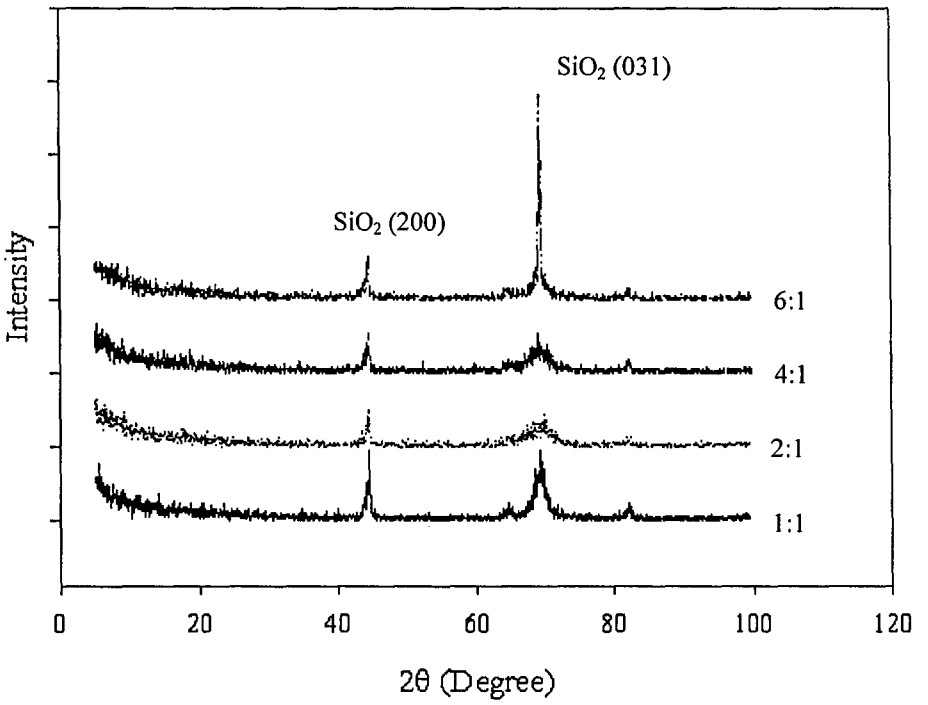

Figure 4.16: Pattern of XRD for samples prepared by different TEOS/MTES ratio (1:1, 2:1. 4:1, and 6:1) and heat treated at 400 °C.

4.4 Characterization of Atomic Force Microscopy (AFM)

AFM is used to investigate the surface topography of the thin film. Surface topographies of sample prepared by TEOS/MTES ratio of 4:1 and annealed at different temperatures are presented in Figs.4.17 to 4.19.

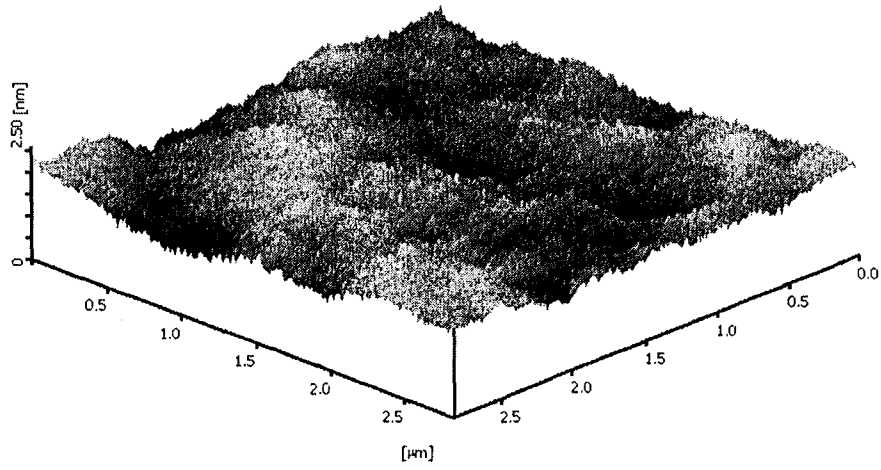

Figure 4.17: Surface topography of sample annealed at 300 °C.

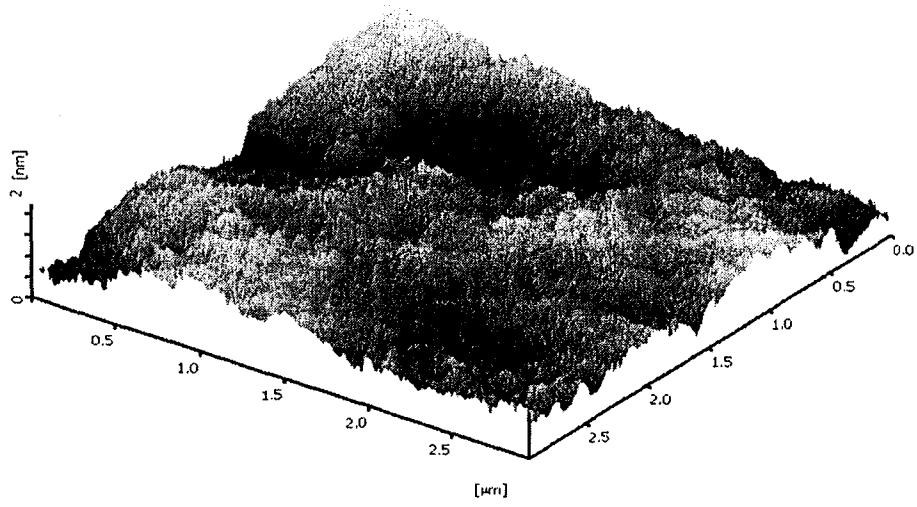

Figure 4.18: Surface topography of sample annealed at 400 °C.

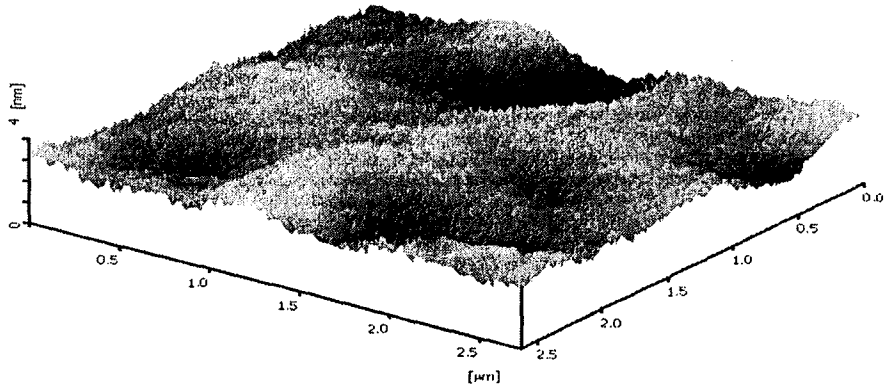

Figure 4.19: Surface topography of sample annealed at 500 °C.

The result qualitatively revealed that annealing temperature would change the topography of the film. Quantitatively, root-mean-square roughness (RMS), n point mean height (Rz), and surface mean height (Ra) of the investigated surfaces have been extracted and their results are presented in Figs. 4.20, 4.21, and Fig 4.22, respectively.

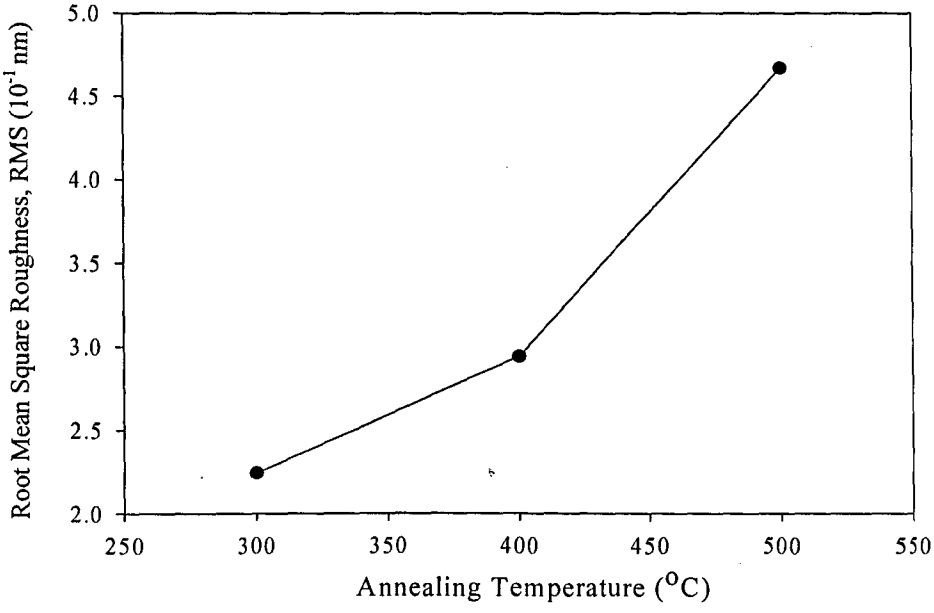

Figure 4.20: Effect of annealing temperature on root-mean-square roughness (RMS) of the film surface.

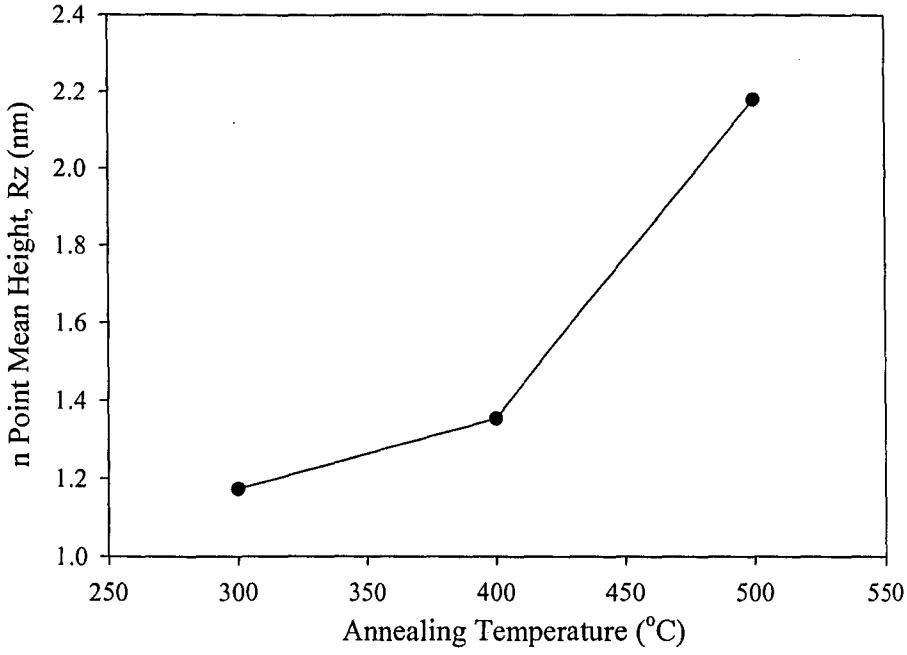

Figure 4.21: Effect of annealing temperature on n point mean height (Rz) of film surface.

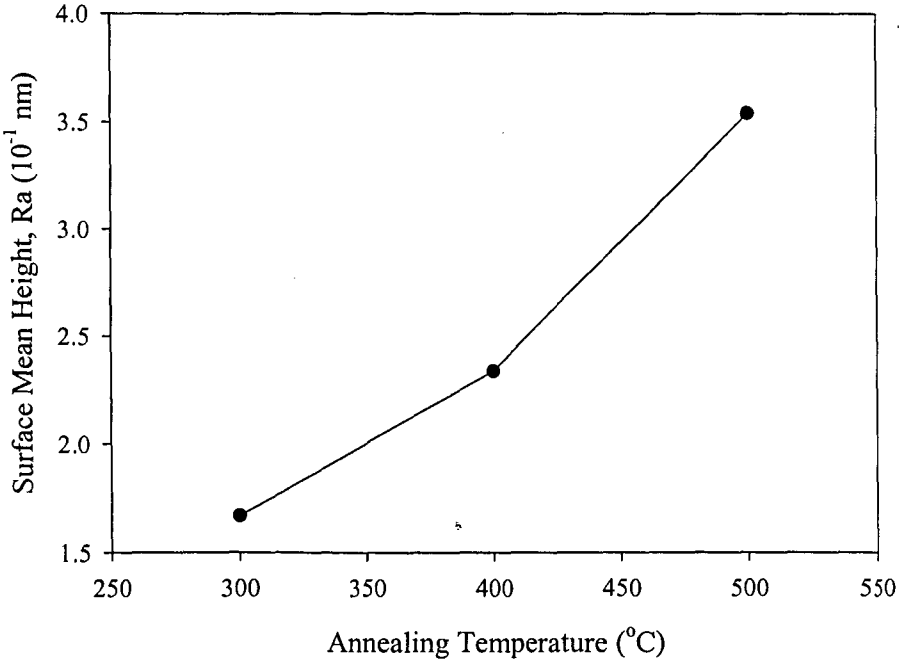

Figure 4.22: Effect of annealing temperature on surface mean height (Ra) of the film surface.

The value of RMS, Rz, and Ra are increased with the increase of annealing temperature. The change of surface structure and topography are obviously observed when the temperature increased from 300 °C to 500°C. The surface of the film becomes rougher as the annealing temperature increases may attribute to the grain growth process [Tian *et al.*, 2005].

4.5 Characterization of Scanning Electron Microscopy (SEM)

Figure 4.23 shows a SEM micrograph of a sample prepared by TEO/MTES ratio of 4:1 and annealed at 400 °C. The magnification of the image is 10,000 X. There is no obvious grain, microstructure, and pore in the image. This indicates that the film is covered well on the Si substrate. The same observations have been recorded for those samples annealed at 300 and 500 °C.

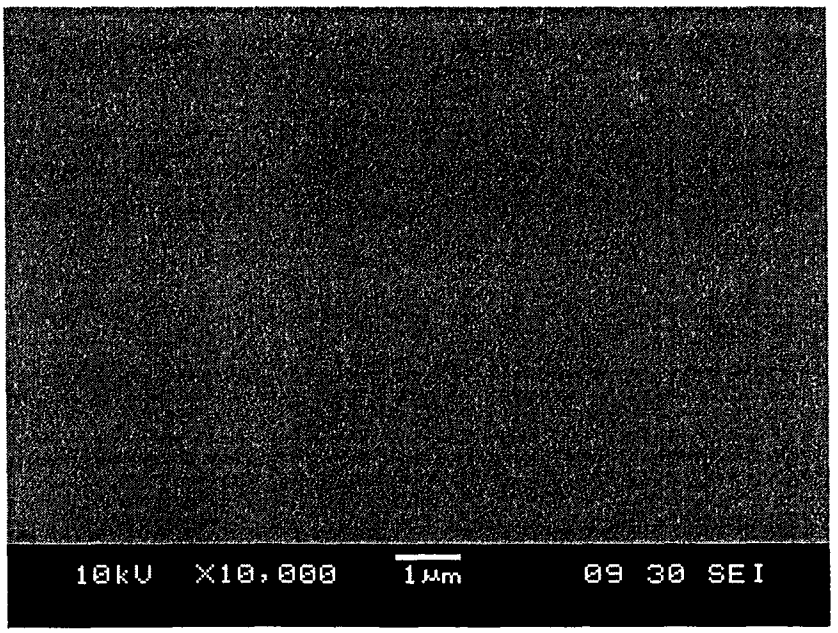

Figure 4.23: SEM micrograph of sample prepared by TEOS/MTES ratio of 4:1 and annealed at 400 °C.

4.6 Characterization of Energy Dispersive X-Ray Analysis (EDX)

From the EDX result, elements of Si, O, have been detected and C for samples prepared by TEOS/MTES ratio of 4:1 and annealed at different temperatures (Fig. 4.24). Since the results of FTIR and XRD revealed that the films are SiO_2, therefore we could confirm that the Si and O elements are originated from SiO_2. The presence of C element may due to the organic precursor source used in this work. Based on the EDX result, it is clear that a slight reduction of O weight percent has been detected in sample annealed at 500 °C. This indicates oxygen deficiency and it is in agreement with the explanation given in the section of FTIR and XRD results [He *et al.*, 2005].

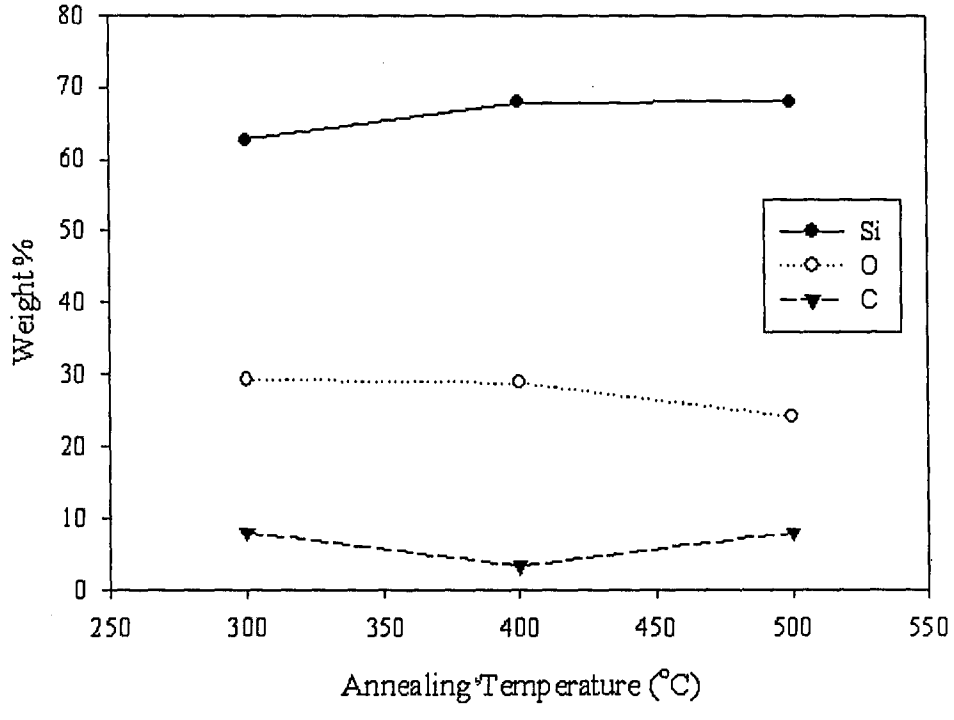

Figure 4.24: Weight percentage of various elements detected in samples with TEOS / MTES ratio of 4:1 and annealed at different temperatures.

4.7 Characterization of Electrical Property

I-V test has been performed on the film with TEOS/MTES ratio of 4:1 and annealed at different temperatures. This test is to investigate the insulating property of the film as a function of applied voltage. Stoneham et al., (2005) stated that dielectric film should have low leakage current in order to act as good insulator. The evolution of the I–V characteristics with applied voltage indicates that different conduction mechanisms occur depending on annealing temperature. The leakage current mechanisms commonly reported in dielectric thin films include ohmic conduction (usually at low field), space-charge-limited conduction (SCLC), Poole-Frenkel conduction, and Schottky conduction [Yang et al., 2004]. Measurement of I-V curve was done using two methods. The first one is to investigate the I-V characteristics of a nano-region of the sample using a *conductive atomic force microscope* (C-AFM). While the other method is to investigate the micro-region of the sample using a I-V meter.

The obtained I-V measurements are transformed into current density-electric field (J-E) plots based on Eqs. (4.6) and (4.7). The equations are as follow:

$$\text{Density current, } J = I / A \tag{4.6}$$

where I is current in Ampere (A) unit and A is area in cm^2 unit

$$\text{Electric field, } E \cong V / t_{ox} \tag{4.7}$$

where V is applied voltage in MV unit and t_{ox} is oxide thickness in cm unit.

A sample of calculation is provided in the following sub-section.

Example of calculation:

Sample annealed at 500 °C:

Density current, J = I / A

$$= 2.40 \times 10^{-9} / 4.908 \times 10^{-12} \text{ cm}^2$$

$$= 488.99 \text{ A / cm}^2$$

Electric field, $E \cong V / t_{ox}$

$$\cong (3.52 \times 1 \times 10^{-6} \text{ MV}) / 120 \times 10^{-7} \text{ cm}$$

$$\cong 0.29 \text{ MV / cm}$$

Figure 4.25 shows the I-V plot of nano-region obtained from C-AFM. It is obvious that leakage current reduces as the annealing temperature increases. Leakage current at 80 V for film treated at 300 °C is about 4.05 nA, it is reduced to 3.75 nA at 400 °C, and 3.52 nA at 500 °C. This result proven that the electrical property of the film can be improved by increasing the annealing temperature.

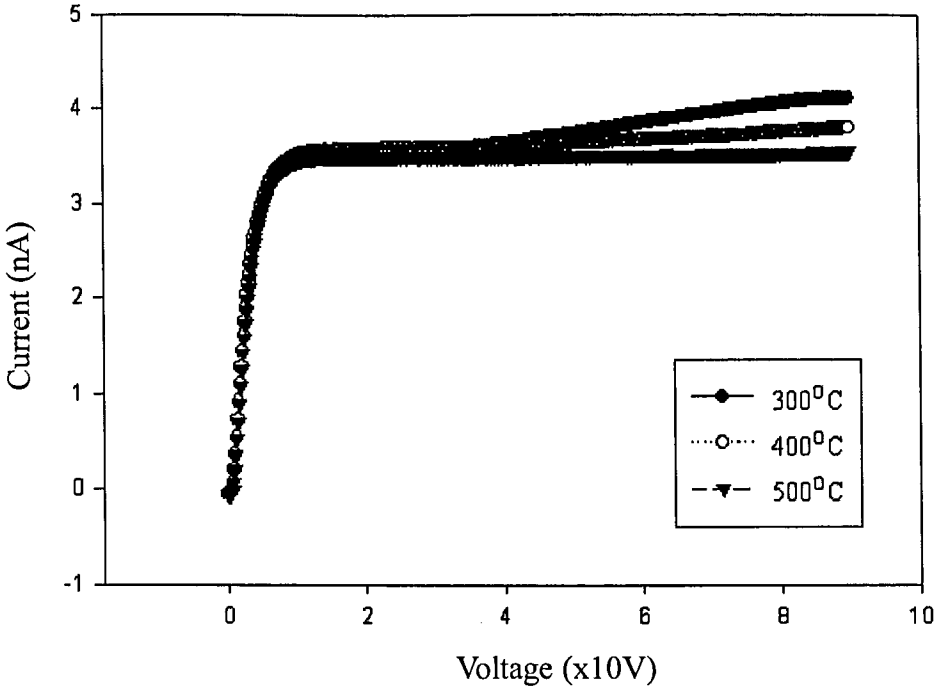

Figure 4.25: Current-voltage characteristics of nano-region of sample prepared by TEOS/MTES of 4:1 and annealed at different temperatures.

Similar trend of the leakage current as a function of annealing temperature has been revealed for micro-region samples (Fig. 4.26). When annealing temperature increases, the density current is reduced. This indicates that leakage current is also reduced. The current density at 0.41 MV/cm for sample annealed at 300 °C is about -1.119 A/cm^2, it reduced to -4.469 A/cm^2 at 400 °C, and -4.832 A/cm^2 at 500 °C. The breakdown field of the investigated film has been extracted from the J-E plots. This field refers to an instantaneous increase of J value at a particular electric field. It is obvious that sample annealed at 400 and 300 °C have demonstrated a sharp increase of J at 0.58 and 0.38 MV/cm, while there is no significant increase in sample annealed at

500 °C.

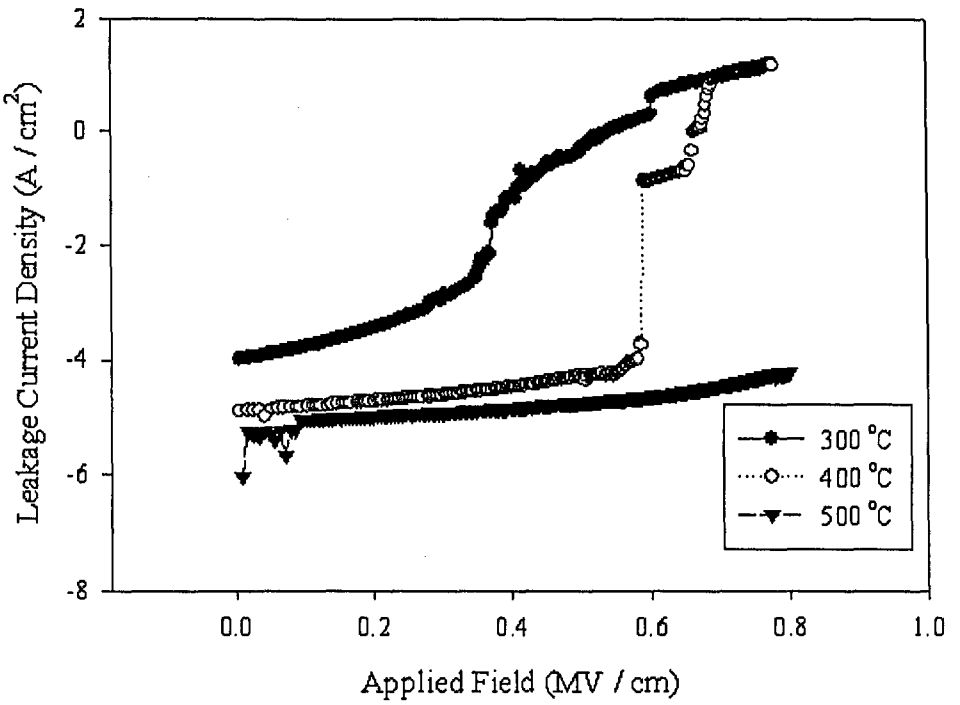

Figure 4.26: Current density –electric field characteristics of micro-region of sample prepared by TEOS/MTES of 4:1 and annealed at different temperatures.

The increment of breakdown field and reduction of leakage current at higher annealing temperature may be attributed to the increase of surface roughness as what has been revealed in Fig. 4.20. As the surface becomes rough, the probability of a region with thicker oxide is high. The thicker oxide may restrict the movement of charge passing through the oxide. Therefore, a lower leakage current is detected. Besides surface roughness, crystallite size also affecting the leakage current in an insulating film. As the crystallite size increases (as annealing temperature increases from 300 to 400 °C), less grain boundary is available in the film. This boundary is acting as a preferable path

for current conduction. When this boundary reduces, the probability of current passing through this path is being reduced and its leakage current is also reduced. However, for sample annealed at 500 °C, crystallite size does not play a main role to reduce the leakage current. As at this annealing temperature, the produced film has demonstrated a deficiency of oxygen as being proven by EDX and also suggested by FTIR. This may act as a donor-like trap for the injected electron. As the electron being injected from Si into the oxide, majority of the electron is captured and neutralized in the trap. This is not happening in samples annealed at 300 and 400 °C. Therefore, the leakage current is much lower than those samples.

CHAPTER 5: CONCLUSION AND SUGGESTION

This chapter presents the research conclusion of the effect of temperature and TEOS/MTES ratio of precursor for the sol-gel derived low dielectric ocnstant SiO_2 thin film on Si.

5.1 Conclusion

Uniform low dielectric constant silica thin films were fabricated using sol-gel process. The processing temperature had great effect on the physical and electrical properties of the films. With increasing annealing temperature, percentage of porosity has been increased while the dielectric constant and refractive index has been decreased. FTIR, XRD, and EDX results have shown that the deposited thin film is SiO_2. The high value of RMS and Rz as well as the donor-like trap in the bulk oxide for sample annealed at 500 °C was the main caused of the low leakage current.

5.2 Suggestions for future research

i. The annealing process can be replaced by rapid thermal processes (RTP) so that a better control of the ambient condition.

ii. The result of thickness and refractive index that has been measured by Filmetrics should be re-confirmed by an ellipsometer.

iii. Methyltrimethoxysilane (MTMS) and dimethylchlorosilane (DMCS) could be used to replace MTES as organic precursor.

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