HIGH PERFORMANCE CURRENT AMPLIFIER

by

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ACKNOWLEDGEMENTS

JUST TO

My dear family,

Dr. Tun Zainal Azni Zulkifli,

P.M. Dr. Mohamad Awan,

P.M. Dr. Rezaul Hasan,

USM lecturers,

My teachers,

Friends,

And lastly to my dearest father and mother……

They are my life's compass…….

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NOMENCLATURE

A_L	Loop gain	-
C_{bd}	Body drain capacitance of a transistor	F
C_{bs}	Body source capacitance of a transistor	F
C_{gb}	Gate body capacitance of a transistor	F
C_{gd}	Gate drain capacitance of a transistor	F
C_{gs}	Gate source capacitance of a transistor	F
g_{bd}	Body effect conductance drain of a transistor	1/ohm
g_{bs}	Body effect source conductance of a transistor	1/ohm
g_{ds}	Drain Conductance of a transistor	1/ohm
G_L	Loop transimpedance	1/ohm
g_m	Transconductor of a transistor	1/ohm
g_{mb}	Body effect transconductor of a transistor	1/ohm
I_{bias}	Biasing current	A
I_D	Drain Current of a transistor	A
I_{in}	Input current	A
I_{out}	Output current	A
I_q	Quiescent current	A
I_s	Current source	A
L	Length of channel transistor	m
R_{in}	Input impedance	ohm
R_{out}	Output impedance	ohm

R_s	Impedance source	ohm
T	Interval Time	s
V_{bias}	Biasing voltage	V
V_{bs}	Voltage source voltage of a transistor	V
V_{dd}	Drain voltage supply	V
V_{ds}	Drain source voltage of a transistor	V
V_{eff}	Effective voltage	V
V_{gs}	Gate source voltage of a transistor	V
V_{in}	Input voltage	V
V_{out}	Output voltage	V
V_s	Voltage source	V
V_{ss}	Source voltage supply	V
V_{th}	Threshold Voltage of a transistor	V
W	Width of channel transistor	m

HIGH PERFORMANCE CURRENT AMPLIFIER

ABSTRACT

A high bandwidth class AB current amplifier by using few compensation resistor technique and current mirrors is presented and analyzed. The simulation results are obtained using TSpice tool using 0.35μm CMOS TSMC process, at 2.5V power supply. The amplifier utilizes Class AB amplifier topology to achieve high bandwidth. The current amplifier realized with only ten MOS devices, where will always provides very low input resistance, good large signal behavior and GHz bandwidth. Such technique stands as a powerful method of bandwidth enhancement for general circuit using CMOS current mirrors. The original circuit without compensation resistor technique contributes about 5.3 MHz bandwidth and the presented bandwidth is being enhanced from 1 GHz for the uncompensated current amplifier to about 1.13 GHz for the compensated one without affecting the current gain to 2% precision. Besides, the presented amplifier has very low power dissipation and it is about 1.75mW with the current supply for the circuit is about 112μA, so heat sink is not require which provides space saving and cost saving. This amplifier is able to operate at 2.5V supply voltage and it is a standard for the CMOS technology. The simulation result shows the circuit will perform as a good current amplifier at input impedance of 106Ω and output impedance 37kΩ and current gain 20dB. It is the basic for a good current amplifier which always required low input impedance and high output impedance. The phase margin and gain margin of the presented amplifier is about 55deg and –11dB. Since the gain margin is negative and phase margin is about 60deg, theoretically no oscillation are possible for this circuit and the amplifier can perform stable at high frequency.

PENGGANDA ARUS BERPRESTASI TINGGI

ABSTRAK

Sebuah penguat arus kelas AB berjalur lebar tinggi yang menggunakan teknik "compensation" resistor dibentang dan dianalisis dalam tesis ini. Keputusan penyelakuan ini didapati dengan mengunakan Teknology TSMC 0.35μm CMOS bekalan kuasa 2.5V melalui alat penyelakuan TSPice. Penguat Kelas AB diimplementasikan untuk mencapai jalur lebar yang tinggi. Pengganda arus baru ini terdiri dari 10 MOS yang mempunyai rintangan masukan yang rendah dan berjalur lebar GHz. Rekeabentuk asas bagi penguat arus ini yang tidak menggunakan teknik "compensation" resistor hanya berjalur 5.3MHz sahaja and pengganda arus berstruktur FDCM baru ini telah membaiki jalur lebar dari 1 GHz hingga 1.13 GHz dengan keadaan tidak mempengaruhi gandaan arus yang asas dalam ketepatan 2%. Selain itu, penguat arus ini mempunyai haba terjana yang serendah 1.75mW dengan arus bekalan 112μA, oleh itu penguat ini tidak memerlukan pembenam haba dan menjimatkan ruang. Penguat ini dapat beroperasi pada bekalan 2.5V and bekalan ini adalah standard untuk teknologi.CMOS. Keputusan penyelakuan menunjukkan penguat arus ini bersifar penguat bagus sebab ia mempunyai arus mempunyai rintangan masukan 106Ω, rintangan keluaran 37kΩ dan juga untung arus 20dB. Ini adalah basic untuk sebuah penguat arus yang sentiasa memerlukan rintangan masukan yang rendah dan rintangan keluaran yang tinggi. Phase margin dan gain margin untuk penguat arus ini adalah 55deg dan –11dB. Oleh kerana gain margin adalah negatif dan phase margin adalah lebih kurang 60deg, secara teori, tidak mungkin adalah osilation dan penguat ini bermampu operasi stabil semasa frequensy tinggi.

CHAPTER 1

INTRODUCTION

1.1 Background

Interest in evolution of low voltage supply and low power circuits of analogue circuit designs have grown rapidly from applications on watches and medical electronics to a host of other applications. The increased interest is mainly due to commercial implications of portable equipment, power reduction on non-battery powered system and consumer electronics.

For the past decade, people have predicted there soon would be little need for the analog circuitry because the world would rely on digital circuits. A good example in our live is digital audio. However, although some of the applications have indeed replaced much analogue circuitry with their digital counterparts, the need for the analog circuit design remains important. For example, when digitizing physical signals, analog to digital and digital to analog converters are always needed. In addition, new applications continue to appear in which speed and power consumption requirements often demand the use of high speed analog front ends, such as digital communications over copper wires or wireless communication channels.

Voltage and current modes are two main access keys in investigating the analogue world. Their dual nature can help efficiently in making a comprehensive analysis of the problem, but whether using, the voltage approach or the current one

depends exclusively on the application domain. Current amplifier performs the same functions in the current domain as the conventional amplifier does in the voltage domain [Bruun, 1991]. Currently, current amplifier seems to be favorable from the point of view of both dynamic range and closed loop bandwidth [Lidegey, Payne & Tourmazou, 1991]. On the other hand, the implementation of a high performance class AB amplifier is a hard task due to the need to preserve accuracy, linearity, low power consumption and high speed. With a continuing reduction of MOS transistor channel lengths, resulting in increasing transistor cut off frequencies, modern CMOS silicon processes offer transistor with a higher cut off frequencies.

As a result, the CMOS technology becomes feasible for those wide band analogue applications, which were traditionally built with bipolar devices.

In recent years, current mode signal processing has been widely investigated, and several works have demonstrated that this approach can solve many circuits and systems problems. As can be expected from circuit exploiting current mode techniques, performance in terms of low voltage capability, slew rate, and bandwidth can in principle be maximized [Peregrinus, 1990]. However, when class AB topologies have to be implemented, the need for a complementary structure has prevented, until now, the achievement of true low voltage features. Compared to class A topologies, class AB versions provide better dynamic range [Kawahito & Tadokoro, 1996] and reduced sensitivity to process tolerances. In addition, they exhibit extremely high slew rate value.

Although the well known switched current approach has been used in the past to achieve both class AB and low voltage operation, no effective continuous time approach providing the same performance exist at present [Peregrinus, 1990].

Now, the design of CMOS current amplifier has received considerable interest, since they seem to have a better dynamic range and bandwidth performance than conventional voltage amplifiers. Current amplifiers are particularly suitable for use with temperature sensors, photo sensors, and, in general, whenever the input source or the output is current signals. Moreover, current amplifiers have the interesting features of achieving true multi output device since several current outputs can be embedded.

The higher operating speed possible with current mode circuits, as compared to voltage mode circuits, has recently motivated renewed interest in current mode circuits and current mode signal processing. The interest is made evident by publication in the technical literature [Peregrinus, 1990], with the current conveyor being by far the most pervasive current mode building block. The inherent speed advantage of the current mode circuits stems from the fact that a current mode circuit is a network with low impedance nodes, and correspondingly small voltage swings. These small voltage swings significantly reduce the effect of voltage slewing at internal circuit nodes since the parasitic capacitances which are always present there, and must be charged and discharged, undergo only small voltage excursions [Gibert, 1968].

The first current conveyor was introduced in 1968 [Sedra & Smith, 1968] and reformulated, in the second-generation version [Sedra & Smith, 1970], and since then, numerous applications have been devised for these building blocks. Although good

designs, both discrete and integrated, have been reported for second-generation version [Wilson, 1984], very few current conveyor circuits are available.

1.2 Contribution Of The Proposed Circuit

For wide band current applications, current mirrors compensated with a resistor are proposed and advantageous to achieve high performance current amplifier. An elegant technique for improving current amplifier bandwidth is applied. This technique improves the unity gain frequency of about 100MHz when comparing the uncompensated circuit and the compensated one. Support with Tspice simulations, this topology allows extending the bandwidth without sacrificing other design parameters such as power consumption, output swing and the current gain. This technique seems to be useful in some applications such as industrial, biomedical, current conveyor and aerospace fields and many signal-processing circuits, which use wide band current amplifiers. It seems ideal for high performance amplification of bi-directional current signals.

The proposed amplifier has also potential in integrated circuit form for high-speed continuous time and sampled data analogue signal processing applications.

1.3 Objective

The objective of this research work is to design a high performance amplifier with low input impedance, high output impedance, high bandwidth, optimizes phase margin, low input noise ,low output noise and low power dissipation.

CHAPTER 2

FUNDAMENTALS AND LITERATURE

2.1 Introduction

In this chapter fundamental building blocks and literature survey are described. These blocks include a variety of current mirrors, single-stage amplifiers with active loads and differential pairs. A good knowledge of these building blocks is necessary for an analogue circuit designer.

2.2 Simple CMOS Current Mirror

A simple CMOS current mirror is shown in Fig. 2.1. It is assumed that both the transistors are operating in the active region and both the transistors are of the same size. If the finite output impedances of the transistors are ignored, then M_1 and M_2 will have the same current since they both have the same gate-source voltage.

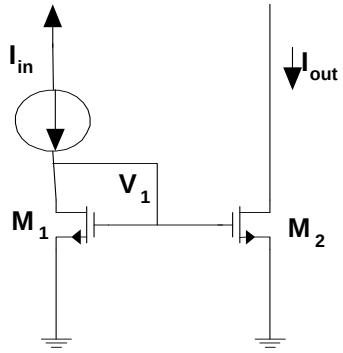

Fig. 2.1 A simple CMOS current mirror.

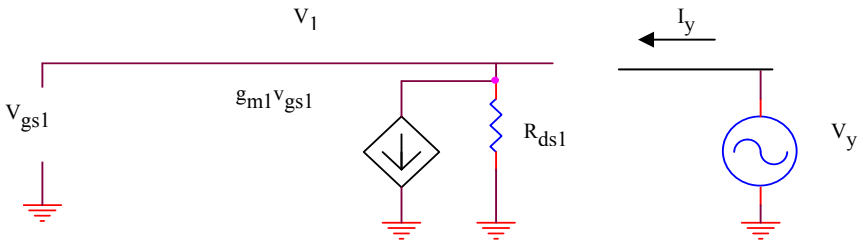

Fig. 2.2 Equivalent small-signal model for M_1.

Consider the small-signal model for M_1 alone, as shown in Fig. 2.2. Note that M_1 is diode connected (i.e., its drain and gate are connected) and that I_{in} does not exist in the small-signal model; I_{in} was replaced with an open circuit because it is an independent current source. Also note that a low-frequency small-signal model is used for M_1 (all the capacitors are ignored in the model).

This circuit's Thevenin equivalent output is found by applying a test signal voltage, V_y, at V_1 and measuring the signal current I_y, as shown. Here, the current I_y is given by

$$I_y = \frac{V_y}{r_{ds1}} + g_{m1}V_{gs1} + g_{m1}V_y \qquad (2.1)$$

And recalling that the output impedance is given by V_y/I_y, the output impedance of the circuit is equal to $1/g_{m1} \| r_{ds1}$. Because typically $r_{ds1} >> 1/g_{m1}$, the output impedance is approximated to $1/g_{m1}$.

Using the model just described leads to the simplified small-signal model for the overall current mirror, as shown in Fig. 2.3, where V_{gs2} has been connected to ground via a resistance of $1/g_{m1}$. Since no current flows through the $1/g_{m1}$ resistor, V_{gs2} equals 0 no matter what voltage level V_x is applied to the current-mirror output. This should come as no surprise, since MOS transistors operate unilaterally at low frequencies. Thus, since $g_{m2}V_{gs2} = 0$, the circuit is simplified to the equivalent small-signal model shown in Fig. 2.4. The small-signal output impedance, r_{out}, is simply equal to r_{ds2}.

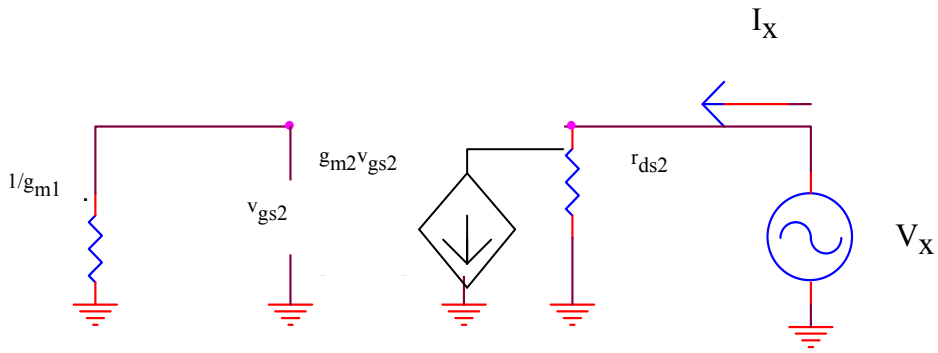

Fig. 2.3 A small-signal model for the current mirror of Fig. 2.1.

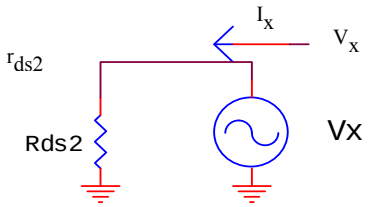

Fig. 2.4 A simplified small-signal model of the above figure.

2.3 Common-Source Amplifier

A common use of simple current mirrors is in a single-stage amplifier with an active load, as shown in Fig. 2.5. This common-source topology is the most popular gain, especially when high-input impedance is desired.

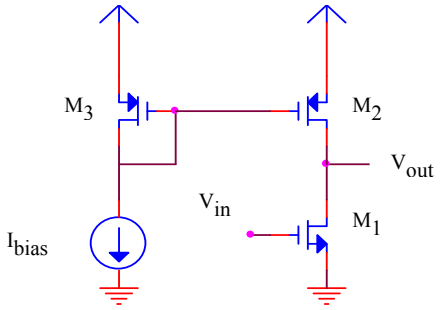

Fig. 2.5 A common source amplifier with a current mirror active load.

Here, an n-channel common-source amplifier has a p-channel current mirror used as an active load to supply the bias current for the drive transistor. By using an active load, a high-impedance output load can be realized without using excessively large resistor or large power-supply voltage. As a result, for a given power-supply voltage, a larger voltage gain can be achieved using an active load then would be possible if a resistor were used for the load. An active load makes use of non-linear,

large signal transistor equations to create simultaneous conditions of large bias currents and large small-signal resistances.

A small-signal equivalent circuit for low-frequency analysis of the common-source amplifier is shown in Fig. 2.6 below.

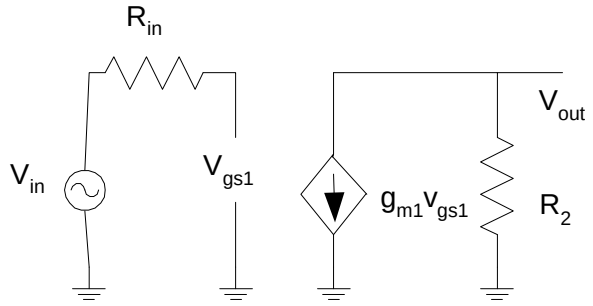

Fig. 2.6 A small signal equivalent circuit for the common source amplifier.

V_{in} and R_{in} are the Thevenin equivalent of the input source. It is assumed that the bias voltages are such that both transistors are in the active region. The output resistance, R_2, is made up of the parallel combination of the drain-to-source resistance of M_1, that is, r_{ds1}, and the drain-to-source resistance of M_2, that is, r_{ds2}. Notice that voltage-controlled current source modeling the body effect has not been included since the source is at a small-signal ground, and, therefore, this source always has 0 current. Using small-signal analysis, we have $V_{gs1} = V_{in}$ and, therefore,

$$A_V = \frac{V_{out}}{V_{in}} = -g_{m1}R_2 = -g_{m1}(r_{ds1} \square r_{ds2}) \tag{2.2}$$

Depending on the device size, current, and the technology used, a typical gain of this circuit is in the range of –10 to –100. To achieve similar gains with resistive loads, much larger power-supply voltages than 5V must be used. This resistive load approach also greatly increases the power dissipation. However, it should be mentioned here that for low gain, high frequency stages, it might be desirable to use resistor loads because they often have less parasitic capacitances associated with them.

2.4 Source-Follower Or Common Drain Amplifier

Another general use of current mirrors is to supply the bias current of source-follower amplifiers as shown in Fig. 2.7. In this example, M_1 is the source follower and M_2 is an active load that supplies the bias current of M_1.

These amplifiers are commonly used as voltage buffers and are therefore commonly called source followers. They are also referred to as common-drain amplifiers, since the input and output nodes, respectively, with the drain node being at small-signal ground. Although the dc level of the output voltage is not the same as the dc level of the input voltage, ideally the small-signal voltage gain is close to unity. In reality, it is somewhat less that unity. Although this circuit does not generate voltage gain, it does have the ability to generate current gain.

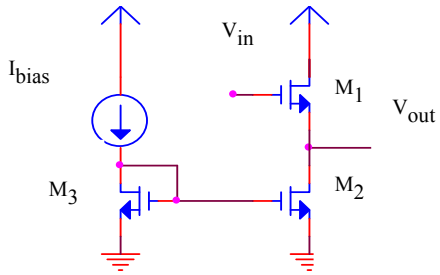

Fig. 2.7 A source follower stage with a current mirror used to supply the bias current.

A small-signal model for low-frequency analysis of this source-follower is shown in Fig. 2.8. Note that the voltage-controlled current source that models the body effects of MOS transistors has been included. This body effect is included because the source is not at small-signal ground and the body effect is the major limitation on the small-signal gain.

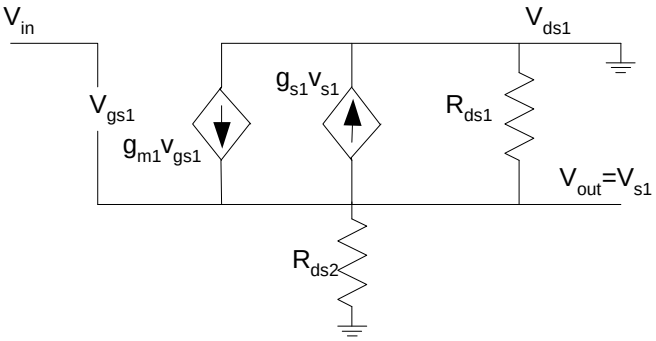

Fig. 2.8 A low frequency model of the source follower amplifier.

Writing the nodal equation at V_{out}, and noting that $V_{gs1}= V_{in}-V_{out}$, we have,

$$V_{out}G_{s1} - g_{m1}(V_{in} - V_{out}) = 0 \tag{2.3}$$

Where G_{s1} is $1/R_{s1}$ and the value of R_{s1} is given by

$$R_{s1} = r_{ds1} \parallel r_{ds2} \parallel \frac{1}{g_{s1}} \tag{2.4}$$

Solving for V_{out}/V_{in}, we have,

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{(g_{m1} + G_{S1})} = \frac{g_{m1}}{(g_{m1} + g_{s1} + g_{ds1} + g_{ds2})} \tag{2.5}$$

Normally, g_{s1} is on the order of one-tenth to one-fifth that of g_{m1} [John & Martin, 1997]. Also, the transistor output admittances, g_{ds1} and g_{ds2}, might be one-tenth of the body-effect parameter, g_{s1}. Therefore, it is seen that the body-effect parameter is the major source of error causing the gain to be less than unity. Notice that there is no signal flow from the output to the input

2.5 Common Gate Amplifier

A common-gate amplifier with an active load is shown in Fig. 2.9. This stage is commonly used, as a gain stage when relatively small input impedance is desired. For example, it might be designed to have an input impedance of 50Ω to terminate a 50-Ω transmission line. Another common application for a common-gate amplifier is the first stage of an amplifier designed to amplify current rather than voltage.

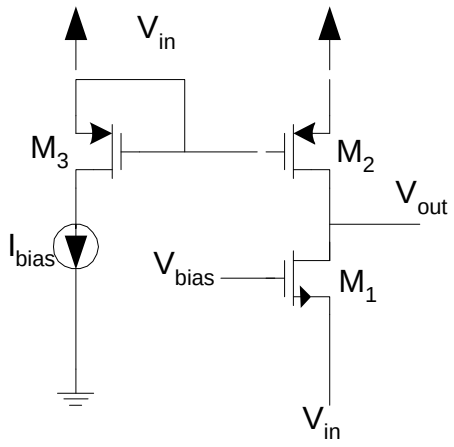

Fig. 2.9 A common gate amplifier with current mirror active load.

If we use straightforward small-signal analysis, when the impedance seen at V_{out} (in this case, the output impedance of the current mirror formed by M_2) is much less than r_{ds1}, the input impedance, $\mathbf{r_{out}}$, is found to be $1/g_{m1}$ at low frequencies. However, in integrated applications, the impedance seen at V_{out} is often on the same order of magnitude or even much greater than r_{ds1}. In this case, the input impedance at low frequencies can be considerable larger than $1/g_{m1}$. To see this result consider the small signal model shown in Fig. 2.10. In this model, the voltage-dependent current source that models the body effect has been included. Notice that $V_{gs1} = -V_{s1}$ and therefore the two current source can be combined into single current source as shown in Fig. 2.11.

This simplification is always possible for transistor that has a grounded gate in small-signal model, and considerably simplifies taking the body effect into account. Specifically, one can simply ignore the body effect for transistors with grounded gates, and then, after the analysis is complete, simply replace the constant g_{mi} with $g_{mi}+g_{si}$. However, for this example, include the body-effect parameter throughout the analysis.

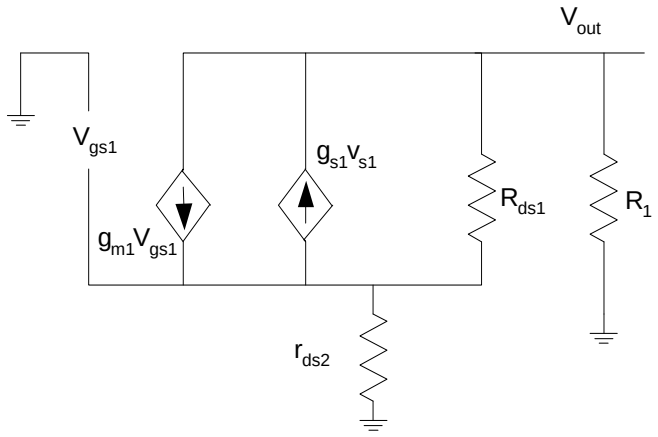

Fig. 2.10 A small signal model of the common gate amplifier at the low frequencies.

With $R_1 = g_{d3} \parallel \frac{1}{g_{m3}}$

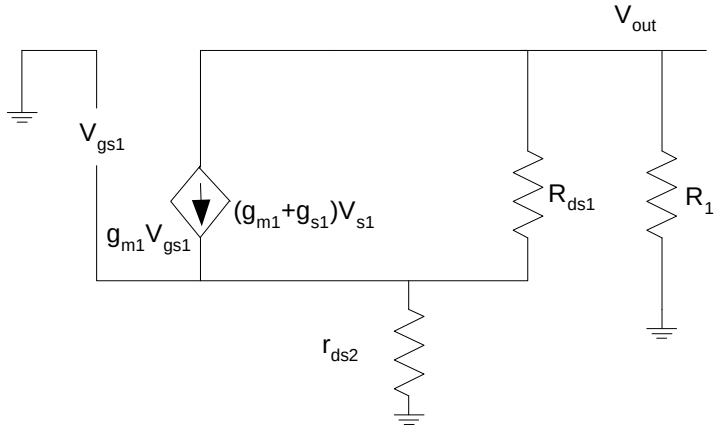

Fig. 2.11 A simplified small signal model of the common gate amplifier.

At node V_{out}, we have

$$V_{out}(G_1 + g_{ds1}) - V_{s1}g_{ds1} - (g_{m1} + g_{s1})V_{s1} = 0 \qquad (2.6)$$

Rearranging slightly, we have

$$\frac{V_{out}}{V_{s1}} = \frac{(g_{m1} + g_{s1} + g_{ds1})}{(G_1 + g_{ds1})} \tag{2.7}$$

Where it should be noted that this gain is equal to

$$\frac{g_{m1}}{G_1 + g_{ds1}} \tag{2.8}$$

The current going into the source of M_1 is given by

$$i_s = V_{s1}(g_{m1} + g_{s1} + g_{ds1}) - V_{out} g_{ds1} \tag{2.9}$$

Combining the above two equation to find the input admittance $Y_{in}=1/r_{in,}$ we have

$$Y_{IN} = \frac{I_s}{V_{s1}} = \frac{(g_{m1} + g_{s1} + g_{ds1})}{(1 + \frac{g_{ds1}}{G})} \approx \frac{g_{m1}}{(1 + \frac{g_{ds1}}{G_1})} \tag{2.10}$$

Alternatively, we have

$$r_{in} = \frac{1}{Y_{in}} \approx \frac{1}{g_{m1}}(1 + \frac{R_1}{R_{ds1}}) \tag{2.11}$$

With the p-channel active load is shown in Fig. 2.9, $R_l = r_{ds2}$. Since, in this case, R_l is approximately the same magnitude as r_{ds1}, the input impedance, r_{in}, is about $2/g_{m1}$ for low frequencies-twice as large as expected value of $1/g_{m1}$. This increased input

impedance must be taken into account in applications such as the transmission-lines transmissions. In some example, the current-mirror output impedance realized by M_2 is much larger than r_{ds1}, and so the input impedance for this common-gate amplifier is much larger than $1/g_{m1}$.

The attenuation form the input to the transistor source can be considerable for the common-gate amplifier when R_s is large. This attenuation is given by

$$\frac{V_{s1}}{V_{IN}} = \frac{G_s}{(G_s + Y_{in})}$$

(2.12)

With,

$$G_s = \frac{1}{R_s}$$

(2.13)

Using the admittance divider rule (this rule states that the gain is the ratio of the admittances connected between two nodes, divided by the sum of that admittance between the second node and the ground.

$$\frac{V_{s1}}{V_{IN}} = \frac{G_s}{(G_s + (\frac{g_{m1} + g_{s1} + g_{ds1}}{1 + \frac{g_{ds1}}{G_s}})} \qquad (2.14)$$

Using 2.7 and 2.14, we find that the overall dc gain is given by

$$A_v = \frac{V_{out}}{V_{in}} = \frac{G_s}{G_s + \frac{g_{m1}}{1 + \frac{g_{ds1}}{G_L}}} \left(\frac{g_{m1}}{G_L + g_{ds1}}\right) \tag{2.15}$$

2.6 Source Degenerated Current Mirrors

A current mirror can be realized using only two transistors, where the output impedance of this current source was seen to be r_{ds2}. To increase this output impedance, a source degenerated current mirror can be used, as shown in Fig. 2.12. The small signal model for this current mirror is shown in Fig. 2.13. Since no current flow into the gate, the gate voltage is 0V.

Note the current I_x sourced by the applied voltage source is equal to the current through the degeneration resistor, R_s. Therefore, we have

$$V_s = I_x R_s \tag{2.16}$$

Also, note that

$$V_{gs} = -v_s \tag{2.17}$$

Setting i_x equal to the totals current through $g_{m2}v_{gs}$ and r_{ds2} gives

$$i_x = g_{m2}v_{gs} + \frac{v_x - v_s}{r_{ds2}} \tag{2.18}$$

Substituting (2.16) and (2.17) into (2.18) gives

$$i_x = -i_x g_{m2} R_s + \frac{V_x - \frac{I_x R_s}{R_{ds2}}}{r_{ds2}} \tag{2.19}$$

Rearranging, we find the output impedance to be given by

$$r_{out} = \frac{v_x}{I_x} = r_{ds2}(1 + R_s(g_{m2} + g_{ds2})) \approx r_{ds2}(1 + R_s g_{m2}) \tag{2.20}$$

Where g_{ds2} is equal to $1/ r_{ds2}$, which is much less than g_{m2} (recall that $g_m = 1/r_s$). Thus, the output impedance has been increased by a factor approximately equal to $(1+R_{sd}g_{m2})$.

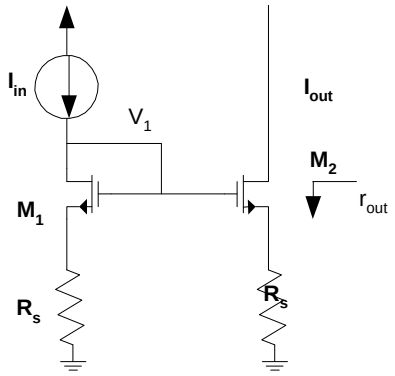

Fig. 2.12 A current mirror with source degeneration.

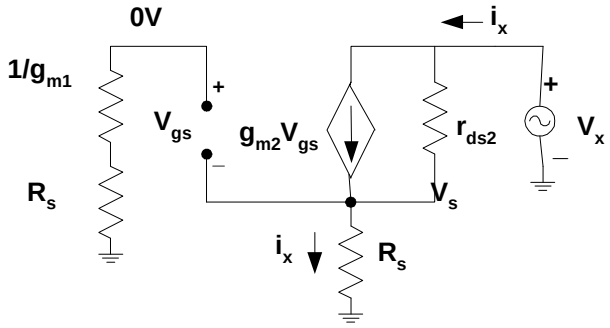

Fig. 2.13 A small signal model for the source degenerated current source.

The formula can often be applied to moderately complicated circuits to quickly estimate the impendence looking into a node. Such an example follows, in the derivation of the output impedance of cascode current mirrors.

It should be noted that the above derivation ignores the body effect of the transistor even though the source of the transistor is not connected to a small signal ground, the body effect can be taken into account by simply replacing g_{m2} in equation (2.20) with $g_{m2} + g_{s2}$. This substitution result in

$$r_{out} = \frac{v_x}{i_x} = r_{ds2}(1 + R_s(g_{m2} + g_{s2} + g_{ds2})) \approx r_{ds2}(1 + R_s(g_{m2} + g_{s2})) \quad (2.21)$$

2.7 Cascode Current Mirrors

A cascode current mirror is shown in Fig. 2.14. First, note that the output impedance looking into the drain of M_2 is simply r_{ds2} , which is seen using an analysis very similar to that, which was used for simple current mirror. Thus, the output impedance degeneration resistor or the value r_{ds2}. Making use of equation (2.20), and noting that M_4 is now the cascode4 transistor rather than M_2, we have

$$r_{out} = r_{ds4}(1 + R_s(g_{m4} + g_{s4} + g_{ds4})) \quad (2.22)$$

Where now $R_s = r_{ds2.}$ Therefore, the output impedance is given by

$$r_{out} = r_{ds4}(1 + r_{ds2}(g_{m4} + g_{s4} + g_{ds4})) \approx r_{ds4}(r_{ds2}g_{m4}) \quad (2.23)$$

Thus, the output impedance has been increased by a factor of $g_{m4}r_{ds2}$, which is an upper limit on the gain of a single transistor MOS gain stage, and might be a value between 10 and 100, depending on the transistor sizes and currents and the technology being used. This significant increase in output impedance can be instrumental in realizing single stage amplifier with large low frequency gains.

There is a disadvantage in using a cascode current mirror; it reduces the maximum output signal swings possible before transistors enter the triode region. To understand this reduction, recall that for an n channel transistor to be in the active region (also called the saturation or pinch off region) its drain source voltage must be greater than V_{eff}.

$$V_{eff} = V_{GS} - V_{tn} \tag{2.24}$$

By theory,

$$V_{eff} = \sqrt{\frac{2I_D}{\mu C_{ox}\frac{W}{L}}} \tag{2.25}$$

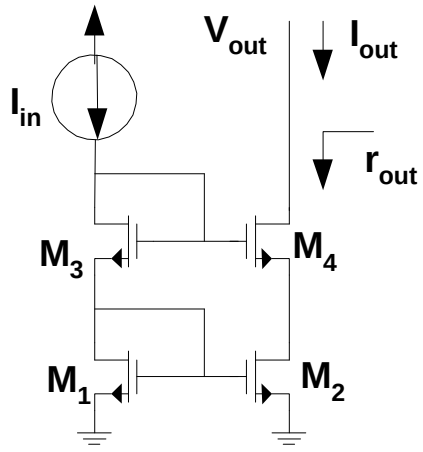

Fig. 2.14 A cascode current mirror.

If assume all transistors have the same sizes and currents, then they also all have the same V_{eff} and, therefore, the same gate source voltages. $V_{GSi} = V_{eff} + V_{tn}$. Also, from Fig. 2.14, we see that

$$V_{G3} = V_{GS1} + V_{GS3} = 2V_{eff} + 2V_{tn} \tag{2.26}$$

$$V_{DS2} = V_{G3} - V_{GS4} = V_{G3} - (V_{eff} + V_{tn}) = V_{eff} + V_{tn} \tag{2.27}$$

Thus, the drain source voltage of M_2, is larger that the minimum needed to place it at the edge of the active region. Specifically, the drain source voltage of M_2 is V_{tn} (about 0.8 V) greater that what is required. Since the smallest output voltage, **V_{D4},** can be without M_4 entering the triode region is given by $V_{DS2} + V_{eff}$, the minimum allowed voltage for the Vout is given by

$$V_{out} > V_{DS2} + V_{eff} = 2V_{eff} + V_{tn} \tag{2.28}$$

Which, again, V_{tn} greater than the minimum value of 2 V_{eff}. This loss of signal swing is a serious disadvantage when modern technologies are used that might have a maximum allowed power supply voltage as small as 3 V.

2.8 Wilson Current Mirror

Another commonly used current mirror is the Wilson current mirror, shown in Fig. 2.15.

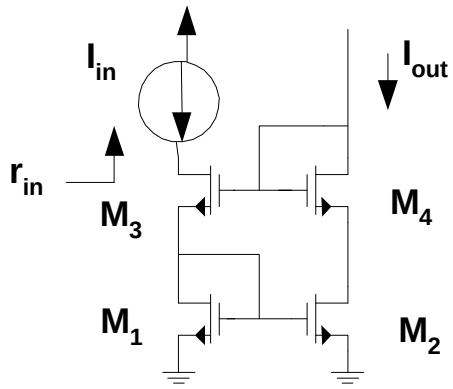

Fig. 2.15 A Wilson current mirror.

It is an example of using shunt series feedback to increase the output impedance. Basically, M_2 senses the output current and then mirror it to I_{D1}, which, in turn, is subtracted from the input current, I_{in}. Note that I_{D1} must precisely equal $I_{in;}$ otherwise the voltage at the gate of M_3, M_4 would either increases or decrease, and the negative feedback loop forces this equality. This feedback arrangement increases the output impedance by an amount equal to 1 plus the loop gain. Assuming all devices are matched, the output impedance without the feedback due to M_1, M_3 would be $2r_{ds4}$, taking into account that M_4 has source degeneration equal to $1/g_{m2}$, which is responsible for 2 factors. The loop gain is approximately given by

$$A_L \approx \frac{g_{m1}(r_{ds1} \square r_{in})}{2} \tag{2.29}$$

Where r_{in} is the input impedance of the biasing current source I_{in}. The factor of ½ is due to the voltage attenuation from the gate of M_4 to its source, caused by the

source degeneration of the diode connected M_2. Assuming r_{in} is approximately equal to r_{ds1}, and then the loop gain is given by

$$A_L \approx \frac{g_{m1} r_{ds1}}{4} \tag{2.30}$$

And the output impedance is therefore given by

$$r_{out} \approx \frac{r_{ds4} g_{m1} r_{ds1}}{2} \tag{2.31}$$

This is roughly one half the output impedance for that of a cascode current mirror. For the reason, the cascode current mirror is often preferred over the Wilson current mirror. In terms of output voltage swing. The minimum allowed voltage across the current mirror, before M_4 enters the triode region, is $\mathbf{2V_{eff} + V_{tn}}$, which is similar to that of the cascode current mirror.

Finally, it should be noted that M_3 is not required in the Wilson current mirror. It has been included to give M_1 and M_2 the same drain source bias voltage, and thus minimizes inaccuracies caused by the large signal output impedances of the transistors. Without this transistor, the output current would be slightly smaller than the input current because V_{DS1}. However, the small signal output impedance would remain the same.