Fabrication and Electrical Characterization of Silicon Bipolar Transistors in a 0.5-μm based BiCMOS Technology

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Abstract - Bipolar transistors are well known for its high current driving capability and current gains, while CMOS transistors are dominant in the integrated circuit market because of its low power consumption and small size advantage. The combination of both types of transistor on the same chip provides a high performance circuit with a high packing density. In this work 0.5-μm BiCMOS technology is fully utilized to realize silicon bipolar transistors with optimized performance. Preliminary electrical results are presented on bipolar transistors fabricated for the first time in Malaysia. Significant improvements in electrical device performance can be achieved by optimizing the emitter drive-in temperature and choice of annealing system.

I. Introduction

BiCMOS technology has emerged has a natural way of merging the best features of bipolar and CMOS devices into a design methodology which is more powerful than either of the two separate components by themselves [1]. The growing market of high frequency mixed-signal IC's ranging from telecommunication circuits, wireless products, high speed networked computing systems, high speed data acquisition systems, to global positioning system receivers, etc. has attracted many IC vendors to develop high performance mixed-signal BiCMOS technology [2]. BiCMOS is also used in advanced microprocessors [3],[4]. The idea here is to use CMOS for most of the circuits, but "sprinkle" in bipolars where they provide most performance leverage. This approach requires sophisticated design tools in order to make the most judicious use of the bipolar devices.

In this paper, preliminary electrical results of Si bipolar transistors obtained in a 0.5-μm based BiCMOS technology is presented. Electrical results in the form of Gummel plots and output characteristics are presented to demonstrate the high performance achievable. The effect of varying the emitter drive-in temperature on the electrical characteristics is also presented.

II. Experimental procedure

The *npn* bipolar transistors were fabricated in a 0.5-μm BiCMOS technology [5]. Table I is a summary of the process flow, where the first and third columns show processing steps for the formation of the CMOS and bipolar devices respectively. The second column shows processing steps that are common to both types of devices.

The starting material is p-type <100>, 10-20 Ω.cm, 150mm wafers. The base region was formed by implanting (4x) 4.0 x 10^{12} cm^{-2} Boron at 20KeV through 11nm of screen oxide. 230nm of spacer oxide was then deposited, followed by base annealing at 800°C for 30 minutes in dry N_2.

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The emitter window was formed by wet etching in BOE solution. Prior to 300nm undoped polysilicon deposition, all wafers were given a standard HF clean. The undoped polysilicon was deposited in a ASM 400 horizontal furnace at a temperature of 610^{0}C. The polysilicon was doped by implanting 4.0 x 10^{16} cm^{-2} Arsenic at 80KeV. After polysilicon patterning and PECVD oxide deposition, the wafers were given an emitter drive-in at either 930^{0}C for 3 min. (furnace anneal (FA)) or 970^{0}C for 1 min. (Rapid Thermal Annealling (RTA)), all in dry N_2. The RTA machine used was a SSTEACH 8200. The process was completed by contact hole formation and metallization.

Figure 1 shows a schematic diagram of the resulting 0.5-μm BiCMOS device architecture used in this work.

	BiCMOS	
CMOS		Bipolar
		1) 1st alignment mark 2) n+ Buried Collector. 3) p-epitaxial layer
	4) 2nd alignment mark	
5) n-well 6) p-well		
		7) n collector
	8) Well drive-in	
		9) n+ collector plug
	10) Active region 11) n-channel stop 12) LOCOS	
		13) Gate oxidation
14) n-channel doping 15) p-channel doping 16) Polysilicon gate 17) n- LDD		
		18) Base Formation
	19) Spacer Oxide deposition	
		20) Emitter window 21)Undoped PolySi dep 22) Arsenic implant 23) PolySi etching 24) Emitter drive-in
	25) Sidewall Spacer 26) S/D n+ diffusion	
27) P+ ion implant		
	28) S/D p+ diffusion	
29) B+ ion implant		
	30) Metallization	

Table 1: Summary of the 0.5-μm BiCMOS process flow.

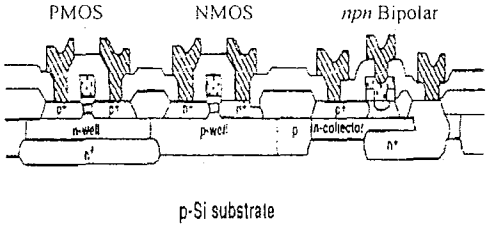
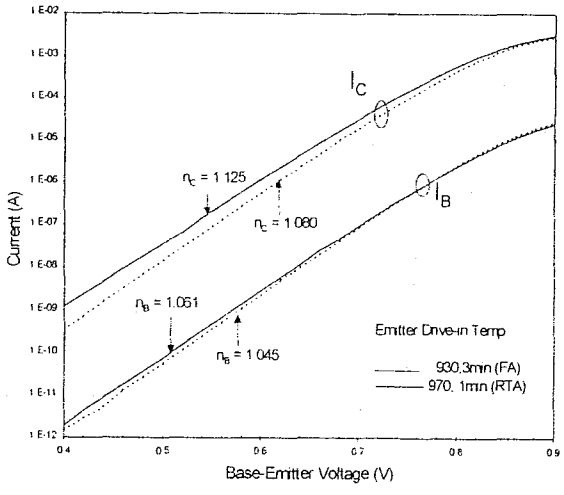


Figure 1: Schematic diagram of the 0.5-μm BiCMOS device architecture.

Electrical characterisation in the form of Gummel plots and output characteristics was performed on a Keithley Source Measuring Unit Model 236 attached to a personal computer at T=300K. Some of the electrical device parameters was extracted using a Hewlett-Packard DC Parametric Automatic Wafer Tester Model 4062.

III. Results and discussion

Figure 2 shows Gummel plots for the two types of transistor. It is observed that there is a slight difference in the base current, i.e the transistor given an emitter drive-in of 930^{0}C for 3 min. (FA) has a greater base current ideality factor, (n_B=1.061) compared to the 970^{0}C, 1 min. (RTA) transistor (n_B=1.045). However, there exists a large difference in the collector current. The transistor given an emitter drive-in at 930^{0}C for 3 min. (FA) exhibits a very non-ideal collector current (n_C=1.125) compared to the 970^{0}C, 1 min. (RTA) transistor (n_C=1.080); as shown by the extracted values of collector



current ideality factor, n_C.

Figure 2: Gummel plots for the two types of transistor. (V_{CB}=0V, T=300K, A_E=0.6μm x 6 μm).

The almost identical base current obtained for the two types of transistor can be explained by the identical polysilicon emitter processing. In particular, all transistors received

the same HF interface treatment prior to undoped polysilicon deposition. This results in almost identical polysilicon/silicon structure, hence producing almost similar base currents [6].

The non-ideal collector and base currents for the transistor given an emitter drive-in at 930^{0}C for 3 min. (FA), could be due to insufficient doping at the perimeter of the emitter. The results suggest that at a temperature of 930^{0}C, the Arsenic dopants in the polysilicon do not diffuse deep enough into the substrate hence producing a non-uniform emitter/base junction. This in turn causes the base and collector currents to become non-ideal [7]. Increasing the emitter drive-in temperature to 970^{0}C, 1 min. by RTA improves the ideality factor of the base and collector currents (as shown in figure 2): as a more uniform emitter/base junction is formed.

Figure 2 also shows that the collector current ideality factor, n_C is larger than that for the base current, n_B for both types of transistor. One possible reason for this phenomena to arise is that there could be possible leakage currents contributing towards the overall collector current, caused by defects at the base-collector junctions. The defects could have been induced during Boron implantation into the single-crystal silicon to form the base region [8], [9]. This will result in a non-ideal collector current. Further investigations is required to confirm this effect.

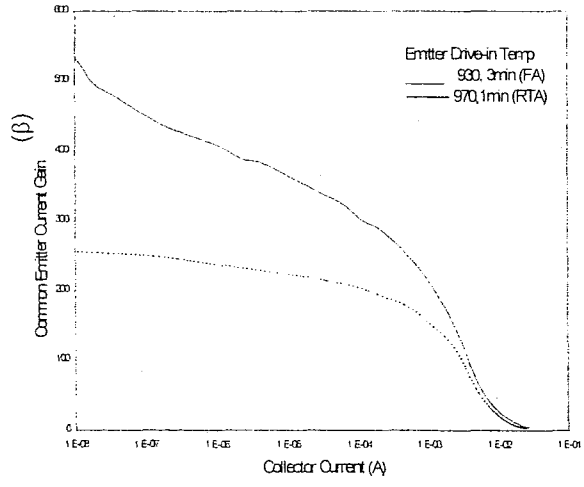


Figure 3: Current gain, β vs. I_C for the two types of transistor (T=300K).

Figure 3 shows the current gain, β as a function of collector current for the two types of transistor. It can be seen that β for the transistor given an emitter drive-in at 970^{0}C for 1 min. (RTA) is almost constant for the range of collector current shown, with a mean value of 250. As for the transistor given an emitter drive-in at 930^{0}C for 3 min. (FA), the β shows unstable characteristics over the collector current range. The increase in β with decreasing collector current can be explained by the very non-ideal collector current obtained.

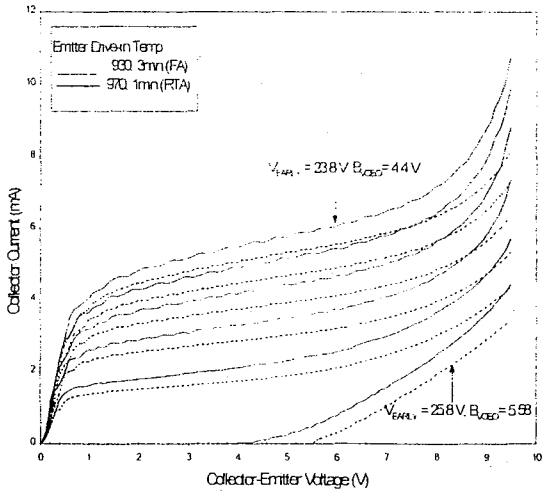


Figure 4: Output characteristics for the two types of transistor (ΔI_B=10μA, T=300K).

Figure 4 shows output characteristics (I_C vs. V_{CE}) for the two types of transistor. Again this figure clearly shows that an emitter drive-in at 970^{0}C, 1min. (RTA) produces a much flatter collector current and improves the output characteristics significantly. Higher breakdown and Early voltages are obtained compared to the transistor given an emitter drive-in at 930^{0}C, 3 min. (FA). This is of course desirable for both analog and digital applications [10].

Table 2 shows electrical device parameters of the two types of transistor extracted automatically using the DC parametric tester. It can be seen the transistor given an emitter drive-in at 970^{0}C, 1 min. (RTA) has better overall values compared with those of the transistor with an emitter drive-in at 930^{0}C, 3 min. (FA). Note that the emitter, base and collector

resistances obtained are acceptably low for high performance operation which indicate that the transistors fabricated are suitable for both digital and analog applications.

	930°C, 3 min. (FA)	970°C, 1 min. (RTA)
Emitter Resistance, R_E (Ω)	8.8	10.3
Collector Resistance, R_C (Ω)	81.8	79.4
Base Sheet Resistance, R_{BS} (kΩ/)	4.3	4.2
C-E breakdown voltage, BV_{CEO} (V)	6.27	6.50
C-B breakdown voltage, BV_{CBO} (V)	17.37	17.50
E-B breakdown voltage, BV_{EBO} (V)	5.38	5.25
Early Voltage, E_A (V)	29.0	30.6

Table 2: Extracted device parameters obtained for the two types of transistor (A_E=0.6μm x 10 μm, T=300K).

IV. Conclusions

Preliminary electrical results of silicon bipolar transistors obtained in a 0.5-um based BiCMOS technology has been presented. It is shown that significant improvements in device performance can be achieved by optimising the emitter drive-in temperature. In particular it has been demonstrated that an emitter drive-in at 970°C, 1min. by Rapid Thermal Annealing (RTA) compared to 930°C, 3min. by Furnace Annealing (FA) improves the electrical characteristics of the transistor. However, further investigations is required to identify the reason for the collector current ideality factor, n_C being larger than the base current ideality factor, n_B.

In summary it can be concluded that it is possible to obtain high performance silicon bipolar transistors suitable for both digital and analog applications in a 0.5-um based BiCMOS technology.

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