High Speed CMOS VCO For Advanced Communications

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by

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ABSTRAK

Peningkatan keperluan bagi komunikasi tanpa wayar dalam suara dan data telah memotivasikan kerja-kerja untuk meningkatkan tahap intregrasi dalam pemancar-penerima berfrekuensi radio (RF) baru-baru ini. Satu kaedah mengenai ini merupakan mencipta semua fungsi RF dalam satu teknologi CMOS kos rendah, supaya RF dan bahagian jalur-dasar boleh dimuatkan dalam satu cip tunggal. Ini seterusnya menjadikan, rekaan pengayun yang berfrekuensi tinggi, hinggaran fasa dan ketaran masa yang rendah, lebih rumit dengan menggunakan kaedah-kaedah yang biasa.

Dalam tesis ini, Pengayun CMOS yang dikawal secara digital dengan 16 bit telah diterangkan. Di sini, keupayaan asas suatu pengayun yang menggunakan skim masa negatif, skim masa arah kembar and skim register kawalan perkataan dengan sel masa pembeza telah dikaji. Kelebihan sel ini dalam mengeluarkan frekuensi operasi juga dikaji. Keputusan mencadangkan bahawa, frekuensi operasi pengayun jenis ini boleh diubah dengan mengubahkan masa bagi sel masa pembeza.

Untuk membuktikan konsep yang dicadangkan, suatu cip ujian bagi DVCO telah difabrikasikan di MOSIS dengan menggunakan teknologi CMOS HP0.5µ. Keputusan ujian bagi DVCO terkawal secara digital oleh 16 bit, memperlihatkan julat jalur dari 1.4 GHz hingga 2.1 GHz dengan frekuensi nominal pada 1.7 GHz. DVCO ini juga, memberikan kestabilan frekuensi di bawah keadaan perubahan suhu. Gandaan frekuensi terhadap perubahan pada daftar kawalan perkataan dalam bentuk mono pada beberapa MHz juga diperhatikan. Ini membolehkan kuncian frekuensi yang lebih jitu bagi

Gelung Fasa Terkunci Digital (DPLL). Ketaran yang paling buruk yang diperhatikan ialah 80 ps, yang mana merupakan lebih baik daripada kerja-kerja dilakukan sebelum ini. Simulasi pada pengayun ini juga menunjukkan bising fasa sebanyak -102 dBc/Hz pada ofset 10 KHz daripada frekuensi pembawa 1 GHz sambil melesapkan 150 mW kuasa pada bekalan 3.3 Volt.

ABSTRACT

The fast growing demand of wireless communications for voice and data has driven recent efforts to dramatically increase the level of integration in RF transceivers. One approach to this challenge is to implement all the RF functions in the low-cost CMOS technology, so that RF and baseband sections can be combined in a single chip. This in turn dictates an integrated CMOS implementation of the local oscillators with the same or even better frequency, phase noise and jitter performance than its discrete counterpart, generally a difficult task using conventional approaches with the available low-Q integrated inductors.

In this thesis, a 16-bit digitally controlled CMOS voltage controlled oscillator (DVCO) is described. Here, the fundamental performance limit of a local oscillator design using negative skewed delay scheme, dual delay path scheme and control word register scheme with differential delay cell as base is investigated. The distinctive frequency operation pattern based on the source-coupled differential CMOS delay cell implementation is analyzed. The result suggests that operating frequency, can be controlled by varying the delay of differential delay cells.

To demonstrate the proposed concept, some prototypes of this DVCO implemented in MOSIS HP0.5µ CMOS process were fabricated. Experimental results of a 16 Bit CWR controlled 5-stage DVCO achieved controllable frequency range of 1.4 – 2.1 GHz with a linear/quasi-linear range of around 1.7 GHz. This CMOS DVCO design provides improved frequency stability under thermal fluctuations. Monotone frequency gain (frequency vs control-word transfer function) with fine stepping (tuning) in several MHz was verified. This augurs the prospect of accurate frequency lock in a

CMOS all digital PLL (ADPLL) application in digital VLSI communication systems. Worst case jitter due to digital control transitions at pathological control-word boundaries for the CMOS DVCO was observed to be less than 80 ps, which is lower than most of the previously proposed VCOs. Simulation on this oscillator also achieves -102 dBc/Hz phase noise at 10 KHz offset from carrier frequency of 1 GHz while dissipating 150 mW from a 3.3 Volt supply.

To

My Wife

Hithayarani S Kandavelu

And Son

Karthigeyan R Chakaravarty

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Acknowledgements

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My acknowledgements would not be complete without expressing my gratitude towards God. I feel very fortunate to come to know Him during my undergraduate and graduate years at USM and have continually been blessed by His endless love ever since. He is the true shepherd of my life.

Chapter 1

Introduction

1.0 Motivation

In most modern communication systems timing information, in the form of clock or oscillator signals, plays a critical role in system performance. In many of these applications, clock signals are used to drive mixers or sampling circuits in which variations in the sampling instant, both random and systematic, are important performance parameters. For some systems, the timing information is provided through a local crystal oscillator, or an externally supplied timing source. In this case, the task of minimizing timing error amounts to minimizing the noise introduced through the distribution and buffering of clocks in the system. In many other applications, however, a local version of the clock is required at a different frequency or phase than the reference, in which case a phase-locked-loop (PLL), or similar circuit, is often employed to create the required signal. For systems such as these, minimizing timing error requires careful attention to all of the sources of noise in the PLL, and their interactions in the PLL system as a whole. Applications which require phase-locked-loops are often the most challenging, since attaining high performance levels often contributes considerable expense and complexity to the system. Furthermore, for any given application, there are a number of different timing error sources which may be important to the system. Systems which employ PLLs include applications such as optical communication systems, disk drive systems, and local area networks, where a PLL is used for clock and data recovery.

Other systems include radio transmitters and receivers which use phase-locked-loops for frequency synthesis. And, in complex digital systems such as microprocessors, network routers, and digital signal processors, the clocks used at various points in the system are often synchronized through a phase-locked or delay-locked loop to minimize clock skew. There are several types of timing error, or uncertainty, that are important in communication systems. The first is random variations in the sampling phase of a signal, called timing jitter, or in the frequency domain, phase noise. This is often due to thermal noise and 1/f noise in the active and passive devices which make up the components of the PLL system, particularly the voltage-controlled-oscillator (VCO).

In addition, systematic variations in sampling phase can occur due to injection of signals from other parts of the circuit causing AC variation in the phase, called spurious tones. Sudden changes in the supply or substrate can also cause frequency offsets and phase drift. These sources of noise can often be minimized through advanced circuit techniques. The effect of device thermal noise, however, is fundamental, and in applications such as RF frequency synthesis, it often sets the performance limit for the system. In most RF frequency synthesis applications, a low phase noise oscillator is employed for optimal performance. This implementation usually requires an external resonator, such as a varactor tuned LC-tank, with a high quality factor ("Q"). In an increasing number of applications, however, a fully-monolithic solution to the VCO is desired. Already present in clock synthesis and clock recovery applications, on-chip ring-oscillators and voltage-controlled-delay chains have resulted in a reduced cost and complexity in many systems. But the phase noise requirements of radio receiver applications is generally more restrictive, raising questions as to their applicability for RF frequency synthesis. This dissertation describes the fundamental, thermal noise-

induced performance limits in ring-oscillator VCO's and their applicability to RF frequency synthesis. Design techniques for low phase noise and low timing jitter circuits are described, that are useful to all applications. The key trade-offs available to the designer at the buffer/delay cell level, the oscillator level, and the phase-locked loop level are all explored. Furthermore, this dissertation describes the design of frequency synthesizers for high integration radio receivers, where a monolithic implementation to the VCO is desired. Comparisons are made with other implementations, including implementations with onchip LC-tuned circuits.

1.1 Objectives

The main objectives of this project is:

- To design a high speed, preferably 1GHz atleast, voltage controlled oscillator (VCO).
- To design a wider range of operating frequency, atleast 500Mhz margin, for the VCO to enable it being used in multiple applications.
- To design multi-bit digital controllability for the VCO in which the digital control tunes the oscillator to the desired frequency.
- Improved Ring Oscillator Techniques

1.2 Contributions

The key contributions of this work are:

1. An analytical method for analyzing thermal noise-induced timing jitter in delay stages, taking into account time varying noise sources and interstage

amplification. With this technique the jitter performance of CMOS differential, resistively loaded, source-coupled delay cells has been tied to delay cell design parameters and shown to have an inverse dependence on the square root of the load capacitance at the output of each inverter stage and an inverse dependence on the gate-to-source bias above threshold of the source coupled devices in the balanced state.

2. A very deep analysis of Negative Skewed Delay Scheme, Dual Delay Path Scheme and Control Word Register Scheme and how they result into higher operating frequency and wider range of operating frequency.

3. The design and implementation of ring oscillator VCOs using the above mentioned techniques has been described, including issues such as coarse and fine tuning, maximum frequency of operation, and design of high frequency VCOs.

4. Experimental and T-Spice simulation results for a ring-oscillator test array fabricated in a 0.5μ, double-poly double-metal CMOS process are described, which show good agreement with the analytical predictions for the frequency response.

1.3 Thesis Organization

In Chapter 2 the analysis of timing jitter and phase noise is initiated with a look at thermal noise induced timing jitter in inverter delay cells. Expressions for timing jitter

and phase noise at several levels of system implementation will be derived in terms of basic delay cell and oscillator design parameters. In Chapter 3 the negative skew delay, dual delay path and control Word registers schemes are analyzed for a high speed , low-jitter and low-phase VCO design. In the following chapter, Chapter 4, the circuit implementation of ring-oscillators and delay cells will be described. And in Chapter 5 simulation results will be provided along with the layout techniques and the experimental results. The thesis concludes with Chapter 6.

Chapter 2

Jitter and Phase Noise in CMOS Ring Oscillators

2.0 Introduction

In this chapter, the thermal noise induced jitter contribution of an individual delay cell was determined in terms of delay cell design parameters. In this Chapter, we will complete the picture by looking at the implications for the design of low-jitter and low-phase-noise VCOs using inverter delay cells. Also considered will be the phase noise and timing jitter of buffers, or inverter delay chains, not configured in a ring.

2.1 Timing Jitter in Ring Oscillator VCOs

In this section the cycle-to-cycle jitter of a ring oscillator VCO will be determined from the thermal noise induced jitter in the inverter cells that it is composed of. The cycle-to-cycle jitter of a VCO is also useful for determining the steady state output jitter in a PLL and for determining the phase noise spectrum of an oscillator.

Suppose the goal is to design a ring-oscillator with a fixed period, T_0, and minimal timing jitter. For an N-stage configuration the period of the oscillator is given by

$$T_0 = 2N \cdot t_d \qquad \text{Eq (2.1)}$$

Where t_d is delay through each stage. If the noise sources in successive stages are independent then the total jitter variance for once cycle of oscillation is, similarly

$$\overline{\Delta t_{vco}}^2 = 2N \cdot \overline{\Delta t_d}^2 \qquad \text{Eq (2.2)}$$

since the jitter variances of each stage will add. In fact, for multiple cycles of oscillation, the total timing error variance relative to a reference transition at time t=0 is given by

$$\overline{\Delta t_{tot}}^2(t) = \frac{\overline{\Delta t_{vco}}^2}{T_0} \cdot t \qquad \text{Eq (2.3)}$$

There is an important assumption underlying this equation, however. This equation assumes that not only are the noise sources independent between delay stages, but the noise sources themselves have a "white" spectrum so that the noise in different periods of oscillation is uncorrelated. When 1/f noise is considered, this is not true. In that case the linear accumulation of timing jitter in Eq (2.3) will change to a different slope. This is described in [1]. However, for time differences smaller than the reciprocal of the 1/f noise corner frequency, the result in Eq (2.3) holds.

In the work presented here we are primarily interested in ring-oscillators as VCO's for use in phase-locked-loops. In that case, errors in the VCO output are corrected for frequencies within the bandwidth of the loop. For reasonable 1/f noise corner frequencies and reasonable loop bandwidths, the impact of 1/f noise on the

output of the PLL is not significant. Therefore the focus of this section will be devoted to the impact of device thermal noise.

The cycle-to-cycle jitter of a VCO can therefore be found by substituting the result for the jitter from [2] which yields,

$$\overline{\Delta t_{vco}}^2 \cong 2N \cdot \frac{kTC_L}{2(I_{SS})^2} \cdot (a_v \xi)^2 \qquad \text{Eq (2.4)}$$

where k is the Boltzmann Constant (1.4×10^{-23} JK^{-1}), T is temperature is degrees Kelvin, C_L is the load capacitance of the circuit, a_v is the gain, ξ is the noise contribution factor, I_{SS} is the supply to substrate current and V_{SW} is the voltage swing. The Eq(2.4) is problematic, however, since it depends on the number of delay stages, making it hard to separate this issue from other design parameters when trying to minimize timing jitter. A much better equation results by making the substitution of $2N=T_0/t_d$ from equation Eq (2.1). In that case

$$\overline{\Delta t_{vco}}^2 \cong T_0\left(\frac{I_{SS}}{C_L V_{SW}}\right)\times \frac{kTC_L}{2(I_{SS})^2} \cdot (a_v \xi)^2 \qquad \text{Eq (2.5)}$$

which simplifies to

$$\overline{\Delta t_{vco}}^2 \cong \frac{kT}{I_{SS}} \cdot \frac{a_v \xi^2}{2(V_{GS}-V_T)} \cdot T_0 \qquad \text{Eq (2.6)}$$

The last step employs the approximation for the inter-stage gain, $a_v \cong V_{SW}/(V_{GS}-V_T)$, described in [2].

Equation Eq (2.6) is a very useful result. The cycle-to-cycle jitter of the VCO is now expressed in terms of the period of the oscillator being designed, rather than in terms of the number of stages. The rest of this section will be devoted to understanding the implications of this result which answers a number of important questions regarding low-jitter VCO design. Along the way some common misconceptions about ring-oscillator design will be discussed, and some fallacies dispelled.

To design for low jitter, equation Eq (2.6) suggests that the (V_{GS}-V_T) bias point of the NMOS differential pair transistors in the inverter cells should be made as large as possible. It was also shown there, that (V_{GS}-V_T) was constrained by voltage gain and voltage swing considerations. In general, (V_{GS}-V_T) is chosen as large as possible while maintaining an inter-stage gain, $a_v \cong V_{SW}/(V_{GS}-V_T)$, greater than one, by a sufficient safety margin.

Also suggested by equation Eq (2.6) is that the gain should be minimized, as well as the noise contribution factor, ξ. The conclusion is that a_v and ξ where relatively insensitive to the circuit design parameters that could be freely changed in a design, and therefore less important in optimizing for low timing jitter.

2.1.1 Timing Jitter as a Function of Power Consumption

The main result of equation Eq (2.6) is that with everything else fixed, the timing jitter variance improves with an increase in supply current. Since power consumption depends on the quiescent current level, this implies, at least for the class of circuits considered here, a direct trade-off between power consumption and timing jitter. If the tail current, I_{SS}, per stage is increased, then the jitter variance of the ring oscillator will decrease proportionally. In order to keep $(V_{GS}-V_T)$ constant as well as the delay per stage, this implies scaling the widths of the differential pair and load transistors along with the current. Here we see the result of these implications for the minimization of jitter in the VCO. Therefore, the timing jitter variance can be improved freely for a ring oscillator with an increase in power consumption, and a corresponding increase in the active circuit area of the ring. This observation is approximately true over a wide range of currents.

Increasing the current by a factor of two will improve the r.m.s. jitter by a factor of the square root of 3[2]. Increasing the current by a decade (10 times), will reduce the jitter variance by 10 dB. Interestingly, the implications of equations Eq (2.6) to *first order* do not change with changes in supply voltage and technology scaling. If $(V_{GS}-V_T)$ is proportional to the supply voltage, then for a constant jitter, decreasing the supply voltage requires increasing the supply current by the same amount. This means that the power consumption stays the same. Scaling of the gate length gives access to higher speeds, but equation Eq (2.6) states that for a fixed period, T_0, the jitter is inversely proportional to the current itself, and does not depend directly on the gate length. The effects of velocity saturation for very short gate lengths will not have a major impact on this equation either since no form for the current equation has been assumed.

2.1.2 Timing Jitter as a Function of Configuration

Another interesting result of equation Eq (2.6) is that the jitter variance of the ring oscillator depends on the period of the oscillator itself, and not (to first order) on the exact configuration. Consider the following example. Each of the oscillators in Figure 2.1 have the same output period. The first is a six stage differential inverter ring with time delay, t_d, per stage (the ring is configured with an odd number of inversions so that it will oscillate). The second oscillator is a smaller, three-stage ring assumed to have delay cells with the same tail current, I_{SS}, and $(V_{GS}-V_T)$, but with a divider following it so that it has the same output period. The jitter in the divider will not effect the phase of the signal being passed around the ring and can therefore be neglected in this example. Divider jitter is similar to jitter in buffers. It effects the phase of the output, but does not effect period of VCO. The third oscillator is also configured as a three stage ring, but extra load capacitance has been added to the output of each stage so that they have a delay of twice that in the other two oscillators .

Therefore this ring also has the same period. Since each of the oscillators in Figure 2.1 has the same period, and each is assumed to have delay cells with same tail current, I_{SS}, and $(V_{GS}-V_T)$, equation Eq (2.6) predicts that they will all have the same output timing jitter. This is an important result. It says that there is no inherent advantage to using a longer ring-oscillator, unless multiple, parallel phases with closer spacing are needed. In fact, oscillators (b) and (c) are superior from the perspective of power consumption. For a given power specification a three-stage ring can use twice the current per stage and therefore have an jitter variance that is lower by a factor of two.

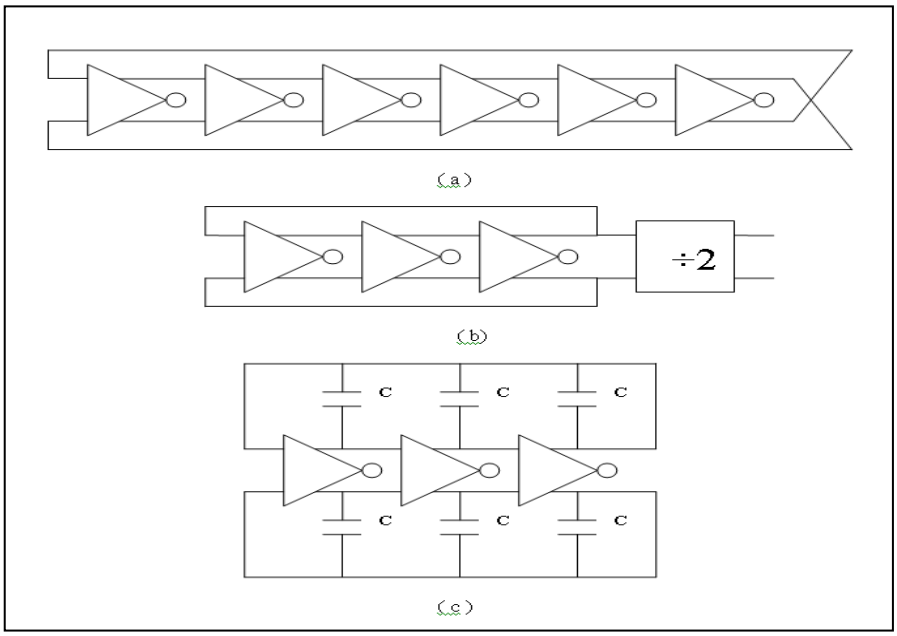

Figure 2.1 Oscillator Configurations with same output period

The decision between the divider approach in (b) and the slower delay cell approach in (c) depends on the application. The divider power can often be kept small compared to that in the ring, and the addition of a divider adds a fixed amount of additional area. For frequencies that are much slower than the natural frequency of the three stage ring, it is often easier to cascade dividers to attain a lower frequency than to continue to scale up the load capacitance in between stages. For frequencies closer to the natural frequency of a three stage ring, however, the approach in (c) is often the most straightforward.

The idea of lowering the time-delay per stage by lowering the slew-rate of the output transition as in configuration (c) goes against the grain of conventional thinking. This situation will be reconciled shortly, in the section on common misconceptions in low-jitter VCO design.

2.1.3 Timing Jitter as a Function of Output Period

The final implications of equation Eq (2.6) involve the timing jitter performance as a function of the output period, T_0, of the ring-oscillator being designed. This equation predicts that the jitter variance is actually larger for lower-frequency designs. However, a more useful Figure of merit in some applications in the normalized timing jitter. If the jitter of the VCO is normalized to the output period, then we find:

$$\frac{\Delta t_{vco\text{-}rms}}{T_0} = \sqrt{\frac{kT}{I_{SS}} \cdot \frac{a_v \xi^2}{2(V_{GS} - V_T)} \cdot \frac{1}{T_0}} \qquad \text{Eq (2.7)}$$

This equation shows that the VCO timing error as a percentage of the overall output period improves for lower frequency designs and increases for higher frequencies. This implies that higher frequency oscillators will have more timing jitter for the same power consumption, and suggests that thermal noise induced timing jitter considerations are increasingly important with higher frequency designs.

2.1.4 Common Misconceptions in Low-Jitter VCO Design

There are a few common misconceptions in low-jitter VCO and buffer design that are addressed by the result in equation Eq (2.6). The first pertains to the role of the inter-stage gain in determining jitter and the second to the optimal number of stages for a ring.

The basic path from voltage noise to timing jitter through the first crossing approximation was illustrated. The output timing jitter was said to be related to the voltage noise through the slope of the output waveform (as a function of time) at the nominal threshold crossing time. A common misconception is to confuse the DC transfer characteristic of an inverter delay cell with its slewing behavior. For a DC sweep at the input of an inverter cell, a higher gain inverter will have a differential output that responds with a sharper slope. Does an improvement in slope mean an improvement in timing jitter? The answer is "not-necessarily" since the slope of the output transient is related to the slew-rate of the inverter and not the DC gain.

For inverter delay cells with reasonable gains ($a_v \geq 1$), the slope of the output transient is given by the average slew rate. For the class of circuits considered here, this is approximately I_{SS}/C_L . While it is true that an inverter with a higher gain can switch current from one side of the delay cell to the other more sharply in response to a changing input, it is also true that a lower gain cell will begin switching the current sooner, since its output characteristic is in its active region (not saturated) for a wider range of input voltages. The end result is that, with the exception of very low gain cells ($a_v \leq 1$), which are not useful in general anyway, the effects of small-signal gain on the slope of the output transient and on the time-delay per stage are second-order.

The small-signal gain does effect the timing jitter, however, through inter-stage amplification. A higher gain per stage means that there is more amplification of noise between stages. This is the reason for the a_v term in the numerator of equation Eq (2.6). Note that the proportionality to a_v seen in the expression for voltage noise is stronger, but one factor of a_v is used when simplifying the expression for the normalized timing

jitter, allowing the result to be expressed in terms of (V_{GS}-V_T) rather than V_{SW} (swing voltage). Also effected by the inter-stage gain is the noise contribution factor. For a given output resistance, higher gain means a larger g_m for the NMOS devices, and hence a higher noise contribution relative to the PMOS.

Therefore, contrary to one line of thinking, the timing jitter of a VCO is not improved by increasing the gain per stage, but is actually improved through inverter cells with a lower small-signal gain, reducing the inter-stage amplification and the relative NMOS device noise contributions.

The second misconception which is common in low-jitter VCO design is that the timing jitter improves for ring-oscillators with a higher number of stages. In the section on jitter as a function of configuration, however, a different claim was made. Namely, that VCO timing jitter for a fixed output period was independent of the number or stages used. And furthermore, from a power consumptions perspective, VCOs with fewer stages are preferred.

The reasoning behind using a larger number of stages stems from the following chain of ideas. First, the jitter variance per cycle for a ring oscillator with N stages and output period is given by Eq (2.1) and Eq (2.2) respectively which have been reproduced below for convinience.

$$\overline{\Delta t_{VCO}}^2 = 2N \cdot \overline{\Delta t_d}^2 \qquad \text{Eq (2.8)}$$

$$T_0 = 2N \cdot t_d \qquad \text{Eq (2.9)}$$

Next, consider doubling the number of stages. If the output period is to be preserved, then the slew-rate per stage has to double so that the time delay is half of its original value. This means that the jitter variance per delay stage which is proportional to the output voltage noise divided by the slew-rate squared decreases by a factor of four. The jitter variance for the ring oscillator is now given by

$$\overline{\Delta t_{VCO-2}}^2 = 2(2N) \cdot \frac{\overline{\Delta t_d}^2}{4} = \frac{1}{2} \cdot 2N \cdot \overline{\Delta t_d}^2 \qquad \text{Eq (2.10)}$$

which is an improvement by a factor of two. The r.m.s. jitter for the VCO improves by $\sqrt{2}$.

This chain of reasoning overlooks a critical point, however. Namely, when changing the slew-rate of the inverters the output bandwidth changes as well. If the time delay per stage is doubled, by reducing CL at the output, or increasing the current per stage (note that $R_L=V_{SW}/I_{SS}$), then the noise bandwidth is doubled as well. The timing jitter variance per stage, therefore will increase by a factor of two due to noise bandwidth, and decrease by a factor of four due to the slew-rate enhancement. The net change is an improvement by a factor of two, and the total output jitter is the same as before.

$$\overline{\Delta t_{VCO-2}}^2 = 2(2N) \cdot \frac{\overline{\Delta t_d}^2}{2} = 2N \cdot \overline{\Delta t_d}^2 \qquad \text{Eq (2.11)}$$

2.2 Phase Noise

In the previous section the cycle-to-cycle jitter of a ring-oscillator VCO was determined from the thermal noise sources in the devices which make up the ring. Useful relationships have been established between jitter performance and delay cell design parameters. In this section the attention turns back to phase noise and to finding a link from VCO timing jitter to the frequency domain. The goal of this section is to derive an expression for VCO phase noise in terms of the basic design parameters of the VCO. Phase noise was measured in dBc/Hz at an offset frequency, f_m, away from the carrier. This measure was a comparison of the power in a 1-hz bandwidth at that off-f_m set to the total power of the carrier. In this case the phase noise is represented with a single sideband instead of a double, with the x-axis being the offset frequency itself.

This is a plot of the spectral density of phase fluctuations, as opposed to the spectrum of an output sinusoid with a given phase noise, which is the plot in Figure 2.2(a).

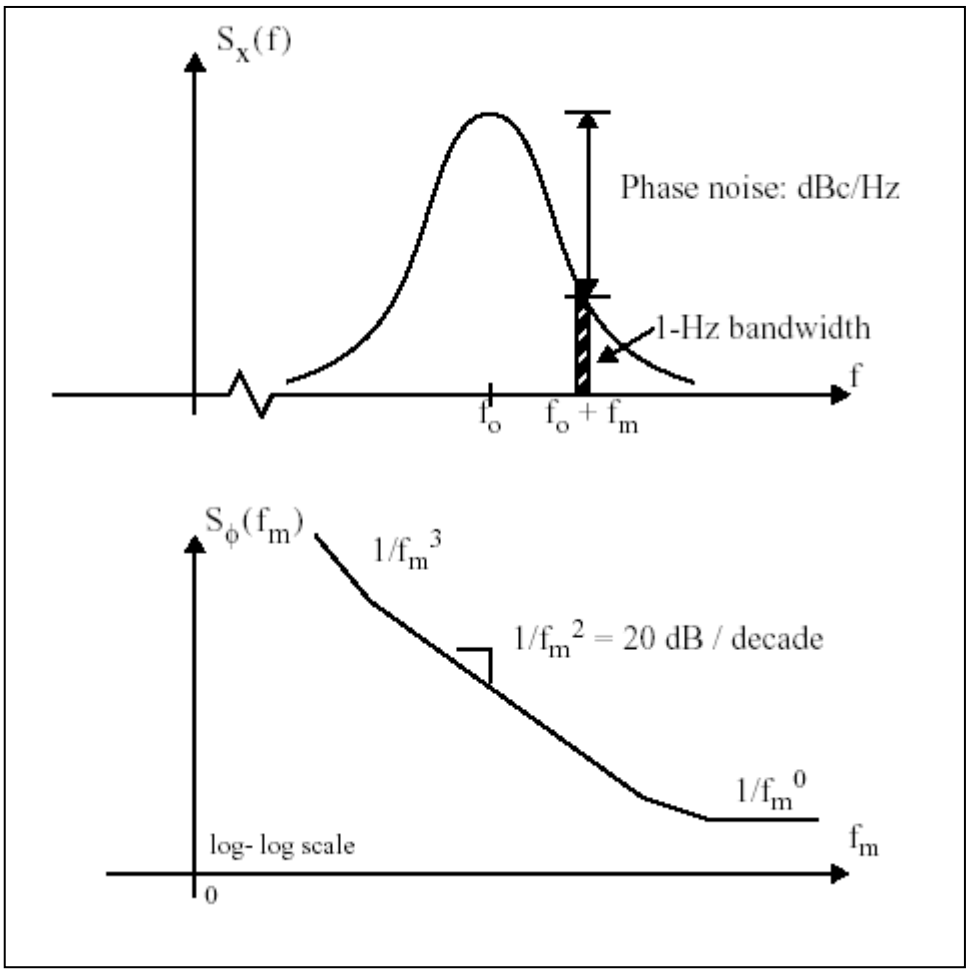

Figure 2.2 Oscillator Phase Noise
(a) power spectrum of oscillator
(b) phase fluctuation power spectral density

This distinction is worth noting here, since the analysis will focus on deriving phase noise from phase and frequency fluctuations directly, rather than the output spectrum. Consider a signal

$$X(t) = A\cos(2\pi f_o t + \theta(t)) \qquad \text{Eq (2.12)}$$

If $\theta(t)$ is a noisy, random signal then X(t) is said to exhibit phase noise. The power spectrum of the signal X(t) in such a case, looks like $S_x(f)$ in Figure 2.2(a). The sidebands of the output signals power spectrum are related to $\theta(t)$. Another perspective on the noise process, however, is to look at the spectral representation of $\theta(t)$ directly. This is called the spectral density of phase fluctuations, $S_\theta(f)$, and is the representation pictured in Figure 2.2(b). Still other useful characterizations of the signal in (E2.12) exist, including the spectral density of frequency fluctuations and normalized frequency fluctuations. The instantaneous frequency of the signal in (E2.12) is given by the time derivative of the cosine argument.

$$f_{inst}(t) = f_o + \frac{d\theta}{dt} \qquad \text{Eq (2.13)}$$

The difference, $\Delta f = f_{inst} - f_o$ is called the spectral density of frequency fluctuations. Similarly, the spectrum of $y = \Delta f / f_o$ is called the spectral density of normalized frequency fluctuations. Relationships between each of these expressions are given in [3] and can be summarized by

$$S_\theta(f) = \left(\frac{1}{f_m}\right)^2 S_{\Delta f}(f) = \left(\frac{f_o}{f_m}\right)^2 S_y(f) \qquad \text{Eq (2.14)}$$

For frequencies far enough away from carrier, the phase noise in dBc/Hz measured from the power spectrum of X in Figure 2.2(a), is the same as the spectral density of phase fluctuations in rad^2 / Hz shown in 2.2(b). This is discussed in [3].

2.3.1 Phase Noise / Timing Jitter Relationship

In this section a link is sought from cycle-to-cycle timing jitter in a VCO to its output phase noise spectrum. Consider a VCO with nominal period T_0, and with a timing error accompanying each period that is gaussian, with zero mean and variance $\overline{\Delta t_{vco}}^2$. If this timing error is expressed in terms of phase ($\Delta\phi = 2\pi\Delta t / T_0$), then the variance of the phase error per cycle of oscillation is given by

$$\sigma_\phi^2 = (2\pi)^2\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \qquad \text{Eq (2.15)}$$

The total phase error as a function of time is the sum of all past phase errors. For the thermal noise sources considered here, the noise contributions are white and there is no correlation from cycle-to-cycle. With independent timing errors for each cycle of oscillation, the total phase error is a random variable which exhibits a random walk. The phase noise of the output spectrum can be modeled as a Wiener process and will be analyzed similarly to a laser phase noise analysis performed by Barry & Lee in [4]. A second approach to this analysis can also be taken which yields the same result.

A Wiener process is a one in which the variance of a random variable increases linearly with time. This is a good model for independent cycle-to-cycle timing errors in a VCO. Written as a continuous signal the phase error is given by

$$\phi(t) = \int_0^t \phi'(t)dt \qquad \text{Eq (2.16)}$$

where the time derivative, or instantaneous frequency error $\phi'(t)$ is considered to be a zero mean white gaussian process with power spectral density

$$S_{\phi'}(\omega) = 2\pi\Delta\vartheta \qquad \text{Eq (2.17)}$$

Since phase is the integral of frequency, the power spectral densities of phase and frequency fluctuations are related by a factor of $1/\omega^2$.

$$S_{\phi}(\omega) = \frac{1}{\omega^2}(2\pi\Delta\vartheta) \qquad \text{Eq (2.18)}$$

The term is called the "line-width" of the spectrum. And is the general specification for phase noise in lasers. In this analysis, this term will be related back to the cycle-to-cycle jitter σ_T^2.

The phase error accumulated between any two points in time can be denoted by the random variable

$$\Phi(t1, t2) \equiv \phi(t1) - \phi(t2) = \int_{t2}^{t1} \phi'(u)du \qquad \text{Eq (2.19)}$$

The variance of this random variable is shown in [4] to be

$$\sigma_{\Phi}^{2} = E\left[\int_{t2}^{t1}\int_{t2}^{t1}\phi'(u)\phi'(v)dudv\right] \qquad \text{Eq (2.20)}$$

$$\sigma_{\Phi}^{2} = 2\pi\Delta\vartheta\int_{t2}^{t1}\int_{t2}^{t1}\delta(u-v)dudv = 2\pi\Delta\vartheta|t1-t2| \qquad \text{Eq (2.21)}$$

The variance of the phase error, therefore increases linearly with time. However, we also know that for a separation of one period of oscillation, t_1-t_2 = T_o, the variance of the phase error is σ_T^2 , as in equation Eq (2.15).

$$E\{|\phi(t)|^2\} = (2\pi)^2\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \qquad \text{Eq (2.22)}$$

therefore

$$(2\pi)^2\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 = 2\pi\Delta\vartheta T_0 \qquad \text{Eq (2.23)}$$

and from Eq (2.18), the phase noise power spectral density is given by

$$S_{\phi}(\omega) = \frac{1}{\omega^2}(2\pi\Delta\vartheta) = 2\pi\frac{\omega_0}{\omega^2}\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \qquad \text{Eq (2.24)}$$

Expressed in terms of frequency, f, (using $\omega = 2\pi f$) this result is

$$S_{\phi}(f) = \frac{f_0}{f^2}\left(\frac{\Delta t_{vco-rms}}{T_0}\right)^2 \qquad \text{Eq (2.25)}$$

Plotted on a log-log scale, the phase noise as a function of offset frequency looks like the graph in Figure 2.3. The absolute height depends on the center frequency of oscillation, f_0 , and the ratio of the timing error per cycle of oscillation to the oscillation period. This means that for a fixed percentage jitter ($\Delta t_{vco-rms} / T_0$), higher frequencies of oscillation have inherently higher phase noise at a given offset frequency.

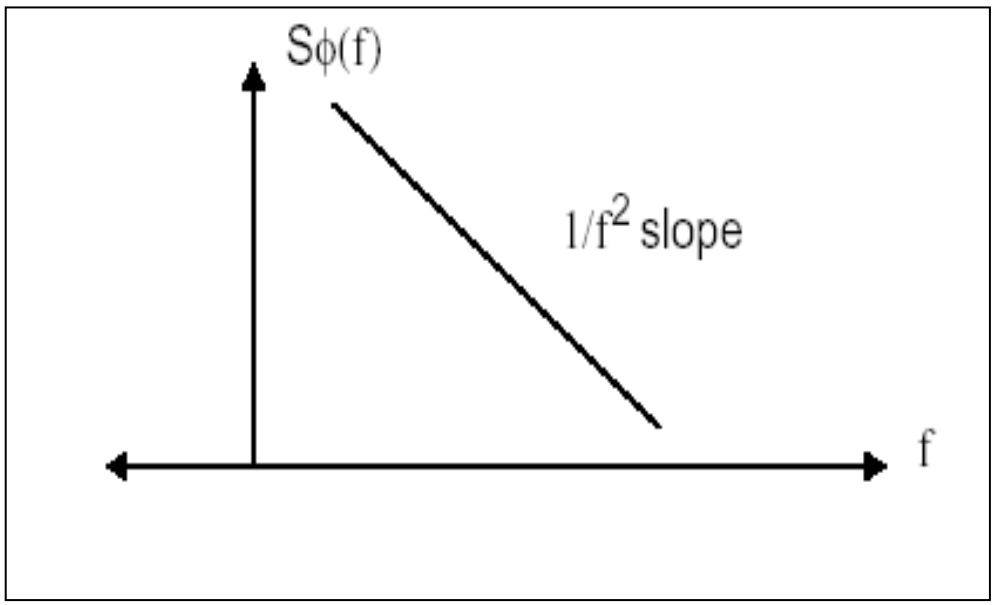

Figure 2.3 Phase Noise Power Spectral Density

2.3.2 Phase Noise in Ring Oscillators

With the relationship between phase noise and timing jitter established in equation Eq (2.25), phase noise can now be related to the delay-cell design parameters considered earlier. Using the result for cycle-to-cycle jitter from the previous section equation Eq (2.6)) and rearranging terms, we arrive at

$$S_{\phi}(f_m) = \left(\frac{f_0}{f_m}\right)^2 \bullet \left(\frac{F_1 kT}{I_{SS}(V_{GS} - V_T)}\right) \qquad \text{Eq (2.26)}$$

where the offset frequency is now denoted by f_m, the distance of the offset frequency from carrier. This equation shows that phase noise is related to the ratio of the center frequency to the offset frequency squared, times a factor related to delay cell device design. The familiar thermal noise factor kT is in the numerator, and is multiplied by the term F_1. This term is just a simplified constant equal to the 1/2 times the inter-stage gain, a_v , times the noise contribution factor ξ.

$$F_1 = \frac{a_v \cdot \xi^2}{2} \qquad \text{Eq (2.27)}$$

These two parameters where discussed in the section on cycle-to-cycle VCO jitter, where it was determined that were relatively insensitive to delay cell design tradeoffs. For typical ring-oscillators, a_v is in the range of 1.5 to 3 and ξ is in the range of 2 to 3. In the denominator of the second term in Eq (2.26) we also find the product of the tail current per delay stage times the gate-to-source bias above threshold for the NMOS differential pair transistors. As described previously, (V_{GS}-V_T) is constrained by

voltage swing and gain requirements, but I_{SS} can be scaled to reduce cycle-to-cycle jitter, or in this case, phase noise. Once again, a scaling of I_{SS} implies a corresponding scaling of gate width W, so that $(V_{GS}-V_T)$ remains constant.

From equation Eq (2.26), it is apparent that increasing the current consumed per delay stage will reduce the phase noise. The rate of improvement is 10dB per decade increase in current. For the current-mode-logic delay cells considered here, which consume static power, the power consumption is proportional to the current as well. In addition, if gate widths are scaled proportionally with the ratio of current to $(V_{GS}-V_T)$, then total circuit area will increase as well. A comparison of predicted performance for a typical ring-oscillator design at three different power levels is shown in Figure 2.4[2]. Here, the phase noise is plotted on a log-log scale versus offset frequency, falling at a rate of 20 dB/decade with increasing offset due to the $(1/f_m^2)$ term in Eq (2.26). Predicted phase noise at a 1 MHz offset is given for 1 mW, 10 mW, and 100 mW designs. The phase noise at a given offset improves 10 dBc/Hz with each decade increase in power consumption.

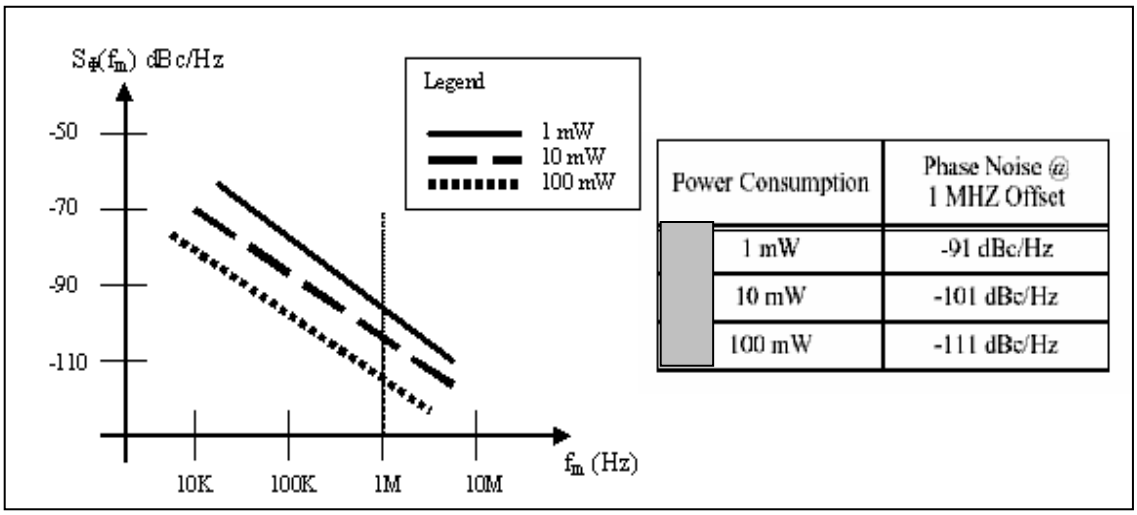

Figure 2.4: Phase Noise vs Power Consumption

The general form of the phase noise equation in Eq (2.26) is in good agreement with the classical phase noise derivation for LC-tank oscillators. Analysis in [5], [6] and [7] predict a phase noise expression that has the same dependence on the ratio of center frequency to offset frequency $(f_0 / f_m)^2$.

$$S_\phi(f_m) = \left(\frac{f_0}{f_m}\right)^2 \bullet \left(\frac{1}{Q^2}\right)\left(\frac{FkT}{4P}\right) \qquad \text{Eq (2.28)}$$

In addition, phase noise depends on a factor F, related to the amplifier in the LC oscillator forward path, times the thermal noise energy kT. The factor F is analogous to the F_1 term in Eq (2.26). Also common to both equations is a term with units of power in the denominator. For the LC oscillator this is the output power of the oscillator itself. In the ring-oscillator case, the product of I_{SS} and $(V_{GS}-V_T)$ has units of power and is proportional to the static power consumed in the ring oscillator VCO (since $(V_{GS}-V_T)$ is related to V_{dd} through the inter-stage gain, and the product of I_{SS} and V_{dd} is the total power consumption per cell). What differs between the two is the additional factor of $(1/Q^2)$ in equation Eq (2.28). This term shows that LC type oscillators have an additional phase noise improvement related to the quality factor of the resonator. This quality factor depends on resistive losses in the elements comprising the LC tuned circuit. For typical off-chip LC tank elements, Q's on the order of 6-60 are possible, resulting in phase noise improvements of 40 to 60 dBc/Hz, everything else being the same. For LC VCO's employing on-chip elements for the LC, such as spiral or bond-wire inductors, and varactors integrated with the rest of the active circuitry, Q's on the order of 3-to-8 have been observed [8, 9, 10, 11]. This corresponds to phase noise

improvements on the order of 9.5 to 18 dBc/Hz. Of course the other parameters, the factor F, and the power consumed in an oscillator vary from case to case as well.

Unlike ring-oscillator VCO's however, the trade-off between power consumption and phase noise is complicated by other circuit design considerations. The power consumed in an LC oscillator is related to the resistive loss in its circuit elements, which are in turn related to the Q of the LC-tank. Therefore, changing the power term in equation Eq (2.28) implies a change in the circuit Q. Ultimately, the choice of center frequency and the range of practical inductor and varactor sizes available to the designer determine the circuit Q and the power consumption in the oscillator. In some cases, as described by Craninkcx & Steyaert in [12], the phase noise actually improves with lower power consumption, P, due to these other considerations.

For ring-oscillator VCOs, however, there is freedom for the designer to change the current per stage, I_{SS}, over several orders of magnitude, allowing for a range of possible phase noise performance levels. Since device sizes are scaled with the current, this implies an increase in area as well. In some applications there are other incentives to increase the size and power consumption of the ring as well. In a PLL for instance, it makes sense that the VCO power budget is at least as high as for the other components of the system. Also, for applications where the VCO is called upon to drive mixers or sampling circuits with reasonably high capacitive loads, a larger VCO is favored. Ultimately there will be buffers between the ring-oscillator and the load, but starting with a larger ring can ease the requirements on buffer design.